

INA27x 电压输出、单向测量电流分流监控器

1 特性

- 宽共模范围：-16V 至 +80V
- CMRR: 120dB
- 精度：
 - ±0.5mV 失调电压（典型值）
 - ±0.2% 增益误差（典型值）
 - 2.5 $\mu\text{V}/^\circ\text{C}$ 温漂（典型值）
 - 50 ppm/ $^\circ\text{C}$ 增益漂移（最大值）
- 带宽：高达 130kHz
- 两种可用增益选项：
 - 14 V/V (INA270)
 - 20 V/V (INA271)
- 静态电流：700 μA （典型值）
- 电源：+2.7V 至 +18V
- 可用于滤波

2 应用

- 电源管理
- 汽车
- 电信设备
- 笔记本电脑
- 电池充电器
- 手机
- 焊接设备

3 说明

INA270 和 INA271 系列器件电压输出、电流感应放大器可在独立于电源电压的 -16V 至 +80V 共模电压中检测分流电阻上的压降。INA270 和 INA271 引脚排列可随时用于滤波。

INA270 和 INA271 具有两种增益选项：14 V/V 和 20 V/V。130kHz 带宽简化了在电流控制环路中的使用。

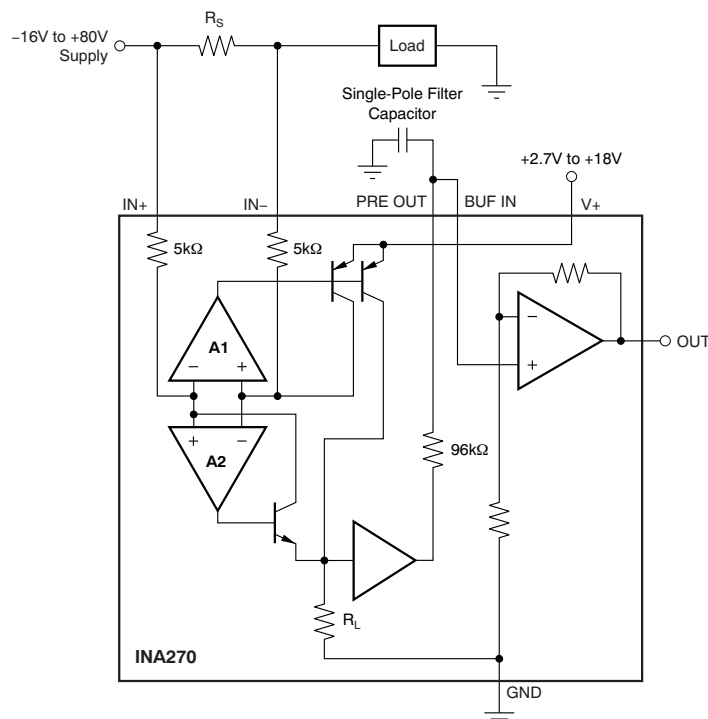
INA270 和 INA271 由一个 +2.7V 至 +18V 单电源供电，消耗电源电流为 700 μA （典型值）。器件具有 -40 $^\circ\text{C}$ 至 +125 $^\circ\text{C}$ 扩展额定工作温度范围，采用 SOIC-8 封装。

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA27x	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (November 2014) to Revision E	Page
• 为第 1 页的图添加了标题	1
• Updated <i>ESD Ratings</i> table to current standards	4
• Changed Figure 16 : changed op amp input to BUF IN pin from negative to positive	12
• 添加了社区资源部分	19

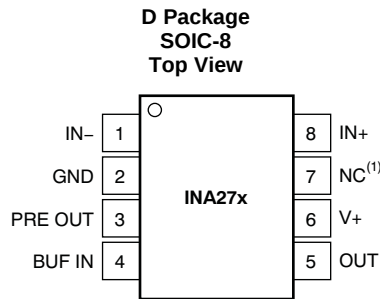
Changes from Revision C (May 2010) to Revision D	Page
• 更改了格式以符合最新数据表标准	1
• 添加了处理额定值、引脚说明 与建议运行条件 表和特性 说明、器件功能模式、应用和实施、电源相关建议、布局、器件和文档支持 以及机械、封装和可订购信息部分	1
• 更改了精度 和静态电流 特性 项目符号：从规格和值的最大值更改成了典型值	1
• 更改了两种可用增益选项 特性 项目符号中的措辞	1
• 更改了说明 部分用于澄清说明	1
• 添加了器件信息表	1
• Deleted Ordering Information table	3
• Changed Input, <i>Full-Scale Input Voltage</i> parameter conditions in Electrical Characteristics table.....	5
• Changed title of <i>First- or Second-Order Filtering</i> section.....	12
• Changed title of <i>Power Supply Recommendations</i> section.....	17

Changes from Revision B (July 2008) to Revision C	Page
• Corrected Figure 17 y-axis	14
• Corrected Figure 18 y-axis	14

5 Device Comparison Table

DEVICE	GAIN
INA270	14 V/V
INA271	20 V/V

6 Pin Configuration and Functions



NOTE (1): NC denotes no internal connection.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BUF IN	4	Analog input	Connect to output of filter from PRE OUT
GND	2	Analog	Ground
IN–	1	Analog input	Connect to load side of shunt resistor
IN+	8	Analog input	Connect to supply side of shunt resistor
NC	7	—	Connect to ground
OUT	5	Analog output	Output voltage
PRE OUT	3	Analog output	Connect to input of filter to BUF IN
V+	6	Analog input	Power supply, +2.7 V to +18 V

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

	MIN	MAX	UNIT
Supply voltage (V_S)		+18	V
Analog inputs, V_{IN+} , V_{IN-} :	Differential, $(V_{IN+}) - (V_{IN-})$		V
	Common-mode		V
Analog output: OUT and PRE OUT pins	GND – 0.3	$(V+) + 0.3$	V
Input current into any pin		5	mA
Operating temperature	–55	+150	°C
Junction temperature		+150	°C
Storage temperature, T_{stg}	–65	+150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CM}	Common-mode input voltage	–16	12	80	V
V _S	Operating supply voltage	2.7	5	18	V
T _A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA27x	UNIT
		D (SOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	78.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	71.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	68.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	22.0	°C/W
ψ _{JB}	Junction-to-board characterization parameter	67.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{ V}$, $V_{CM} = +12\text{ V}$, $V_{SENSE} = 100\text{ mV}$, and PRE OUT connected to BUF IN, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{SENSE}	Full-scale input voltage	$V_{SENSE} = (V_{IN+}) - (V_{IN-})$		0.15	$(V_S - 0.2) / \text{Gain}$	V
V_{CM}	Common-mode input range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-16		+80	V
CMRR	Common-mode rejection ratio	$V_{IN+} = -16\text{ V}$ to $+80\text{ V}$	80	120		dB
	CMRR over temperature	$V_{IN+} = +12\text{ V}$ to $+80\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	100	120		dB
V_{OS}	Offset voltage, RTI ⁽¹⁾			± 0.5	2.5	mV
	V_{OS} over temperature	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 3	mV
dV_{OS}/dT	V_{OS} vs temperature	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		2.5	20	$\mu\text{V}/^\circ\text{C}$
PSR	V_{OS} vs power-supply	$V_S = +2.7\text{ V}$ to $+18\text{ V}$, $V_{CM} = +18\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		5	100	$\mu\text{V}/\text{V}$
I_B	Input bias current, V_{IN-} pin	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 8	± 16	μA
	PRE OUT output impedance ⁽²⁾			96		k Ω
	Buffer input bias current			-50		nA
	Buffer input bias current temperature coefficient			± 0.03		nA/ $^\circ\text{C}$
OUTPUT ($V_{SENSE} \geq 20\text{ mV}$)⁽³⁾						
G	Gain	INA270 total gain		14		V/V
		INA271 total gain		20		V/V
G_{BUF}	Output buffer gain			2		V/V
	Total gain error	$V_{SENSE} = 20\text{ mV}$ to 100 mV		$\pm 0.2\%$	$\pm 1\%$	
	Total gain error Over temperature	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 2\%$	
	Total gain error vs temperature	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			50	ppm/ $^\circ\text{C}$
	Total output error ⁽⁴⁾			$\pm 0.75\%$	$\pm 2.2\%$	
	Total output error	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 1.0\%$	$\pm 3.0\%$	
	Nonlinearity error	$V_{SENSE} = 20\text{ mV}$ to 100 mV		$\pm 0.002\%$		
R_O	Output impedance, pin 5			1.5		Ω
	Maximum capacitive load	No sustained oscillation		10		nF
VOLTAGE OUTPUT⁽⁵⁾ ($R_L = 10\text{ k}\Omega$ to GND)						
	Swing to V+ power-supply rail	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$(V+) - 0.05$	$(V+) - 0.2$	V
	Swing to GND ⁽⁶⁾	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$V_{GND} + 0.003$	$V_{GND} + 0.05$	V
FREQUENCY RESPONSE						
BW	Bandwidth	$C_{LOAD} = 5\text{ pF}$		130		kHz
	Phase margin	$C_{LOAD} < 10\text{ nF}$		40		Degrees
SR	Slew rate			1		V/ μs
t_s	Settling time (1%)	$V_{SENSE} = 10\text{ mV}$ to 100 mV_{PP} , $C_{LOAD} = 5\text{ pF}$		2		μs

(1) RTI means *Referred-to-Input*.

(2) Initial resistor variation is $\pm 30\%$ with an additional $-2200\text{-ppm}/^\circ\text{C}$ temperature coefficient.

(3) For output behavior when $V_{SENSE} < 20\text{ mV}$, see the [Accuracy Variations as a Result of \$V_{SENSE}\$ and Common-Mode Voltage](#) section.

(4) Total output error includes effects of gain error and V_{OS} .

(5) See typical characteristic curve *Output Swing vs Output Current* and the [Accuracy Variations as a Result of \$V_{SENSE}\$ and Common-Mode Voltage](#) section.

(6) Ensured by design; not production tested.

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Electrical Characteristics (continued)

 At $T_A = +25^\circ\text{C}$, $V_S = +5\text{ V}$, $V_{CM} = +12\text{ V}$, $V_{SENSE} = 100\text{ mV}$, and PRE OUT connected to BUF IN, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NOISE, RTI⁽¹⁾						
e_n	Voltage noise density			40		nV/ $\sqrt{\text{Hz}}$
POWER SUPPLY						
V_S	Operating range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	+2.7		+18	V
I_Q	Quiescent current	$V_{OUT} = 2\text{ V}$		700	900	μA
	I_Q over temperature	$V_{SENSE} = 0\text{ mV}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		350	950	μA
TEMPERATURE RANGE						
	Specified temperature range		-40		+125	$^\circ\text{C}$
	Operating temperature range		-55		+150	$^\circ\text{C}$
θ_{JA}	Thermal resistance, SO-8			150		$^\circ\text{C/W}$

7.6 Typical Characteristics

At $T_A = +25^\circ\text{C}$, $V_S = +12\text{ V}$, $V_{CM} = 12\text{ V}$, and $V_{SENSE} = 100\text{ mV}$, unless otherwise noted.

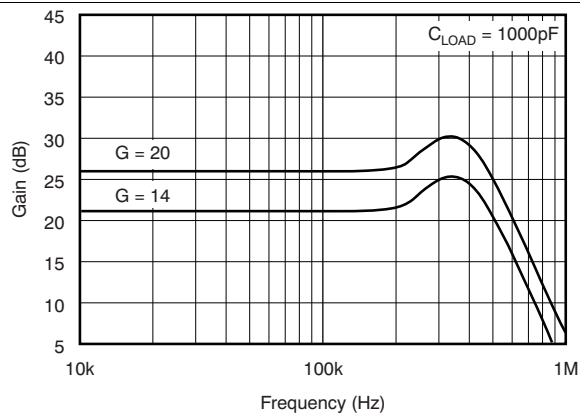


Figure 1. Gain vs Frequency

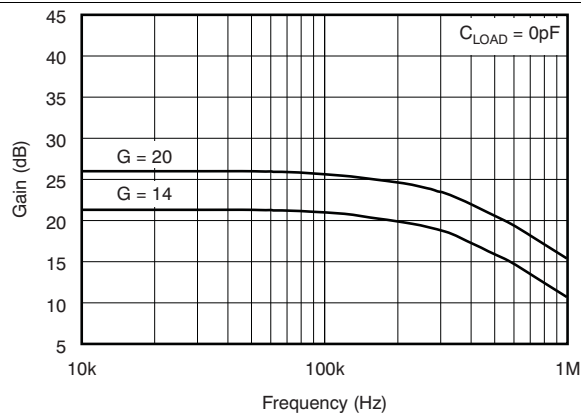


Figure 2. Gain vs Frequency

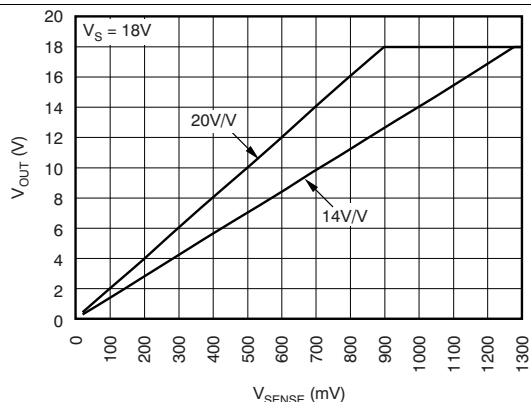


Figure 3. Gain Plot

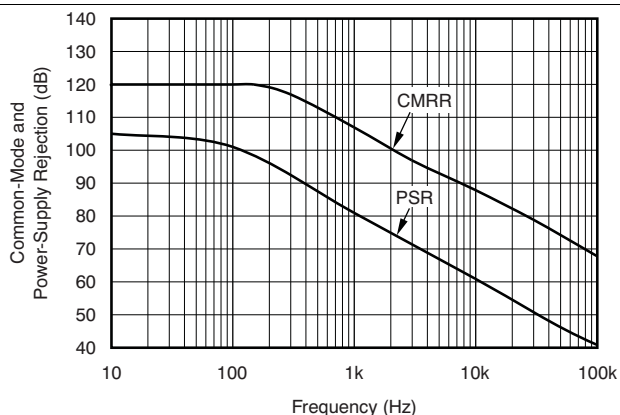


Figure 4. Common-Mode and Power-Supply Rejection vs Frequency

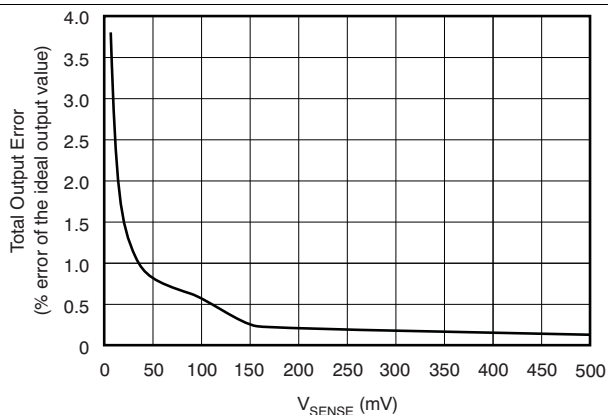


Figure 5. Total Output Error vs V_{SENSE}

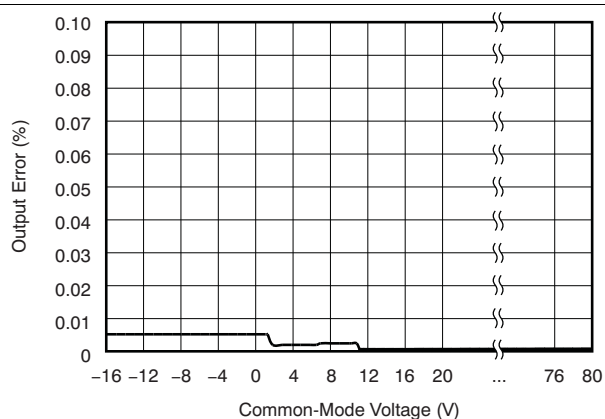


Figure 6. Output Error vs Common-Mode Voltage

Typical Characteristics (continued)

At $T_A = +25^\circ\text{C}$, $V_S = +12\text{ V}$, $V_{CM} = 12\text{ V}$, and $V_{SENSE} = 100\text{ mV}$, unless otherwise noted.

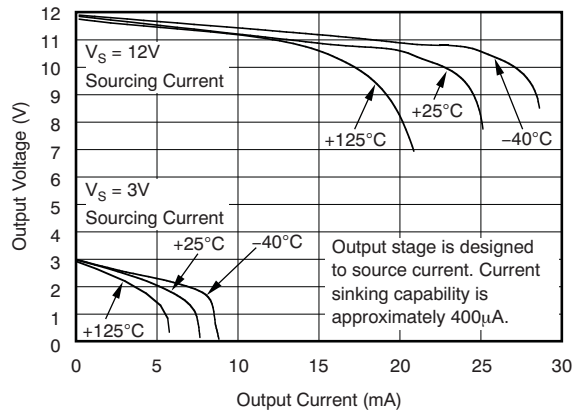


Figure 7. Positive Output Voltage Swing vs Output Current

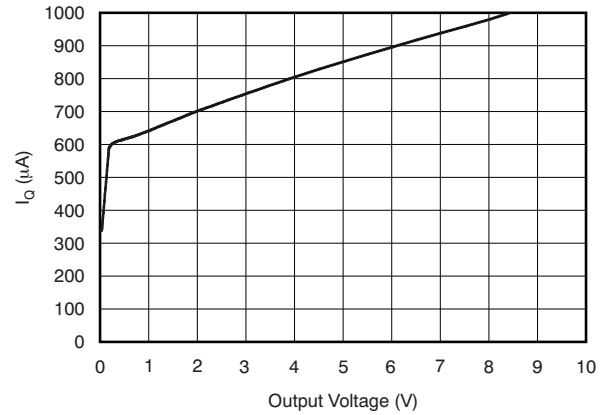


Figure 8. Quiescent Current vs Output Voltage

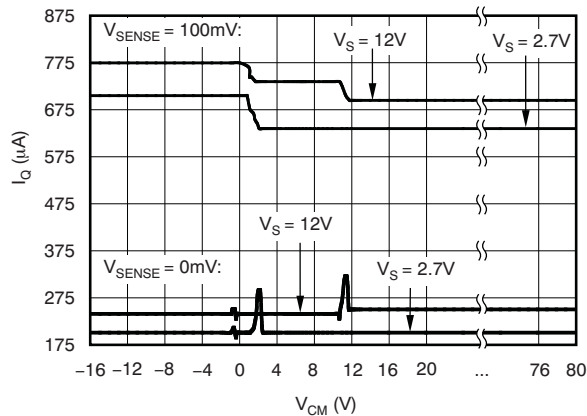


Figure 9. Quiescent Current vs Common-Mode Voltage

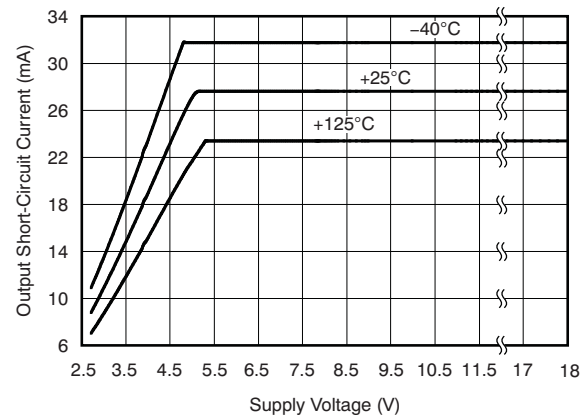


Figure 10. Output Short-Circuit Current vs Supply Voltage

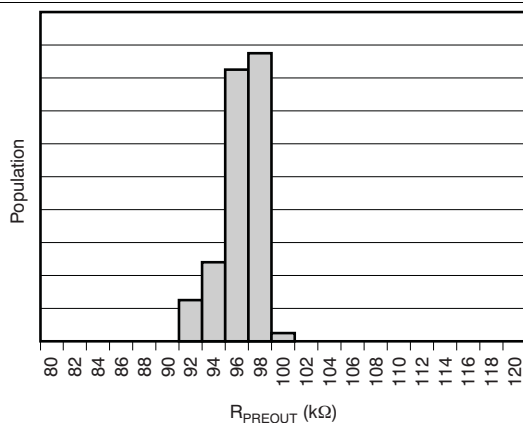


Figure 11. PRE OUT Output Resistance Production Distribution

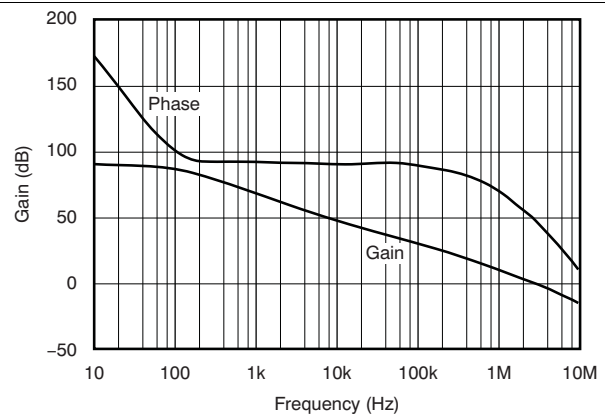
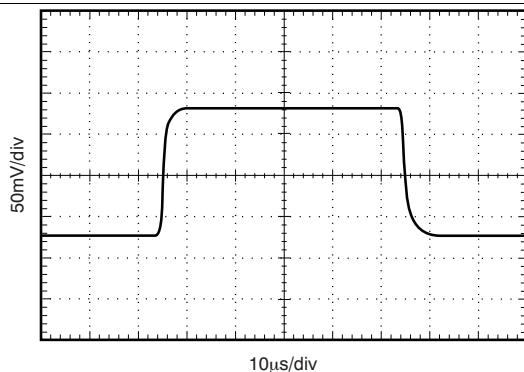


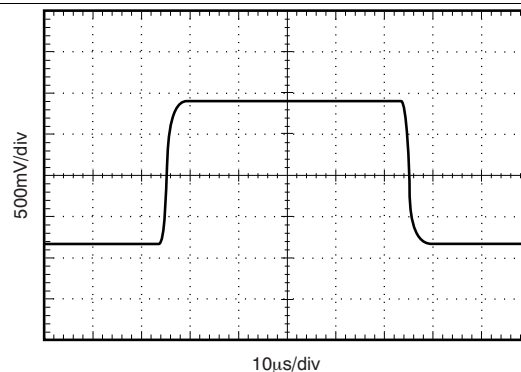
Figure 12. Buffer Gain vs Frequency

Typical Characteristics (continued)

At $T_A = +25^\circ\text{C}$, $V_S = +12\text{ V}$, $V_{CM} = 12\text{ V}$, and $V_{SENSE} = 100\text{ mV}$, unless otherwise noted.



**Figure 13. Small-Signal Step Response
(10-mV to 20-mV Input)**



**Figure 14. Large-Signal Step Response
(10-mV to 100-mV Input)**

8 Detailed Description

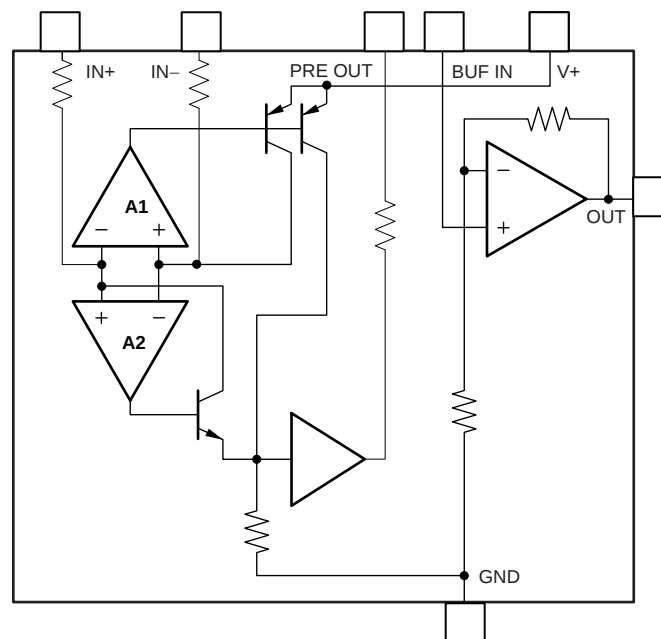
8.1 Overview

The INA270 and INA271 family of current-shunt monitors with voltage output can sense drops across current shunts at common-mode voltages from -16 V to $+80\text{ V}$, independent of the supply voltage. The INA270 and INA271 pinouts readily enable filtering.

The INA270 and INA271 are available with two output voltage scales: 14 V/V and 20 V/V . The 130-kHz bandwidth simplifies use in current-control loops.

The INA270 and INA271 operate from a single $+2.7\text{-V}$ to $+18\text{-V}$ supply, drawing a maximum of $900\text{ }\mu\text{A}$ of supply current. The devices are specified over the extended operating temperature range of -40°C to $+125^{\circ}\text{C}$ and are offered in an SOIC-8 package.

8.2 Functional Block Diagram



Feature Description (continued)

Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it never allows the INA270 and INA271 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA270 and INA271 are not suited to using external resistors in series with the inputs because the internal gain resistors can vary up to $\pm 30\%$, but are tightly matched (if gain accuracy is not important, then resistors can be added in series with the INA270 and INA271 inputs with two equal resistors on each input).

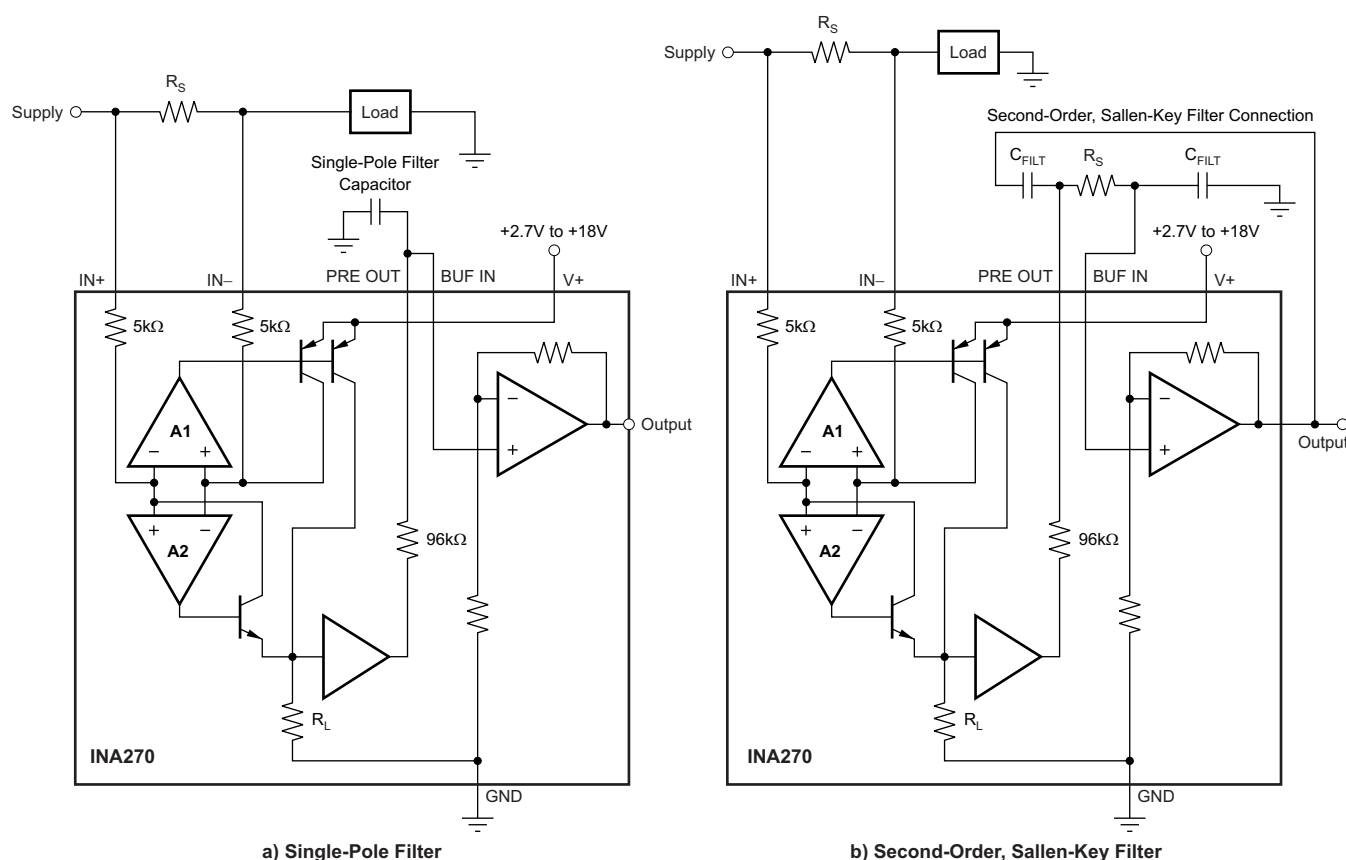
8.4 Device Functional Modes

8.4.1 First- or Second-Order Filtering

The output of the INA270 and INA271 is accurate within the output voltage swing range set by the power-supply pin, V+.

The INA270 and INA271 readily enable the inclusion of filtering between the preamp output and buffer input. Single-pole filtering can be accomplished with a single capacitor because of the 96-k Ω output impedance at PRE OUT on pin 3, as shown in Figure 16a.

The INA270 and INA271 readily lend themselves to second-order Sallen-Key configurations, as shown in Figure 16b. When designing these configurations consider that the PRE OUT 96-k Ω output impedance exhibits an initial variation of $\pm 30\%$ with the addition of a $-2200\text{-ppm}/^\circ\text{C}$ temperature coefficient.



NOTE: Remember to use the appropriate buffer gain (INA270 = 1.4, INA271 = 2) when designing Sallen-Key configurations.

Figure 16. The INA270–INA271 can be Easily Connected for First- or Second-Order Filtering

Device Functional Modes (continued)

8.4.2 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA270 and INA271 current shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} - V_{IN-}$) and common-mode voltage (V_{CM}) relative to the supply voltage, V_S . V_{CM} is expressed as $(V_{IN+} + V_{IN-}) / 2$; however, in practice, V_{CM} is used as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

Normal Case 1: $V_{SENSE} \geq 20 \text{ mV}$, $V_{CM} \geq V_S$

Normal Case 2: $V_{SENSE} \geq 20 \text{ mV}$, $V_{CM} < V_S$

Low V_{SENSE} Case 1:

$V_{SENSE} < 20 \text{ mV}$, $-16 \text{ V} \leq V_{CM} < 0$

Low V_{SENSE} Case 2:

$V_{SENSE} < 20 \text{ mV}$, $0 \text{ V} \leq V_{CM} \leq V_S$

Low V_{SENSE} Case 3:

$V_{SENSE} < 20 \text{ mV}$, $V_S < V_{CM} \leq 80 \text{ V}$

8.4.2.1 Normal Case 1: $V_{SENSE} \geq 20 \text{ mV}$, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\text{mV} - 20\text{mV}}$$

where

- V_{OUT1} = Output voltage with $V_{SENSE} = 100 \text{ mV}$ and
- V_{OUT2} = Output voltage with $V_{SENSE} = 20 \text{ mV}$. (1)

Then the offset voltage is measured at $V_{SENSE} = 100 \text{ mV}$ and referred to the input (RTI) of the current shunt monitor, as shown in Equation 2.

$$V_{OS\text{RTI}} (\text{Referred-To-Input}) = \left[\frac{V_{OUT1}}{G} \right] - 100\text{mV} \quad (2)$$

In the *Typical Characteristics*, the *Output Error vs Common-Mode Voltage* curve (Figure 6) shows the highest accuracy for the this region of operation. In this plot, $V_S = 12 \text{ V}$; for $V_{CM} \geq 12 \text{ V}$, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq 20 \text{ mV}$ output specifications in the *Electrical Characteristics* table.

8.4.2.2 Normal Case 2: $V_{SENSE} \geq 20 \text{ mV}$, $V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the device functions, as illustrated in the *Output Error vs Common-Mode Voltage* curve (Figure 6). As noted, for this graph $V_S = 12 \text{ V}$; for $V_{CM} < 12 \text{ V}$, the output error increases when V_{CM} becomes less than 12 V , with a typical maximum error of 0.005% at the most negative $V_{CM} = -16 \text{ V}$.

8.4.2.3 Low V_{SENSE} Case 1: $V_{SENSE} < 20 \text{ mV}$, $-16 \text{ V} \leq V_{CM} < 0$; and Low V_{SENSE} Case 3: $V_{SENSE} < 20 \text{ mV}$, $V_S < V_{CM} \leq 80 \text{ V}$

Although the INA270 family of devices are not designed for accurate operation in either of these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA270 or INA271, knowing what the behavior of the devices is in these regions is important.

Device Functional Modes (continued)

When V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of $V_{OUT} = 60$ mV for $V_{SENSE} = 0$ mV. When V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as specified in the [Electrical Characteristics](#). Figure 17 shows this effect using the INA271 (gain = 20).

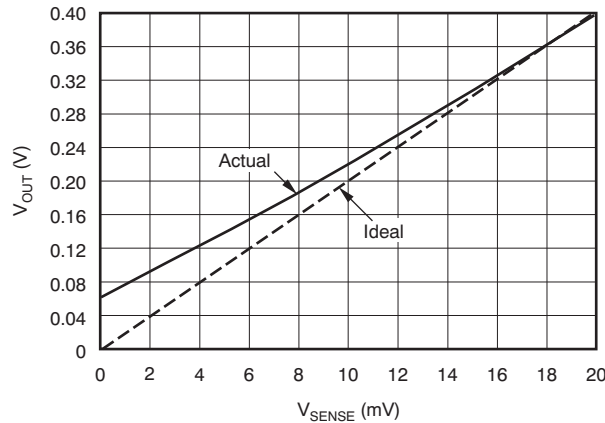
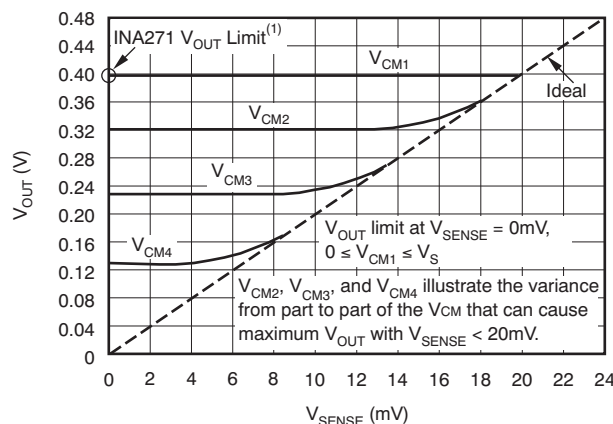


Figure 17. Example For Low V_{SENSE} Cases 1 and 3 (INA271, Gain = 20)

8.4.2.4 Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, 0 V $\leq V_{CM} \leq V_S$

This region of operation is the least accurate for the INA270 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for [Normal Case 2](#).

This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, when V_{SENSE} approaches 20 mV, device operation is closer to that described by [Normal Case 2](#). Figure 18 shows this behavior for the INA271. The V_{OUT} maximum peak for this case is determined by maintaining a constant V_S , setting $V_{SENSE} = 0$ mV, and sweeping V_{CM} from 0 V to V_S . The exact V_{CM} at which V_{OUT} peaks during this case varies from device to device. The maximum peak voltage for the INA270 is 0.28 V; for the INA271, the maximum peak voltage is 0.4 V.



NOTE: (1) INA271 V_{OUT} Limit = 0.4V. INA270 V_{OUT} Limit = 0.28V.

Figure 18. Example for Low V_{SENSE} Case 2 (INA271, Gain = 20)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA270 and INA271 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference terminal to adjust the functionality of the output signal offers multiple configurations discussed throughout this section. There is also a filtering feature to remove unwanted transients and smooth the output voltage.

9.2 Typical Application

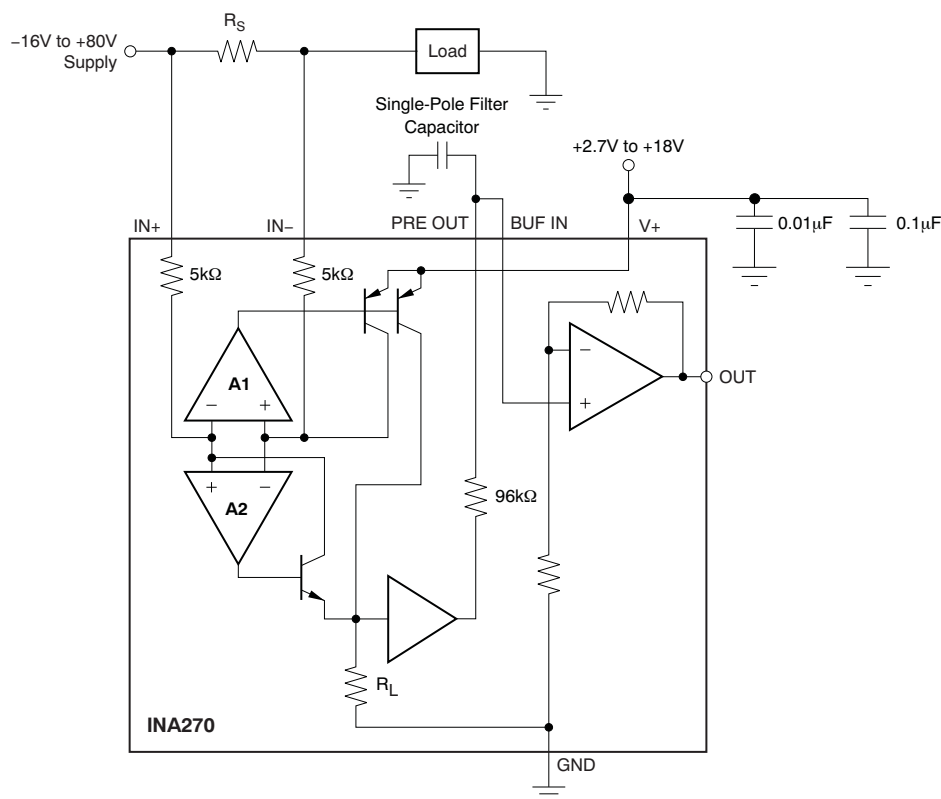


Figure 19. Filtering Configuration

9.2.1 Design Requirements

In this application, the device is configured to measure a triangular periodic current at 10 kHz with filtering. The average current through the shunt is the information that is desired. This current can be either solenoid current or inductor current where current is being pulsed through.

Selecting the capacitor size is based on the lowest frequency component to be filtered out. The amount of signal that is filtered out is dependant on this cutoff frequency. From the cutoff frequency, the attention is 20 dB per decade.

Typical Application (continued)

9.2.2 Detailed Design Procedure

Without this filtering capability, an input filter must be used. When series resistance is added to the input, large errors also come into play because the resistance must be large to create a low cutoff frequency. By using a 10-nF capacitor for the single-pole filter capacitor, the 10-kHz signal is averaged. The cutoff frequency made by the capacitor is set at 166 Hz frequency. This frequency is well below the periodic frequency and reduces the ripple on the output and the average current can easily be measured.

9.2.3 Application Curves

Figure 20 shows the output waveform without filtering. The output signal tracks the input signal with a large ripple. If this current is sampled by an ADC, many samples must be taken to average the current digitally. This process takes additional time to sample and average and is very time consuming, thus is unwanted for this application.

Figure 21 shows the output waveform with filtering. The output signal is filtered and the average can easily be measured with a small ripple. If this current is sampled by an ADC, only a few samples must be taken to average. Digital averaging is now not required and the time required is significantly reduced.

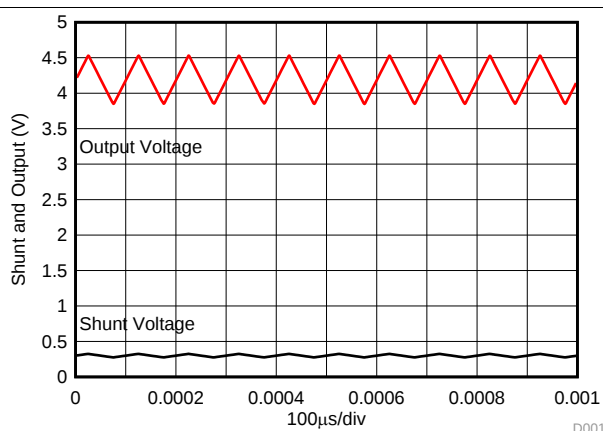


Figure 20. Without Filtering

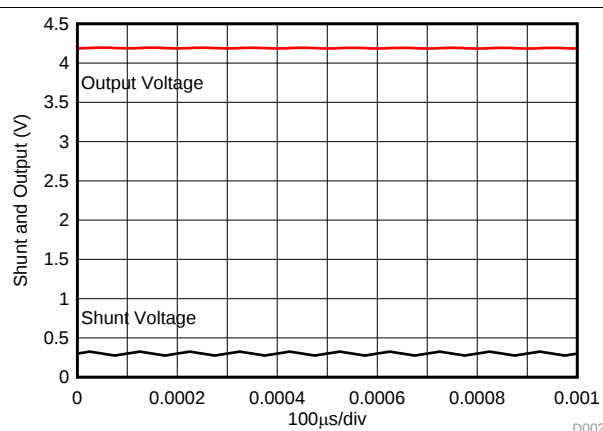


Figure 21. With Filtering

10 Power Supply Recommendations

The input circuitry of the INA270 and INA271 can accurately measure beyond its power-supply voltage, $V+$. For example, the $V+$ power supply can be 5 V, whereas the load power-supply voltage is up to +80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

10.1 Shutdown

The INA270 and INA271 do not provide a shutdown pin; however, because these devices consume a quiescent current less than 1 mA, they can be powered by either the output of logic gates or by transistor switches to supply power. Driving the gate low shuts down the INA270 and INA271. Use a totem-pole output buffer or gate that can provide sufficient drive along with a 0.1- μ F bypass capacitor, preferably ceramic with good high-frequency characteristics. This gate must have a supply voltage of 3 V or greater because the INA270 and INA271 require a minimum supply greater than 2.7 V. In addition to eliminating quiescent current, this gate also turns off the 10- μ A bias current present at each of the inputs. Note that the IN+ and IN- inputs are able to withstand full common-mode voltage under all powered and under-powered conditions. An example shutdown circuit is shown in Figure 22.

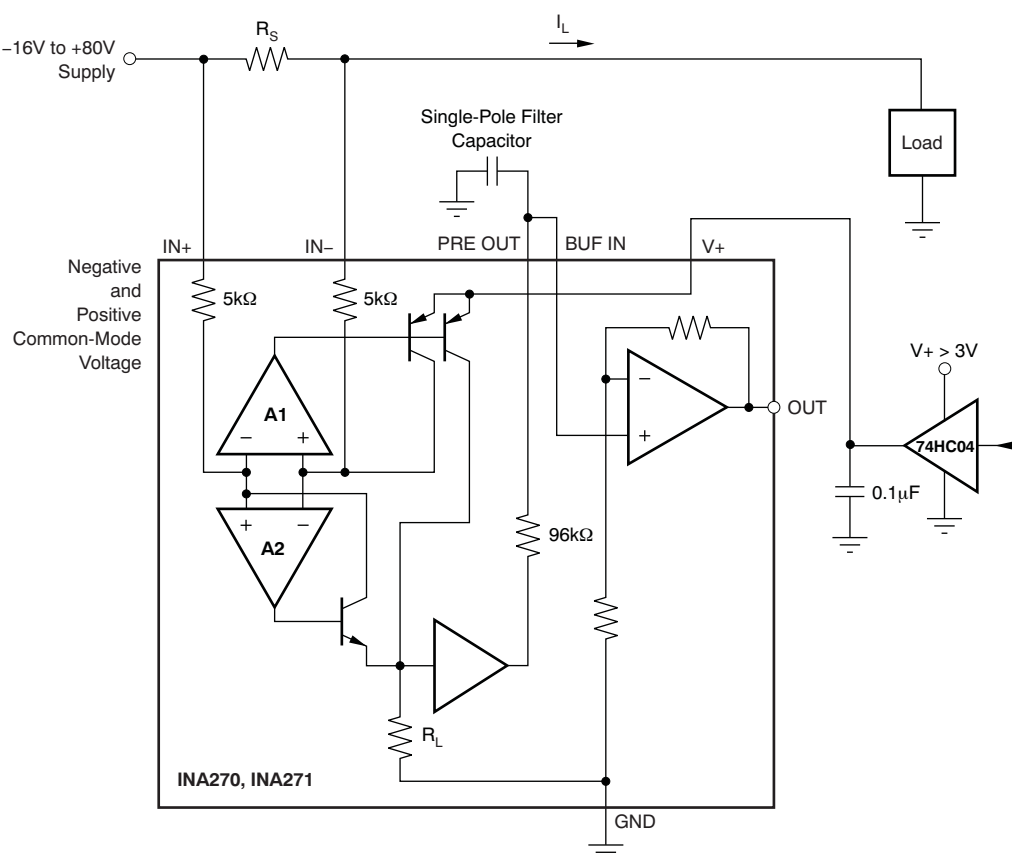


Figure 22. INA270-INA271 Example Shutdown Circuit

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF . Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.1.1 RFI and EMI

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI and EMI sensitivity. PCB layout must locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields. The difference in input pin location of the INA270 and INA271 versus the [INA193 to INA198](#) may provide different EMI performance.

11.2 Layout Example

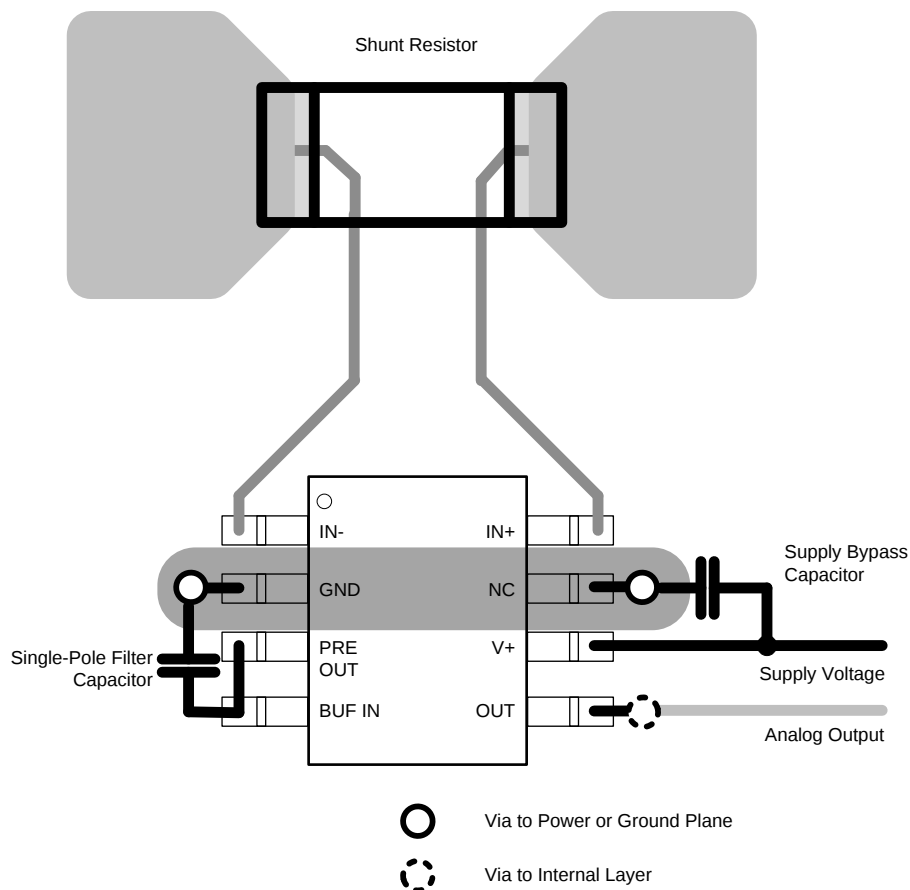


Figure 23. Example Layout

12 器件和文档支持

12.1 Documentation Support

12.1.1 相关文档

如需相关文档，请参阅：

INA270 TINA-TI Spice 模型，[SBOM306](#)

INA270 PSpice 模型，[SBOM485](#)

INA270 TINA-TI 参考设计，[SBOC246](#)

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 1. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
INA270	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
INA271	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA270AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I270A	Samples
INA270AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I270A	Samples
INA271AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I271A	Samples
INA271AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I271A	Samples
INA271AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I271A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF INA271 :

NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA270AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA271AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA270AIDR	SOIC	D	8	2500	350.0	350.0	43.0
INA271AIDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

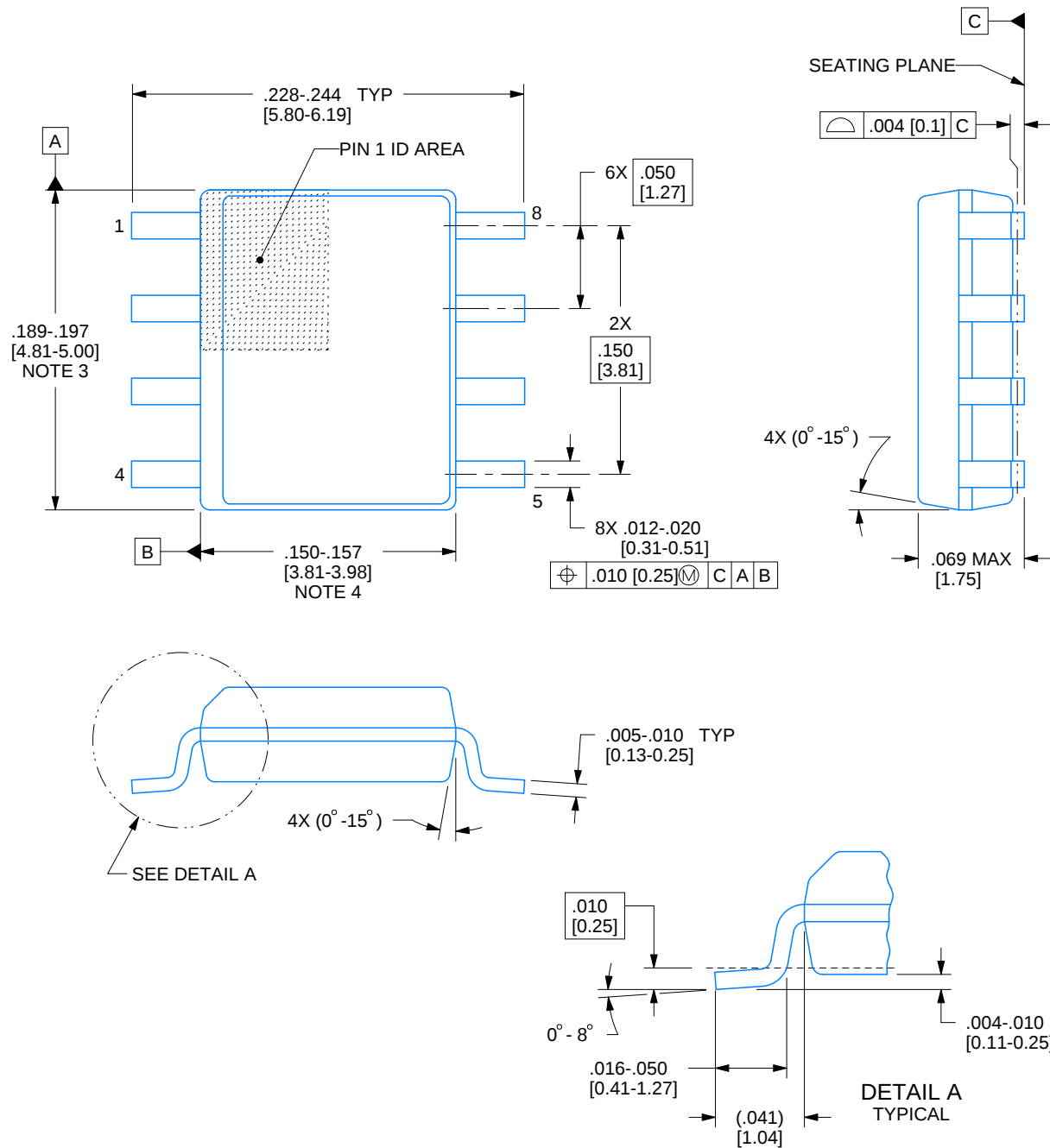
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA270AID	D	SOIC	8	75	505.46	6.76	3810	4
INA271AID	D	SOIC	8	75	505.46	6.76	3810	4
INA271AIDG4	D	SOIC	8	75	505.46	6.76	3810	4

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

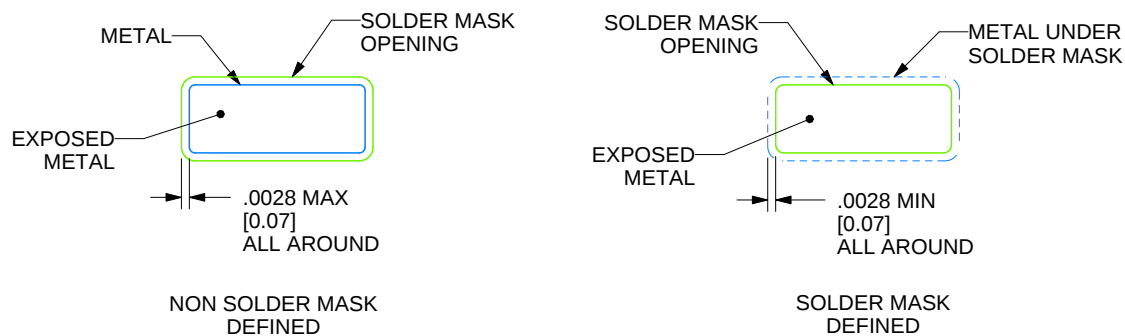
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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