

## DS90CP02 1.5 Gbps 2x2 LVDS Crosspoint Switch

Check for Samples: [DS90CP02](#)

### FEATURES

- 1.5 Gbps per Channel
- Low Power: 70 mA in Dual Repeater Mode @1.5 Gbps
- Low Output Jitter
- Non-Blocking Architecture Allows 1:2 Splitter, 2:1 Mux, Crossover, and Dual Buffer Configurations
- Flow-Through Pinout
- LVDS/BLVDS/CML/LVPECL Inputs, LVDS Outputs
- Single 3.3V Supply
- Separate Control of Inputs and Outputs Allows for Power Savings
- Industrial -40 to +85°C Temperature Range
- 28-lead UQFN-28 Space Saving Package

### DESCRIPTION

The DS90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. The 3.3V supply, CMOS process, and LVDS I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

### Block Diagram

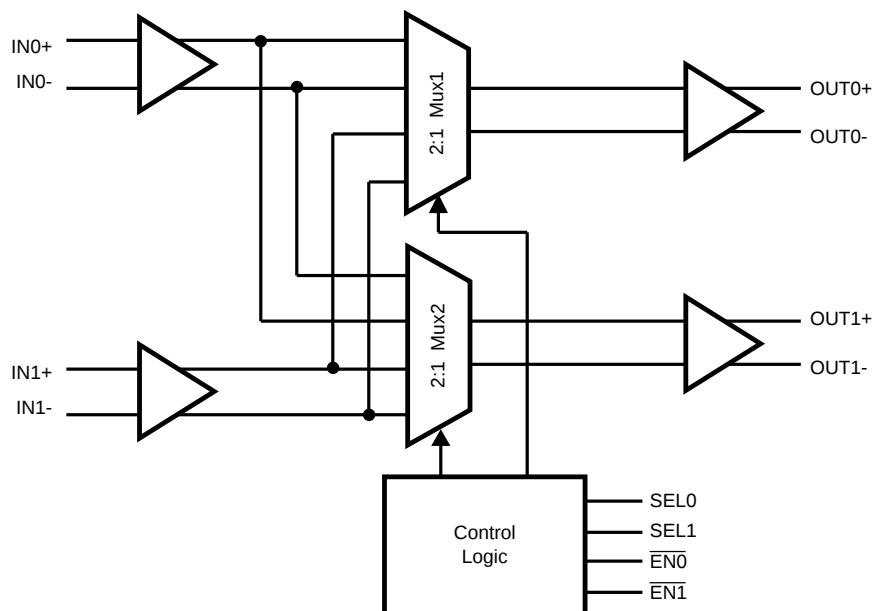


Figure 1. DS90CP02 Block Diagram



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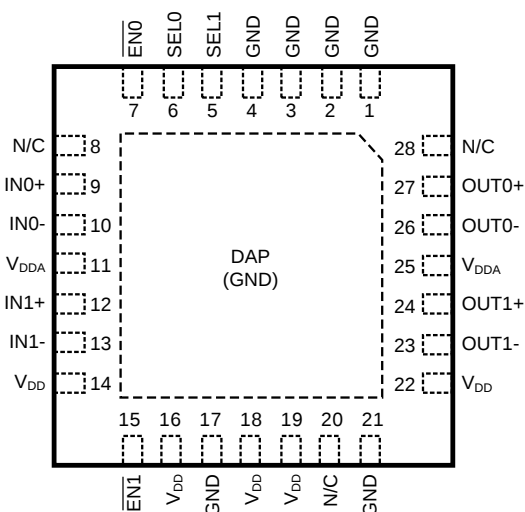
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**Table 1. PIN DESCRIPTIONS**

| Pin Name                                       | Pin Number                       | I/O, Type | Description                                                                                                                                                                                                                                                                                                              |
|------------------------------------------------|----------------------------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DIFFERENTIAL INPUTS COMMON TO ALL MUXES</b> |                                  |           |                                                                                                                                                                                                                                                                                                                          |
| IN0+<br>IN0-                                   | 9<br>10                          | I, LVDS   | Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.                                                                                                                                                                                                                              |
| IN1+<br>IN1-                                   | 12<br>13                         | I, LVDS   | Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.                                                                                                                                                                                                                              |
| <b>SWITCHED DIFFERENTIAL OUTPUTS</b>           |                                  |           |                                                                                                                                                                                                                                                                                                                          |
| OUT0+<br>OUT0-                                 | 27<br>26                         | O, LVDS   | Inverting and non-inverting differential outputs. OUT0± can be connected to any one pair IN0±, or IN1±. LVDS compatible .                                                                                                                                                                                                |
| OUT1+<br>OUT1-                                 | 24<br>23                         | O, LVDS   | Inverting and non-inverting differential outputs. OUT1± can be connected to any one pair IN0±, or IN1±. LVDS compatible .                                                                                                                                                                                                |
| <b>DIGITAL CONTROL INTERFACE</b>               |                                  |           |                                                                                                                                                                                                                                                                                                                          |
| SEL0, SEL1                                     | 6<br>5                           | I, LVTTTL | Select Control Inputs                                                                                                                                                                                                                                                                                                    |
| EN0, EN1                                       | 7<br>15                          | I, LVTTTL | Output Enable Inputs                                                                                                                                                                                                                                                                                                     |
| N/C                                            | 8, 20, 28                        |           | Not Connected                                                                                                                                                                                                                                                                                                            |
| <b>POWER</b>                                   |                                  |           |                                                                                                                                                                                                                                                                                                                          |
| V <sub>DD</sub>                                | 11, 14, 16,<br>18, 19, 22,<br>25 | I, Power  | V <sub>DD</sub> = 3.3V ±0.3V. At least 4 low ESR 0.01 µF bypass capacitors should be connected from V <sub>DD</sub> to GND plane.                                                                                                                                                                                        |
| GND                                            | DAP, 1, 2,<br>3, 4, 17,<br>21    | I, Power  | Ground reference to LVDS and CMOS circuitry.<br>For the UQFN package, the DAP is used as the primary GND connection to the device.<br>The DAP is the exposed metal contact at the bottom of the UQFN-28 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance. |

**Connection Diagram**

**Figure 2. UQFN Top View**  
**DAP = GND**  
**See Package Number NJD0028A**

**Configuration Select Truth Table**

| SEL0 | SEL1 | $\overline{\text{EN0}}$ | $\overline{\text{EN1}}$ | OUT0 | OUT1 | Mode                                              |
|------|------|-------------------------|-------------------------|------|------|---------------------------------------------------|
| 0    | 0    | 0                       | 0                       | IN0  | IN0  | 1:2 Splitter (IN1 powered down)                   |
| 0    | 1    | 0                       | 0                       | IN0  | IN1  | Dual Channel Repeater                             |
| 1    | 0    | 0                       | 0                       | IN1  | IN0  | Dual Channel Switch                               |
| 1    | 1    | 0                       | 0                       | IN1  | IN1  | 1:2 Splitter (IN0 powered down)                   |
| 0    | 1    | 0                       | 1                       | IN0  | PD   | Single Channel Repeater (Channel 1 powered down)  |
| 1    | 1    | 0                       | 1                       | IN1  | PD   | Single Channel Switch (IN0 and OUT1 powered down) |
| 0    | 0    | 1                       | 0                       | PD   | IN0  | Single Channel Switch (IN1 and OUT0 powered down) |
| 0    | 1    | 1                       | 0                       | PD   | IN1  | Single Channel Repeater (Channel 0 powered down)  |
| X    | X    | 1                       | 1                       | PD   | PD   | Both Channels in Power Down Mode                  |
| 0    | 0    | 0                       | 1                       |      |      | Invalid State*                                    |
| 1    | 0    | 0                       | 1                       |      |      | Invalid State*                                    |
| 1    | 0    | 1                       | 0                       |      |      | Invalid State*                                    |
| 1    | 1    | 1                       | 0                       |      |      | Invalid State*                                    |

## APPLICATION INFORMATION

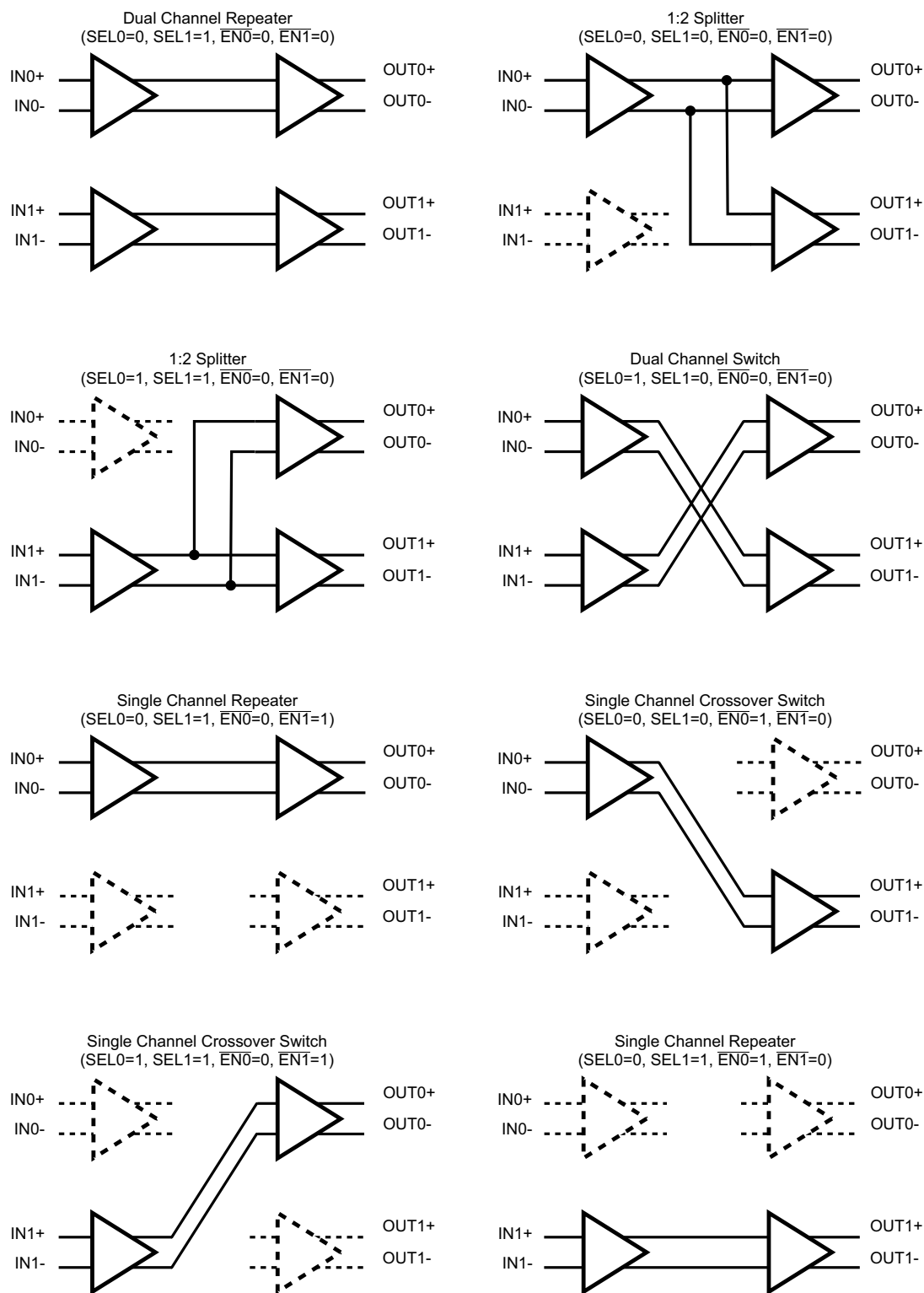


Figure 3. DS90CP02 Configuration Select Decode



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings <sup>(1)(2)</sup>

|                                           |                              |
|-------------------------------------------|------------------------------|
| Supply Voltage ( $V_{DD}$ )               | –0.3V to +4.0V               |
| CMOS Input Voltage                        | –0.3V to ( $V_{DD} + 0.3V$ ) |
| LVDS Receiver Input Voltage               | –0.3V to +3.6V               |
| LVDS Driver Output Voltage                | –0.3V to +3.6V               |
| LVDS Output Short Circuit Current         | 40mA                         |
| Junction Temperature                      | +150°C                       |
| Storage Temperature                       | –65°C to +150°C              |
| Lead Temperature<br>(Soldering, 4sec.)    | +260°C                       |
| Maximum Package Power Dissipation at 25°C |                              |
| UQFN-28                                   | 4.31 W                       |
| Derating above 25°C                       |                              |
| UQFN-28                                   | 34.5 mW/°C                   |
| Thermal Resistance, $\theta_{JA}$         |                              |
| UQFN-28                                   | 29°C/W                       |
| ESD Rating                                |                              |
| HBM, 1.5 k $\Omega$ , 100 pF              | 6.5 kV                       |
| EIAJ, 0 $\Omega$ , 200 pF                 | >250V                        |

- (1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

## Recommended Operating Conditions

|                                  | Min | Typ | Max | Unit |
|----------------------------------|-----|-----|-----|------|
| Supply Voltage ( $V_{DD}$ – GND) | 3.0 | 3.3 | 3.6 | V    |
| Receiver Input Voltage           | 0   |     | 3.6 | V    |
| Operating Free Air Temperature   | –40 | 25  | 85  | °C   |
| Junction Temperature             |     |     | 150 | °C   |

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

| Symbol                                                      | Parameter                                                   | Conditions                                                                                                          | Min  | Typ<br>(1) | Max             | Units |
|-------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|------|------------|-----------------|-------|
| LVTTTL DC SPECIFICATIONS (SEL0, SEL1, EN1, EN2)             |                                                             |                                                                                                                     |      |            |                 |       |
| V <sub>IH</sub>                                             | High Level Input Voltage                                    |                                                                                                                     | 2.0  |            | V <sub>DD</sub> | V     |
| V <sub>IL</sub>                                             | Low Level Input Voltage                                     |                                                                                                                     | GND  |            | 0.8             | V     |
| I <sub>IH</sub>                                             | High Level Input Current                                    | V <sub>IN</sub> = V <sub>DD</sub> = V <sub>DDMAX</sub>                                                              | −10  |            | +10             | μA    |
| I <sub>IL</sub>                                             | Low Level Input Current                                     | V <sub>IN</sub> = V <sub>SS</sub> , V <sub>DD</sub> = V <sub>DDMAX</sub>                                            | −10  |            | +10             | μA    |
| C <sub>IN1</sub>                                            | Input Capacitance                                           | Any Digital Input Pin to V <sub>SS</sub>                                                                            |      | 3.5        |                 | pF    |
| V <sub>CL</sub>                                             | Input Clamp Voltage                                         | I <sub>CL</sub> = −18 mA                                                                                            | −1.5 | −0.8       |                 | V     |
| LVDS INPUT DC SPECIFICATIONS (IN0±, IN1±)                   |                                                             |                                                                                                                     |      |            |                 |       |
| V <sub>TH</sub>                                             | Differential Input High Threshold <sup>(2)</sup>            | V <sub>CM</sub> = 0.8V or 1.2V or 3.55V, V <sub>DD</sub> = 3.6V                                                     |      | 0          | 100             | mV    |
| V <sub>TL</sub>                                             | Differential Input Low Threshold                            | V <sub>CM</sub> = 0.8V or 1.2V or 3.55V, V <sub>DD</sub> = 3.6V                                                     | −100 | 0          |                 | mV    |
| V <sub>ID</sub>                                             | Differential Input Voltage                                  | V <sub>CM</sub> = 0.8V to 3.55V, V <sub>DD</sub> = 3.6V                                                             | 100  |            |                 | mV    |
| V <sub>CMR</sub>                                            | Common Mode Voltage Range                                   | V <sub>ID</sub> = 150 mV, V <sub>DD</sub> = 3.6V                                                                    | 0.05 |            | 3.55            | V     |
| C <sub>IN2</sub>                                            | Input Capacitance                                           | IN+ or IN− to V <sub>SS</sub>                                                                                       |      | 3.5        |                 | pF    |
| I <sub>IN</sub>                                             | Input Current                                               | V <sub>IN</sub> = 3.6V, V <sub>DD</sub> = V <sub>DDMAX</sub> or 0V                                                  | −10  |            | +10             | μA    |
|                                                             |                                                             | V <sub>IN</sub> = 0V, V <sub>DD</sub> = V <sub>DDMAX</sub> or 0V                                                    | −10  |            | +10             | μA    |
| LVDS OUTPUT DC SPECIFICATIONS (OUT0±, OUT1±)                |                                                             |                                                                                                                     |      |            |                 |       |
| V <sub>OD</sub>                                             | Differential Output Voltage, 0% Pre-emphasis <sup>(2)</sup> | R <sub>L</sub> = 100Ω between OUT+ and OUT−                                                                         | 250  | 400        | 575             | mV    |
| ΔV <sub>OD</sub>                                            | Change in V <sub>OD</sub> between Complementary States      |                                                                                                                     | −35  |            | 35              | mV    |
| V <sub>OS</sub>                                             | Offset Voltage <sup>(3)</sup>                               |                                                                                                                     | 1.09 | 1.25       | 1.475           | V     |
| ΔV <sub>OS</sub>                                            | Change in V <sub>OS</sub> between Complementary States      |                                                                                                                     | −35  |            | 35              | mV    |
| I <sub>OS</sub>                                             | Output Short Circuit Current, One Complementary Output      | OUT+ or OUT− Short to GND                                                                                           |      | −60        | −90             | mA    |
| C <sub>OUT</sub>                                            | Output Capacitance                                          | OUT+ or OUT− to GND when TRI-STATE                                                                                  |      | 5.5        |                 | pF    |
| SUPPLY CURRENT (Static)                                     |                                                             |                                                                                                                     |      |            |                 |       |
| I <sub>CC0</sub>                                            | Supply Current                                              | All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT−.         |      | 42         | 60              | mA    |
| I <sub>CC1</sub>                                            | Supply Current - one channel powered down                   | Single channel crossover switch or single channel repeater modes (1 channel active, one channel in power down mode) |      | 22         | 30              | mA    |
| I <sub>CC2</sub>                                            | Supply Current - one input powered down                     | Splitter mode (One input powered down, both outputs active)                                                         |      | 30         | 40              | mA    |
| I <sub>CCZ</sub>                                            | TRI-STATE Supply Current                                    | Both input/output Channels in Power Down Mode                                                                       |      | 1.4        | 2.5             | mA    |
| SWITCHING CHARACTERISTICS—LVDS OUTPUTS (Figure 4, Figure 5) |                                                             |                                                                                                                     |      |            |                 |       |
| t <sub>LHT</sub>                                            | Differential Low to High Transition Time                    | Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V <sub>OD</sub> .                    | 70   | 150        | 215             | ps    |
| t <sub>HLT</sub>                                            | Differential High to Low Transition Time                    |                                                                                                                     | 50   | 135        | 180             | ps    |
| t <sub>PLHD</sub>                                           | Differential Low to High Propagation Delay                  | Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V <sub>OD</sub> between input to output.             | 0.5  | 2.4        | 3.5             | ns    |
| t <sub>PHLD</sub>                                           | Differential High to Low Propagation Delay                  |                                                                                                                     | 0.5  | 2.4        | 3.5             | ns    |
| t <sub>SKD1</sub>                                           | Pulse Skew                                                  | t <sub>PLHD</sub> − t <sub>PHLD</sub>                                                                               |      | 55         | 120             | ps    |

(1) Typical parameters are measured at  $V_{DD} = 3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$ . They are for reference purposes, and are not production-tested.

(2) Differential output voltage  $V_{OD}$  is defined as  $\text{ABS}(\text{OUT+} - \text{OUT-})$ . Differential input voltage  $V_{ID}$  is defined as  $\text{ABS}(\text{IN+} - \text{IN-})$ .

(3) Output offset voltage  $V_{OS}$  is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

## Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified.

| Symbol     | Parameter                               | Conditions                                                                                                                              | Min | Typ<br>(1) | Max | Units |
|------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----|------------|-----|-------|
| $t_{SKCC}$ | Output Channel to Channel Skew          | Difference in propagation delay ( $t_{PLHD}$ or $t_{PHLD}$ ) among all output channels in Splitter mode (any one input to all outputs). | 0   | 130        | 315 | ps    |
| $t_{JIT}$  | Jitter<br>(4)                           | RJ - Clock Pattern<br>750 MHz (5)                                                                                                       |     | 1.4        | 2.5 | psrms |
|            |                                         | DJ - K28.5 Pattern<br>1.5 Gbps (6)                                                                                                      |     | 42         | 75  | psp-p |
|            |                                         | TJ - PRBS $2^{23}-1$ Pattern<br>1.5 Gbps (7)                                                                                            |     | 93         | 126 | psp-p |
| $t_{ON}$   | LVDS Output Enable Time                 | Time from $\overline{ENx}$ to $OUT\pm$ change from TRI-STATE to active.                                                                 | 50  | 110        | 150 | ns    |
| $t_{OFF}$  | LVDS Output Disable Time                | Time from $\overline{ENx}$ to $OUT\pm$ change from active to TRI-STATE.                                                                 |     | 5          | 12  | ns    |
| $t_{SW}$   | LVDS Switching Time<br>SELx to $OUT\pm$ | Time from configuration select (SELx) to new switch configuration effective for $OUT\pm$ .                                              |     | 110        | 150 | ns    |

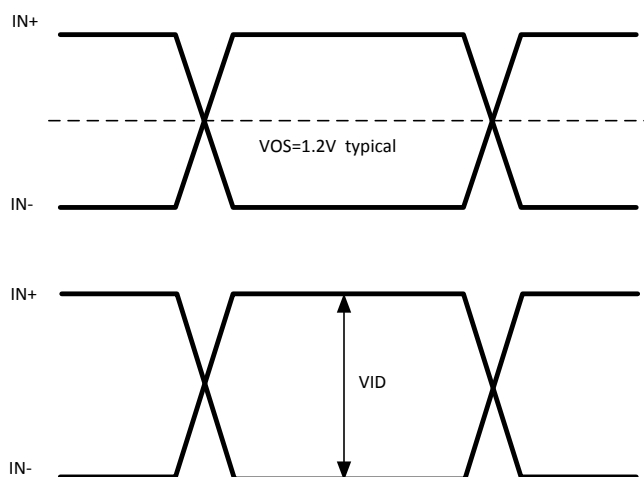
(4) Jitter is not production tested, but guaranteed through characterization on a sample basis.

(5) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage =  $V_{ID} = 500\text{mV}$ , 50% duty cycle at 750MHz,  $t_r = t_f = 50\text{ps}$  (20% to 80%).

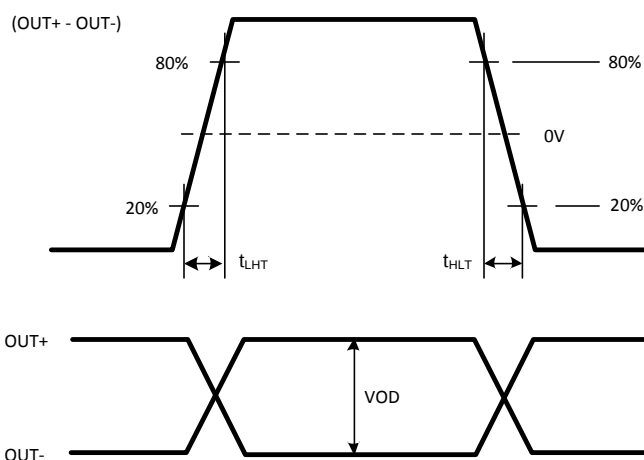
(6) Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage =  $V_{ID} = 500\text{mV}$ , K28.5 pattern at 1.5 Gbps,  $t_r = t_f = 50\text{ps}$  (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

(7) Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage =  $V_{ID} = 500\text{mV}$ ,  $2^{23}-1$  PRBS pattern at 1.5 Gbps,  $t_r = t_f = 50\text{ps}$  (20% to 80%).

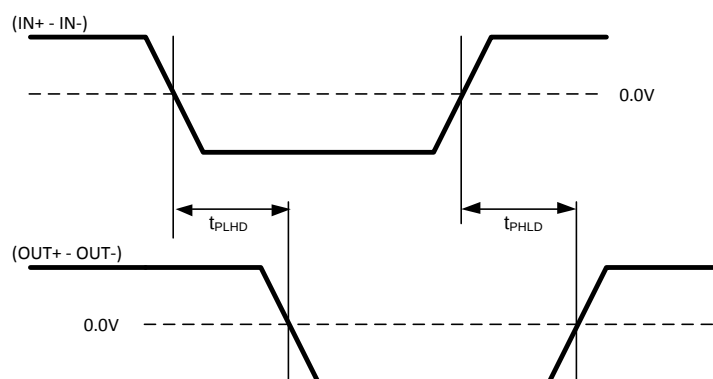
## Timing Diagrams



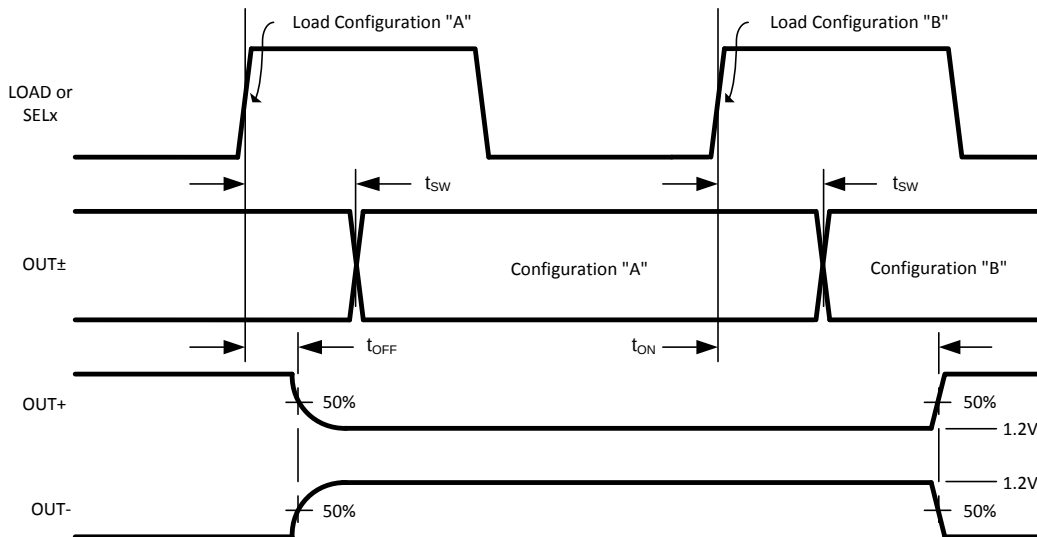
**Figure 4. LVDS Signals**



**Figure 5. LVDS Output Transition Time**

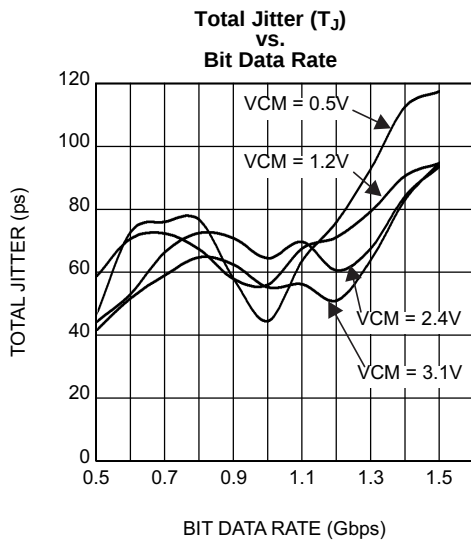


**Figure 6. LVDS Output Propagation Delay**



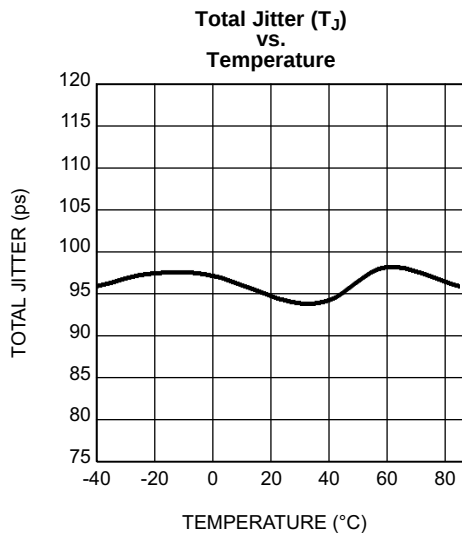
**Figure 7. Configuration and Output Enable/Disable Timing**

## Typical Performance



Total Jitter measured at 0V differential while running a PRBS  $2^{23}-1$  pattern in single channel repeater mode.  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ ,  $V_{ID} = 0.5V$

**Figure 8.**



Total Jitter measured at 0V differential while running a PRBS  $2^{23}-1$  pattern in dual channel repeater mode.  $V_{CC} = 3.3V$ ,  $V_{ID} = 0.5V$ ,  $V_{CM} = 1.2V$ , 1.5 Gbps data rate

**Figure 9.**

REVISION HISTORY

| Changes from Original (March 2013) to Revision A           | Page              |
|------------------------------------------------------------|-------------------|
| • Changed layout of National Data Sheet to TI format ..... | <a href="#">9</a> |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DS90CP02SP/NOPB  | ACTIVE        | UQFN         | NJD                | 28   | 1000           | RoHS & Green    | SN                                   | Level-3-260C-168 HR  | -40 to 85    | CP02SP                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS90CP02SP/NOPB | UQFN         | NJD             | 28   | 1000 | 178.0              | 12.4               | 5.3     | 5.3     | 1.3     | 8.0     | 12.0   | Q1            |

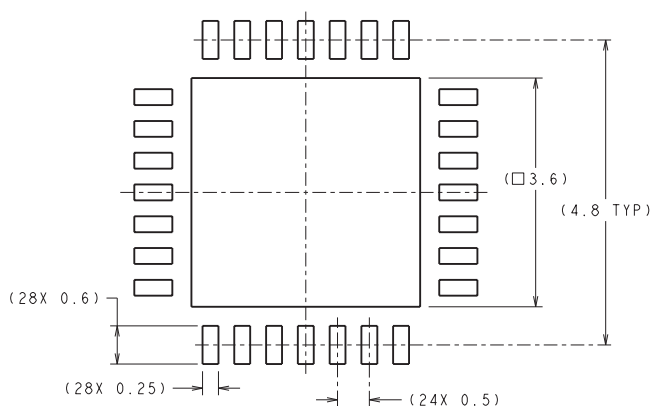
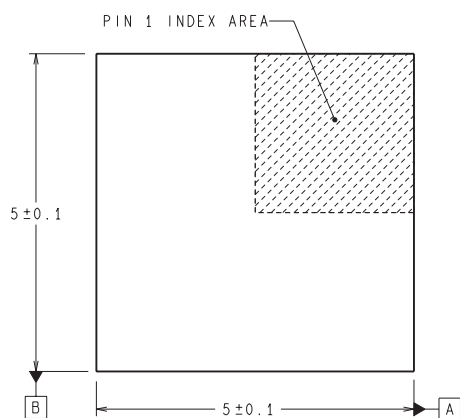
## TAPE AND REEL BOX DIMENSIONS



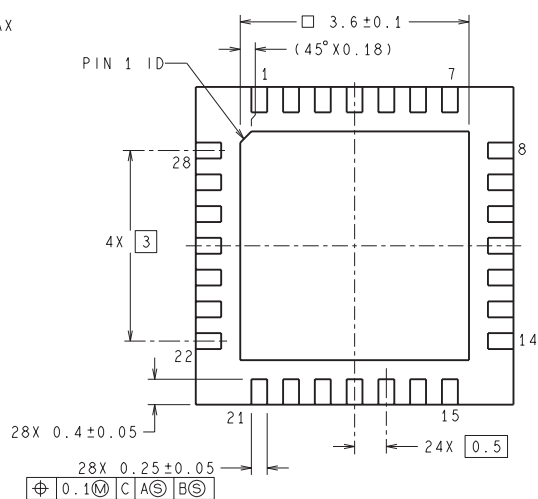
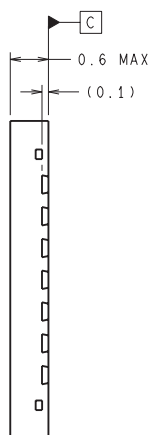
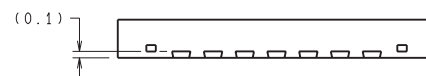
\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS90CP02SP/NOPB | UQFN         | NJD             | 28   | 1000 | 208.0       | 191.0      | 35.0        |

NJD0028A

**RECOMMENDED LAND PATTERN**

**DIMENSIONS ARE IN MILLIMETERS**  
 DIMENSIONS IN ( ) FOR REFERENCE ONLY



SPA28A (Rev A)

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