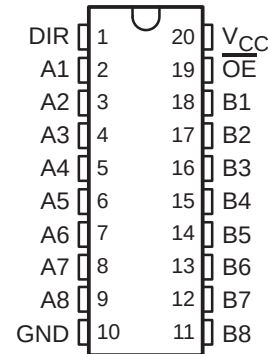


# SN74LVCZ245A OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES275G – JUNE 1999 – REVISED AUGUST 2003

- Operates From 2.7 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.3 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  
<0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
>2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



## description/ordering information

This octal bus transceiver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCZ245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

## ORDERING INFORMATION

| $T_A$         | PACKAGE†   |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N   | Tube of 20   | SN74LVCZ245AN         | SN74LVCZ245AN    |
|               | SOIC – DW  | Tube of 25   | SN74LVCZ245ADW        | LVCZ245A         |
|               |            | Reel of 2000 | SN74LVCZ245ADWR       |                  |
|               | SOP – NS   | Reel of 2000 | SN74LVCZ245ANSR       | LVCZ245A         |
|               | SSOP – DB  | Reel of 2000 | SN74LVCZ245ADBR       | CV245A           |
|               | TSSOP – PW | Tube of 70   | SN74LVCZ245APW        | CV245A           |
|               |            | Reel of 2000 | SN74LVCZ245APWR       | CV245A           |
|               |            | Reel of 250  | SN74LVCZ245APWT       | CV245A           |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

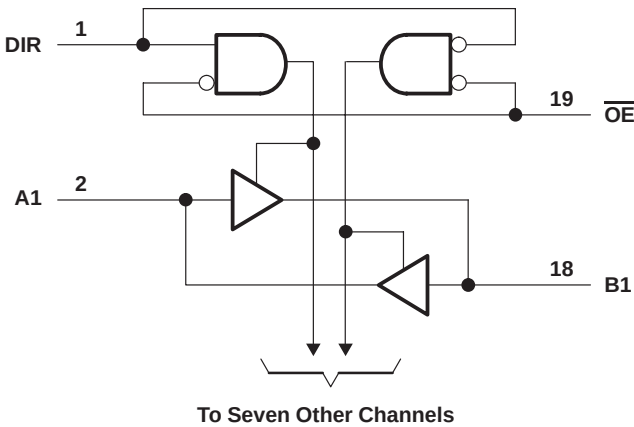
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FUNCTION TABLE

| INPUTS |     | OPERATION       |
|--------|-----|-----------------|
| OE     | DIR |                 |
| L      | L   | B data to A bus |
| L      | H   | A data to B bus |
| H      | X   | Isolation       |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                                  |                            |
|--------------------------------------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                                                   | –0.5 V to 6.5 V            |
| Input voltage range, $V_I$ (see Note 1)                                                          | –0.5 V to 6.5 V            |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | –0.5 V to 6.5 V            |
| Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)          | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                                      | –50 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                                     | –50 mA                     |
| Continuous output current, $I_O$                                                                 | ±50 mA                     |
| Continuous current through $V_{CC}$ or GND                                                       | ±100 mA                    |
| Package thermal impedance, $\theta_{JA}$ (see Note 3):                                           |                            |
| DB package                                                                                       | 70°C/W                     |
| DW package                                                                                       | 58°C/W                     |
| N package                                                                                        | 89°C/W                     |
| NS package                                                                                       | 60°C/W                     |
| PW package                                                                                       | 83°C/W                     |
| Storage temperature range, $T_{stg}$                                                             | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  - The package thermal impedance is calculated in accordance with JESD 51-7.

**SN74LVCZ245A**  
**OCTAL BUS TRANSCEIVER**  
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**recommended operating conditions (see Note 4)**

|                     |                                    |                                  | MIN | MAX             | UNIT |
|---------------------|------------------------------------|----------------------------------|-----|-----------------|------|
| V <sub>CC</sub>     | Supply voltage                     |                                  | 2.7 | 3.6             | V    |
| V <sub>IH</sub>     | High-level input voltage           | V <sub>CC</sub> = 2.7 V to 3.6 V | 2   |                 | V    |
| V <sub>IL</sub>     | Low-level input voltage            | V <sub>CC</sub> = 2.7 V to 3.6 V |     | 0.8             | V    |
| V <sub>I</sub>      | Input voltage                      |                                  | 0   | 5.5             | V    |
| V <sub>O</sub>      | Output voltage                     | High or low state                | 0   | V <sub>CC</sub> | V    |
|                     |                                    | 3-state                          | 0   | 5.5             |      |
| I <sub>OH</sub>     | High-level output current          | V <sub>CC</sub> = 2.7 V          |     | –12             | mA   |
|                     |                                    | V <sub>CC</sub> = 3 V            |     | –24             |      |
| I <sub>OL</sub>     | Low-level output current           | V <sub>CC</sub> = 2.7 V          |     | 12              | mA   |
|                     |                                    | V <sub>CC</sub> = 3 V            |     | 24              |      |
| Δt/Δv               | Input transition rise or fall rate |                                  |     | 6               | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 |                                  | 150 |                 | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     |                                  | –40 | 85              | °C   |

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                    | TEST CONDITIONS                                                              | V <sub>CC</sub>                          | MIN                  | TYP <sup>†</sup> | MAX  | UNIT |
|------------------------------|------------------------------------------------------------------------------|------------------------------------------|----------------------|------------------|------|------|
| V <sub>OH</sub>              | I <sub>OH</sub> = –100 μA                                                    | 2.7 V to 3.6 V                           | V <sub>CC</sub> –0.2 |                  |      | V    |
|                              | I <sub>OH</sub> = –12 mA                                                     | 2.7 V                                    | 2.2                  |                  |      |      |
|                              |                                                                              | 3 V                                      | 2.4                  |                  |      |      |
|                              | I <sub>OH</sub> = –24 mA                                                     | 3 V                                      | 2.2                  |                  |      |      |
| V <sub>OL</sub>              | I <sub>OL</sub> = 100 μA                                                     | 2.7 V to 3.6 V                           |                      |                  | 0.2  | V    |
|                              | I <sub>OL</sub> = 12 mA                                                      | 2.7 V                                    |                      |                  | 0.4  |      |
|                              | I <sub>OL</sub> = 24 mA                                                      | 3 V                                      |                      |                  | 0.55 |      |
|                              |                                                                              |                                          |                      |                  |      |      |
| I <sub>I</sub>               | Control inputs                                                               | V <sub>I</sub> = 0 to 5.5 V              |                      |                  | ±5   | μA   |
| I <sub>off</sub>             |                                                                              | V <sub>I</sub> or V <sub>O</sub> = 5.5 V | 0                    |                  | ±5   | μA   |
| I <sub>OZ</sub> <sup>‡</sup> |                                                                              | V <sub>O</sub> = 0 to 5.5 V              |                      |                  | ±5   | μA   |
| I <sub>OZPU</sub>            | V <sub>O</sub> = 0.5 V to 2.5 V, $\overline{\text{OE}}$ = don't care         | 0 to 1.5 V                               |                      |                  | ±5   | μA   |
| I <sub>OZPD</sub>            | V <sub>O</sub> = 0.5 V to 2.5 V, $\overline{\text{OE}}$ = don't care         | 1.5 V to 0                               |                      |                  | ±5   | μA   |
| I <sub>CC</sub>              | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V                                    |                      |                  | 100  | μA   |
|                              | 3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>§</sup>                                  |                                          |                      |                  | 100  |      |
| ΔI <sub>CC</sub>             | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V                           |                      |                  | 100  | μA   |
| C <sub>i</sub>               | Control inputs                                                               | V <sub>I</sub> = V <sub>CC</sub> or GND  | 3.3 V                | 4                |      | pF   |
| C <sub>io</sub>              | A or B ports                                                                 | V <sub>O</sub> = V <sub>CC</sub> or GND  | 3.3 V                | 6                |      | pF   |

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>§</sup> This applies in the disabled state only.



**SN74LVCZ245A**  
**OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

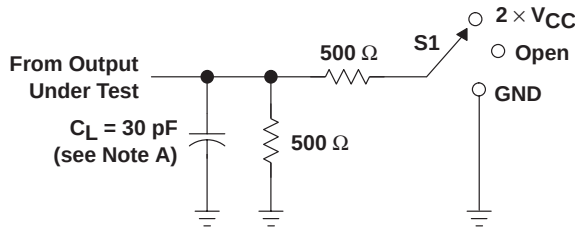
| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | UNIT |
|-----------|-----------------|----------------|-------------------------|-----|------------------------------------------|-----|------|
|           |                 |                | MIN                     | MAX | MIN                                      | MAX |      |
| $t_{pd}$  | A or B          | B or A         |                         | 7.3 | 1.5                                      | 6.3 | ns   |
| $t_{en}$  | $\overline{OE}$ | A or B         |                         | 9.5 | 1.5                                      | 8.5 | ns   |
| $t_{dis}$ | $\overline{OE}$ | A or B         |                         | 8.5 | 1.7                                      | 7.5 | ns   |

operating characteristics,  $T_A = 25^\circ\text{C}$

| PARAMETER                                              |                  |                     | TEST<br>CONDITIONS | $V_{CC} = 3.3\text{ V}$ | UNIT |
|--------------------------------------------------------|------------------|---------------------|--------------------|-------------------------|------|
|                                                        |                  |                     |                    | TYP                     |      |
| $C_{pd}$ Power dissipation capacitance per transceiver | Outputs enabled  | $f = 10\text{ MHz}$ |                    | 42                      | pF   |
|                                                        | Outputs disabled |                     |                    | 3                       |      |

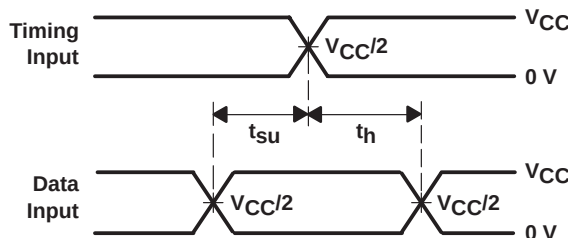
# PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

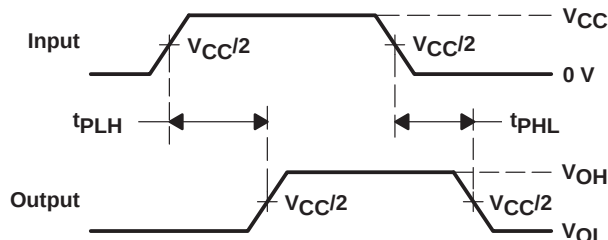


LOAD CIRCUIT

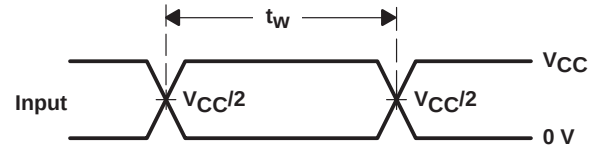
| TEST              | S1                |
|-------------------|-------------------|
| $t_{pd}$          | Open              |
| $t_{PLZ}/t_{PZL}$ | 2 $\times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |



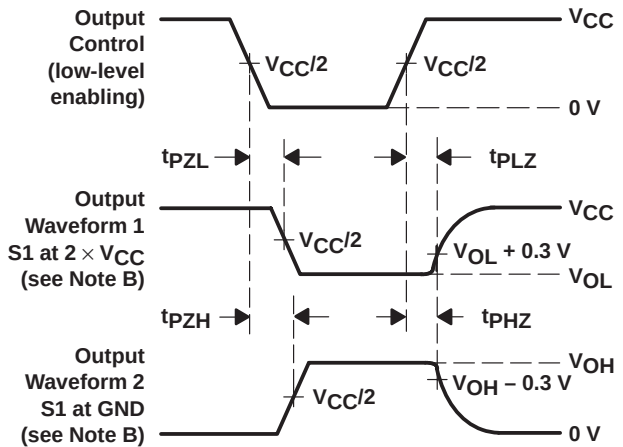
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVCZ245ADBR  | ACTIVE        | SSOP         | DB                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CV245A                  | <a href="#">Samples</a> |
| SN74LVCZ245ADWR  | ACTIVE        | SOIC         | DW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVCZ245A                | <a href="#">Samples</a> |
| SN74LVCZ245ANSR  | ACTIVE        | SO           | NS                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVCZ245A                | <a href="#">Samples</a> |
| SN74LVCZ245APW   | ACTIVE        | TSSOP        | PW                 | 20   | 70             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CV245A                  | <a href="#">Samples</a> |
| SN74LVCZ245APWR  | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CV245A                  | <a href="#">Samples</a> |
| SN74LVCZ245APWT  | ACTIVE        | TSSOP        | PW                 | 20   | 250            | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CV245A                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

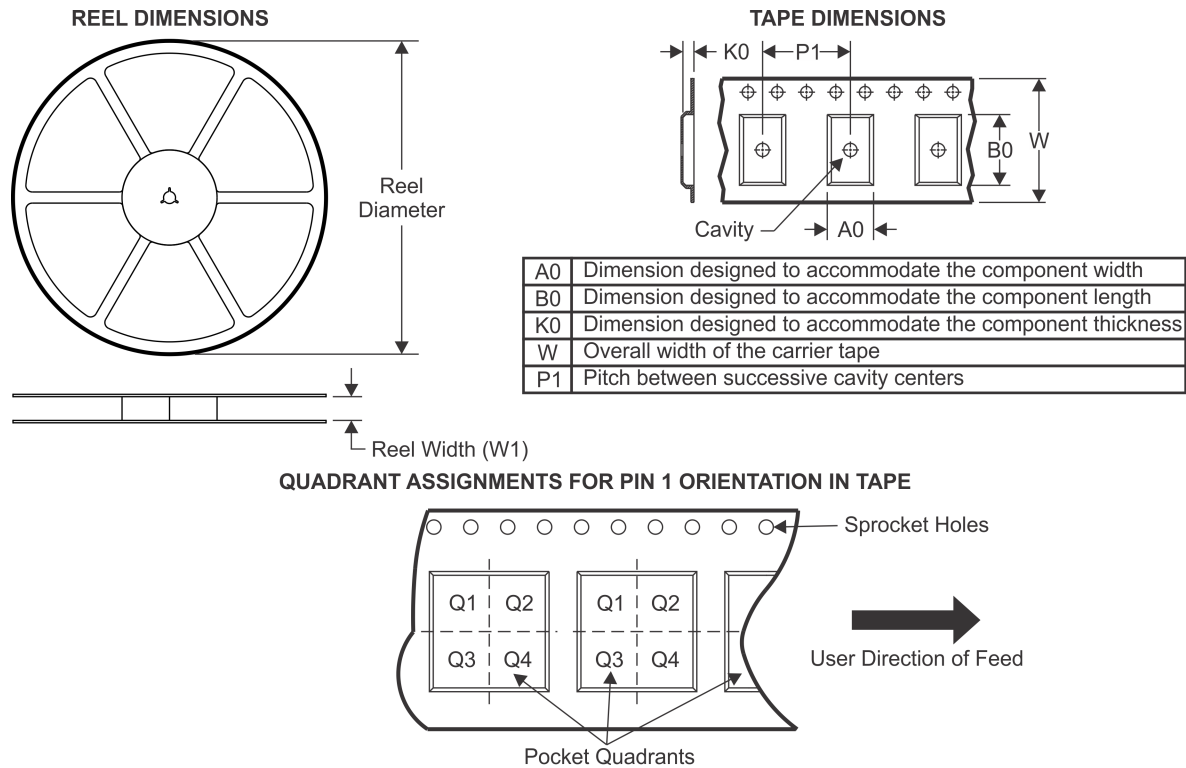
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

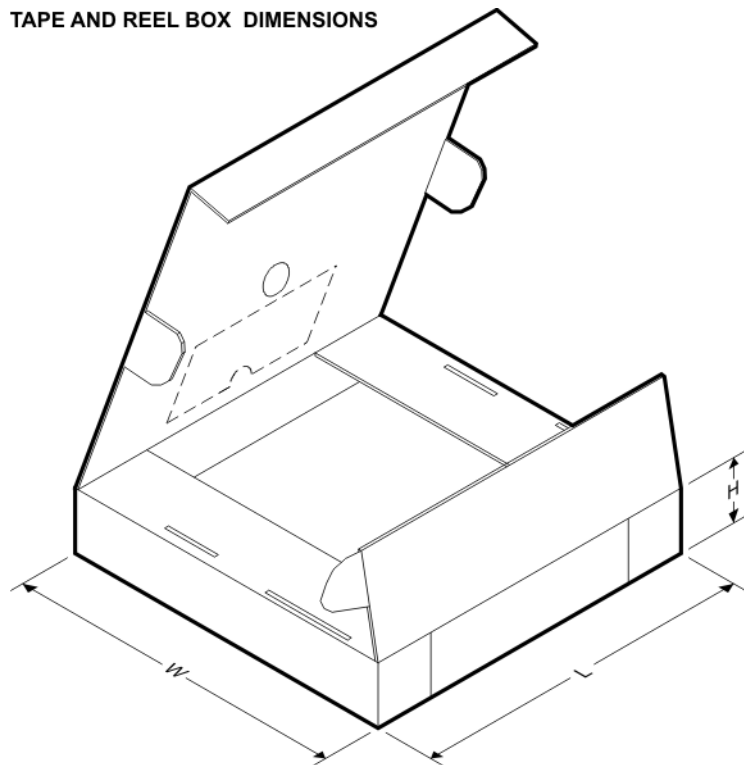


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVCZ245ADBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVCZ245ADWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LVCZ245ANSR | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LVCZ245APWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVCZ245APWT | TSSOP        | PW              | 20   | 250  | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |



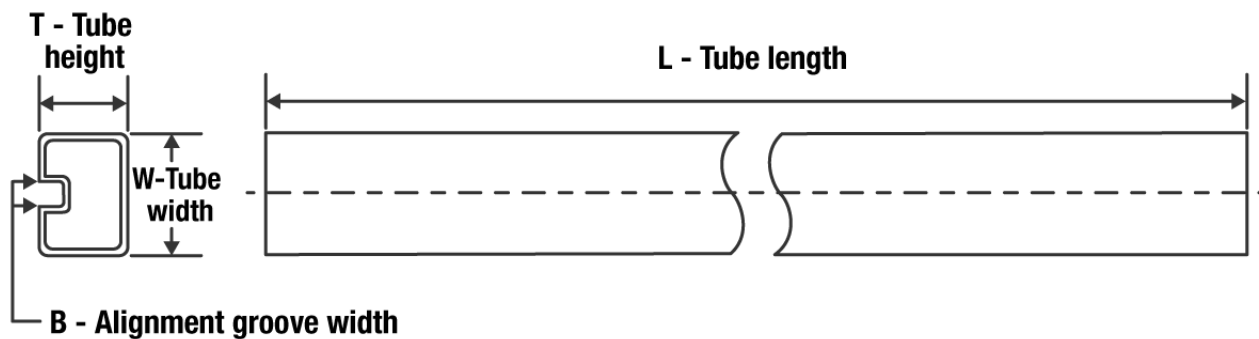
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

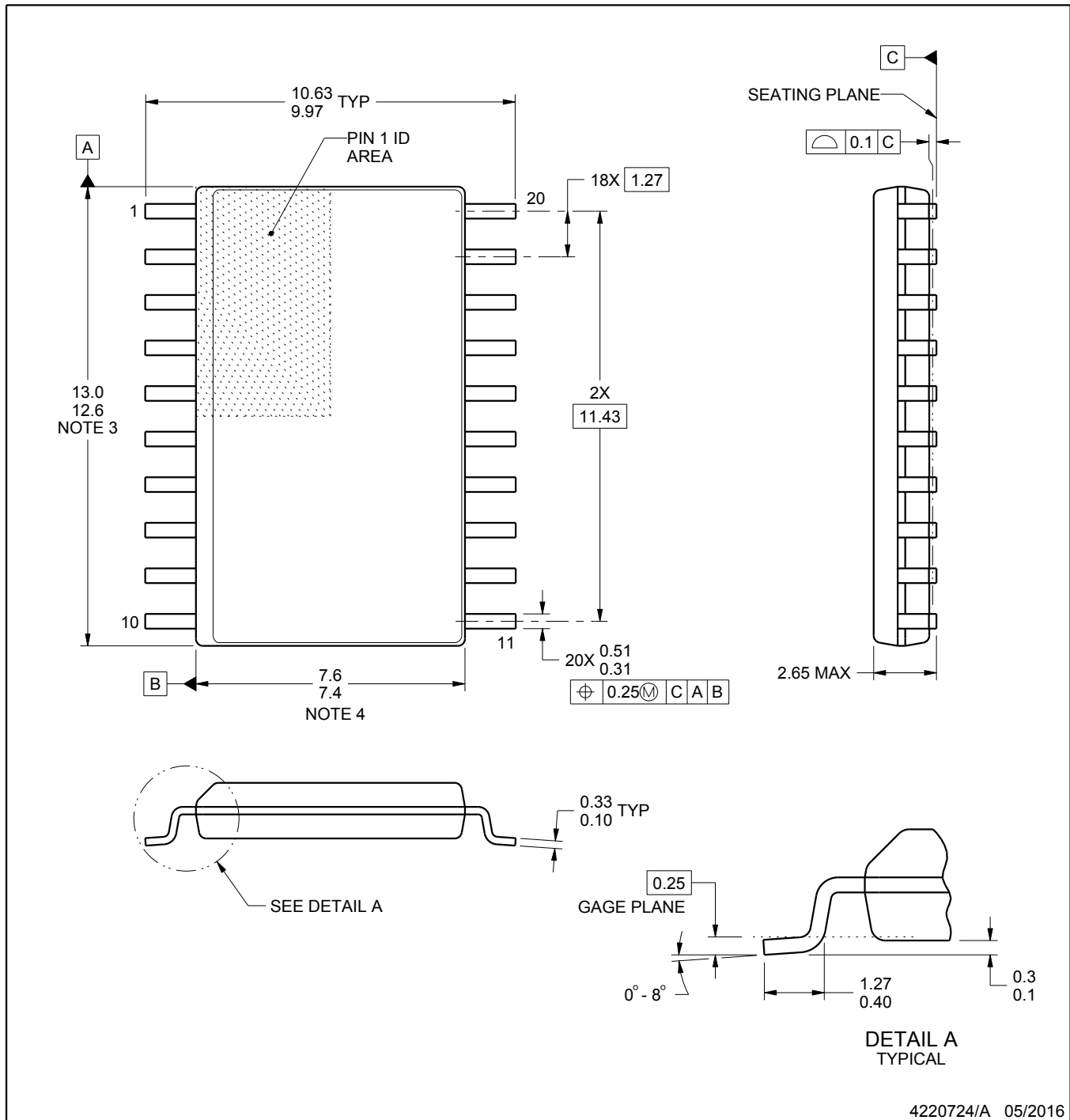
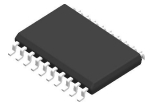
| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVCZ245ADBR | SSOP         | DB              | 20   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVCZ245ADWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVCZ245ANSR | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVCZ245APWR | TSSOP        | PW              | 20   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVCZ245APWT | TSSOP        | PW              | 20   | 250  | 853.0       | 449.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVCZ245APW | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |



4220724/A 05/2016

## NOTES:

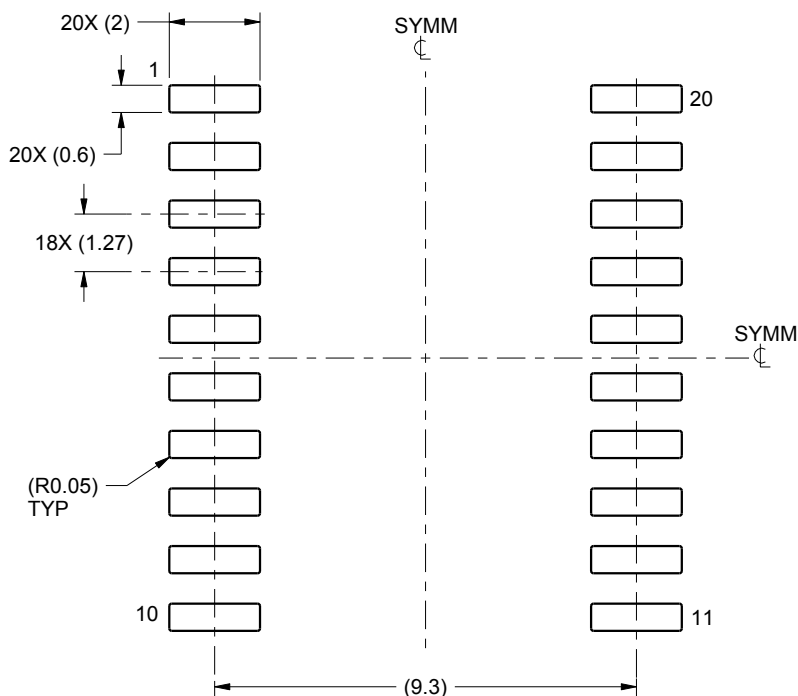
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

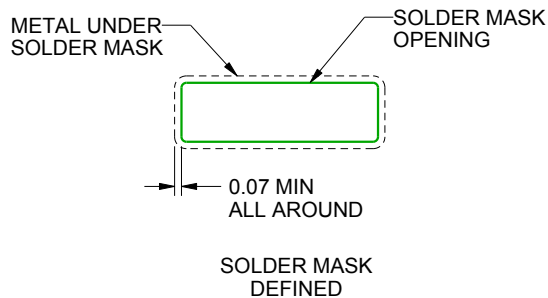
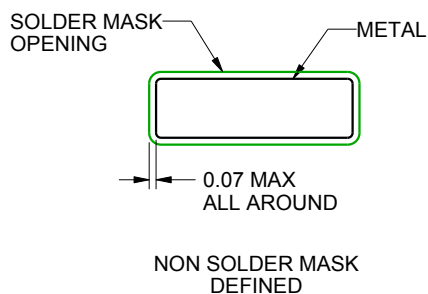
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

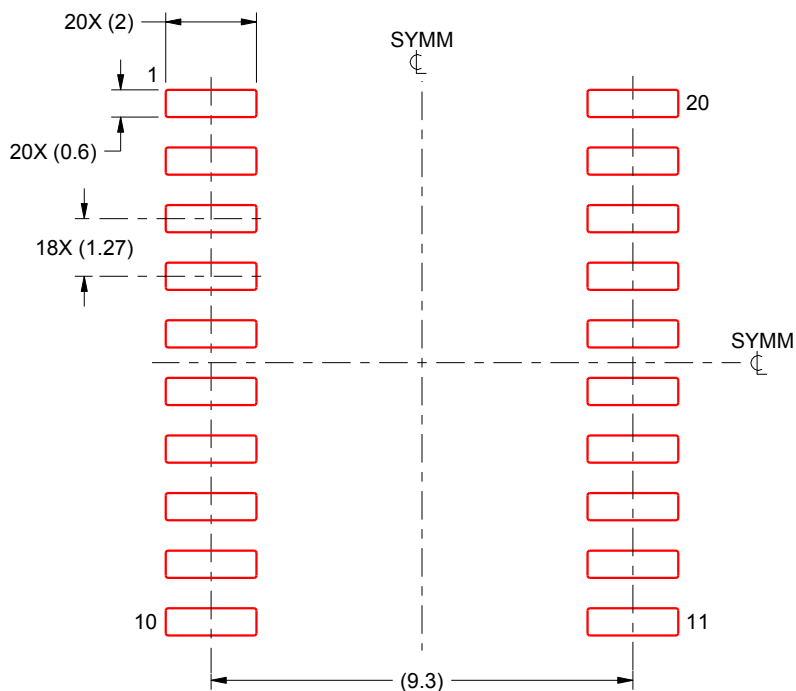
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

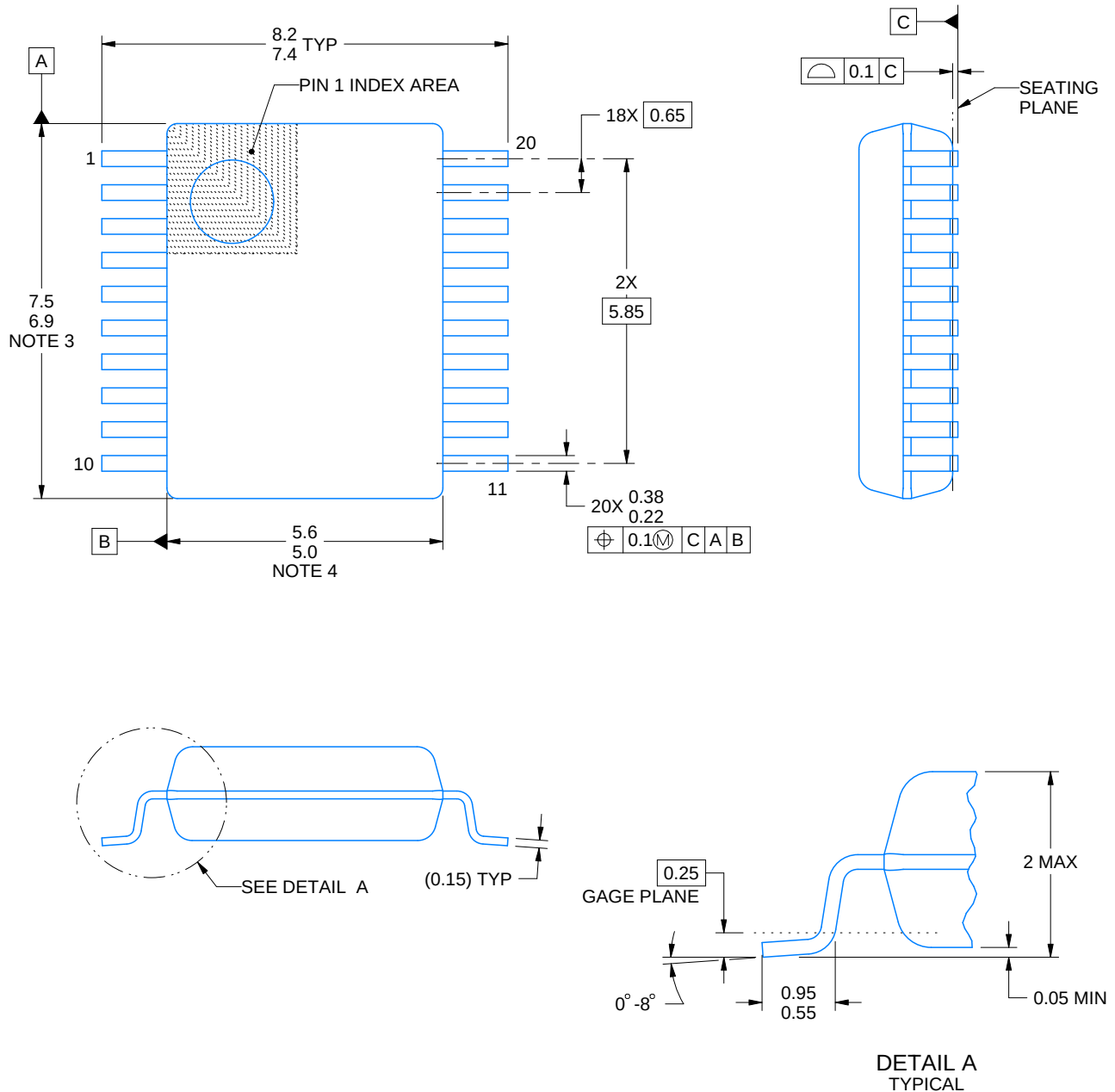
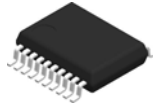


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

## NOTES:

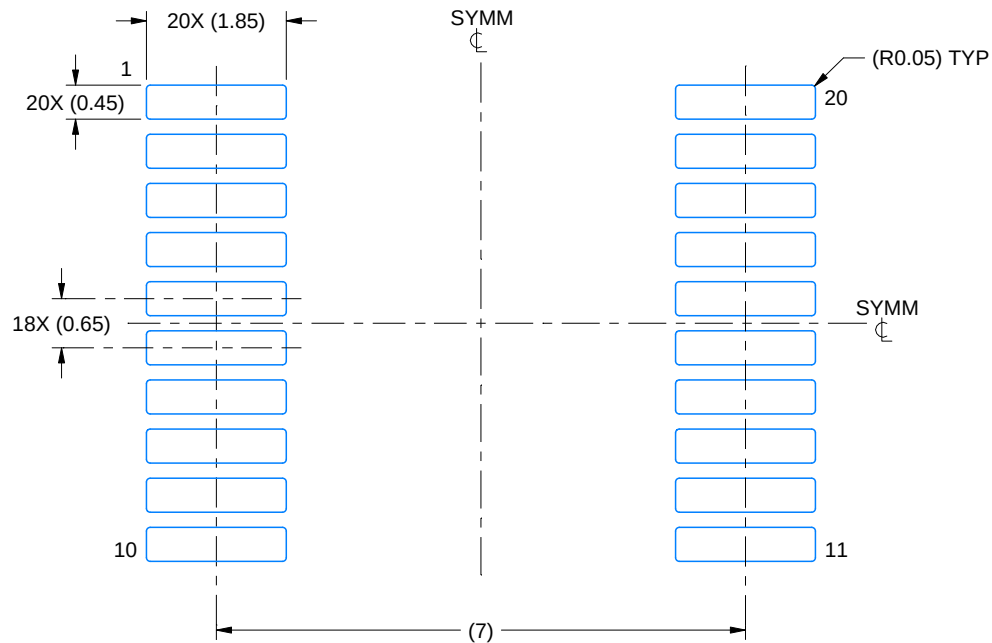
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

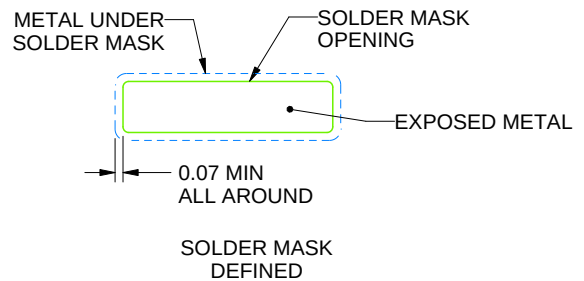
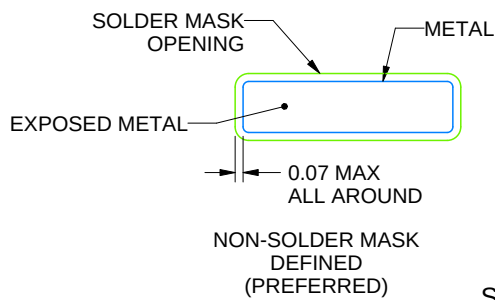
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

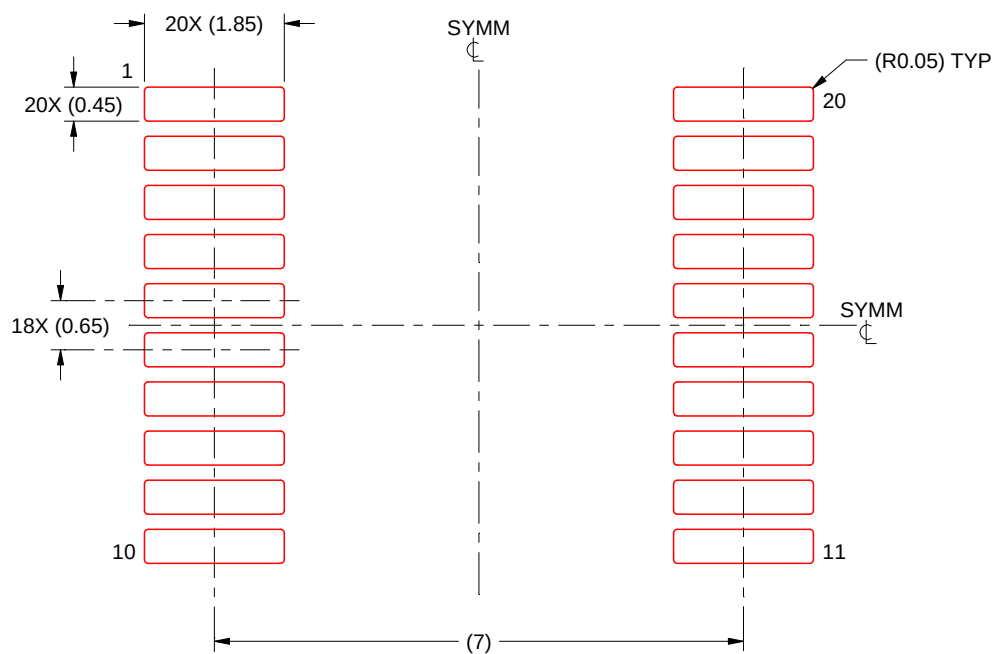
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

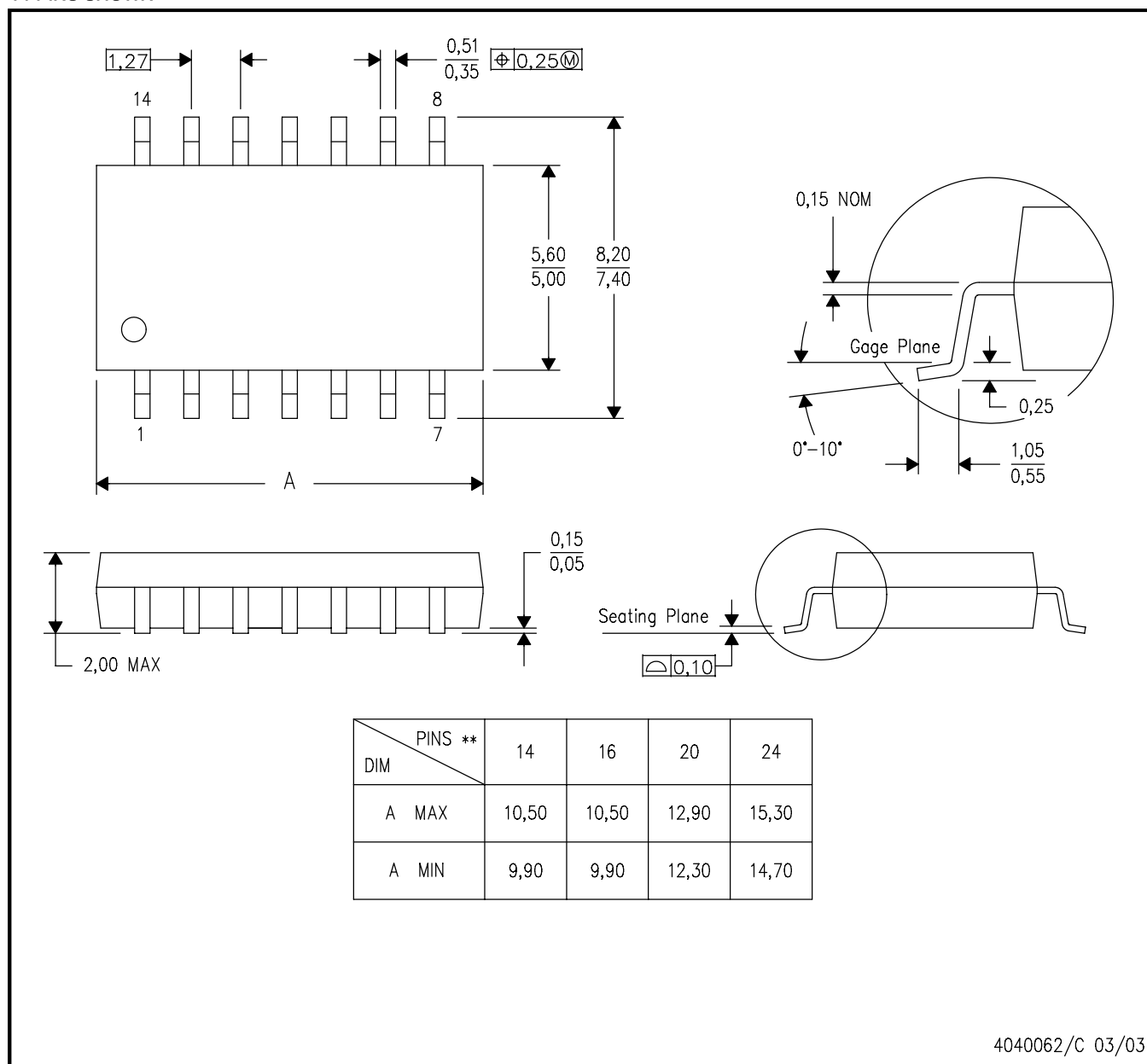


# MECHANICAL DATA

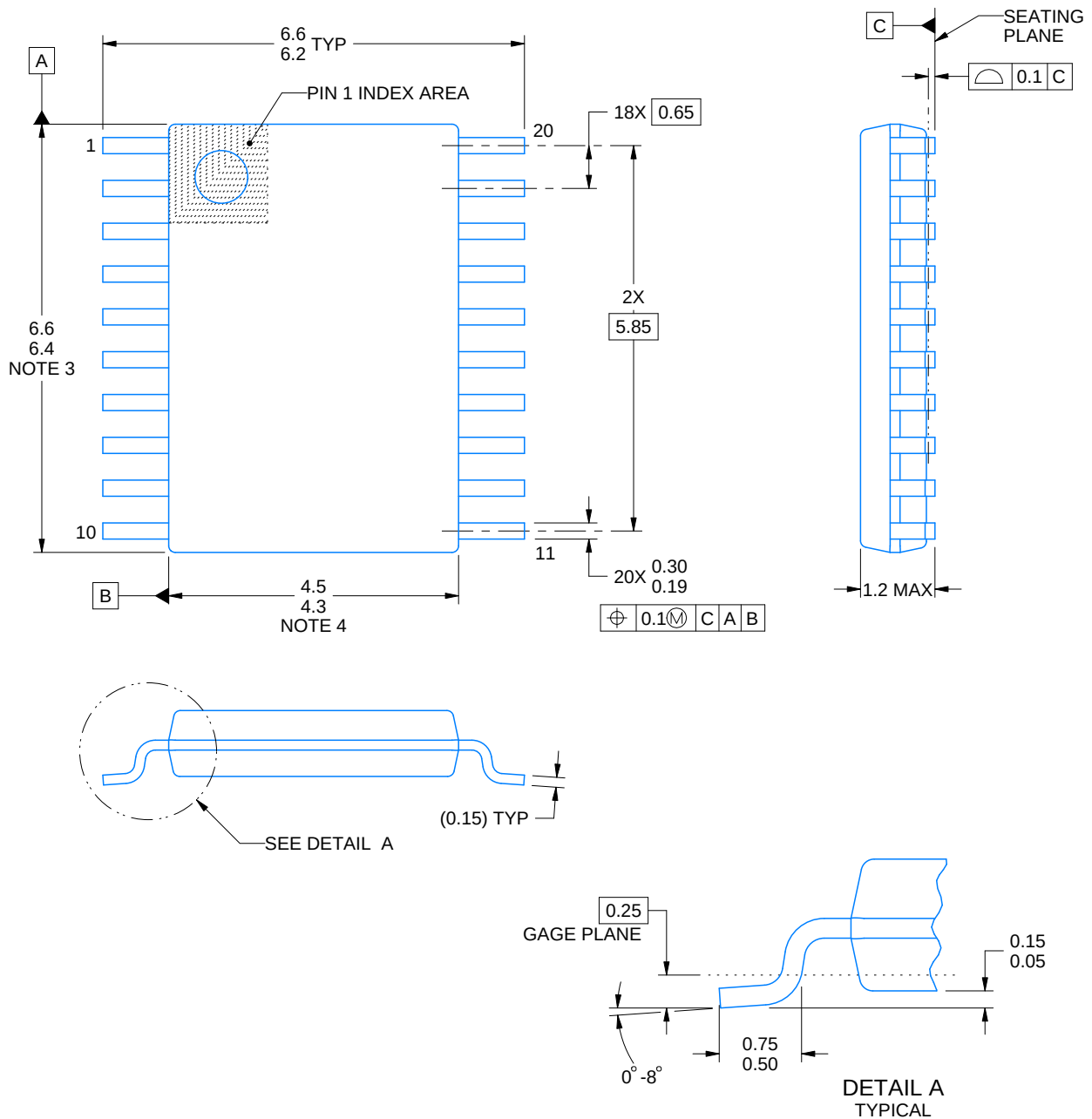
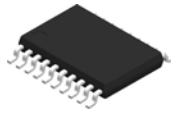
NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



4220206/A 02/2017

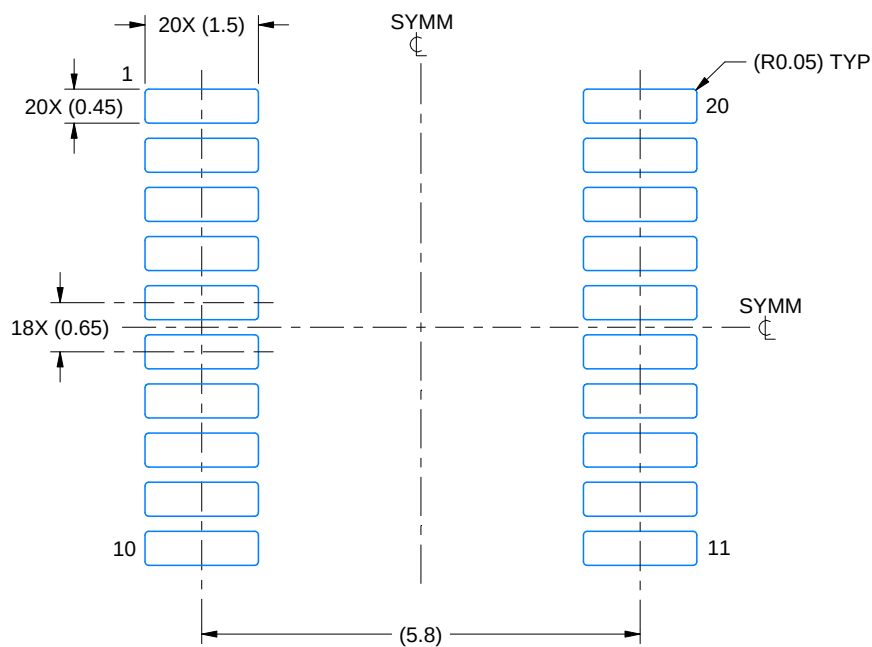
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

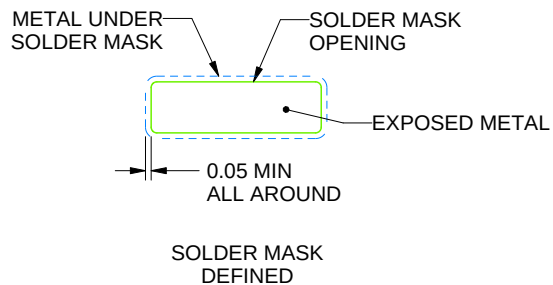
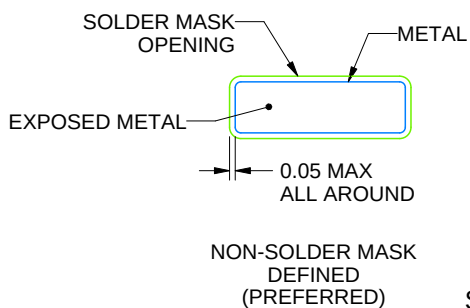
**PW0020A**

**TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

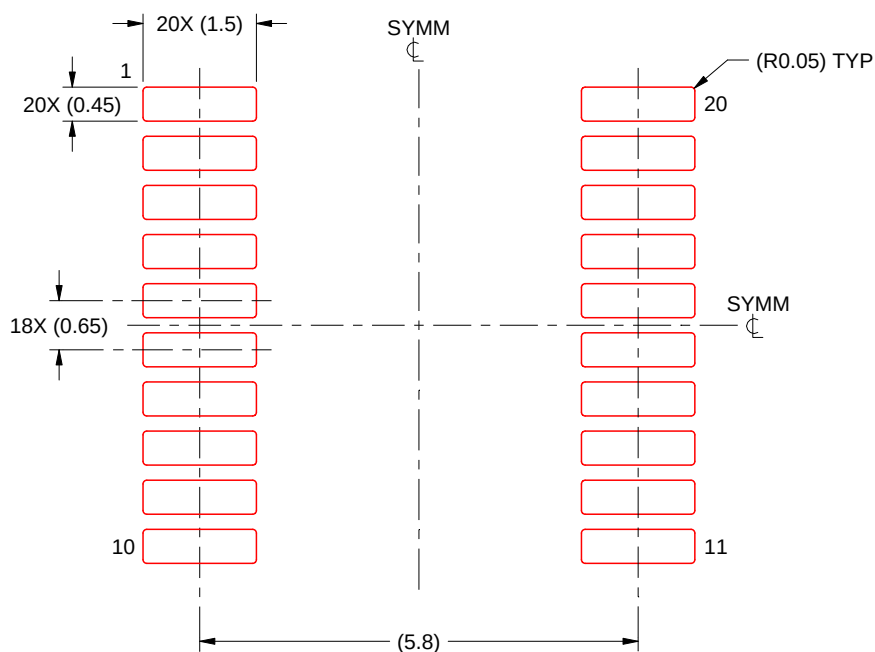
6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

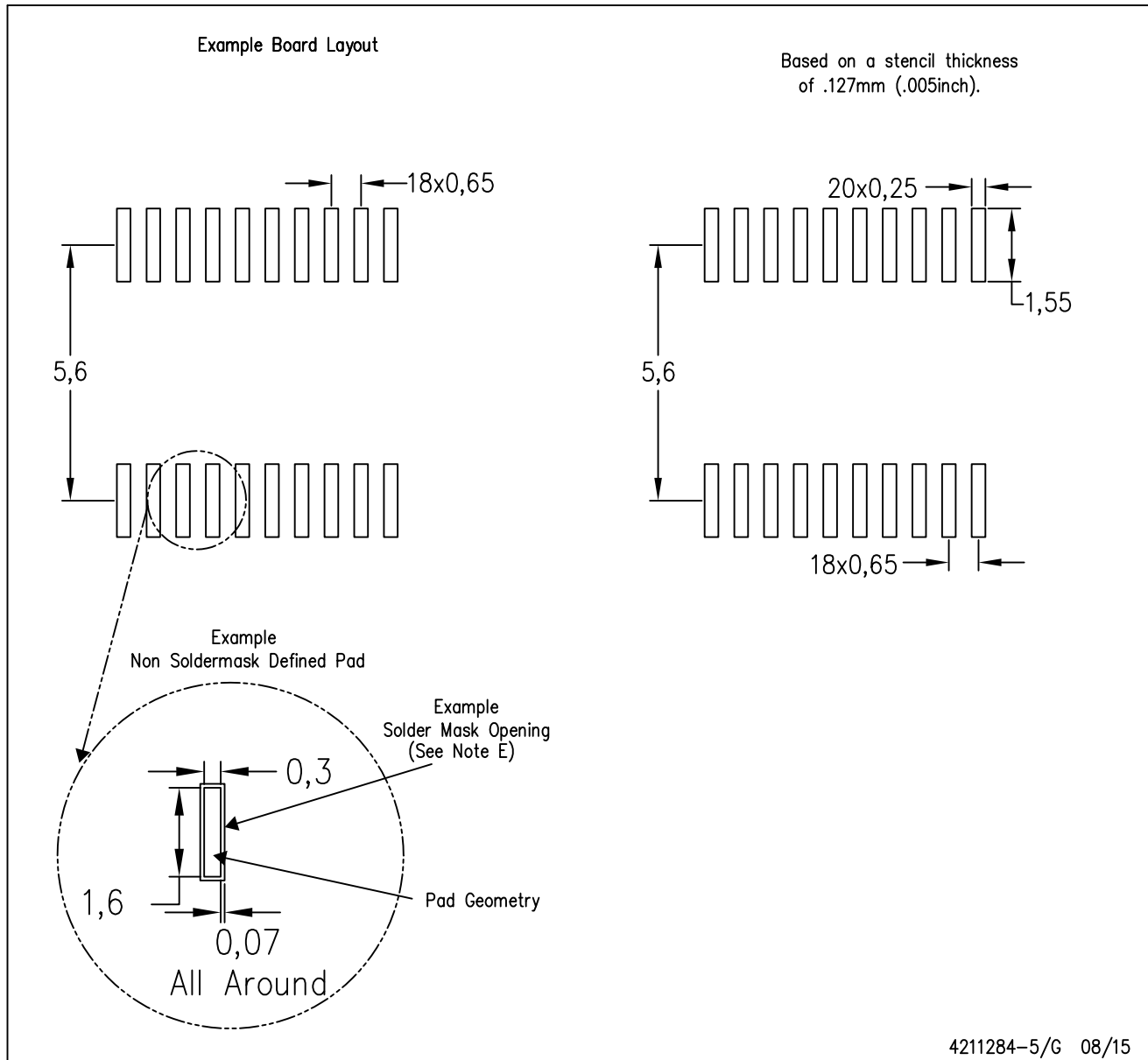
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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