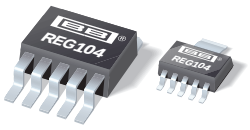
REG104



SBVS025G – SEPTEMBER 2001 – REVISED SEPTEMBER 2005

DMOS
1A Low-Dropout Regulator

FEATURES

- **NEW DMOS TOPOLOGY:**
  Ultra Low Dropout Voltage:
  230mV typ at 1A and 3.3V Output
  Output Capacitor NOT Required for Stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE: 33μV_{RMS}**
- **HIGH ACCURACY: ±2% max**
- **HIGH EFFICIENCY:**
  I_{GND} = 1.7mA at I_{OUT} = 1A
  Not Enabled: I_{GND} = 0.5μA
- **2.5V, 2.7V, 3.0V, 3.3V, 5.0V AND ADJUSTABLE OUTPUT VERSIONS**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES:**
  SOT223-5, DDPAK-5

APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

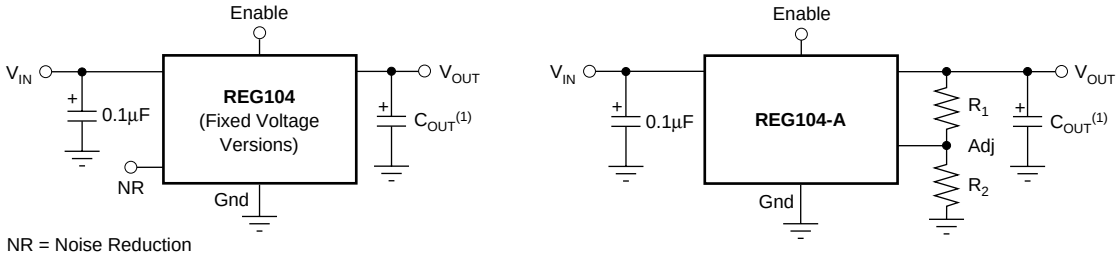
DESCRIPTION

The REG104 is a family of low-noise, low-dropout linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low dropout voltage (only 230mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1µF.

Typical ground pin current is only 1.7mA (at I_{OUT} = 1A) and drops to 0.5µA in *not enabled* mode. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG104 has very low output noise (typically 33μV_{RMS} for V_{OUT} = 3.3V with C_{NR} = 0.01µF), making it ideal for use in portable communications equipment. On-chip trimming results in high output voltage accuracy. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The REG104 is well protected—internal circuitry provides a current limit which protects the load from damage. Thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG104 is available in the DDPAK-5 and the SOT223-5.



NOTE: (1) Optional.

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Input Voltage, V_{IN}	–0.3V to 16V
Enable Input Voltage, V_{EN}	–0.3V to V_{IN}
Feedback Voltage, V_{FB}	–0.3V to 6.0V
NR Pin Voltage, V_{NR}	–0.3V to 6.0V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	–55°C to +150°C
Lead Temperature (soldering, 3s, SOT, and DDPAK)	+240°C
ESD Rating: HBM (V_{OUT} to GND)	1.5kV
HBM (All other pins)	2kV
CDM	500V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

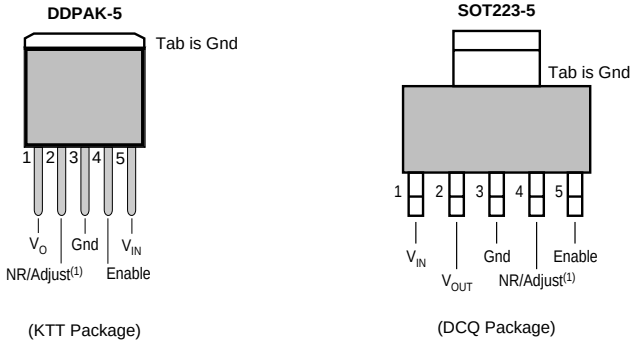
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
REG104**xx-*yyyy/zzz***	**XX** is package designator. **YYYY** is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable). **ZZZ** is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

Top View



(KTT Package) (DCQ Package)

NOTE: (1) For REG104A-A: voltage setting resistor pin.
All other models: noise reduction capacitor pin.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_J = –40°C to +85°C**

At T_J = +25°C, V_{IN} = V_{OUT} + 1V (V_{OUT} = 3.0V for REG104-A), V_{ENABLE} = 2V, I_{OUT} = 10mA, C_{NR} = 0.01µF, and C_{OUT} = 0.1µF[1], unless otherwise noted.

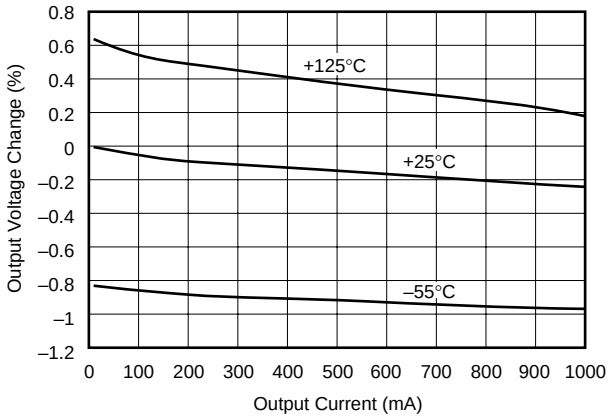
PARAMETER		CONDITION	REG104GA REG104FA MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT}					
REG104-2.5				2.5		V
REG104-2.7				2.7		V
REG104-3.0				3.0		V
REG104-3.3				3.3		V
REG104-5				5		V
REG104-A			V_{REF}		5.5	V
Reference Voltage	V_{REF}			1.295		V
Adjust Pin Current	I_{ADJ}			0.2	1	µA
Accuracy				±0.5	±2	%
T_J = –40°C to +85°C					**±3.0**	%
vs Temperature	**dV_{OUT}/dT**	**T_J = –40°C to +85°C**		**70**		ppm/°C
vs Line and Load		I_{OUT} = 10mA to 1A, V_{IN} = (V_{OUT} + 0.7V) to 15V		±0.5	±2.5	%
T_J = –40°C to +85°C		**V_{IN} = (V_{OUT} + 0.9V) to 15V**			**±3.5**	**%**
DC DROPOUT VOLTAGE[2, 3]	V_{DROP}	I_{OUT} = 10mA		3	25	mV
For all models except 5V		I_{OUT} = 1A		230	400	mV
For 5V model		I_{OUT} = 1A		320	500	mV
For all models except 5V		**I_{OUT} = 1A**			**480**	mV
T_J = –40°C to +85°C						
For 5V models		**I_{OUT} = 1A**			**580**	mV
T_J = –40°C to +85°C						
VOLTAGE NOISE						
f = 10Hz to 100kHz	V_n					
Without C_{NR} (all models)		C_{NR} = 0, C_{OUT} = 0		35µV_{RMS}/V • V_{OUT}		µV_{RMS}
With C_{NR} (all fixed voltage models)		C_{NR} = 0.01µF, C_{OUT} = 10µF		10µV_{RMS}/V • V_{OUT}		µV_{RMS}
OUTPUT CURRENT						
Current Limit[4]	I_{CL}		1.2	1.7	2.1	A
T_J = –40°C to +85°C			**1.0**		**2.2**	A
RIPPLE REJECTION						
f = 120Hz				65		dB
ENABLE CONTROL						
V_{ENABLE} High (output enabled)	V_{ENABLE}		2		V_{IN}	V
V_{ENABLE} Low (output disabled)			–0.2		0.5	V
I_{ENABLE} High (output enabled)	I_{ENABLE}	V_{ENABLE} = 2V to V_{IN}, V_{IN} = 2.1V to 6.5[5]		1	100	nA
I_{ENABLE} Low (output disabled)		V_{ENABLE} = 0V to 0.5V		2	100	nA
Output Disable Time				50		µs
Output Enable Softstart Time				1.5		ms
THERMAL SHUTDOWN						
Junction Temperature						
Shutdown				150		°C
Reset from Shutdown				130		°C
GROUND PIN CURRENT						
Ground Pin Current	I_{GND}	I_{OUT} = 10mA		0.5	0.7	mA
		I_{OUT} = 1A		1.7	1.8	mA
Enable Pin Low		V_{ENABLE} ≤ 0.5V		0.5		µA
INPUT VOLTAGE	V_{IN}					
Operating Input Voltage Range[6]			2.1		15	V
Specified Input Voltage Range		V_{IN} > 2.7V	V_{OUT} + 0.7		15	V
T_J = –40°C to +85°C		**V_{IN} > 2.9V**	**V_{OUT} + 0.9**		**15**	V
TEMPERATURE RANGE						
Specified Range	T_J		–40		+85	°C
Operating Range			–55		+125	°C
Storage Range			–65		+150	°C
Thermal Resistance						
DDPAK-5 Surface Mount	θ_{JC}	Junction-to-Case		4		°C/W
SOT223-5 Surface Mount	θ_{JC}	Junction-to-Case		15		°C/W

NOTES: (1) The REG104 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.
(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at V_{IN} = V_{OUT} + 1V at fixed load.
(3) Not applicable for V_{OUT} less than 2.7V.
(4) Current limit is the output current that produces a 15% change in output voltage from V_{IN} = V_{OUT} + 1V and I_{OUT} = 10mA.
(5) For V_{IN} > 6.5V, see typical characteristic *V_{ENABLE} vs I_{ENABLE}*.
(6) The REG104 no longer regulates when V_{IN} < V_{OUT} + $V_{DROP\ (MAX)}$. In drop-out or when the input voltage is between 2.7V and 2.1V, the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at T_J = +25°C. See typical characteristic *Output Voltage Change vs V_{IN}*.

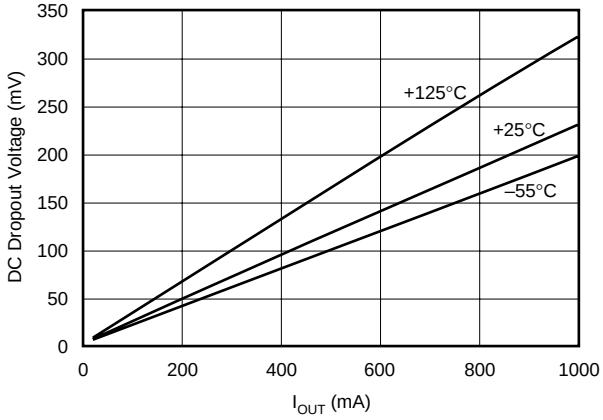
TYPICAL CHARACTERISTICS

For all models, at T_J = +25°C and V_{ENABLE} = 2V, unless otherwise noted.

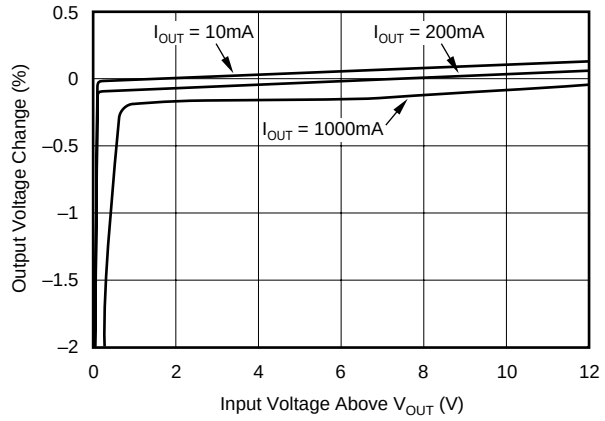
OUTPUT VOLTAGE CHANGE vs I_{OUT}
(V_{IN} = V_{OUT} + 1V, Output Voltage % Change Referred to I_{OUT} = 10mA at +25°C)



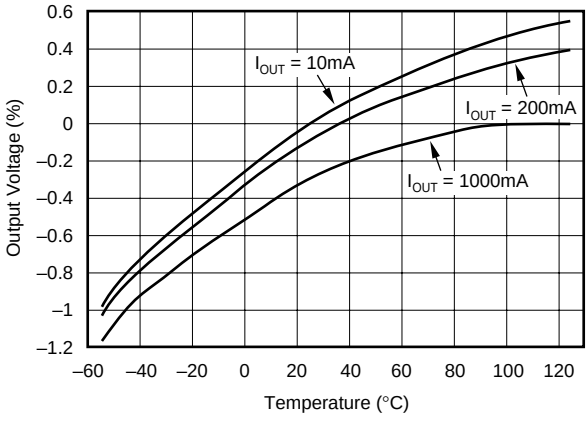
DC DROPOUT VOLTAGE vs I_{OUT}



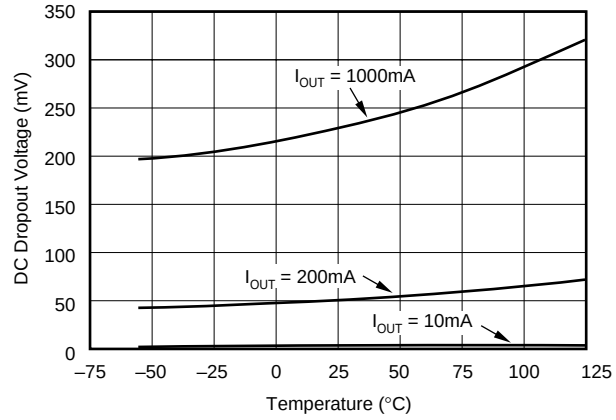
OUTPUT VOLTAGE CHANGE vs V_{IN}
(Output Voltage % Change Referred to V_{IN} = V_{OUT} + 1V at I_{OUT} = 10mA)



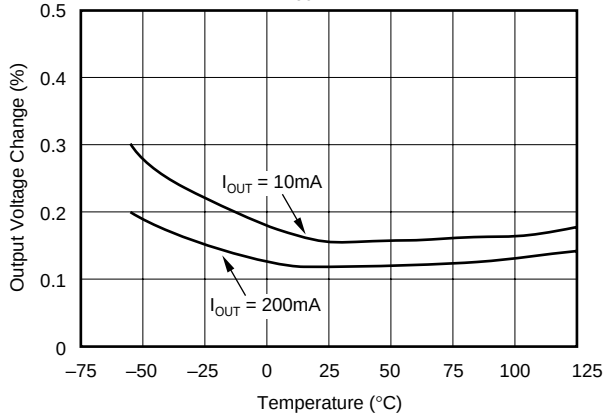
OUTPUT VOLTAGE CHANGE vs I_{OUT}
(Output Voltage % Change Referred to I_{OUT} = 10mA at +25°C)



DC DROPOUT VOLTAGE vs TEMPERATURE



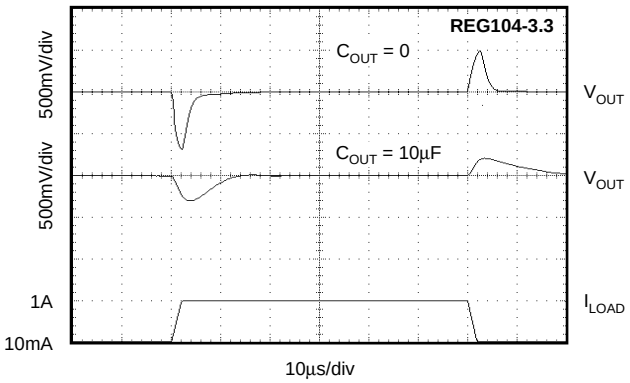
LINE REGULATION vs TEMPERATURE
(V_{IN} = V_{OUT} + 1V to 16V)



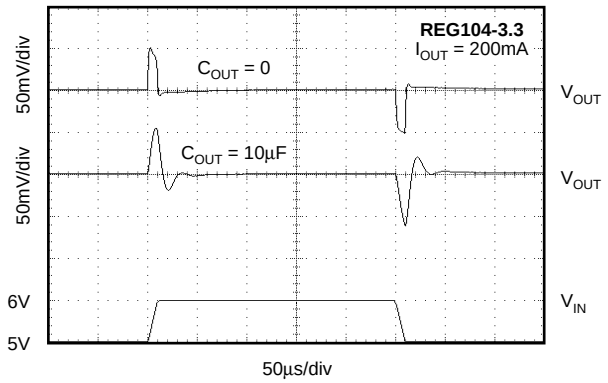
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 2V, unless otherwise noted.

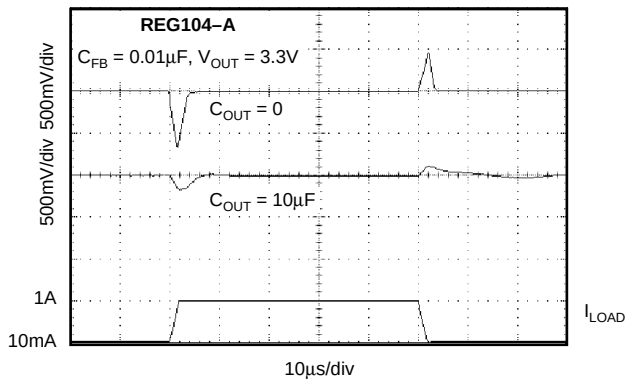
LOAD TRANSIENT RESPONSE



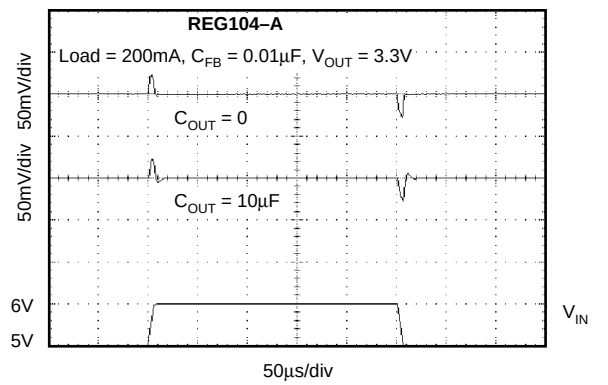
LINE TRANSIENT RESPONSE



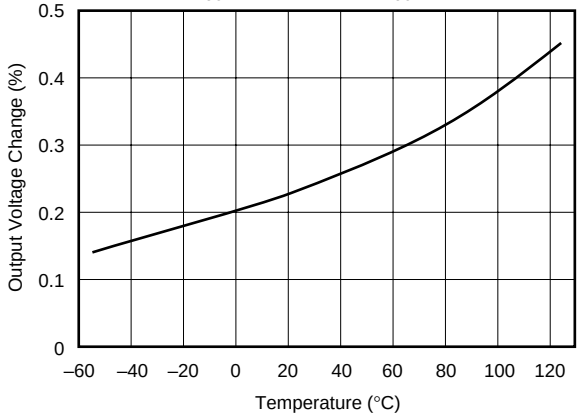
LOAD TRANSIENT RESPONSE



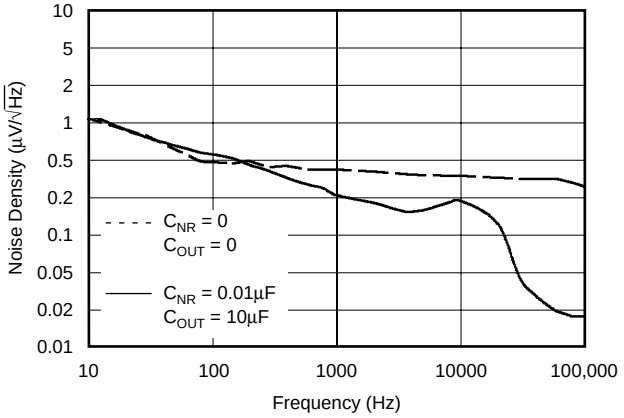
LOAD TRANSIENT RESPONSE



LOAD REGULATION vs TEMPERATURE
(V_{IN} = V_{OUT} + 1V and 10mA < I_{OUT} < 1000mA)



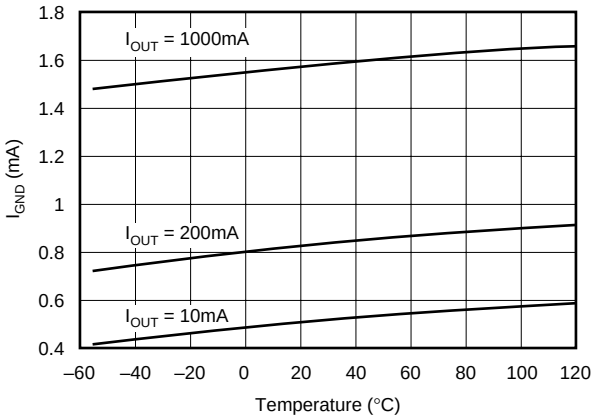
OUTPUT NOISE DENSITY



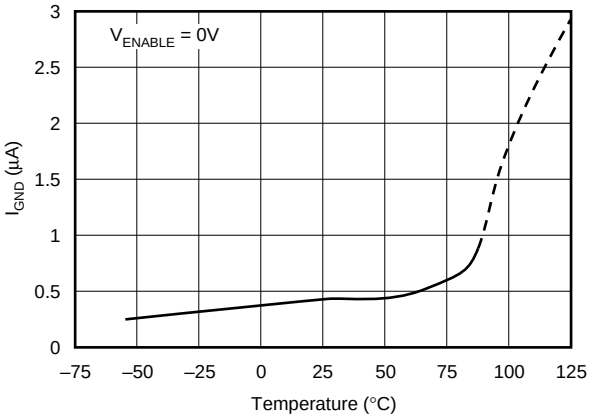
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 2V, unless otherwise noted.

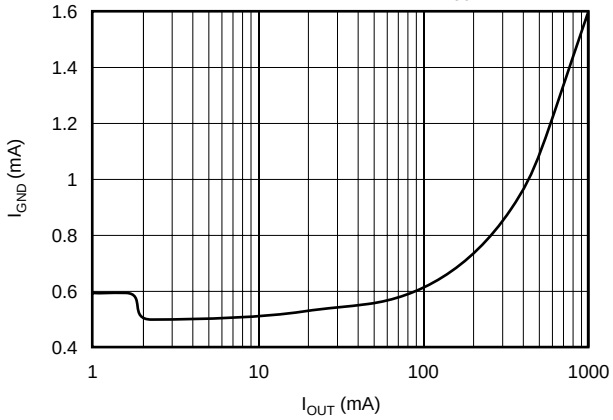
GROUND PIN CURRENT vs TEMPERATURE



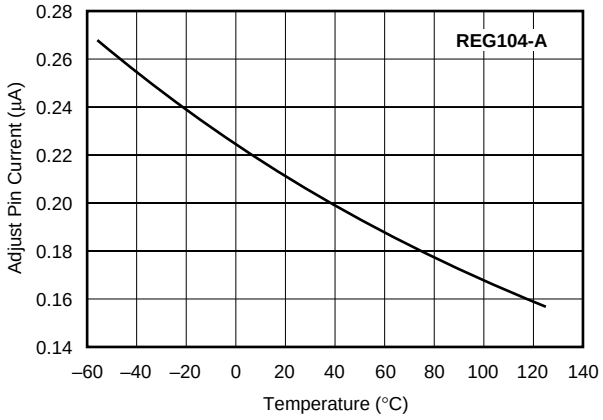
GROUND PIN CURRENT, NOT ENABLED vs TEMPERATURE



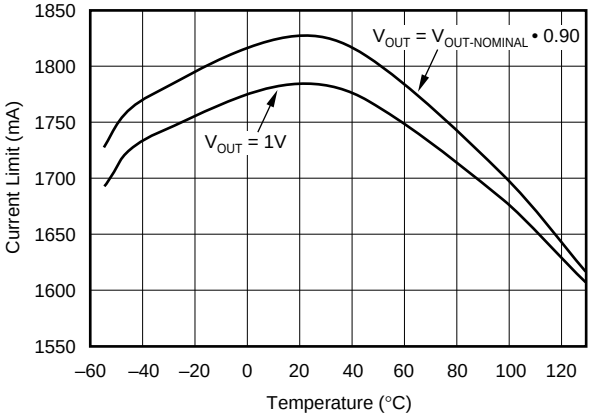
GROUND PIN CURRENT vs I_{OUT}



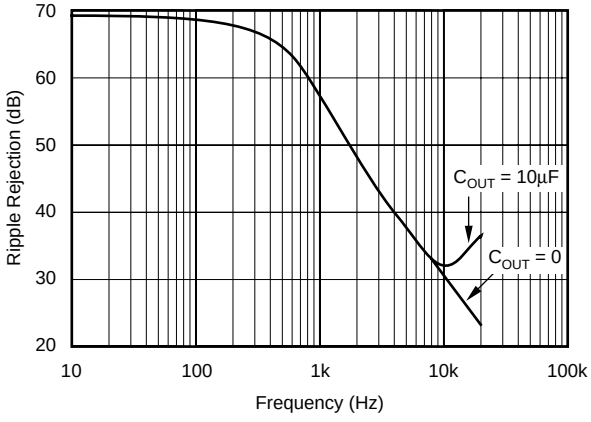
I_{ADJUST} vs TEMPERATURE



CURRENT LIMIT vs TEMPERATURE



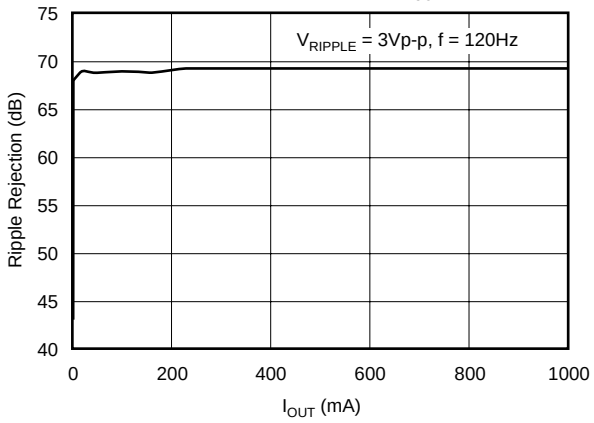
RIPPLE REJECTION vs FREQUENCY



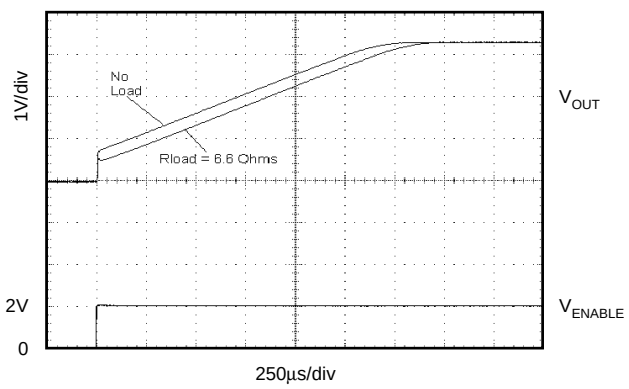
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 2V, unless otherwise noted.

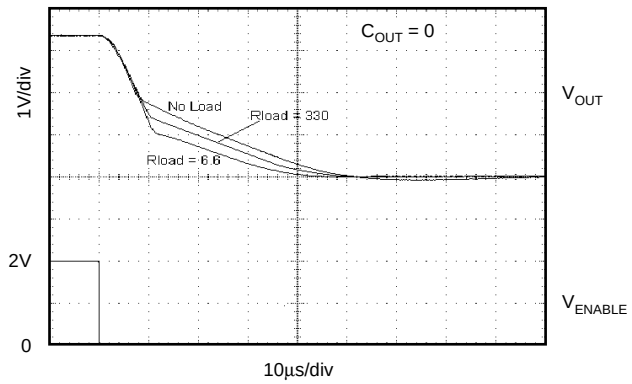
RIPPLE REJECTION vs I_{OUT}



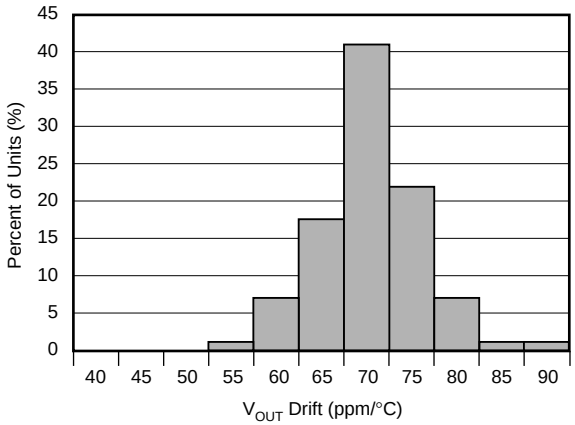
SOFT START



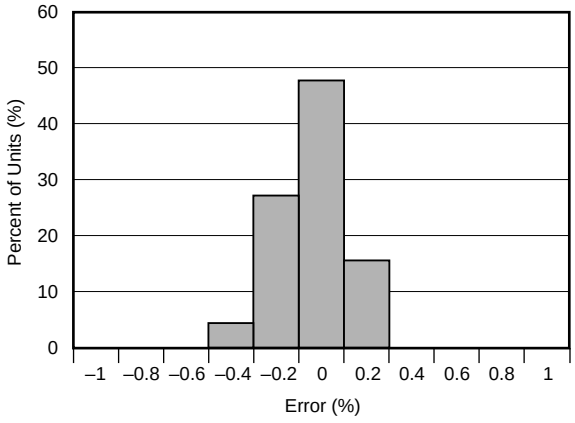
OUTPUT DISABLE TIME



OUTPUT VOLTAGE DRIFT HISTOGRAM



OUTPUT VOLTAGE ACCURACY HISTOGRAM



BASIC OPERATION

The REG104 series is a family of LDO (Low DropOut) linear regulators. The family includes five fixed output versions (2.5V to 5.0V) and an adjustable output version. An internal DMOS power device provides low dropout regulation with near constant ground pin current (largely independent of load and dropout conditions) and very fast line and load transient response. All versions include internal current limit and thermal shutdown circuitry.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG104A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2.

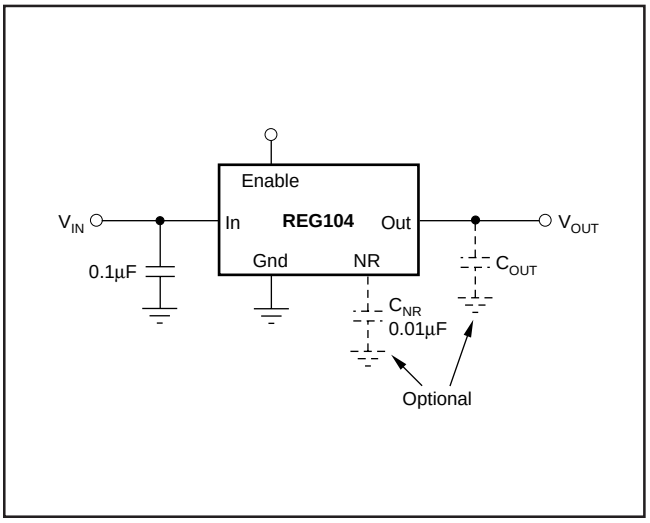


FIGURE 1. Fixed Voltage Nominal Circuit for REG104.

None of the versions require an output capacitor for regulator stability. The REG104 will accept any output capacitor type less than 1µF. For capacitance values larger than 1µF the effective ESR should be greater than 0.1Ω. This minimum ESR value includes parasitics such as printed circuit board traces, solder joints, and sockets. A minimum 0.1µF low ESR capacitor connected to the input supply voltage is recommended.

ENABLE

The Enable pin allows the regulator to be turned on and off. This pin is active HIGH and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition ground-pin current drops to approximately 0.5µA.

When not used, the Enable pin may be connected to V_{IN}. Internal to the part, the Enable pin is connected to an input resistor-zener diode circuit, as shown in Figure 3, creating a nonlinear input impedance.

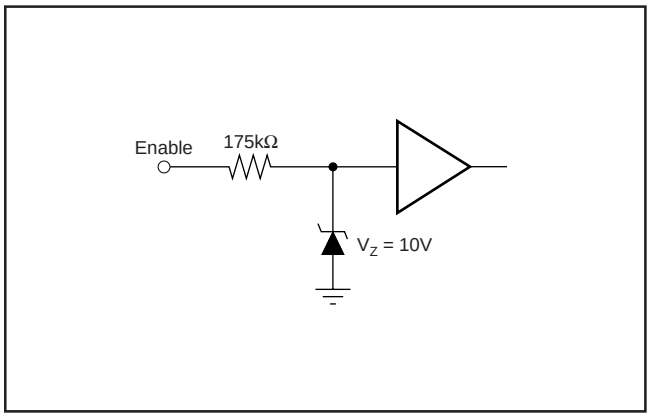
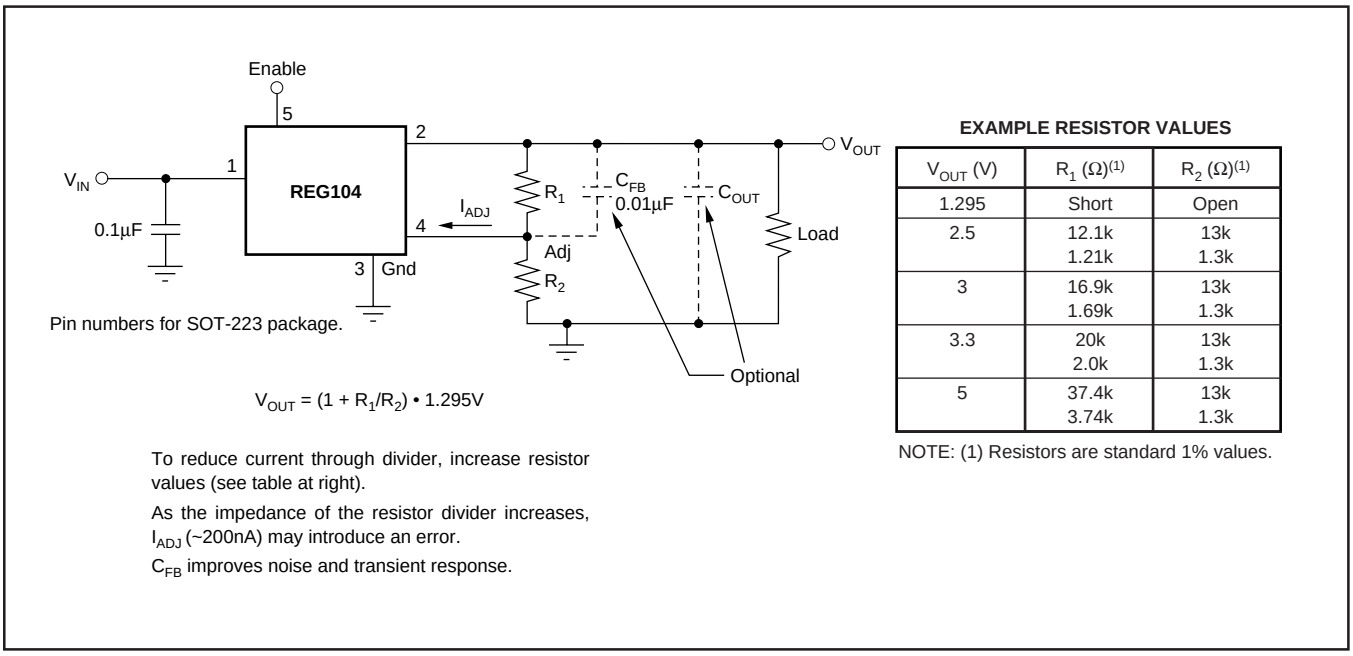


FIGURE 3. Enable Pin Equivalent Input Circuit.



To reduce current through divider, increase resistor values (see table at right).

As the impedance of the resistor divider increases, I_{ADJ} (~200nA) may introduce an error.

C_{FB} improves noise and transient response.

EXAMPLE RESISTOR VALUES

V_{OUT} (V)	R_1 (Ω)(1)	R_2 (Ω)(1)
1.295	Short	Open
2.5	12.1k 1.21k	13k 1.3k
3	16.9k 1.69k	13k 1.3k
3.3	20k 2.0k	13k 1.3k
5	37.4k 3.74k	13k 1.3k

NOTE: (1) Resistors are standard 1% values.

FIGURE 2. Adjustable Voltage Circuit for REG104A.

The Enable Pin Current versus Applied Voltage relationship is shown in Figure 4. When the Enable pin is connected to V_{IN} greater than 10V, a series resistor may be used to limit the current.

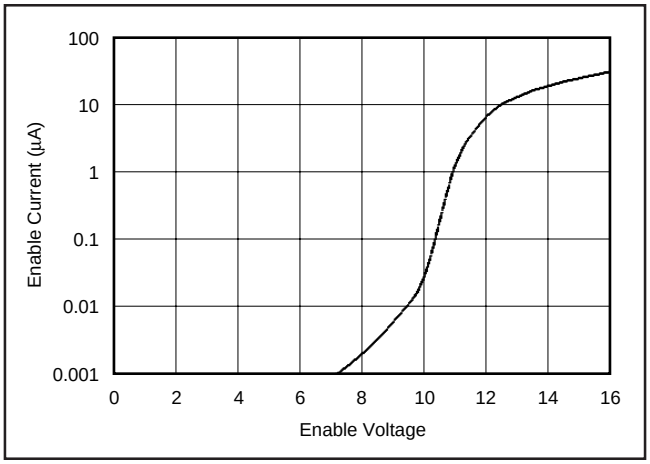


FIGURE 4. Enable Pin Current versus Applied Voltage.

OUTPUT NOISE

A precision band-gap reference is used for the internal reference voltage, V_{REF}, for the REG104. This reference is the dominant noise source within the REG104. It generates approximately $45\mu V_{RMS}$ in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 45\mu V_{RMS} \frac{R_1 + R_2}{R2} = 45\mu V_{RMS} \bullet \frac{V_{OUT}}{V_{REF}}$$

Since the value of V_{REF} is 1.295V, this relationship reduces to:

$$V_N = 35 \frac{\mu V_{RMS}}{V} \bullet V_{OUT}$$

Connecting a capacitor, C_{NR}, from the Noise-Reduction (NR) pin to ground can reduce the output noise voltage. Adding C_{NR}, as shown in Figure 5, forms a low-pass filter for the voltage reference. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 3.5. This noise reduction effect is shown in Figure 6.

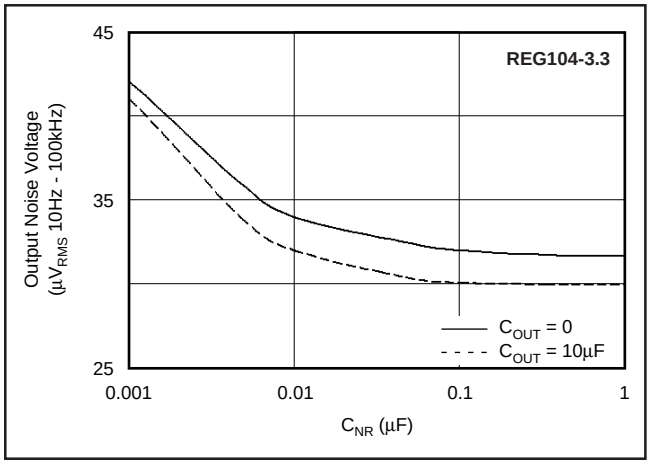


FIGURE 6. Output Noise versus Noise Reduction Capacitor.

The REG104 adjustable version does not have the noise-reduction pin available, however, the adjust pin is the summing junction of the error amplifier. A capacitor, C_{FB},

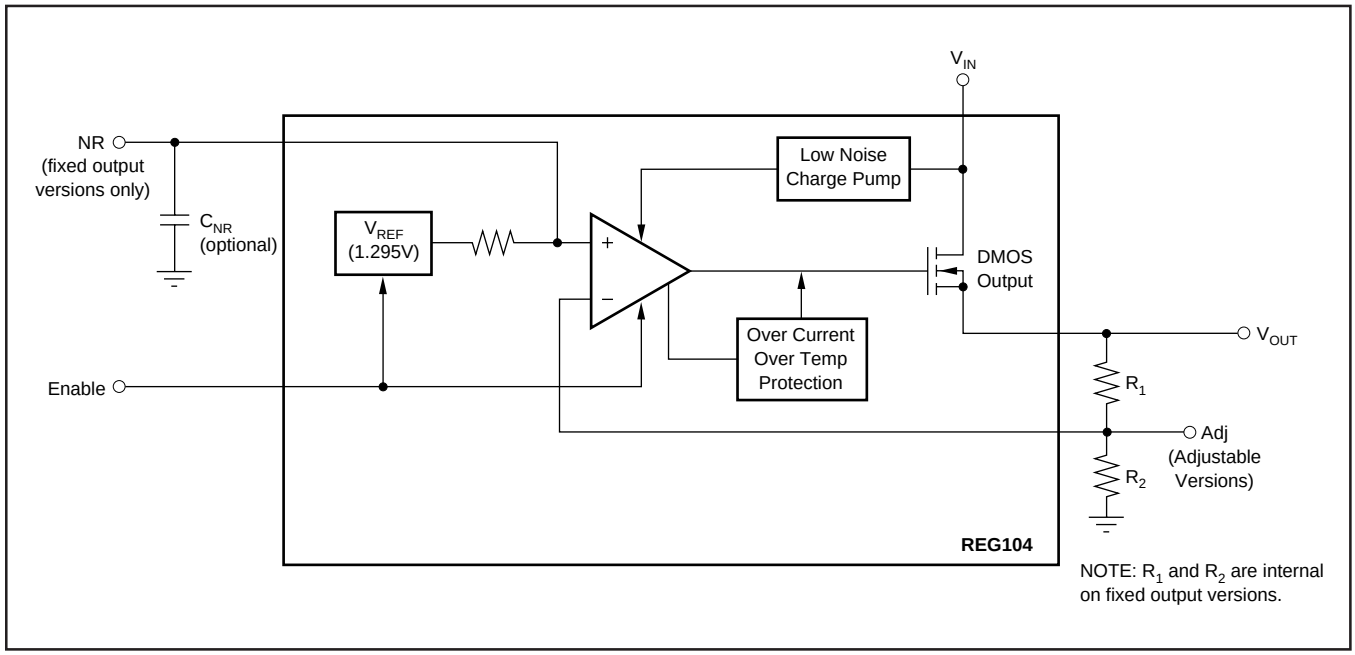


FIGURE 5. Block Diagram.

connected from the output to the adjust pin will reduce both the output noise and the peak error from a load transient. Figure 7 shows improved output noise performance for two capacitor combinations.

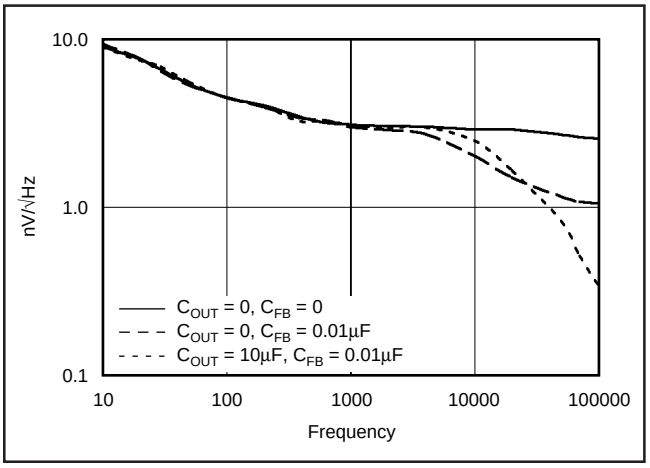


FIGURE 7. Output Noise Density on Adjustable Versions.

The REG104 utilizes an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN}. The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator.

DROP-OUT VOLTAGE

The REG104 uses an N-channel DMOS as the *pass* element. When the input voltage is within a few hundred millivolts of the output voltage, the DMOS device behaves like a resistor. Therefore, for low values of V_{IN} to V_{OUT}, the regulator's input-to-output resistance is the Rds_{ON} of the DMOS pass element (typically 230mΩ). For static (DC) loads, the REG104 will typically maintain regulation down to V_{IN} to V_{OUT} voltage drop of 230mV at full rated output current. In Figure 8, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent dropout under DC load conditions.

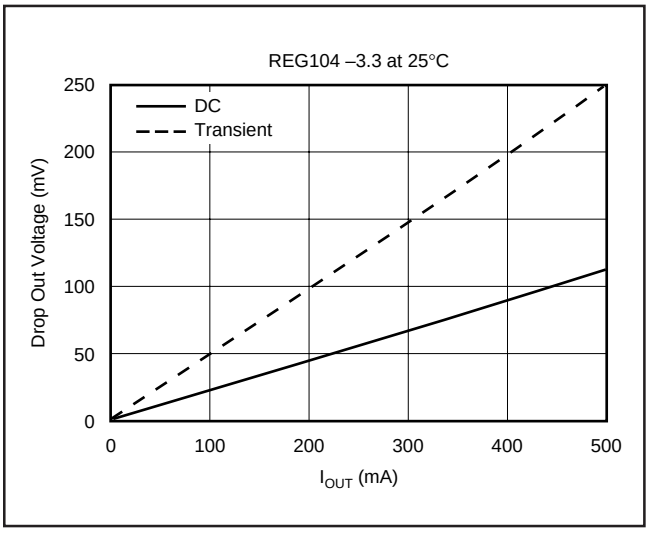


FIGURE 8. Transient and DC Dropout.

For large step changes in load current, the REG104 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this *transient dropout* region is shown as the top line in Figure 8. Values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

In the transient dropout region between *DC* and *Transient*, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available *headroom* V_{IN} to V_{OUT} voltage drop. Under worst-case conditions (full-scale load change with V_{IN} to V_{OUT} voltage drop close to DC dropout levels), the REG104 can take several hundred microseconds to re-enter the specified window of regulation.

TRANSIENT RESPONSE

The REG104 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 10nF) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin will also improve the transient response.

THERMAL PROTECTION

Power dissipated within the REG104 will cause the junction temperature to rise. The REG104 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 150°C, allowing the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG104 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the REG104 into thermal shutdown will degrade reliability.

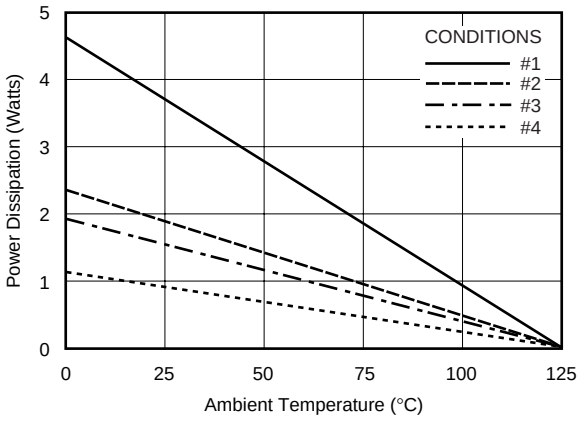
POWER DISSIPATION

The REG104 is available in two different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. While it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several configurations are shown in Figure 9. In all cases the PCB copper area is bare copper, free of solder resist mask, and not solder plated. All examples are for 1-ounce copper. Using heavier copper will increase the effectiveness in moving the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the average output current times the voltage across the output element, V_{IN} to V_{OUT} voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \bullet I_{OUT(AVG)}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.



CONDITION	PACKAGE	PCB AREA	θ_{JA}
1	DDPAK	4in² Top Side Only	27°C/W
2	SOT-223	4in² Top Side Only	53°C/W
3	DDPAK	None	65°C/W
4	SOT-223	0.5in² Top Side Only	110°C/W

FIGURE 9. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

REGULATOR MOUNTING

The tab of both packages is electrically connected to ground. For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation. Figure 10 shows typical thermal resistance from junction to ambient as a function of the copper area for the DDPAK. Figure 11 shows the same relationship for the SOT-223.

Although the tabs of the DDPAK and the SOT-223 are electrically grounded, they are not intended to carry any current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the various REG104 devices are presented in the Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015A), available from the Texas Instruments web site (www.ti.com).

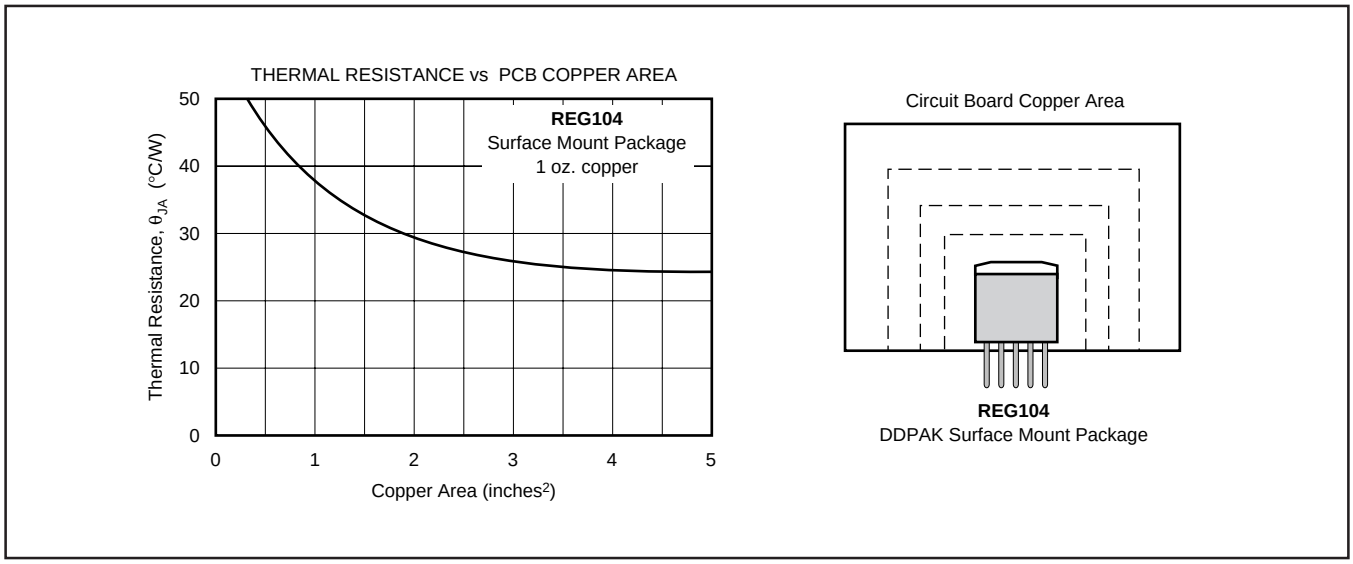


FIGURE 10. Thermal Resistance versus PCB Area for the Five-Lead DDPAK.

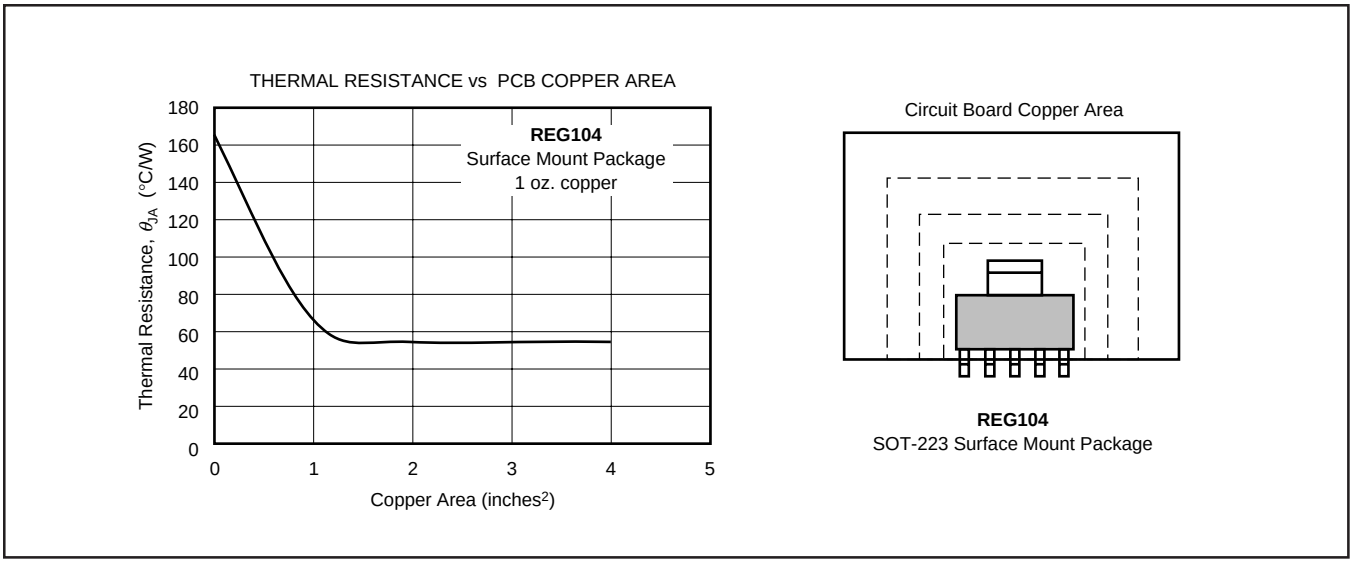


FIGURE 11. Thermal Resistance versus PCB Area for the Five Lead SOT-223.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG104FA-2.5KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR		REG 104FA-2.5	Samples
REG104FA-2.5KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	RoHS & Green	SN	Level-2-260C-1 YEAR		REG 104FA-2.5	Samples
REG104FA-3.3/500	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR		REG 104FA-3.3	Samples
REG104FA-3.3/500G3	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR		REG 104FA-3.3	Samples
REG104FA-5/500	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR		REG 104FA-5	Samples
REG104FA-5/500G3	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR		REG 104FA-5	Samples
REG104FA-A/500	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 85	REG 104FA-A	Samples
REG104FA-A/500G3	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	REG 104FA-A	Samples
REG104GA-2.5	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R104G25	Samples
REG104GA-2.5/2K5	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R104G25	Samples
REG104GA-2.5G4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R104G25	Samples
REG104GA-3.3	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R104G33	Samples
REG104GA-3.3/2K5	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R104G33	Samples
REG104GA-3.3G4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R104G33	Samples
REG104GA-5	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR		R104G50	Samples
REG104GA-5/2K5	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	R104G50	Samples
REG104GA-5/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R104G50	Samples
REG104GA-5G4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R104G50	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG104GA-A	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	R104GA	Samples
REG104GA-A/2K5	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	R104GA	Samples
REG104GA-AG4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R104GA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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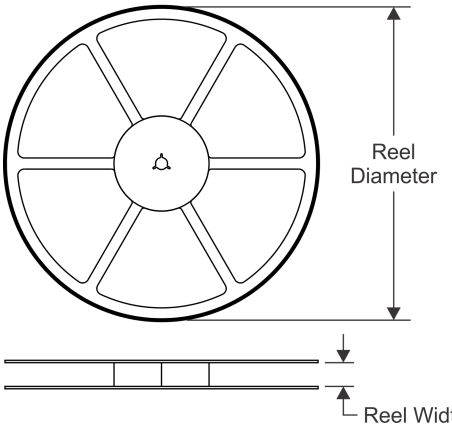
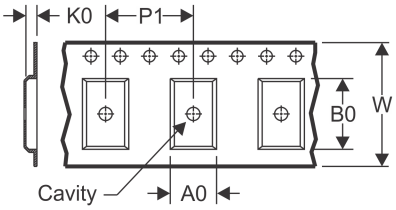
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

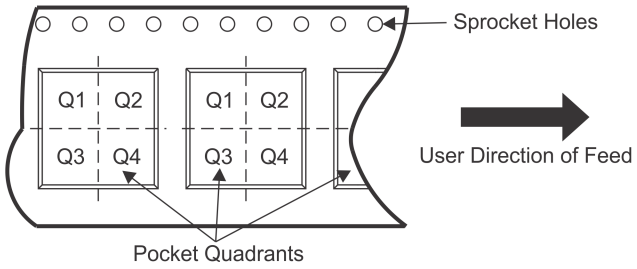


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

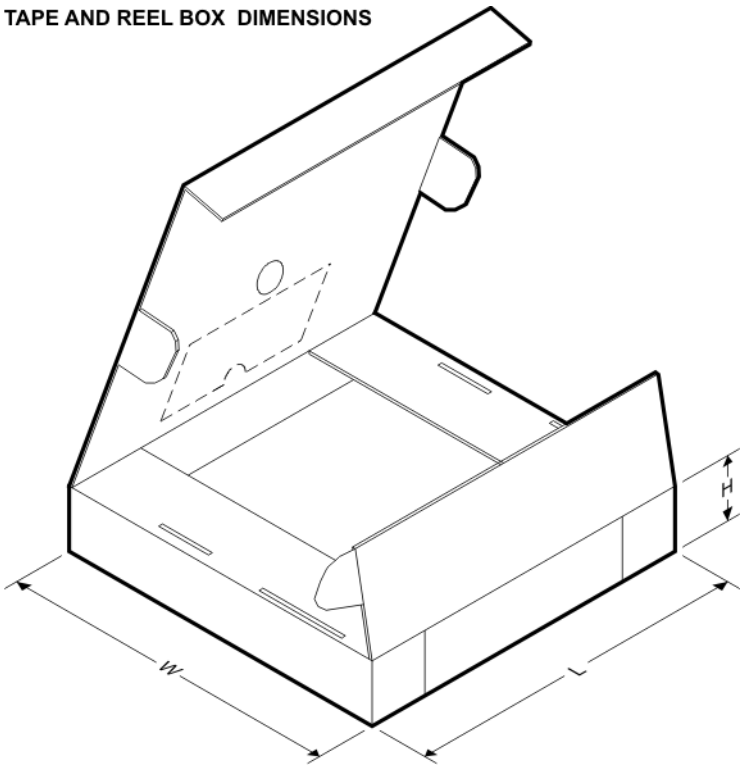
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG104GA-2.5/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-3.3/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-5/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-5/2K5G4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-A/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-A/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

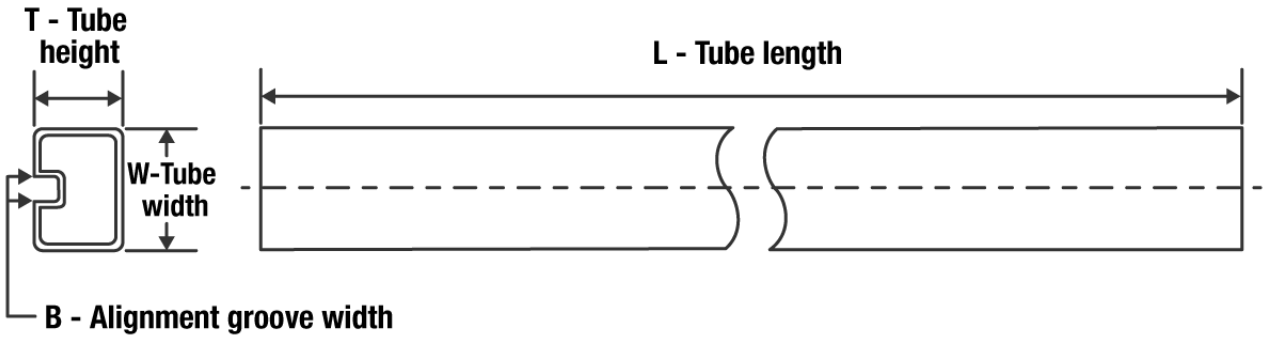
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG104GA-2.5/2K5	SOT-223	DCQ	6	2500	346.0	346.0	41.0
REG104GA-3.3/2K5	SOT-223	DCQ	6	2500	346.0	346.0	29.0
REG104GA-5/2K5	SOT-223	DCQ	6	2500	853.0	449.0	35.0
REG104GA-5/2K5G4	SOT-223	DCQ	6	2500	358.0	335.0	35.0
REG104GA-A/2K5	SOT-223	DCQ	6	2500	346.0	346.0	41.0
REG104GA-A/2K5	SOT-223	DCQ	6	2500	853.0	449.0	35.0

TUBE



*All dimensions are nominal

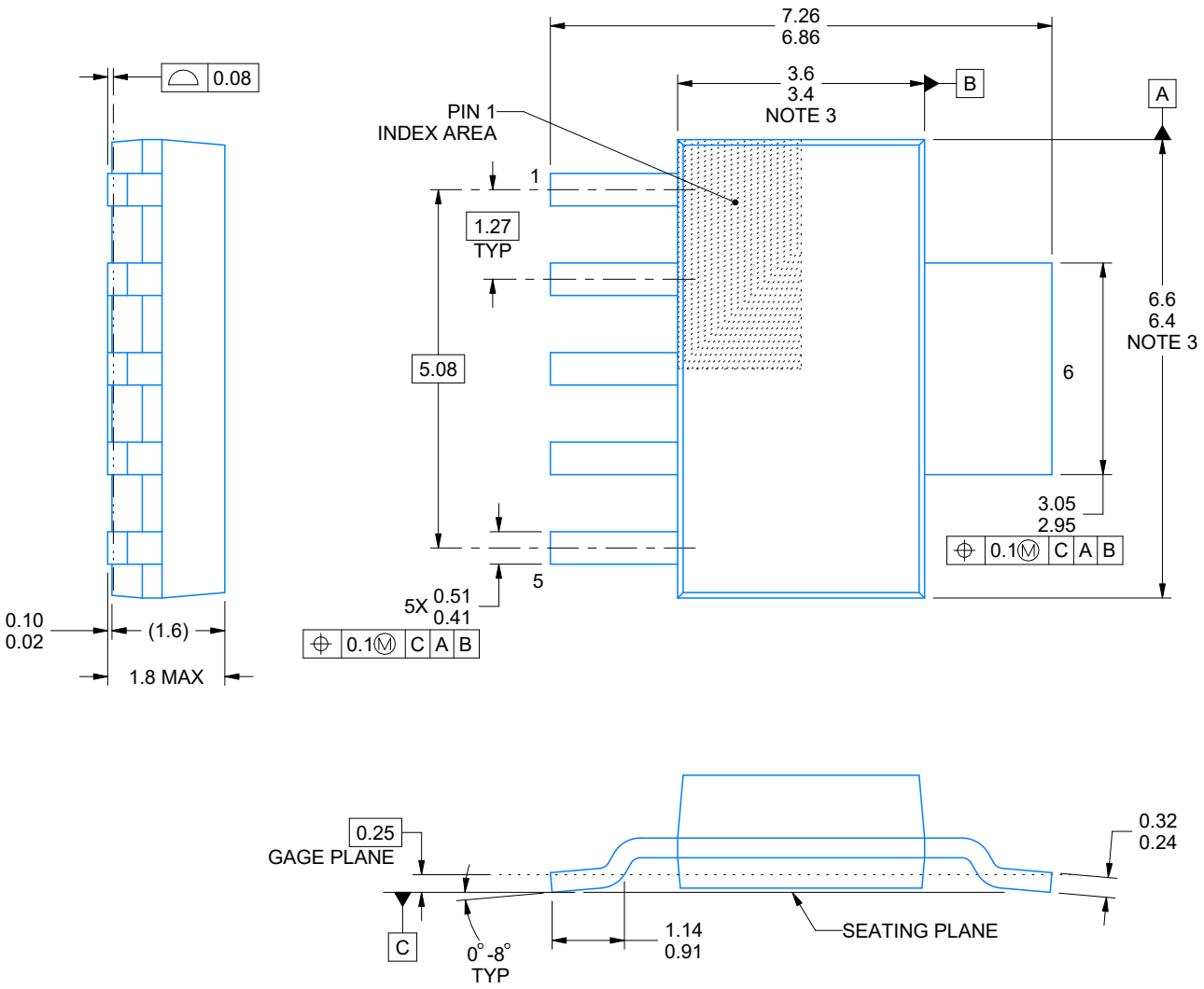
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
REG104GA-2.5	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG104GA-2.5G4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG104GA-3.3	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG104GA-3.3G4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG104GA-5	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
REG104GA-5G4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG104GA-A	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
REG104GA-AG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



4214845/C 11/2021

NOTES:

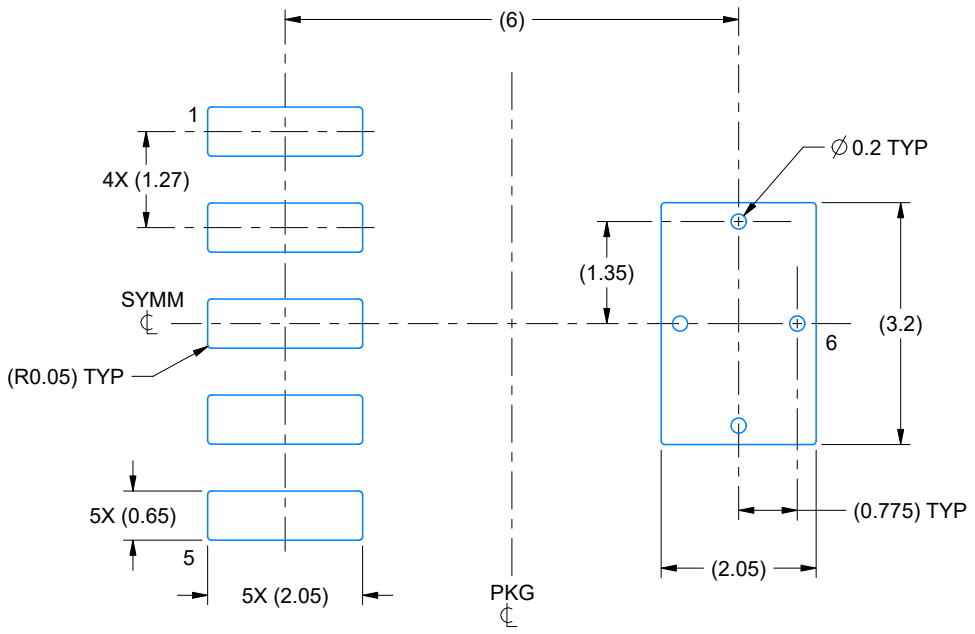
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

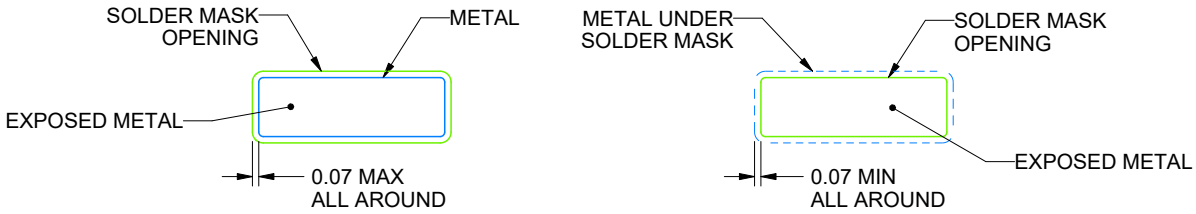
DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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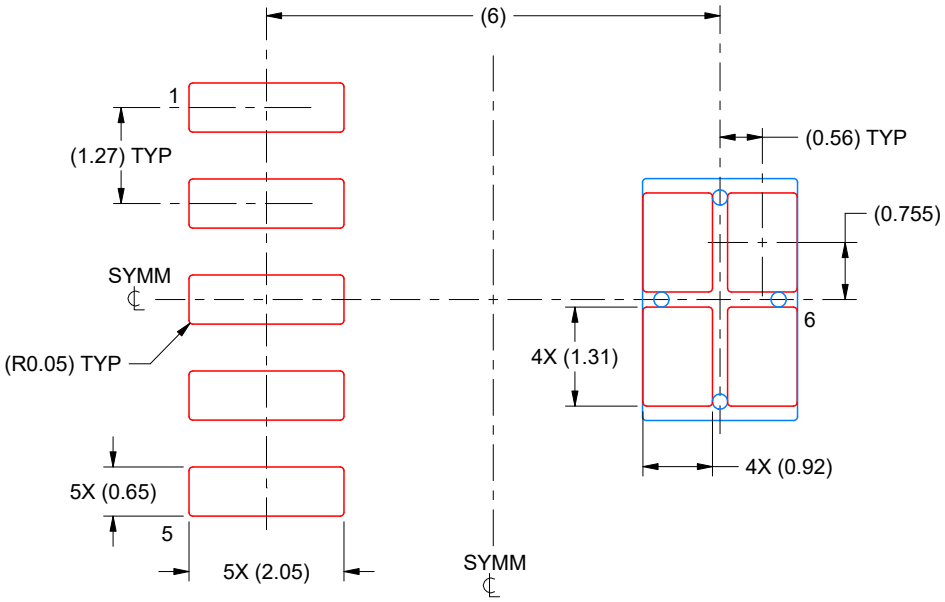
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



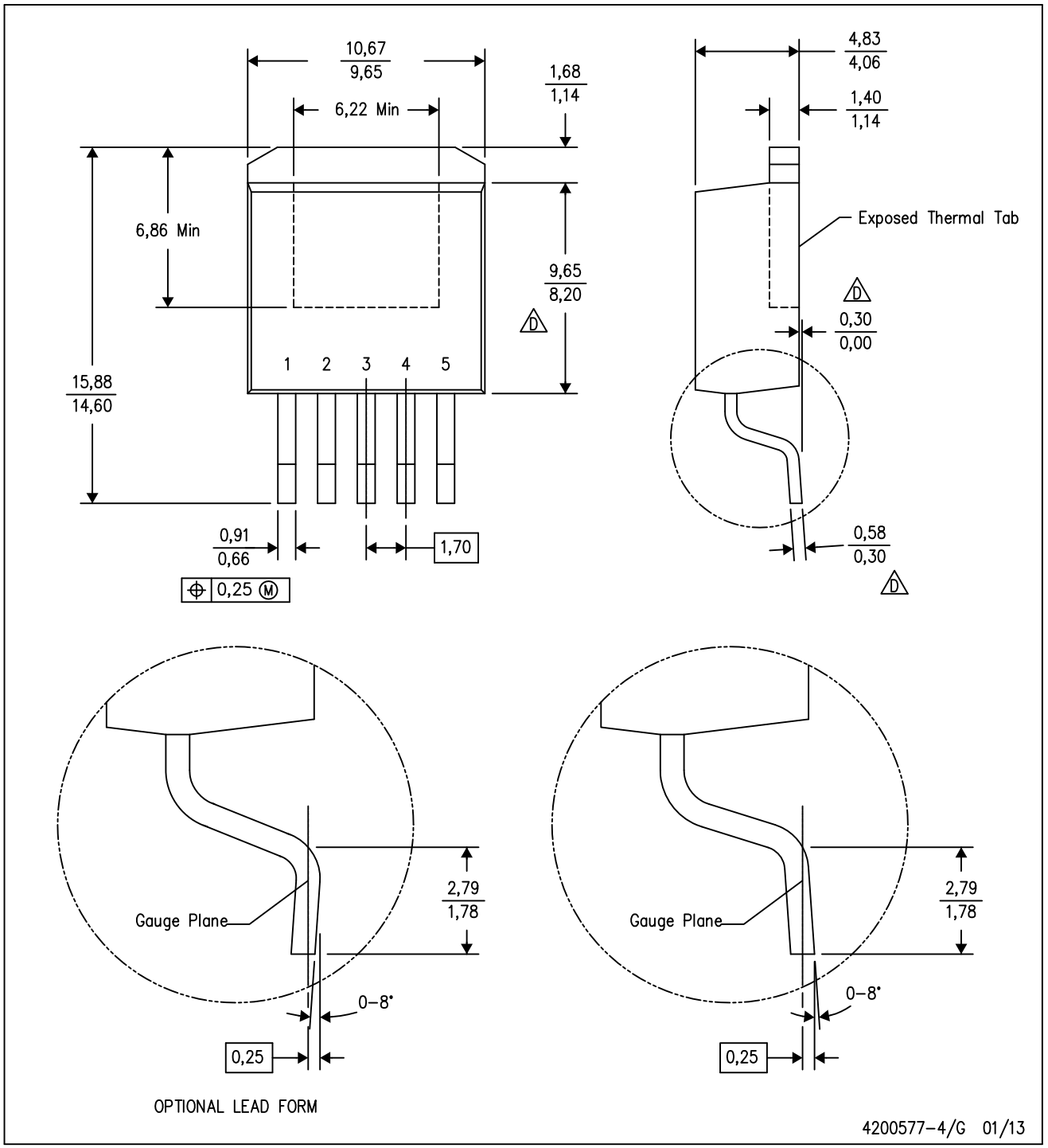
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

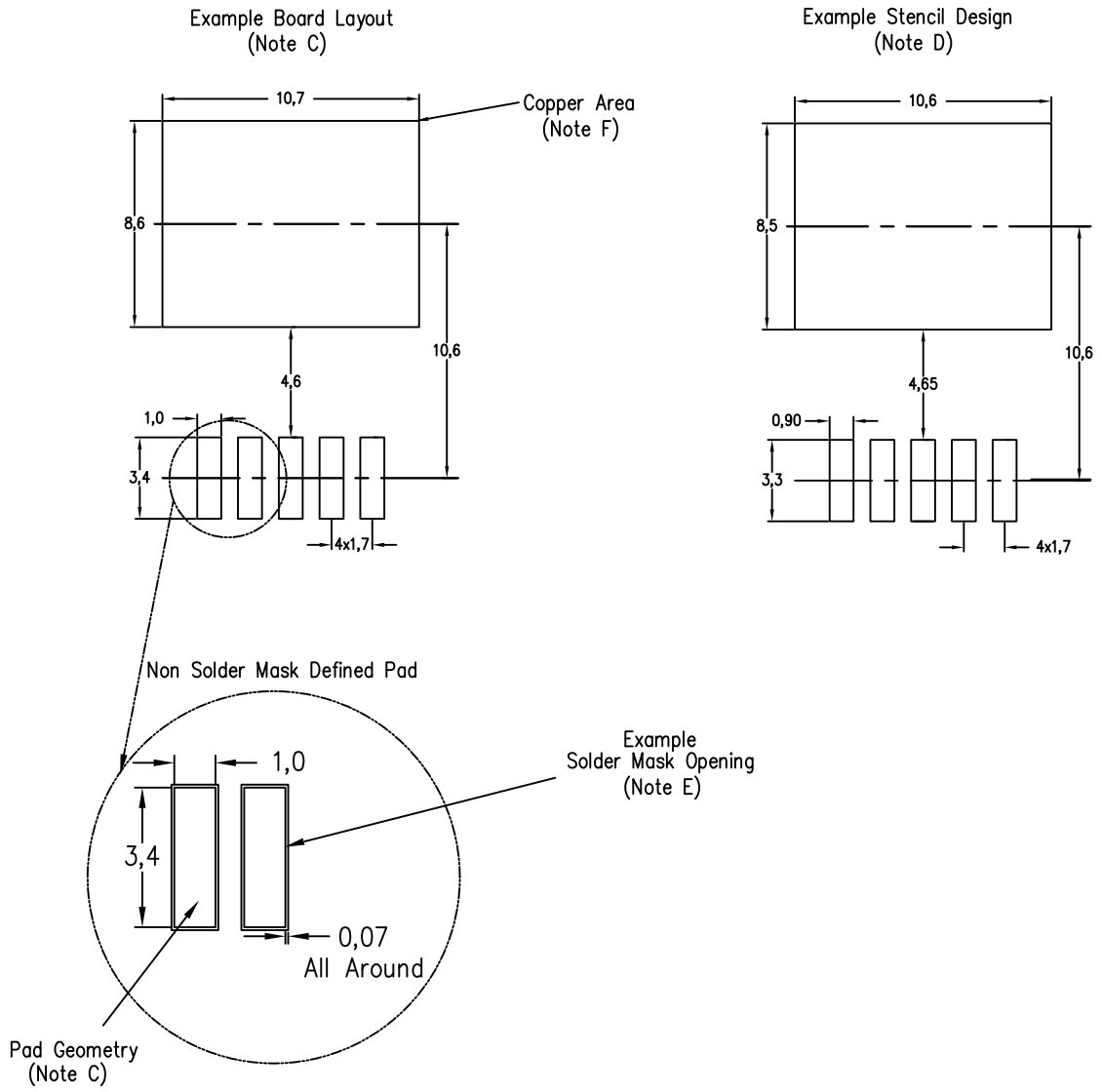
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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