

CMOS Hex Buffers/Converters

High-Voltage Types (20-Volt Rating)

Inverting Type: CD4009UB

Non-Inverting Type: CD4010B

■ CD4009UB and CD4010B Hex Buffer/Converters may be used as CMOS to TTL or DTL logic-level converters or CMOS high-sink-current drivers.

The CD4049UB and CD4050B are preferred hex buffer replacements for the CD4009UB and CD4010B, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

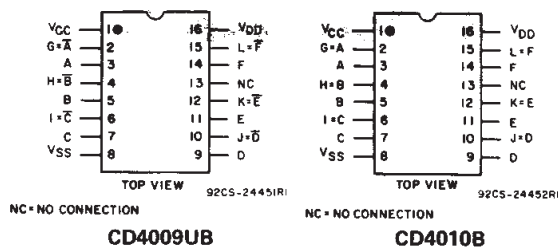
The CD4009UB and CD4010B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shink small-outline packages (PW and PWR suffixes).

Features:

- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- CMOS to DTL/TTL hex converter
- CMOS current “sink” or “source” driver
- CMOS high-to-low logic-level converter
- Multiplexer — 1 to 6 or 6 to 1



TERMINAL ASSIGNMENTS

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max $+265^\circ\text{C}$

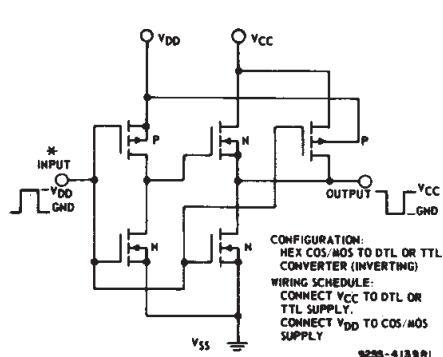


Fig. 1 — Schematic diagram of CD4009UB—
1 of 6 identical stages.

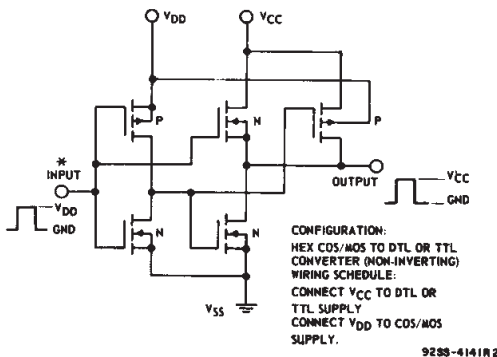
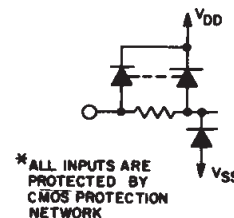
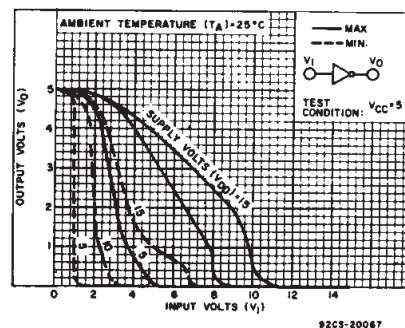
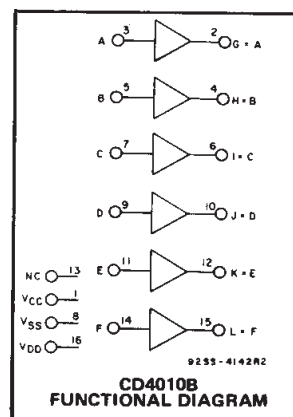
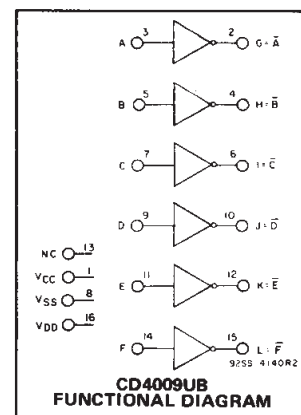


Fig. 2 — Schematic diagram of CD4010B—
1 of 6 identical stages.



CD4009UB, CD4010B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range), V_{DD}	3	18	V
V_{CC}^*	3	V_{DD}	
Input Voltage Range (V_I)	V_{CC}^*	V_{DD}	V

*The CD4009UB and CD4010B have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} > V_I > V_{CC}$.

STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	4.5	3.2	3.1	2.1	1.8	2.6	3.4	—	mA
	0.4	0,5	5	3.75	3.6	2.4	2.1	3	4	—	
	0.5	0,10	10	10	9.6	6.4	5.6	8	10	—	
	1.5	0,15	15	30	40	19	16	24	36	—	
Output High (Source) Current I _{OH} Min.	4.6	0,5	5	-0.25	-0.23	-0.18	-0.15	-0.2	-0.4	—	
	2.5	0,5	5	-1	-0.9	-0.65	-0.58	-0.8	-1.6	—	
	9.5	0,10	10	-0.55	-0.5	-0.38	-0.33	-0.45	-0.9	—	
	13.5	0,15	15	-1.65	-1.6	-1.25	-1.1	-1.5	-3	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage: V _{IL} Max. CD4009UB	4.5	—	5	1				—	—	1	V
	9	—	10	2				—	—	2	
	13.5	—	15	2.5				—	—	2.5	
Input Low Voltage: V _{IL} Max. CD4010B	0.5	—	5	1.5				—	—	1.5	
	1	—	10	3				—	—	3	
	1.5	—	15	4				—	—	4	
Input High Voltage: V _{IH} Min. CD4009UB	0.5	—	5	4				4	—	—	V
	1	—	10	8				8	—	—	
	1.5	—	15	12.5				12.5	—	—	
Input High Voltage: V _{IH} Min. CD4010B	4.5	—	5	3.5				3.5	—	—	
	9	—	10	7				7	—	—	
	13.5	—	15	11				11	—	—	
Input Current, I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

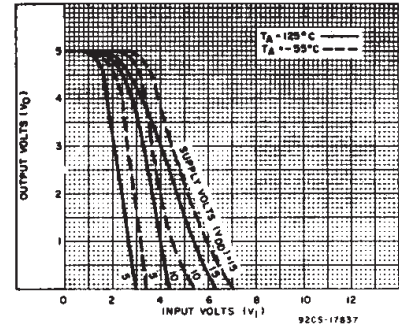


Fig. 4 — Typical voltage transfer characteristics as function of temp.—CD4009UB.

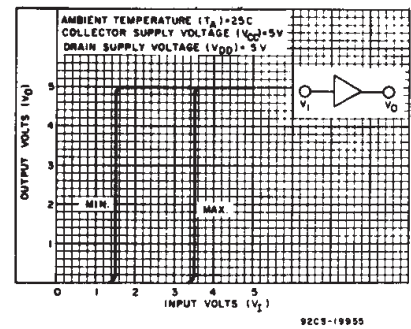


Fig. 5 — Minimum and maximum voltage transfer characteristics ($V_{DD}=5$)—CD4010B.

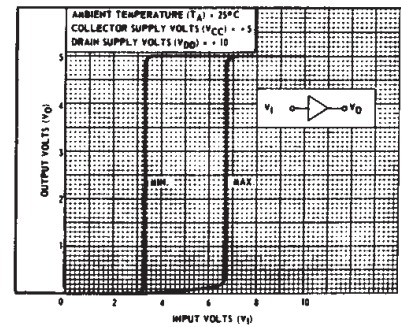


Fig. 6 — Minimum and maximum voltage transfer characteristics ($V_{DD}=10$)—CD4010B.

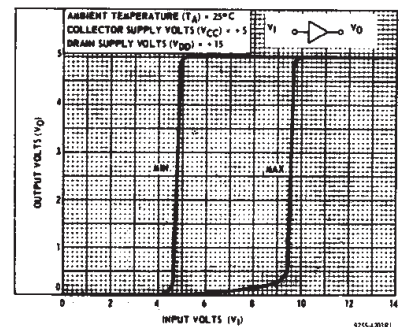


Fig. 7 — Minimum and maximum voltage transfer characteristics ($V_{DD}=15$)—CD4010B.

CD4009UB, CD4010B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$; Input $t_r, t_f=20\text{ ns}$,
 $C_L=50\text{ pF}$, $R_L=200\text{ K}\Omega$

CHARACTERISTIC	CONDITIONS			LIMITS ALL PKGS		UNIT
	V_{DD} (V)	V_I (V)	V_{CC} (V)	TYP.	MAX.	
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	70	140	ns
	10	10	10	40	80	
	10	10	5	35	70	
	15	15	15	30	60	
	15	15	5	30	60	
CD4010B	5	5	5	100	200	ns
	10	10	10	50	100	
	10	10	5	50	100	
	15	15	15	35	70	
	15	15	5	35	70	
High-to-Low, t_{PHL}	5	5	5	30	60	ns
	10	10	10	20	40	
	10	10	5	15	30	
	15	15	15	15	30	
	15	15	5	10	20	
CD4010B	5	5	5	65	130	ns
	10	10	10	35	70	
	10	10	5	30	70	
	15	15	15	25	50	
	15	15	5	20	40	
Transition Time: Low-to-High, t_{TLH}	5	5	5	150	350	ns
	10	10	10	75	150	
	15	15	15	55	110	
High-to-Low, t_{THL}	5	5	5	35	70	ns
	10	10	10	20	40	
	15	15	15	15	30	
Input Capacitance, C_{IN}						pF
CD4009UB	—	—	—	15	22.5	
CD4010B	—	—	—	5	7.5	

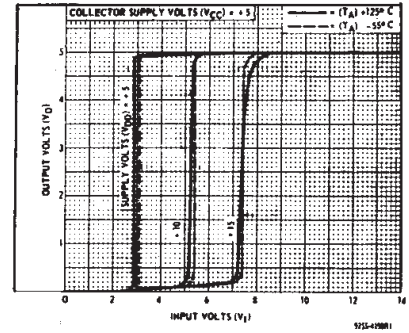


Fig. 8 — Typical voltage transfer characteristics as a function of temperature—CD4010B.

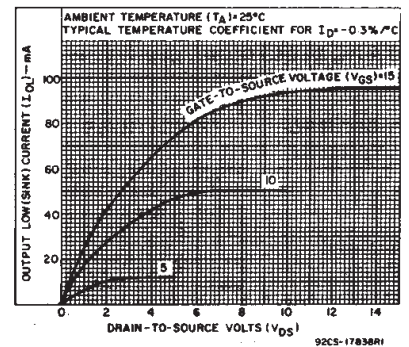


Fig. 9 — Typical output low (sink) current characteristics.

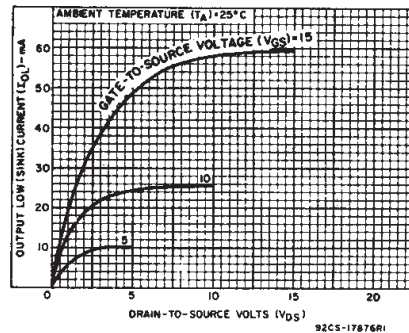


Fig. 10 — Minimum output low (sink) current characteristics.

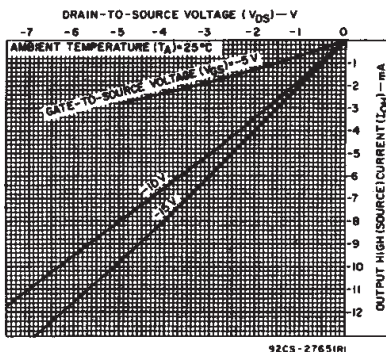


Fig. 11 — Typical output high (source) current characteristics.

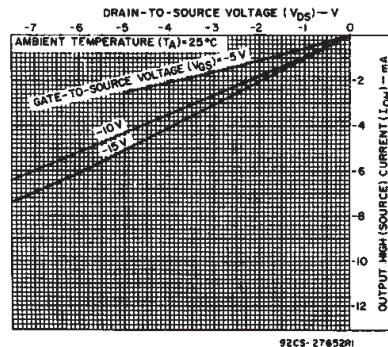


Fig. 12 — Minimum output high (source) current characteristics.

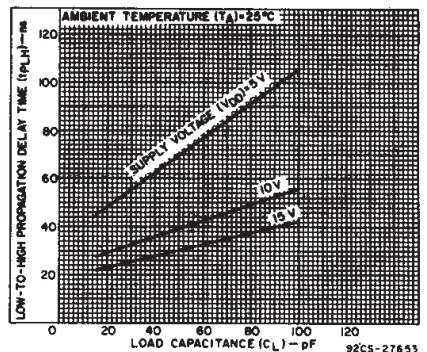


Fig. 13 — Typical low-to-high propagation delay time vs. load capacitance (CD4009UB).

CD4009UB, CD4010B Types

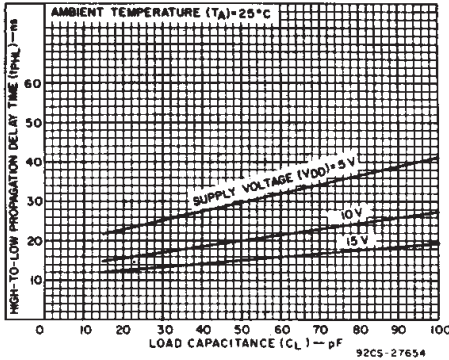


Fig. 14 - Typical high-to-low propagation delay time vs. load capacitance (CD4009UB).

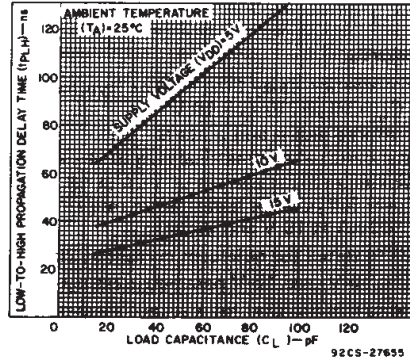


Fig. 15 - Typical low-to-high propagation delay time vs. load capacitance (CD4010B).

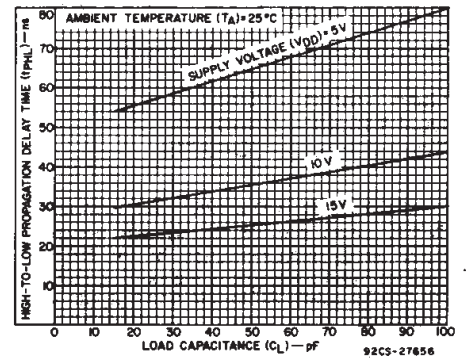


Fig. 16 - Typical high-to-low propagation delay time vs. load capacitance (CD4010B).

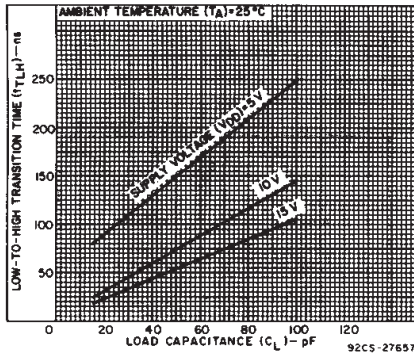


Fig. 17 - Typical low-to-high transition time vs. load capacitance.

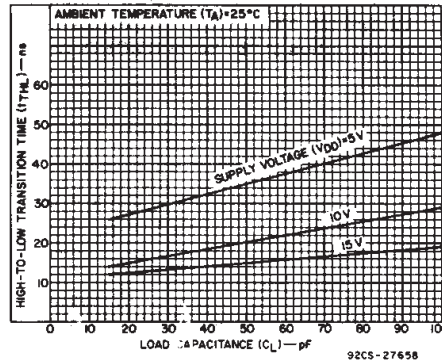


Fig. 18 - Typical high-to-low transition time vs. load capacitance.

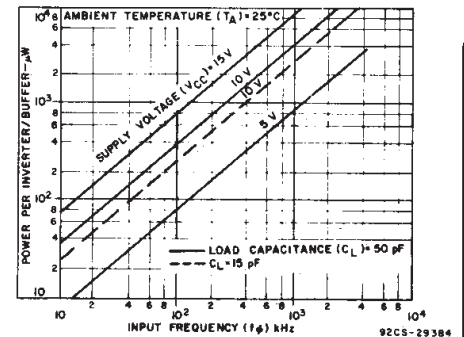


Fig. 19 - Typical dissipation characteristics.

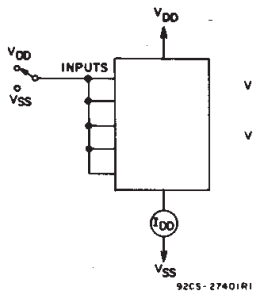


Fig. 20 - Quiescent device current test circuit.

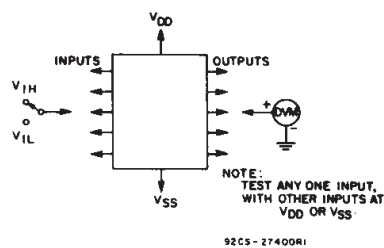


Fig. 21 - Noise immunity test circuit.

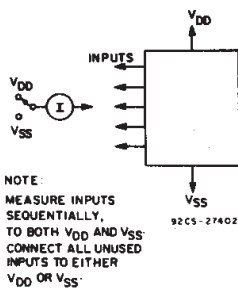
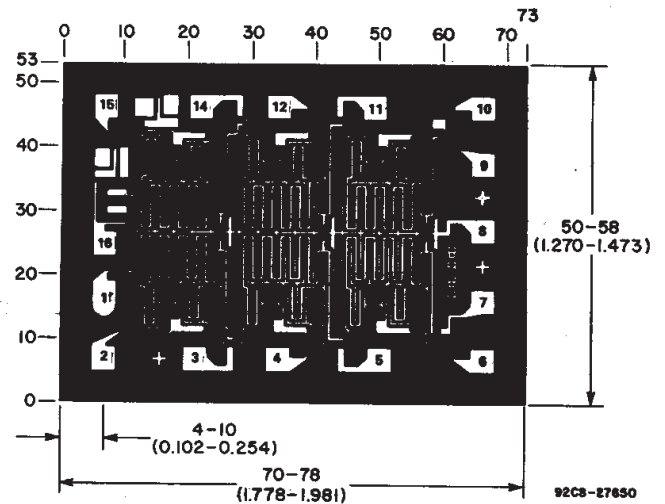


Fig. 22 - Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations Are In Mils (10⁻³ Inch)

Photograph of chip for CD4009UB. Dimensions and pad layout for CD4010B are identical.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4009UBE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4009UBE	Samples
CD4009UBEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4009UBE	Samples
CD4009UBF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4009UBF3A	Samples
CD4009UBM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4009UBM	Samples
CD4009UBMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4009UBM	Samples
CD4009UBPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM009UB	Samples
CD4010BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4010BE	Samples
CD4010BF	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4010BF	Samples
CD4010BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4010BF3A	Samples
CD4010BM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4010BM	Samples
CD4010BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4010BM	Samples
CD4010BMG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4010BM	Samples
CD4010BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4010B	Samples
CD4010BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM010B	Samples
CD4010BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM010B	Samples
CD4010BPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM010B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4009UB, CD4009UB-MIL, CD4010B, CD4010B-MIL :

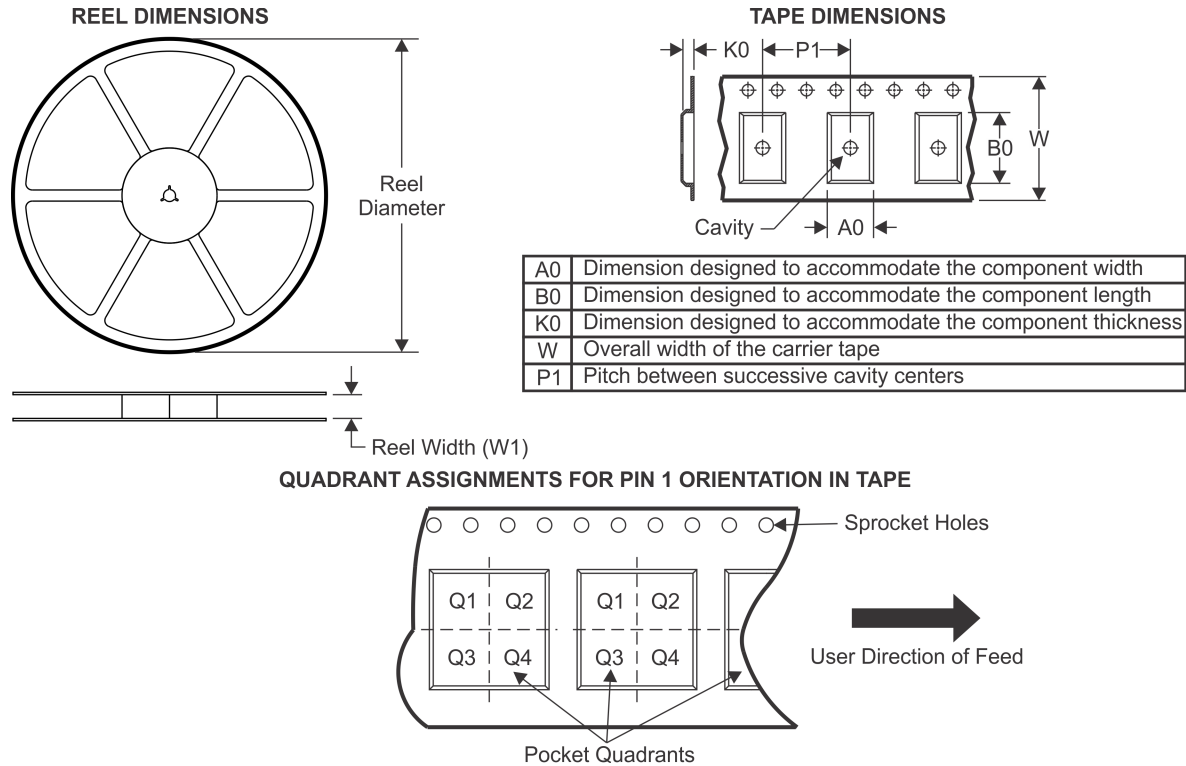
- Catalog : [CD4009UB](#), [CD4010B](#)
- Automotive : [CD4010B-Q1](#), [CD4010B-Q1](#)
- Military : [CD4009UB-MIL](#), [CD4010B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

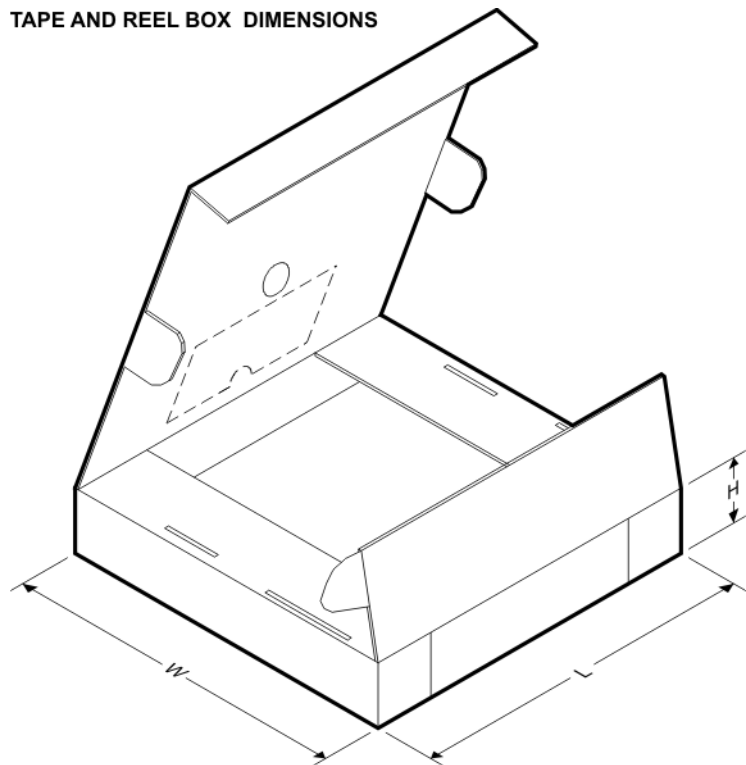
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4009UBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4010BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4010BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4010BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

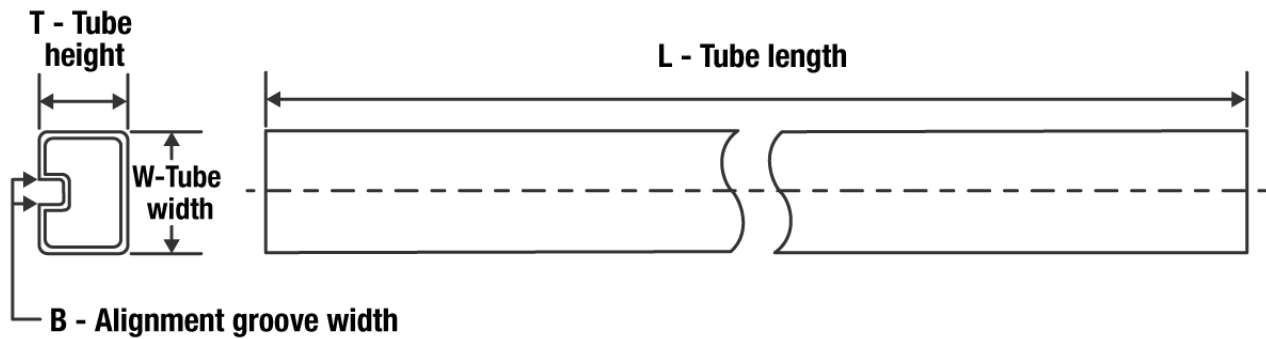
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

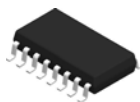
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4009UBPWR	TSSOP	PW	16	2000	853.0	449.0	35.0
CD4010BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4010BNSR	SO	NS	16	2000	853.0	449.0	35.0
CD4010BPWR	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4009UBE	N	PDIP	16	25	506	13.97	11230	4.32
CD4009UBE	N	PDIP	16	25	506	13.97	11230	4.32
CD4009UBEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4009UBEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4009UBM	D	SOIC	16	40	507	8	3940	4.32
CD4010BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4010BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4010BM	D	SOIC	16	40	507	8	3940	4.32
CD4010BMG4	D	SOIC	16	40	507	8	3940	4.32
CD4010BPW	PW	TSSOP	16	90	530	10.2	3600	3.5

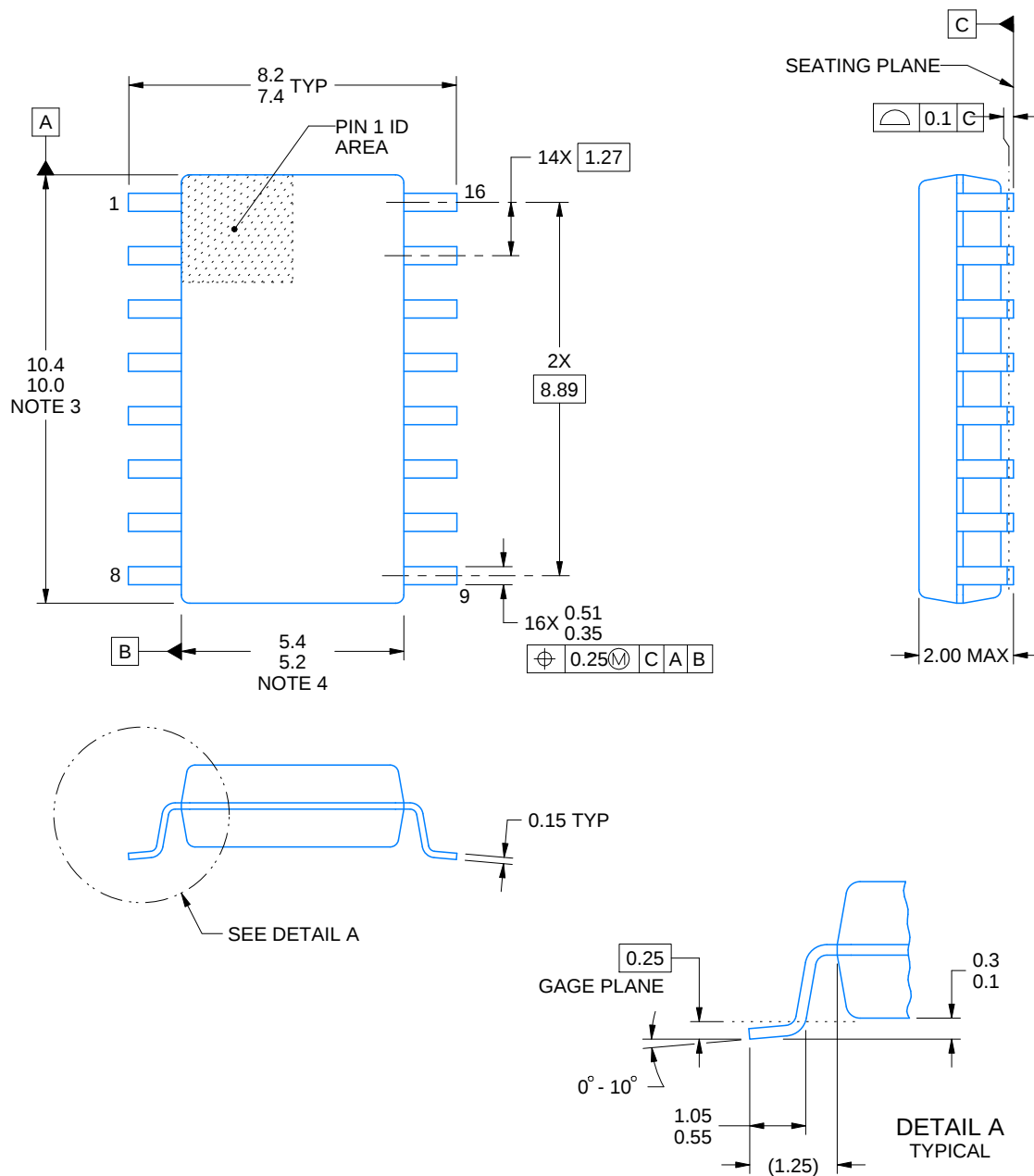


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

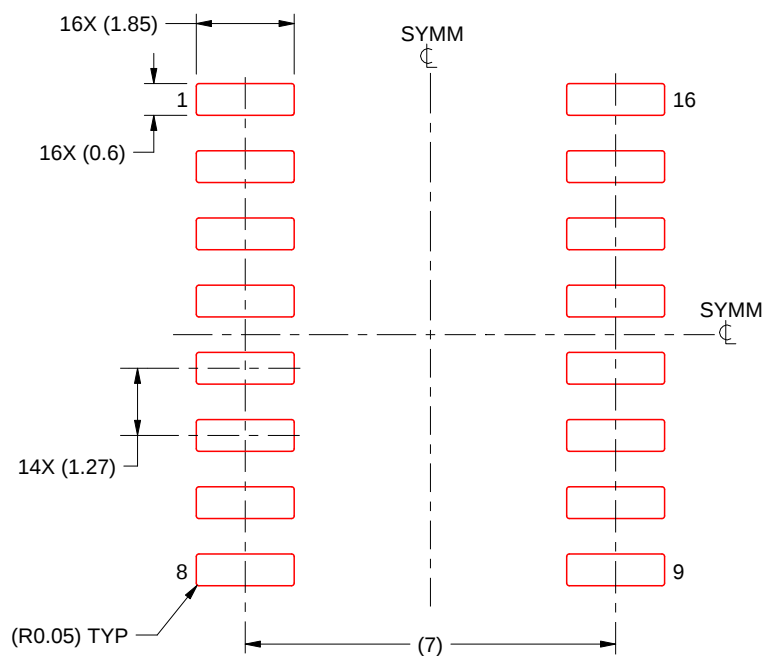
SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

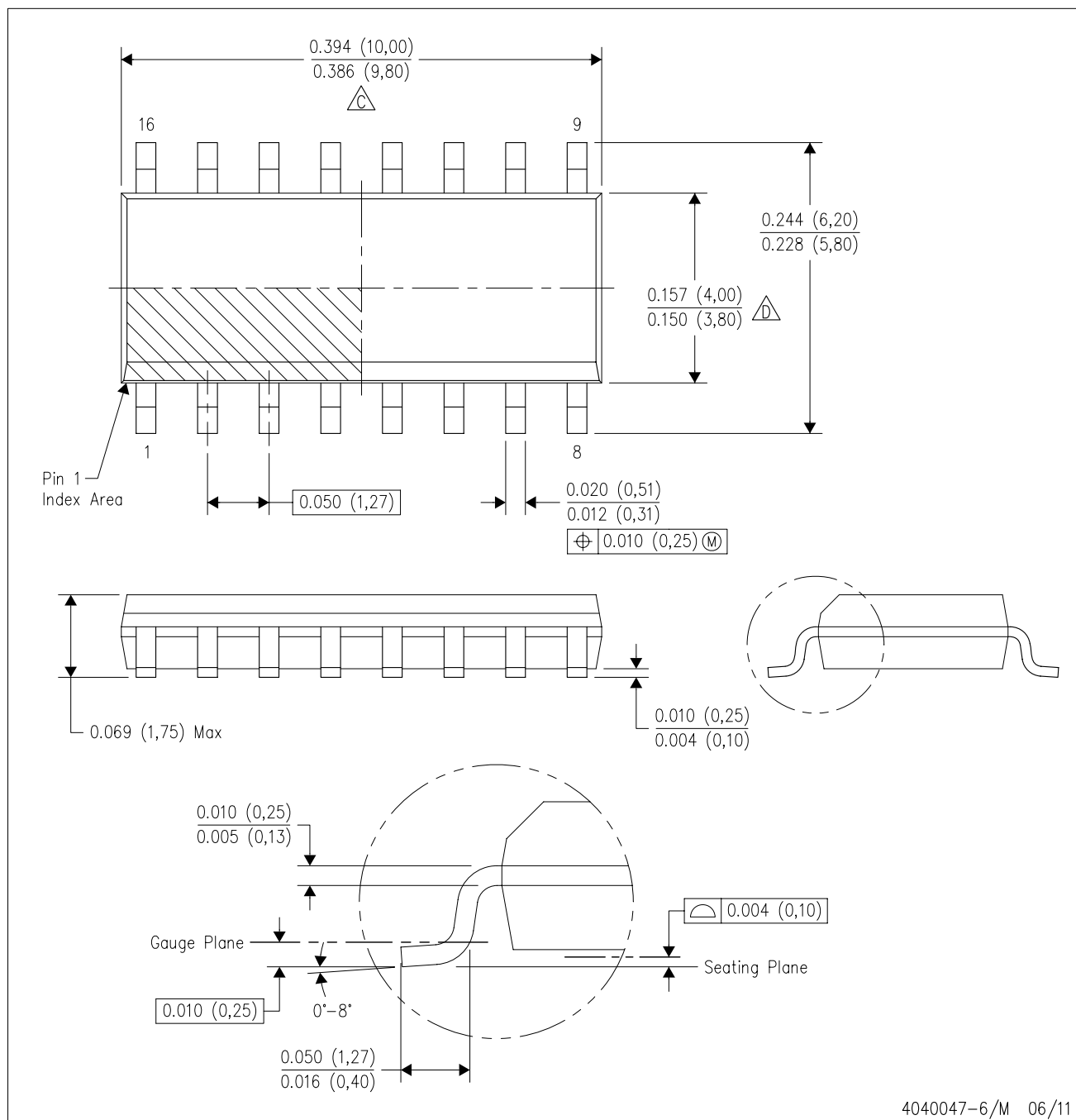
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

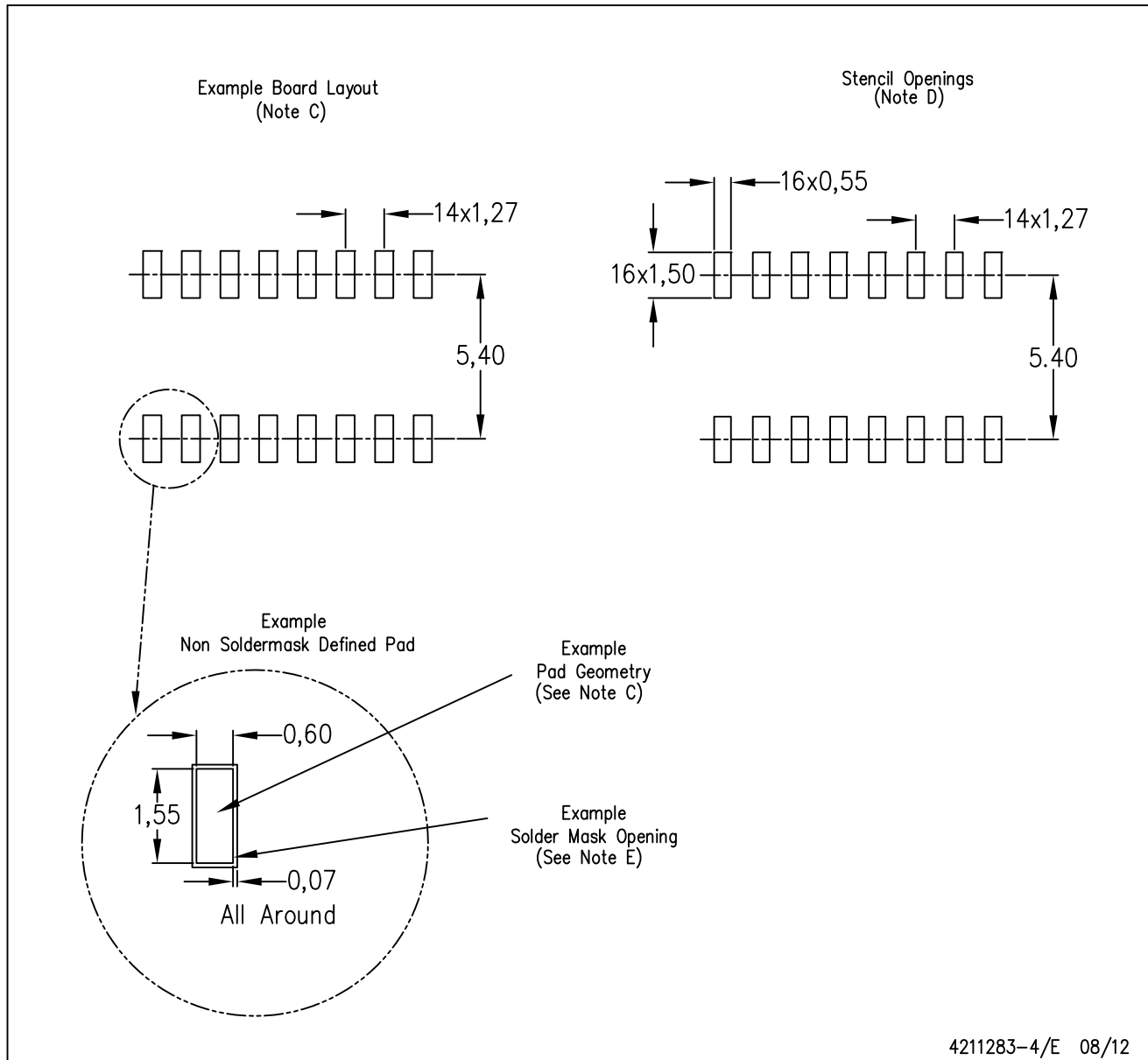
PLASTIC SMALL OUTLINE



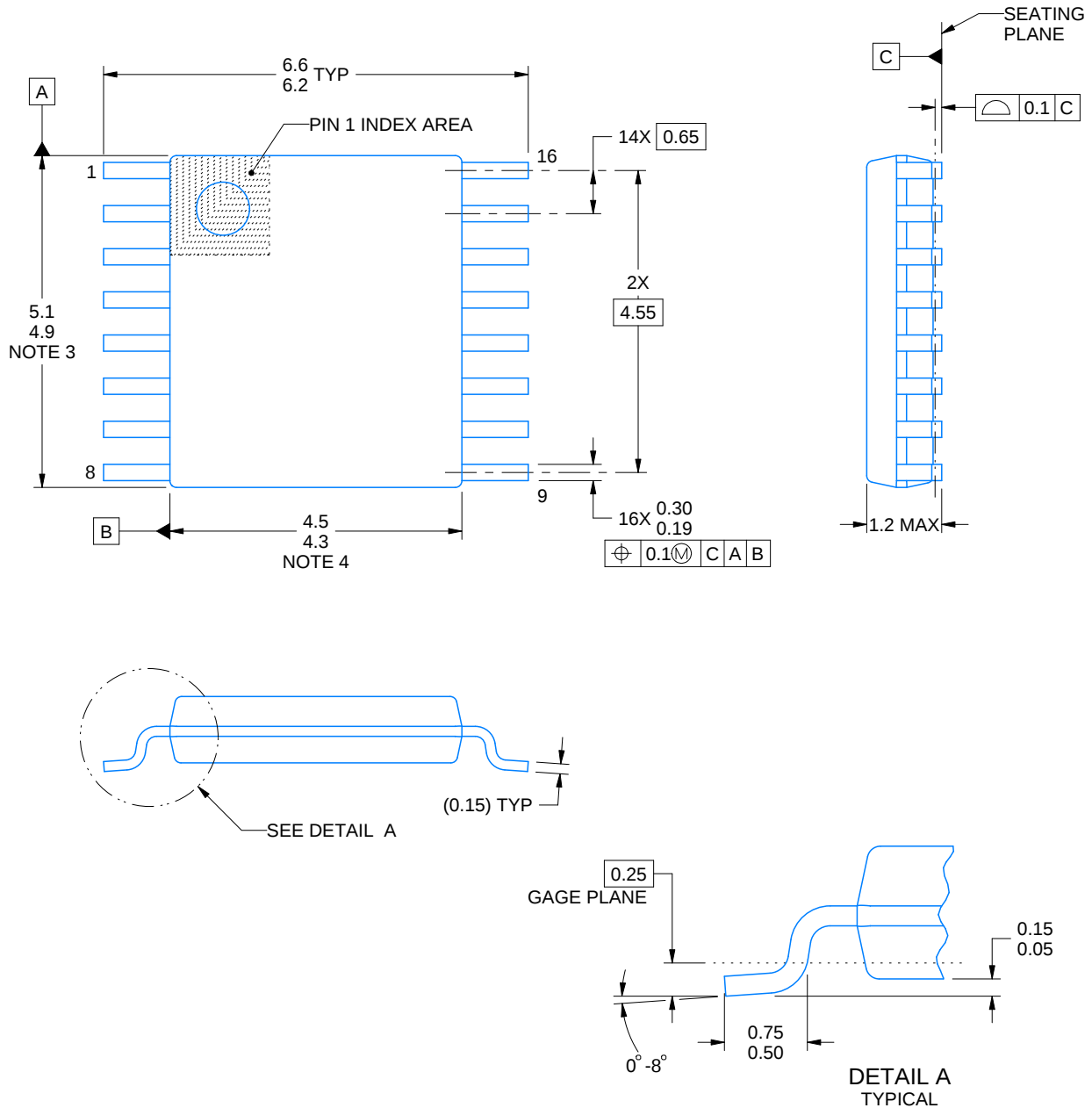
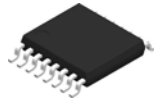
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

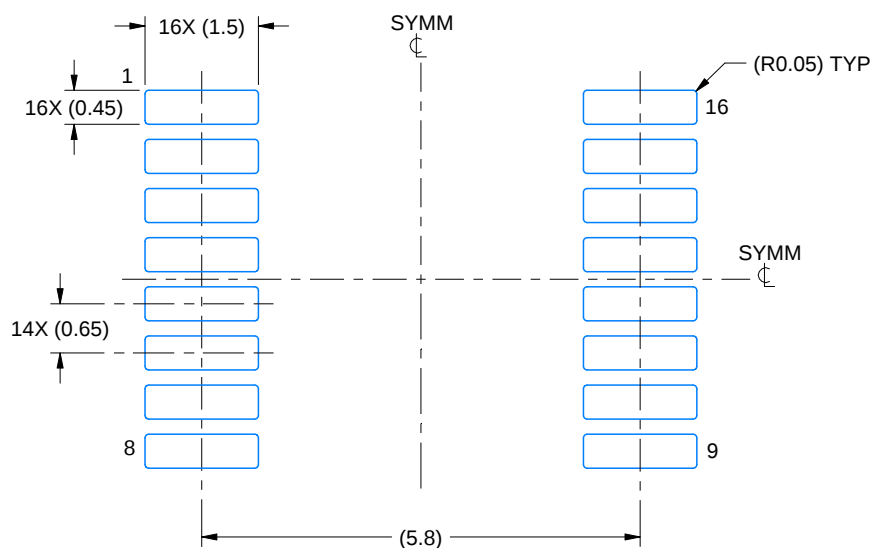
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

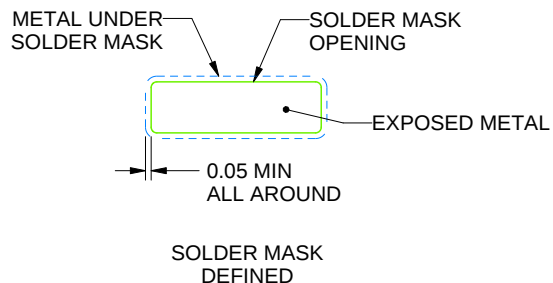
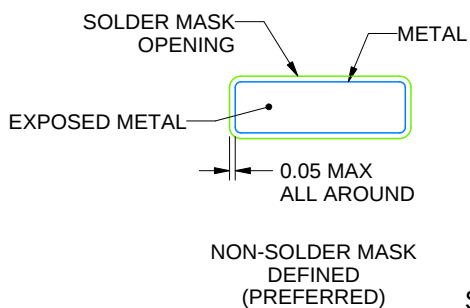
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

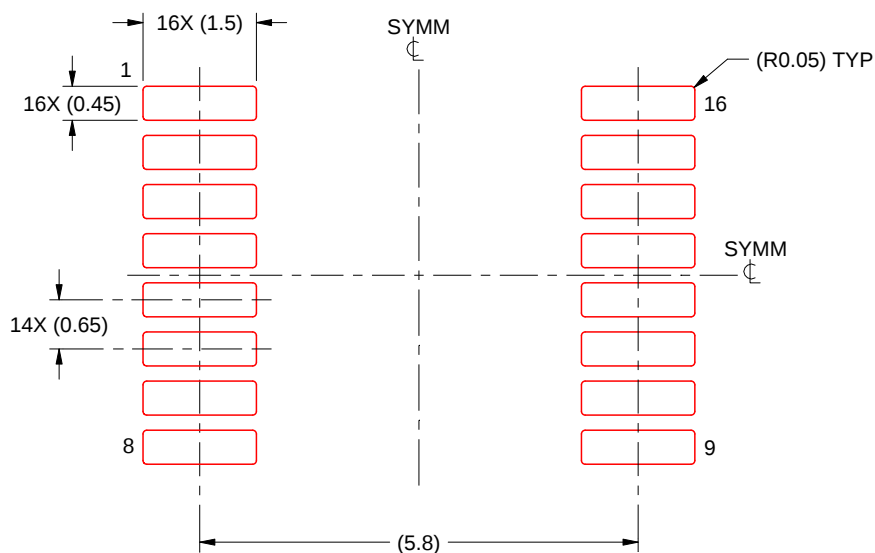
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

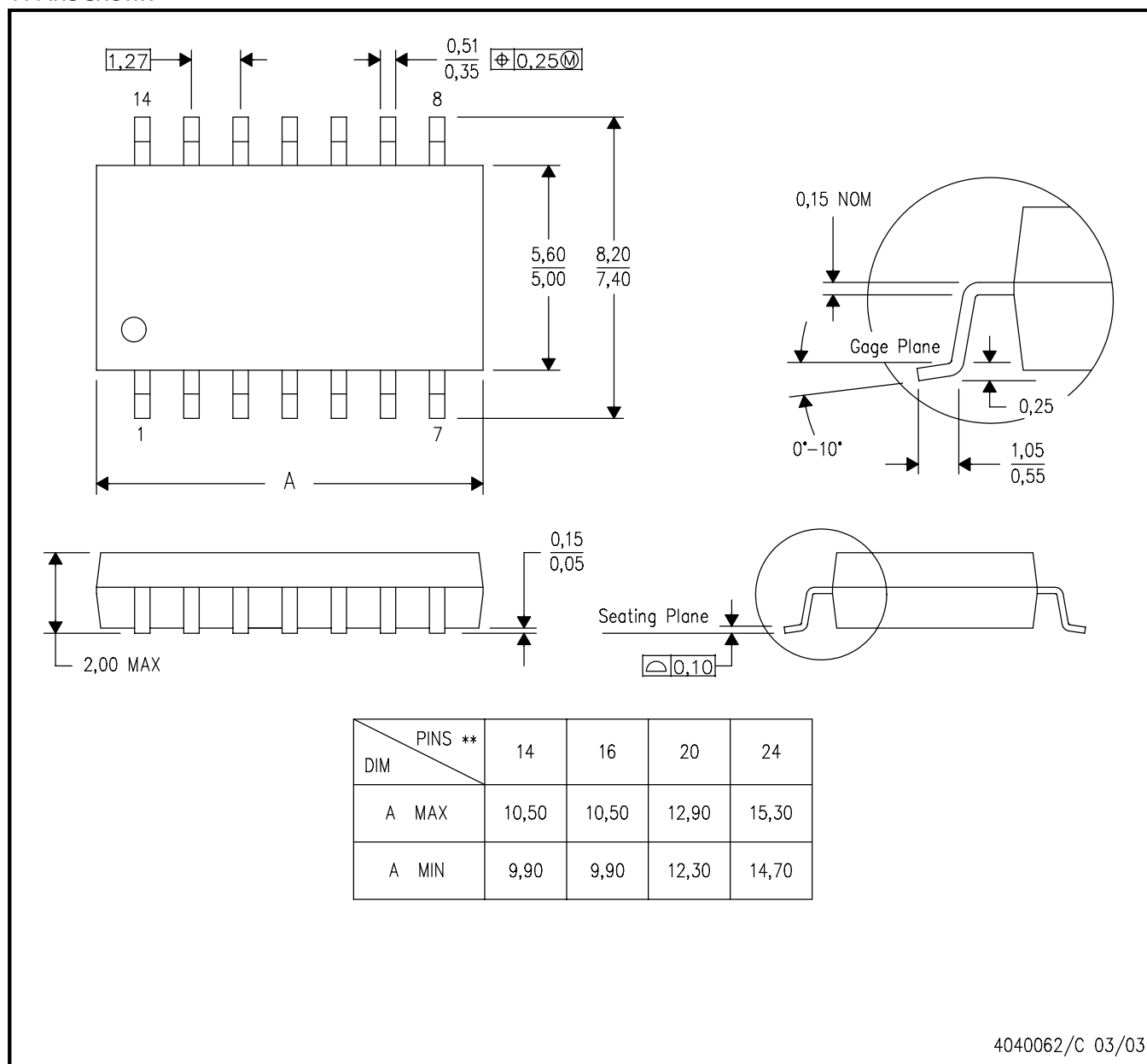
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

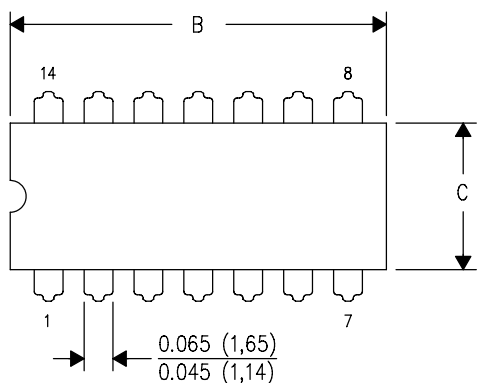


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

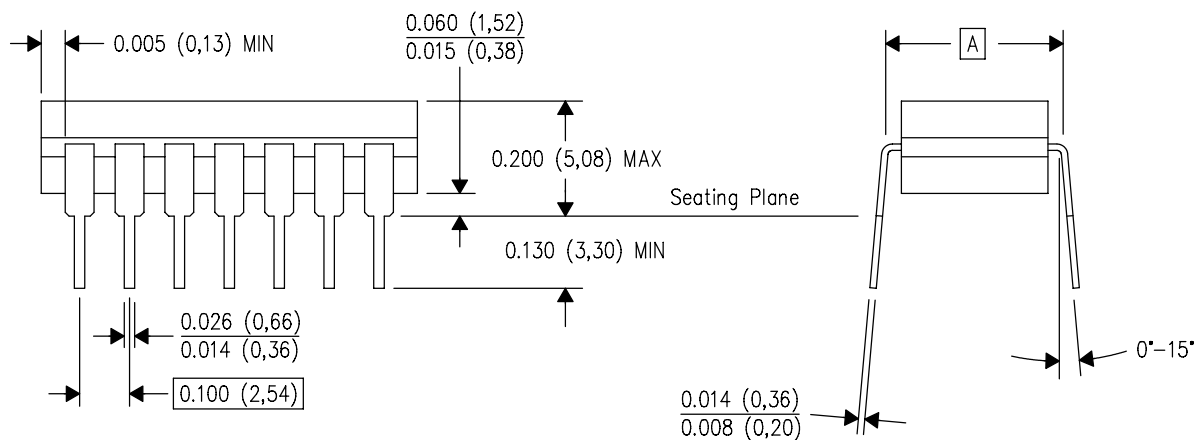
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



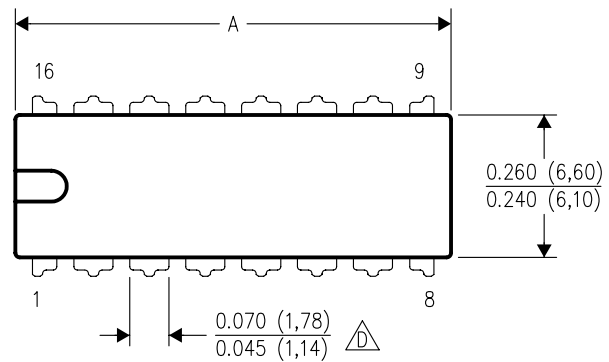
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

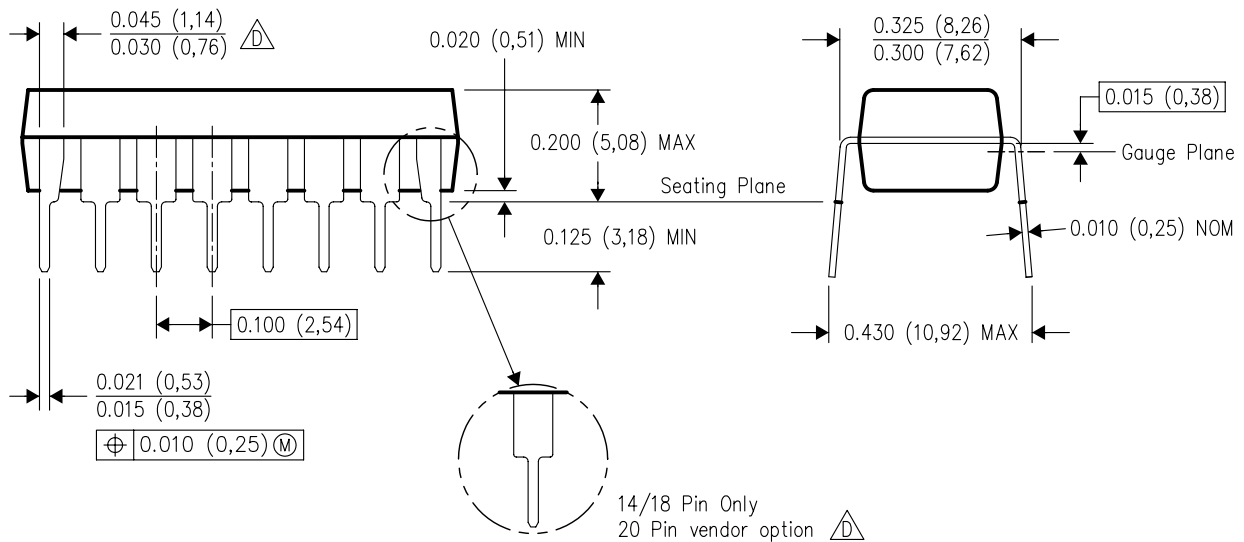
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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