Gigabit 4x4 CROSSPOINT SWITCH

FEATURES

- **Up to 4.25 Gbps Operation**
- **Non-blocking Architecture Allows Each Output to be Connected to Any Input**
- **30 ps of Deterministic Jitter**
- **Selectable Transmit Pre-Emphasis Per Lane**
- **Selectable Receive Equalization**
- **Available Packaging 48 Pin QFN**
- **Propagation Delay Times: 500 ps Typical**
- **Inputs Electrically Compatible With CML Signal Levels**
- **Operates From a Single 3.3-V Supply**
- **Ability to 3-STATE ouputs**
- **Low Power: 560 mW**
- **Integrated Termination Resistors**

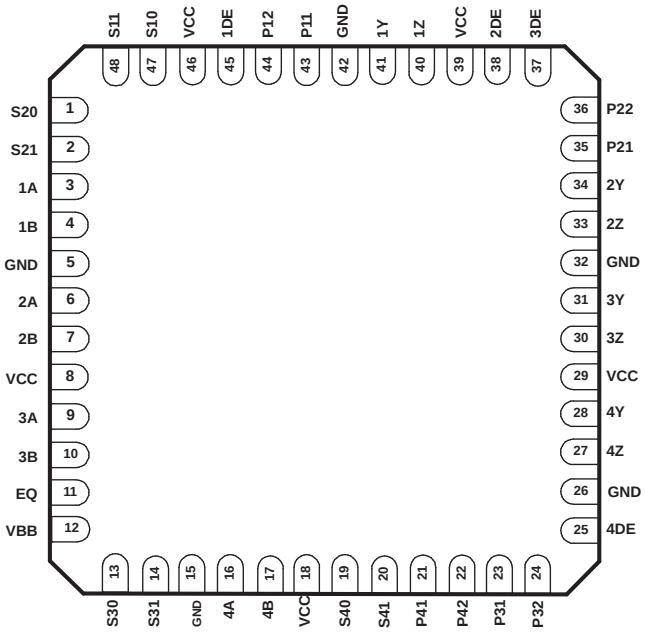
APPLICATIONS

- **Clock Buffering/Clock MUXing**
- **Wireless Base Stations**
- **High-Speed Network Routing**
- **Telecom/Datacom**
- **XAUI 802.3ae Protocol Backplane Redundancy**

DESCRIPTION

The SN65LVCP404 is a 4x4 non-blocking crosspoint switch in a flow-through pin-out allowing for ease in PCB layout. VML signaling is used to achieve a high-speed data throughput while using low power. Each of the output drivers includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVCP404 incorporates 100-Ω termination resistors for those applications where board space is a premium. Built-in transmit pre-emphasis and receive equalization for superior signal integrity performance.

The SN65LVCP404 is characterized for operation from -40°C to 85°C.



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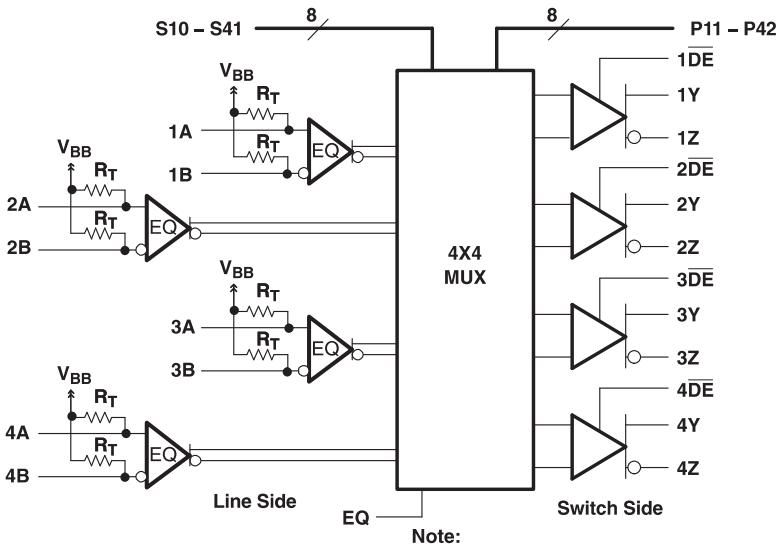
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM



Note:

V_{BB}: Receiver input internal biasing voltage (allows ac coupling)

EQ: Input Equalizer (compensates for frequency dependent transmission line loss of backplanes)

R_T: Internal 50–Ohm receiver termination (100–Ohm differential)

Preemphasis: Output precompensation for transmission line losses

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
High Speed I/O			
xA xB	3, 6, 9, 16 4, 7, 10, 17	Differential Inputs (with 50-Ω termination to Vbb) xA=P; xB=N	Line Side Differential Inputs CML compatible
xY xZ	41, 34, 31, 28 40, 33, 30, 27	Differential Output xY=P; xZ=N	Switch Side Differential Outputs. VML
Control Signals			
x$\overline{DE}$	45, 38, 37, 25	Input	Data Enable; Active Low; LVTTL; When not enabled the ouput is in 3-STATE mode for power savings
S10 - S41	1, 2, 13, 14, 19, 20, 47, 48	Input; S1x = Channel 1 bit one	Switching Selection; LVTTL
P11-P42	43, 44, 35, 36, 23, 24, 21, 22	Input; P1x- Channel 1 bit one	Output Preemphasis Control; LVTTL
EQ	11	Input; Selection for receive equalization setting	EQ = 1 (default) is for the 5 dB setting, EQ = 0 is for the 12 dB setting
Power Supply			
VCC	8, 18, 29, 39, 46	Power	Power Supply 3.3v ±5%
GND	5, 15, 26, 32, 42		
Thermal Pad			The ground center pad of the package must be connected to GND plane.
V_{BB}	12	Input	Receiver input biasing voltage. For ac coupling, V_{BB} should be left floating for optimal bias value. For dc coupling, V_{BB} can driven to change the common mode. V_{BB} should not be tied to ground.

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EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

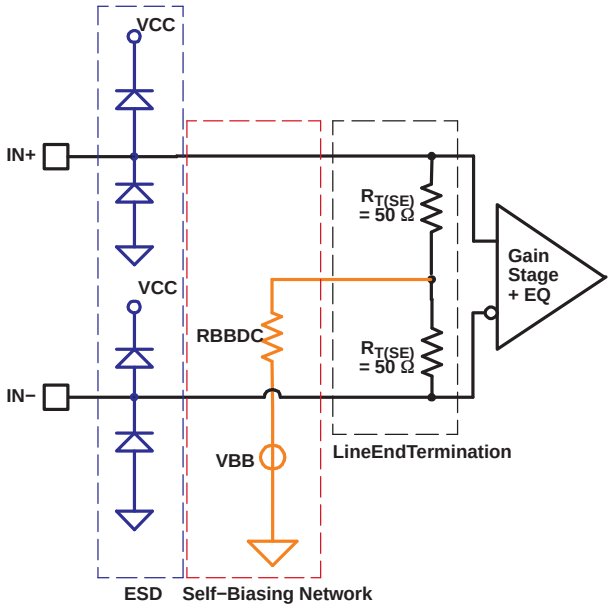

Figure 1. Equivalent Input Circuit Design

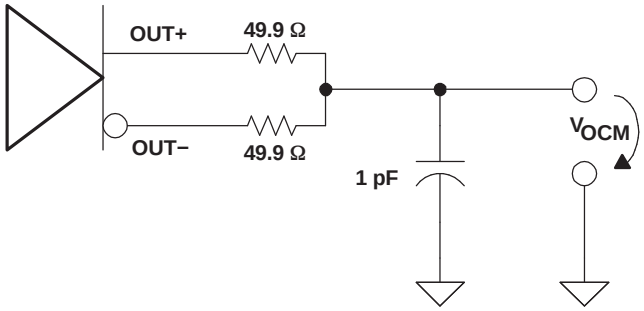

Figure 2. Common-Mode Output Voltage Test Circuit

Table 1. CROSSPOINT LOGIC TABLES

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S41	4Y/4Z
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

AVAILABLE OPTIONS

T_A	DESCRIPTION	PACKAGED DEVICE(1)
		RGZ (48 pin)
-40°C to 85°C	Serial multiplexer	SN65LVCP404

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., SN65LVCP404RGZR).

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PACKAGE THERMAL CHARACTERISTICS

PACKAGE THERMAL CHARACTERISTICS[1]		NOM	UNIT
θ_{JA} (junction-to-ambient)	4-layer JEDEC Board (JESD51-7) using eight GND-vias θ-0.2 on the center pad as shown in the section: *Recommended PCB footprint* with boundary and environment conditions of JEDEC Board (JESD51-2)	33	°C/W
θ_{JB} (junction-to-board)		20	°C/W
θ_{JC} (junction-to-case)		23.6	°C/W
PSI-jt (junction-to-top pseudo)		0.6	°C/W
PSI-jb (junction-to-board pseudo)		19.4	°C/W
θ_{JP} (junction-to-pad)		5.4	°C/W

(1) See application note SPRA953 for a detailed explanation of thermal parameters (http://www-s.ti.com/sc/psheets/spra953/spra953.pdf).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

				UNIT
V_{CC}	Supply voltage range[2]			–0.5 V to 6 V
	Voltage range		Control inputs, all outputs	–0.5 V to (V_{CC} + 0.5 V)
			Receiver inputs	–0.5 V to 4 V
	ESD	Human Body Model[3]	All pins	3 kV
		Charged-Device Model[4]	All pins	500 V
T_J	Maximum junction temperature			See Package Thermal Characteristics Table
	Moisture sensitivity level			2
	Reflow temperature package soldering, 4 seconds			260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

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RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
dR	Operating data rate				4.25	Gbps
V_{CC}	Supply voltage		3.135	3.3	3.465	V
$V_{CC(N)}$	Supply voltage noise amplitude	10 Hz to 2.125 GHz			20	mV
T_J	Junction temperature				125	°C
T_A	Operating free-air temperature (1)		-40		85	°C
DIFFERENTIAL INPUTS						
V_{ID}	Receiver peak-to-peak differential input voltage (2)	$dR_{(in)}$ ≤ 4.25 Gbps	100		1750	mV_{PP}
		1.25 Gbps < $dR_{(in)}$ ≤ 4.25 Gbps	100		1560	mV_{PP}
		$dR_{(in)}$ > 4.25 Gbps	100		1000	mV_{PP}
V_{ICM}	Receiver common-mode input voltage	Note: for best jitter performance ac coupling is recommended.	1.5	1.6	$V_{CC} - \frac{\lvert V_{ID}\rvert}{2}$	V
CONTROL INPUTS						
V_{IH}	High-level input voltage		2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
DIFFERENTIAL OUTPUTS						
R_L	Differential load resistance		80	100	120	Ω

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.
(2) Differential input voltage V_{ID} is defined as | IN+ – IN– |.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
DIFFERENTIAL INPUTS						
V_{IT+}	Positive going differential input high threshold				50	mV
V_{IT-}	Negative going differential input low threshold		–50			mV
$A_{(EQ)}$	Equalizer gain	at 1.875 GHz (EQ=0)		12		dB
$R_{T(D)}$	Termination resistance, differential		80	100	120	Ω
V_{BB}	Open-circuit Input voltage (input self-bias voltage)	AC-coupled inputs		1.6		V
$R_{(BBDC)}$	Biasing network dc impedance			30		kΩ
$R_{(BBAC)}$	Biasing network ac impedance	375 MHz		42		Ω
		2.125 GHz		8.4		
DIFFERENTIAL OUTPUTS						
V_{ODH}	High-level output voltage	R_L = 100 Ω ±1%, Px_2 = Px_1=0; 4 Gbps alternating 1010-pattern; Figure 3		650		mV_{PP}
V_{ODL}	Low-level output voltage			–650		mV_{PP}
$V_{ODB(PP)}$	Output differential voltage without preemphasis (2)		1000	1300	1500	mV_{PP}
V_{OCM}	Output common mode voltage	See Figure 2		1.65		V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			1		mV

(1) All typical values are at T_A = 25°C and V_{CC} = 3.3 V supply unless otherwise noted. They are for reference purposes and are not production tested.
(2) Differential output voltage $V_{(ODB)}$ is defined as | OUT+ – OUT– |.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{(PE)}$	Output preemphasis voltage ratio, $\frac{V_{ODB(PP)}}{V_{ODPE(PP)}}$	R_L = 100 Ω±1%; x = L or S; See Figure 3	Px_2:Px_1 = 00		0		dB
			Px_2:Px_1 = 01		3		
			Px_2:Px_1 = 10		6		
			Px_2:Px_1 = 11		9		
$t_{(PRE)}$	Preemphasis duration measurement	Output preemphasis is set to 9 dB during test Px_x = 1; Measured with a 100-MHz clock signal; R_L = 100 Ω ±1%, See Figure 4			175		ps
r_o	Output resistance	Differential on-chip termination between OUT+ and OUT–			100		Ω
CONTROL INPUTS							
I_{IH}	High-level Input current	VIN = VCC				5	µA
I_{IL}	Low-level Input current	VIN = GND		-125	-90		µA
$R_{(PU)}$	Pullup resistance				35		kΩ
POWER CONSUMPTION							
P_D	Device power dissipation	All outputs terminated 100 Ω			560	750	mW
P_Z	Device power dissipation in 3-State	All outputs in 3-state				600	mW
I_{CC}	Device current consumption	All outputs terminated 100 Ω	PRBS 2^{7-1} pattern at 4.25 Gbps			220	mA

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
MULTIPLEXER						
$t_{(SM)}$	Multiplexer switch time	Multiplexer to valid output		3	6	ns
DIFFERENTIAL OUTPUTS						
t_{PLH}	Low-to-high propagation delay	Propagation delay input to output See Figure 6		0.5	0.7	ns
t_{PHL}	High-to-low propagation delay			0.5	0.7	ns
t_r	Rise time	20% to 80% of $V_{O(DB)}$; Test Pattern: 100-MHz clock signal; See Figure 5 and Figure 8		80		ps
t_f	Fall time			80		ps
$t_{sk(p)}$	Pulse skew, $\lvert t_{PHL} – t_{PLH} \rvert$(2)				20	ps
$t_{sk(o)}$	Output skew(3)	All outputs terminated with 100 Ω		25	100	ps
$t_{sk(pp)}$	Part-to-part skew(4)				300	ps
t_{zd}	3-State switch time to Disable	Assumes 50 Ω to Vcm and 150 pF load on each output			20	ns
t_{ze}	3-State switch time to Enable	Assumes 50 Ω to Vcm and 150 pF load on each output			10	ns
RJ	Device random jitter, rms	See Figure 8 for test circuit. BERT setting 10^{-15} Alternating 10-pattern.		0.8	2	ps-rms

(1) All typical values are at 25°C and with 3.3 V supply unless otherwise noted.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(3) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any two outputs of a single device.
(4) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
DJ	Intrinsic deterministic device jitter (5)(6), peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 8 for the test circuit.	PRBS 2^{7-1} pattern	4.25 Gbps			30	ps
	Absolute deterministic output jitter(7), peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 8 for the test circuit.	PRBS 2^{7-1} pattern	1.25Gbps; EQ=1 Over 25-inch FR4 trace		7		ps
				4.25 Gbps; EQ=0 Over FR4 trace 2-inch to 43 inches long		20		

(5) Intrinsic deterministic device jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation ($DJ_{(OUT)} – DJ_{(IN)}$), where $DJ_{(OUT)}$ is the total peak-to-peak deterministic jitter measured at the output of the device in PSPP. $DJ_{(IN)}$ is the peak-to-peak deterministic jitter of the pattern generator driving the device.
(6) The SN65LVCP404 built-in passive input equalizer compensates for ISI. For a 25-inch FR4 transmission line with 8-mil trace width, the LVCP404 typically reduces jitter by 60 ps from the device input to the device output.
(7) Absolute deterministic output jitter reflects the deterministic jitter measured at the SN65LVCP404 output. The value is a real measured value with a Bit error tester as described in Figure 8. The absolute DJ reflects the sum of all deterministic jitter components accumulated over the link: $DJ_{(absolute)} = DJ_{(Signal\ generator)} + DJ_{(transmission\ line)} + DJ_{(intrinsic(LVCP404))}$.

Table 2. Preemphasis Controls PL_2, PL_1, PS_2, and PS_1

Px_2(1)	Px_1(1)	OUTPUT PREEMPHASIS LEVEL IN dB	OUTPUT LEVEL IN mVpp		TYPICAL FR4 TRACE LENGTH
			DE-EMPHASIZED	PRE-EMPHASIZED	
0	0	0 dB	1200	1200	10 inches of FR4 trace
0	1	3 dB	850	1200	20 inches of FR4 trace
1	0	6 dB	600	1200	30 inches of FR4 trace
1	1	9 dB	425	1200	40 inches of FR4 trace

(1) x = L or S

Table 3. Receive Equalization Settings

EQ	EQUALIZATION	TYPICAL TRACE
1	5 dB	25 inches of FR4
0	12 dB	43 inches of FR4

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PARAMETER MEASUREMENT INFORMATION

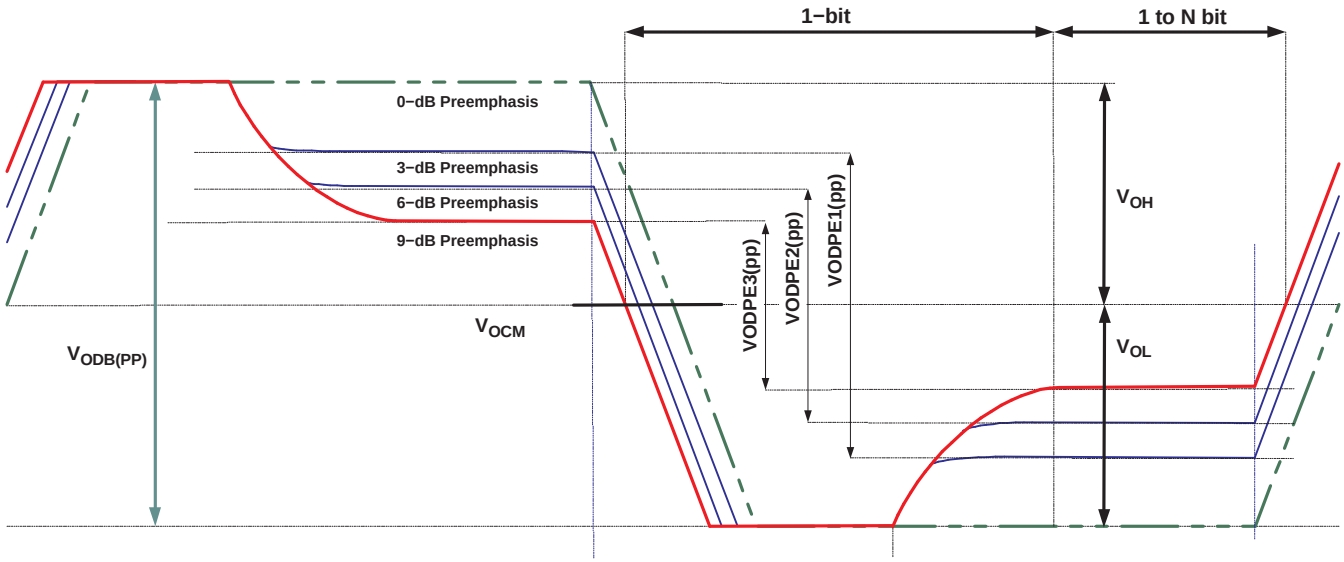

Figure 3. Preemphasis and Output Voltage Waveforms and Definitions

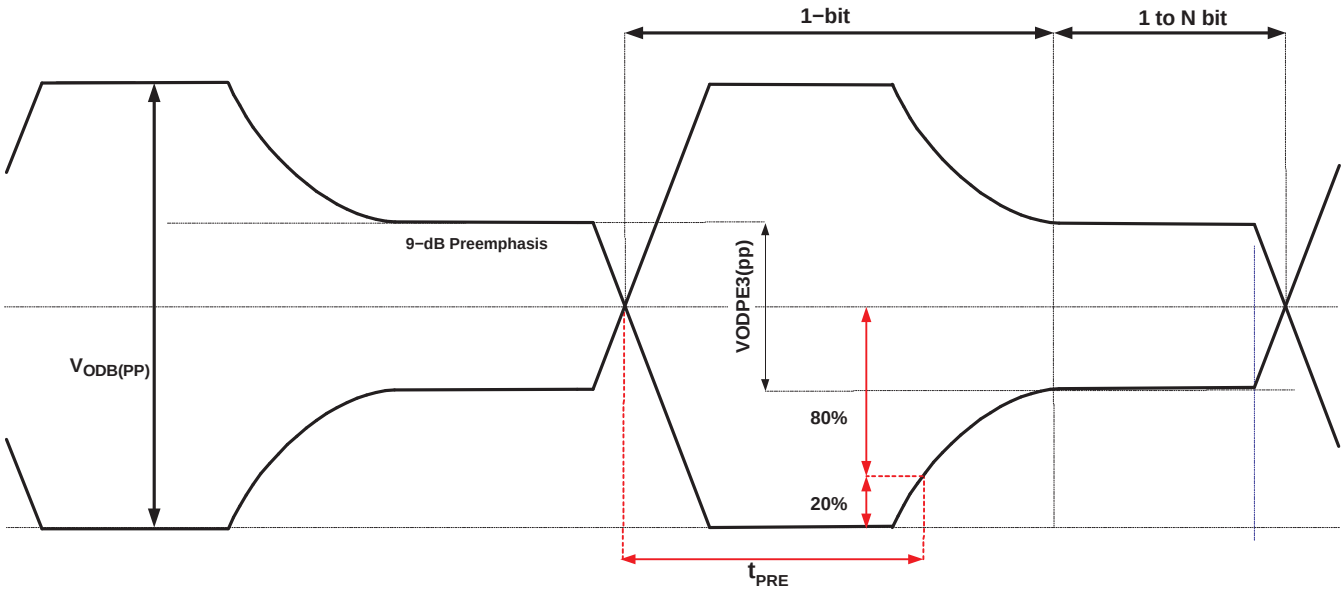

Figure 4. $t_{(PRE)}$ Preemphasis Duration Measurement

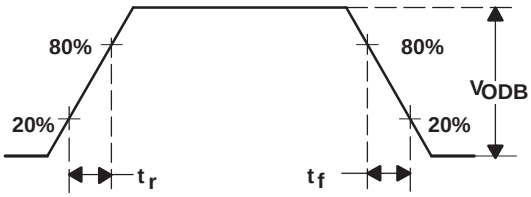

Figure 5. Driver Output Transition Time

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PARAMETER MEASUREMENT INFORMATION (continued)

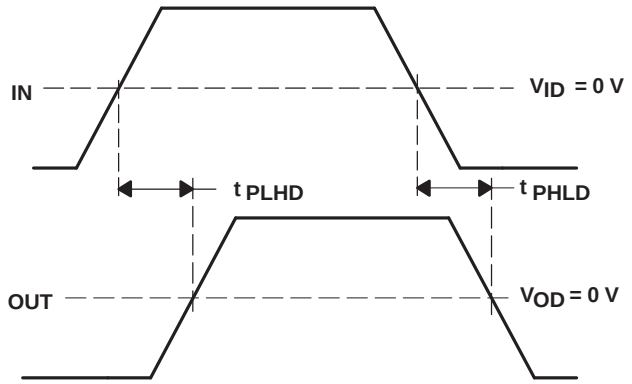
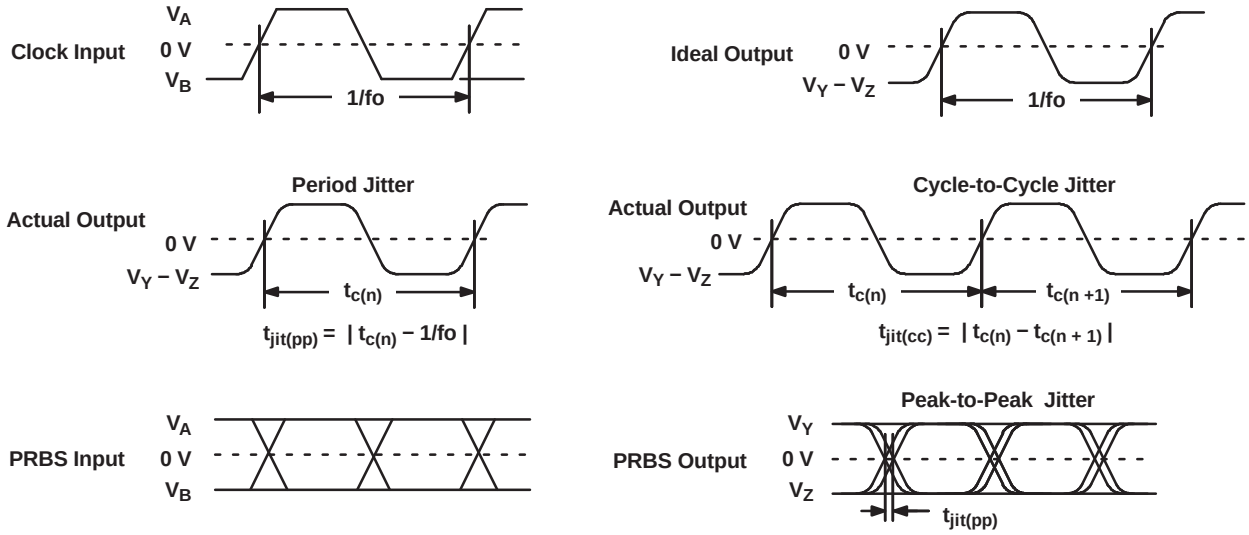


Figure 6. Propagation Delay Input to Output



A. All input pulses are supplied by an Agilent 81250 Stimulus System.

B. The measurement is made with the AgilentParBert measurement software.

Figure 7. Driver Jitter Measurement Waveforms

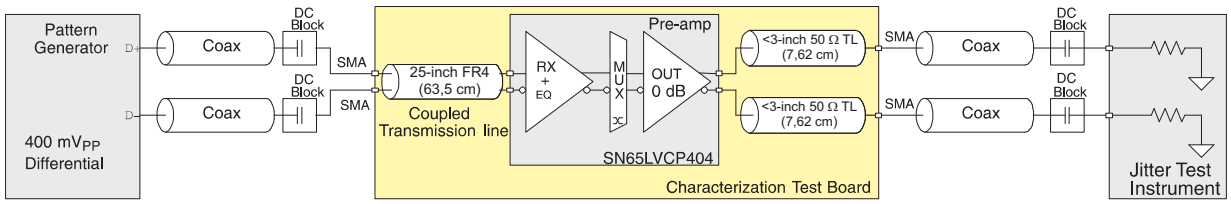


Figure 8. AC Test Circuit — Jitter and Output Rise Time Test Circuit

The SN65LVCP404 input equalizer provides 5-dB frequency gain to compensate for frequency loss of a shorter backplane transmission line. For characterization purposes, a 25-inch (63,5 cm) FR-4 coupled transmission line is used in place of the backplane trace. The 25-inch trace provides roughly 5 dB of attenuation between 375 MHz and 2.125 GHz, representing closely the characteristics of a short backplane trace. The loss tangent of the FR4 in the test board is 0.018 with an effective ε(r) of 4.1.

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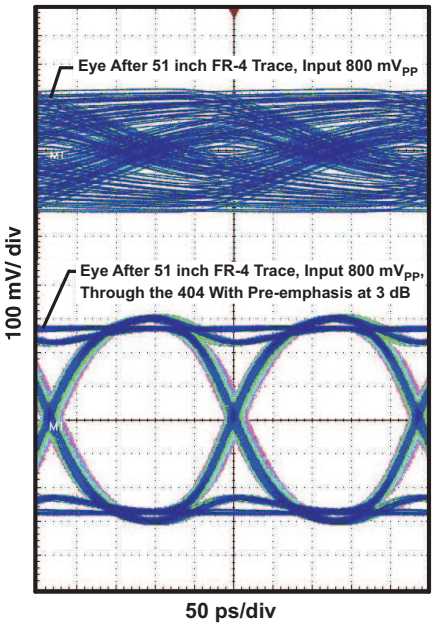
TYPICAL DEVICE BEHAVIOR



NOTE: 51 Inches (129.54 cm) Input Trace, dR = 4.25 Gbps; 2^{7-1} PRBS

Figure 9. Data Input and Output Pattern

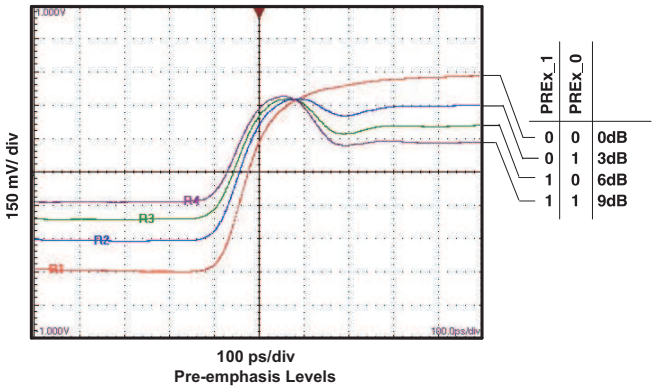


Figure 10. Preemphasis Signal Shape

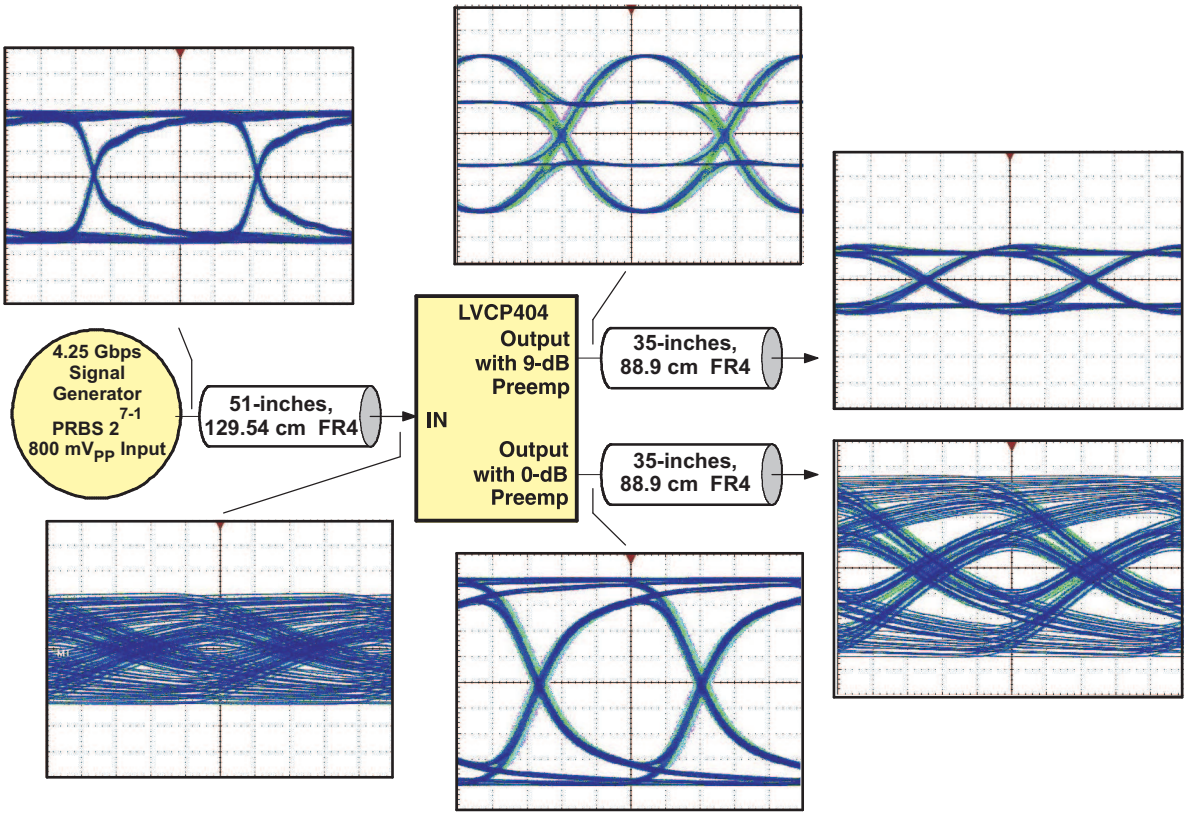


Figure 11. Data Output Pattern

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TYPICAL CHARACTERISTICS

DETERMINISTIC OUTPUT JITTER vs DATA RATE

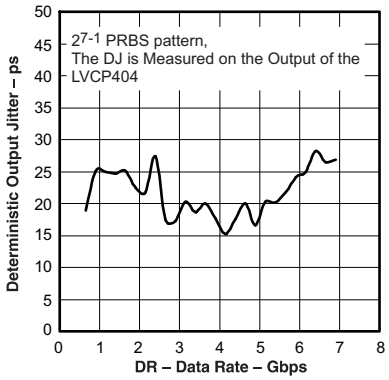


Figure 12.

DETERMINISTIC OUTPUT JITTER vs DIFFERENTIAL INPUT AMPLITUDE

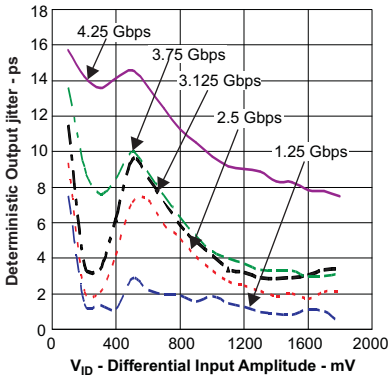


Figure 13.

DIFFERENTIAL OUTPUT VOLTAGE vs DATA RATE

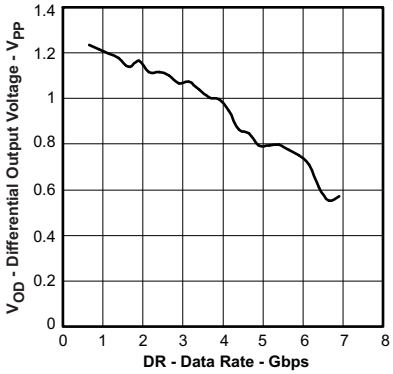


Figure 14.

SUPPLY NOISE vs DETERMINISTIC JITTER vs DATA RATE

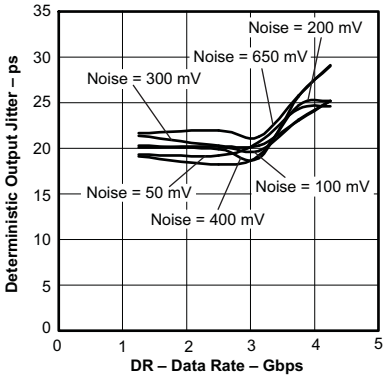


Figure 15.

DETERMINISTIC OUTPUT JITTER vs COMMON-MODE INPUT VOLTAGE

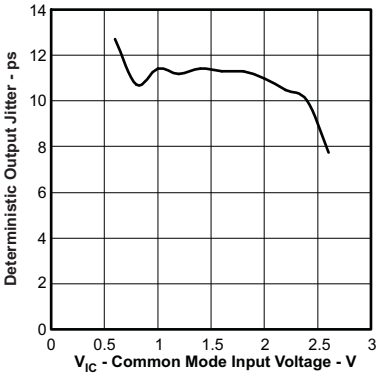
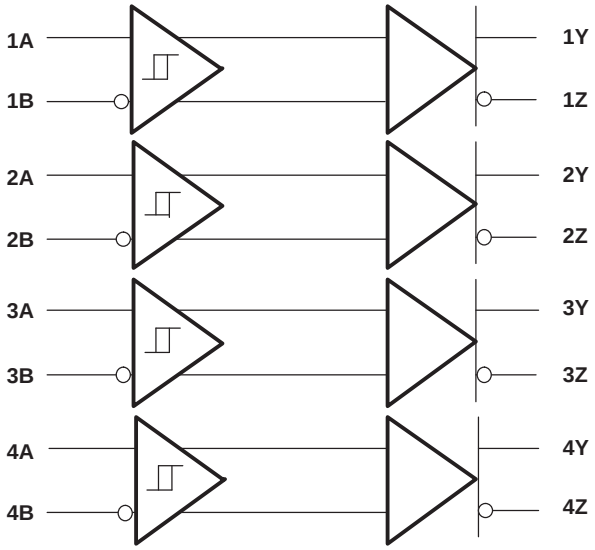


Figure 16.

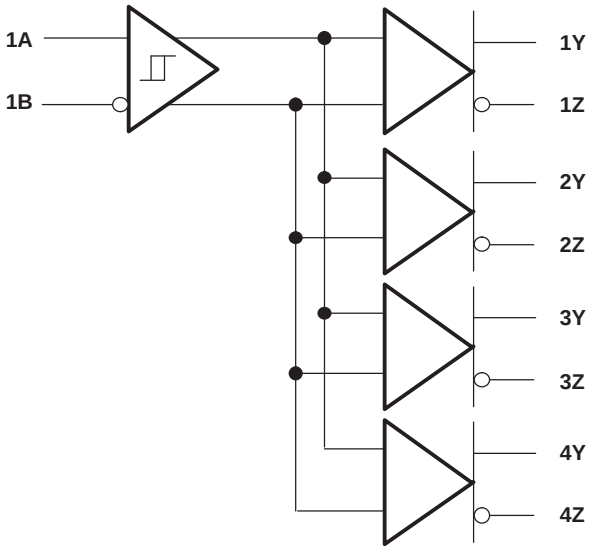
APPLICATION INFORMATION

CONFIGURATION EXAMPLES

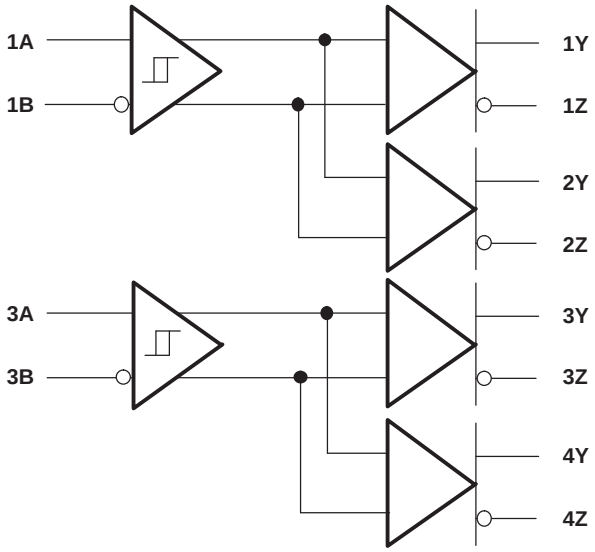
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1



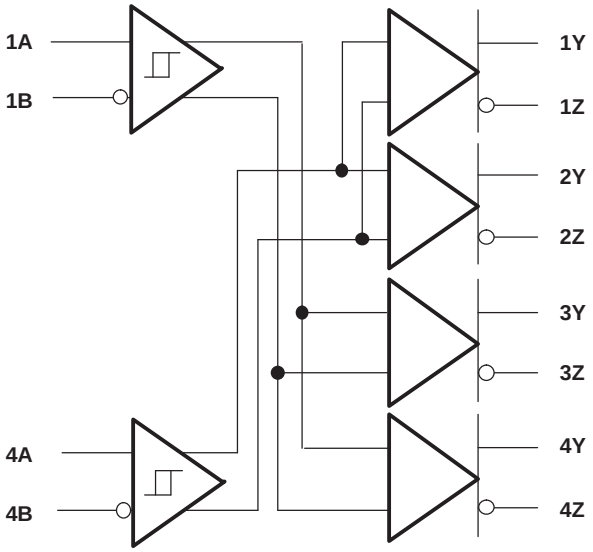
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0



S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0



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BANDWIDTH REQUIREMENTS

Error free transmission of data over a transmission line has specific bandwidth demands. It is helpful to analyze the frequency spectrum of the transmit data first. For an 8B10B coded data stream at 3.75 Gbps of random data, the highest bit transition density occurs with a 1010 pattern (1.875 GHz). The least transition density in 8B10B allows for five consecutive ones or zeros. Hence, the lowest frequency of interest is 1.875 GHz/5 = 375 MHz. Real data signals consist of higher frequency components than sine waves due to the fast rise time. The faster the rise time, the more bandwidth becomes required. For 80-ps rise time, the highest important frequency component is at least 0.6/(π × 80 ps) = 2.4 GHz. Figure 17shows the Fourier transformation of the 375-MHz and 1.875-GHz trapezoidal signal.

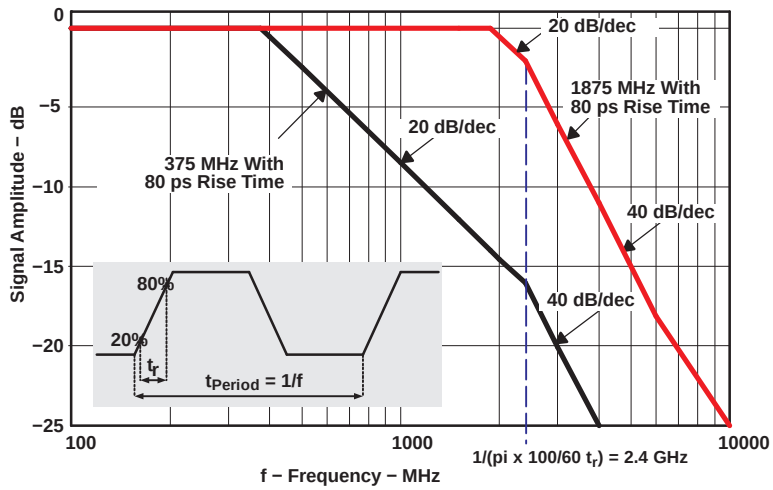

Figure 17. Approximate Frequency Spectrum of the Transmit Output Signal With 80 ps Rise Time

The spectrum analysis of the data signal suggests building a backplane with little frequency attenuation up to 2 GHz. Practically, this is achievable only with expensive, specialized PCB material. To support material like FR4, a compensation technique is necessary to compensate for backplane imperfections.

EXPLANATION OF EQUALIZATION

Backplane designs differ widely in size, layer stack-up, and connector placement. In addition, the performance is impacted by trace architecture (trace width, coupling method) and isolation from adjacent signals. Common to most commercial backplanes is the use of FR4 as board material and its related high-frequency signal attenuation. Within a backplane, the shortest to longest trace lengths differ substantially – often ranging from 8 inches up to 40 inches. Increased loss is associated with longer signal traces. In addition, the backplane connector often contributes a good amount of signal attenuation. As a result, the frequency signal attenuation for a 300-MHz signal might range from 1 dB to 4 dB while the corresponding attenuation for a 2-GHz signal might span 6 dB to 24 dB. This frequency dependent loss causes distortion jitter on the transmitted signal. Each LVCP404 receiver input incorporates an equalizer and compensates for such frequency loss. The SN65LVCP404 equalizer provides 5 dB of frequency gain between 375 MHz and 1.875 GHz, compensating roughly for 20 inches of FR4 material with 8-mil trace width. Distortion jitter improvement is substantial, often providing more than 30-ps jitter reduction. The 5-dB compensation is sufficient for most short backplane traces. For longer trace lengths, it is recommended to enable transmit preemphasis in addition.

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SETTING THE PREEMPHASIS LEVEL

The receive equalization compensates for ISI. This reduces jitter and opens the data eye. In order to find the best preemphasis setting for each link, calibration of every link is recommended. Assuming each link consists of a transmitter (with adjustable pre-emphasis such as LVCP404) and the LVCP404 receiver, the following steps are necessary:

1. Set the transmitter and receiver to 0-dB preemphasis; record the data eye on the LVCP404 receiver output.
2. Increase the transmitter preemphasis until the data eye on the LVCP404 receiver output looks the cleanest.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVCP404RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP404	Samples
SN65LVCP404RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP404	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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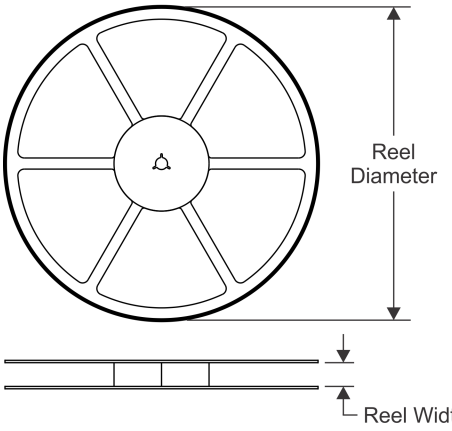
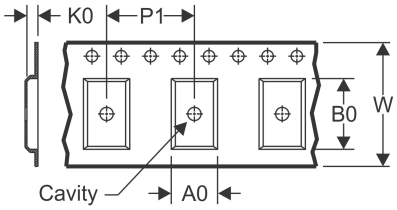
TAPE AND REEL INFORMATION

REEL DIMENSIONS

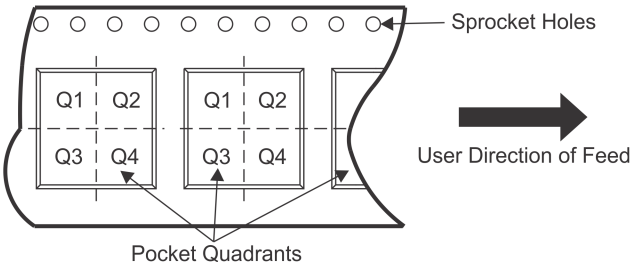


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

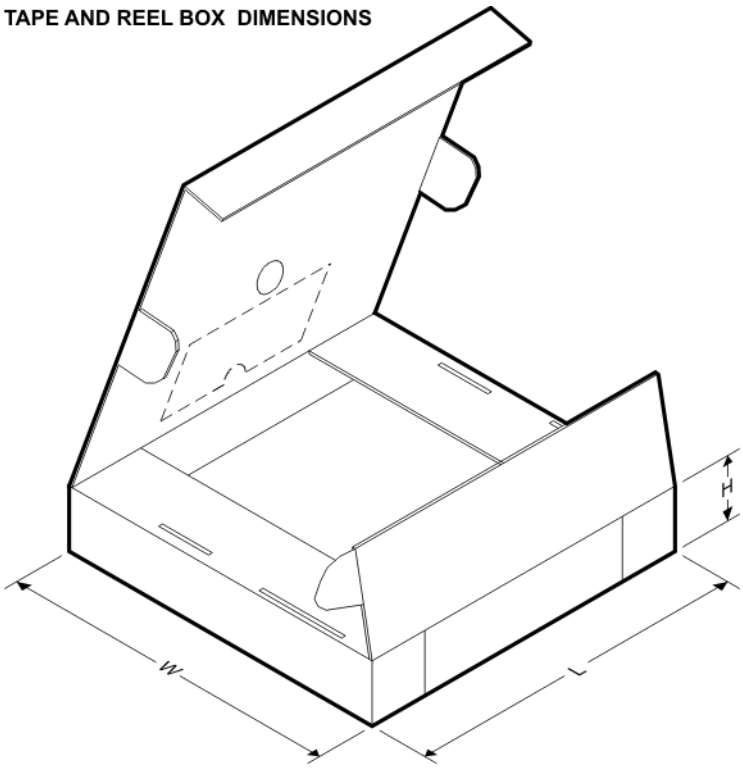
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP404RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN65LVCP404RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP404RGZR	VQFN	RGZ	48	2500	853.0	449.0	35.0
SN65LVCP404RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

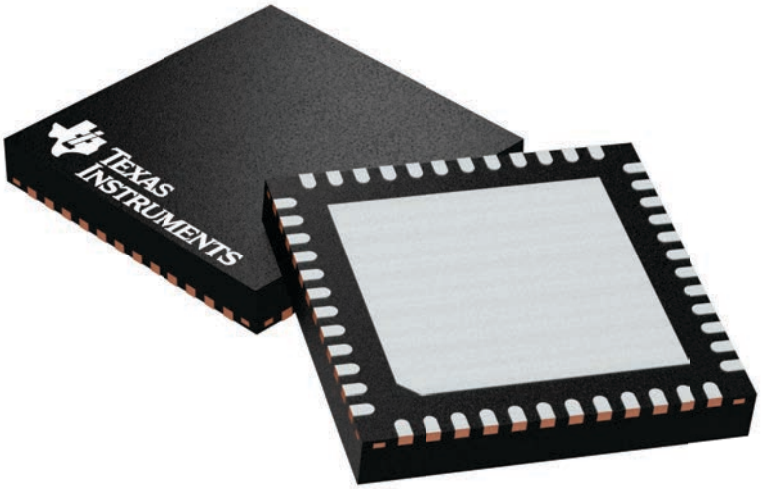
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

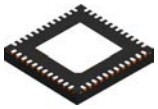
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

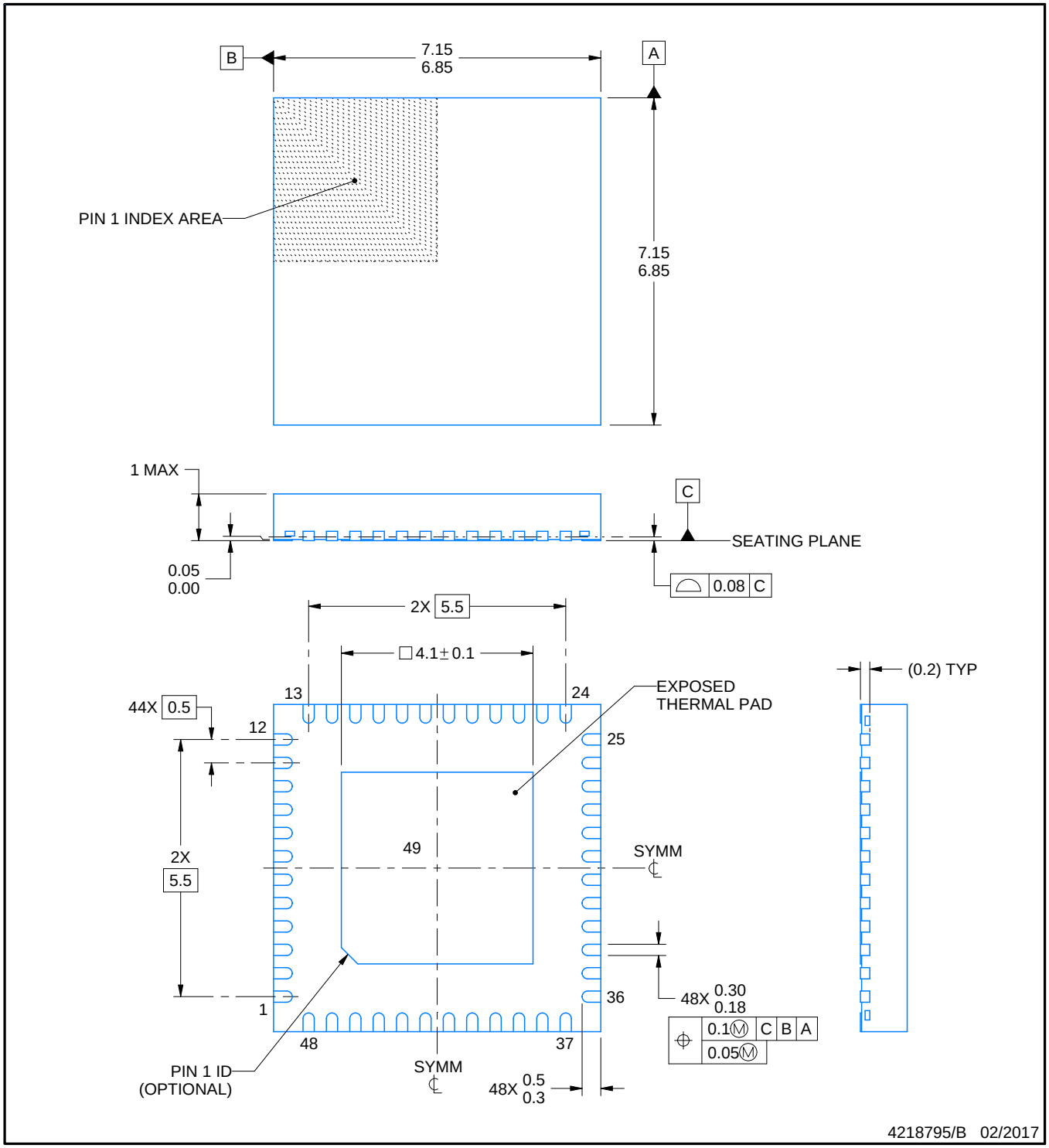
RGZ0048B



PACKAGE OUTLINE

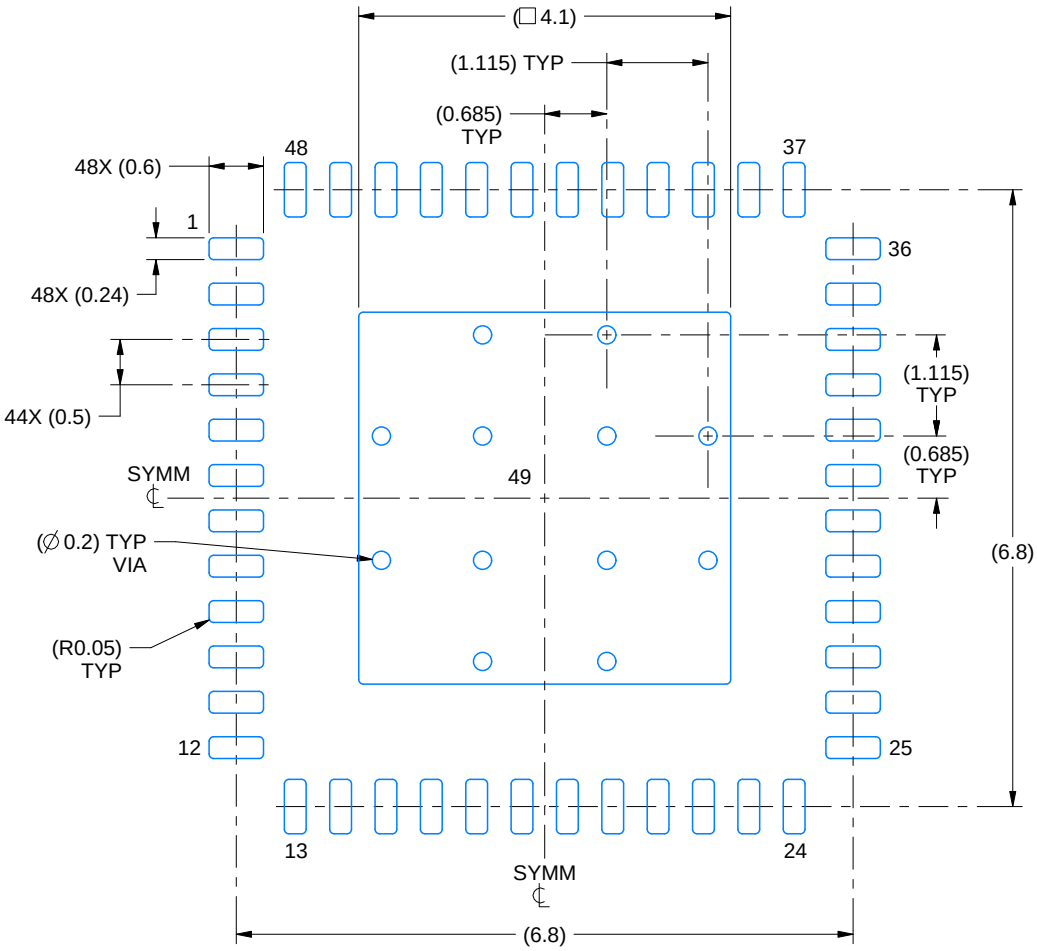
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

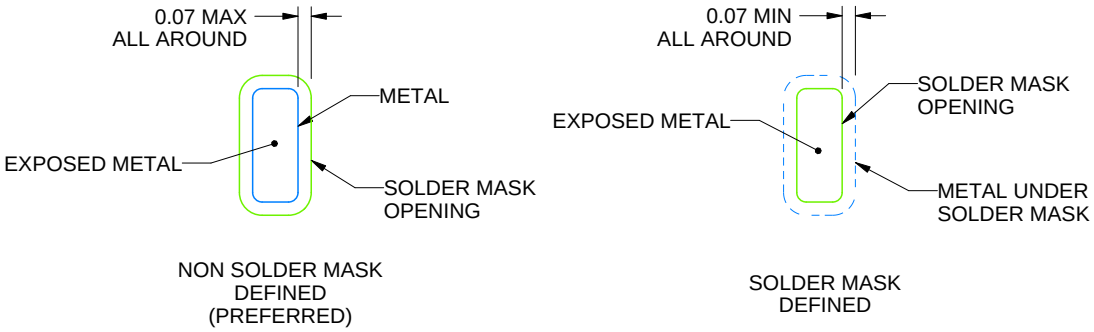


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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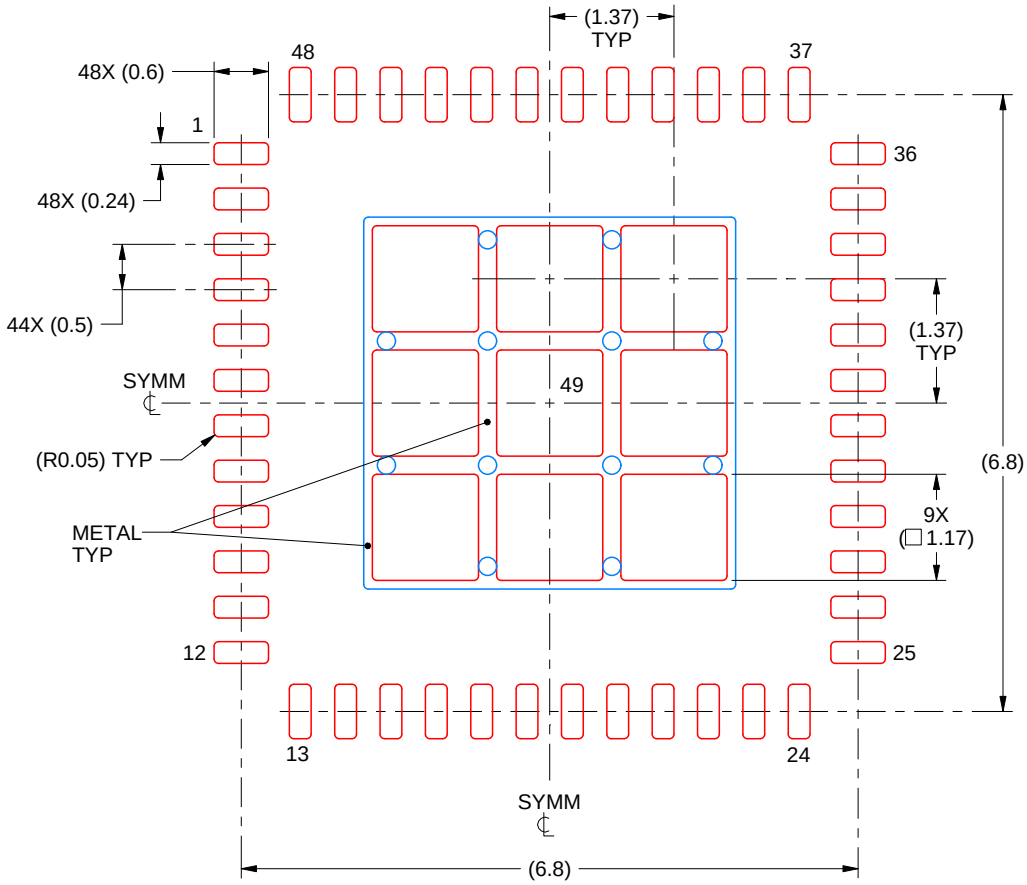
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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