TPS735 500mA、低静态电流、低噪声、高 PSRR 低压降线性稳压器

1 特性

- 输入电压：2.7V 至 6.5V
- 带 EN 引脚的 500mA 低压降稳压器
- 低 I_Q： 45µA
- 提供了多个输出电压版本：
  - 1.2V 至 4.3V 固定输出
  - 1.25V 至 6V 可调输出
- 高 PSRR：1kHz 频率下为 68dB
- 低噪声：13.2µV_{RMS}
- 快速启动时间：45µs
- 使用陶瓷 2.2µF 低 ESR 输出电容器实现稳定运行
- 出色的负载和线路瞬态响应
- 2% 的总体精度（负载、线路和温度，V_{OUT} > 2.2V）
- 极低的压降：500mA 电流下为 280mV
- 2mm × 2mm WSON-6 和 3mm × 3mm SON-8 封装

2 应用

- 后直流/直流转换器纹波滤除
- IP 网络摄像机
- 大型基站
- 恒温器

3 说明

TPS735 低压降 (LDO)、低功耗线性稳压器可提供出色的交流性能以及极低的接地电流。可提供高电源抑制比 (PSRR)、低噪声、快速启动以及出色的线路和负载瞬态响应，同时消耗极低的 45µA（典型值）接地电流。

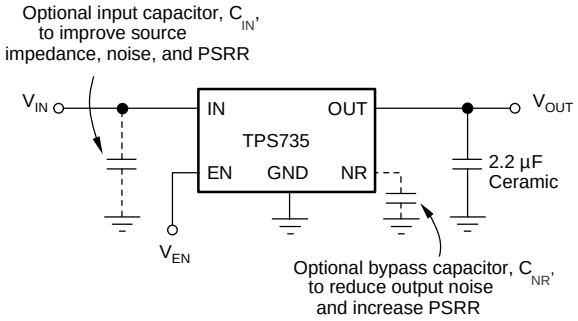
TPS735 器件与陶瓷电容器搭配使用时可保持稳定，并且该器件使用先进的 BiCMOS 制造工艺，能够在输出 500mA 电流时产生 280mV 的典型压降电压。TPS735 器件使用精密电压基准和反馈环路，可在全部负载、线路、过程和温度变化范围内实现 2% 的总体精度 (V_{OUT} > 2.2V)。此器件的额定 T_J = –40°C 至 +125°C，采用薄型 3mm × 3mm SON-8 封装和 2mm × 2mm WSON-6 封装。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
TPS735	WSON (6)	2.00mm × 2.00mm
	SON (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision L (January 2015) to Revision M — **Page**

- 根据最新产品说明书和翻译标准更新了产品说明书文本 ... 1
- 已更改 在文档标题中将“超低噪声”更改成了“低噪声” ... 1
- 已更改 将低 I_Q 从 46µA 更改成了 45µA（在*特性*、*说明* 和*应用信息* 部分中） ... 1
- 已更改 将*特性* 列表中的“标准”更改成了“陶瓷” ... 1
- 已更改 在*特性* 列表中将 6 引脚封装从“SON”更改成了“WSON” ... 1
- 已删除 从 *应用* 部分中删除了“打印机、WiFi®、WiMax 模块、手机、智能手机和微处理器电源” ... 1
- 已添加 在*应用* 部分中添加了“后直流/直流纹波滤除、IP 网络摄像机、大型基站和恒温器” ... 1
- 已更改 将 T_A 更改成了 T_J（在*说明* 部分中） ... 1
- 已更改 在*说明* 部分中将 6 引脚封装从“SON”更改成了“WSON” ... 1
- 已更改 在*器件信息* 表中将封装从 VSON (6) 更改成了 WSON (6) ... 1
- Changed 6-pin DRB package designator from "VSON" to "SON" in *Pin Configurations and Functions* section ... 4
- Changed 6-pin DRV package designator from "VSON" to "WSON" in *Pin Configurations and Functions* section ... 4
- Added "feedback resistor" parameter to *Recommended Operating Conditions* table ... 5
- Changed DRV package designator from "VSON" to "WSON" in *Thermal Information* table ... 6
- Changed DRB package designator from "VSON" to "SON" in *Thermal Information* table ... 6
- 已更改 *TPS735 Ground Pin Current (Disable) vs Temperature* in *Typical Characteristics* section ... 8
- 已更改 *TPS735 Dropout Voltage vs Output Current* in *Typical Characteristics* section ... 8
- Updated Equation 1 ... 14
- 已更改 x-axis scale from "10 ms/div" to "10 µs/div" in 图 17 ... 15
- 已更改 x-axis scale from "10 ms/div" to "10 µs/div" in 图 18 ... 15
- 已更改 V_{OUT} starting value to 0 V in 图 19 ... 15
- Updated Equation 2 ... 17
- Updated Equation 3 ... 17
- 已更改 DRV package designator from "SON" to "WSON" in *Measuring Points for T_T and T_B* ... 19
- 已删除 在*相关文档* 部分中删除了对热性能信息文档的引用 ... 20

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Changes from Revision K (August, 2013) to Revision L **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、 *布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 已添加 在*特性* 列表中添加了第一个项目 1
- 已更改 将*特性* 列表中的第四个项目更改成了“1.2V 固定输出” 1
- 已更改 更改了*特性* 列表中的第八个项目 1
- 已更改 更改了*特性* 列表中的最后一个项目 1
- 已更改 更改了最后一个*应用* 列表项 1
- Changed *Pin Configuration and Functions* section; updated table format and pin descriptions to meet new standards 4
- Changed C_{NR} value notation from 0.01 µF to 10 nF throughout *Electrical Characteristics* 7
- Changed feedback voltage parameter values and measured test conditions 7
- Changed output current limit maximum specified value 7
- Changed power-supply rejection ratio typical specified values for 100 Hz, 10 kHz, and 100 kHz frequency test conditions 7
- 已添加 note (1) to 图 1 8
- 已更改 y-axis title for 图 6 8
- 已更改 y-axis title for 图 7 8
- 已更改 footnote for 图 13 10
- 已更改 reference to noise-reduction capacitor (C_{NR}) to feed-forward capacitor (C_{FF}) in Transient Response 11
- 已更改 noise-reduction capacitor to feed-forward capacitor in 图 16 13
- 已更改 references to "noise-reduction capacitor" (C_{NR}) to "feed-forward capacitor" (C_{FF}) and section title from "Feedback Capacitor Requirements" to "Feed-forward Capacitor Requirements" in *Feed-Forward Capacitor Requirements* section 14
- 已更改 C_{NR} value notation from 0.01 µF to 10 nF in *Output Noise* section 14

Changes from Revision J (May, 2011) to Revision K **Page**

- 已添加 last sentence to first paragraph of *Startup and Noise Reduction Capacitor* section 11

Changes from Revision I (April, 2011) to Revision J **Page**

- Replaced the *Dissipation Ratings* with *Thermal Information* 6
- Revised conditions for *Typical Characteristics* to include statement about TPS73525 device availability 8
- 已添加 *Estimating Junction Temperature* section 18
- Updated *Power Dissipation* section 19

Changes from Revision H (November, 2009) to Revision I **Page**

- Corrected typo in *Electrical Characteristics* table for V_{OUT} specification, DRV package test conditions, $V_{OUT} \leq 2.2V$ 7

Changes from Revision G (March 2009) to Revision H **Page**

- 修订了*特性* 列表中的项目，以显示 280mV 的极低压降 1
- Changed dropout voltage typical specification from 250mV to 280mV 7

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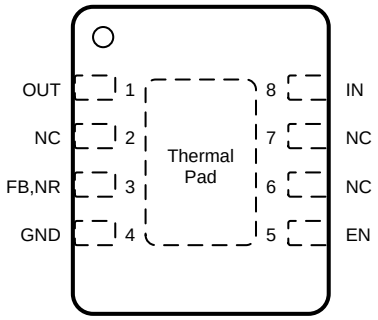
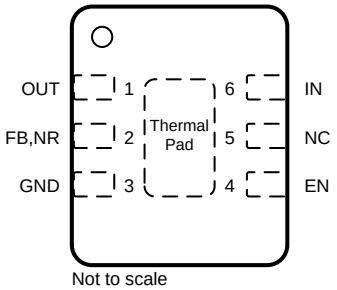
5 Pin Configuration and Functions

DRB Package
8-Pin SON With Exposed Thermal Pad
Top View



Not to scale

DRV Package
6-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

NC - No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO			
	DRV	DRB		
IN	6	8	I	Input supply. A 0.1-µF to 1-µF, low ESR capacitor must be placed from this pin to ground near the device.
GND	3	4	—	Ground. The pad must be tied to GND.
EN	4	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. The EN pin can be connected to the IN pin if not used.
NR	2	3	—	This pin is only available for the fixed voltage versions. Connecting an external capacitor to this pin bypasses noise that is generated by the internal band gap and allows the output noise to be reduced to very low levels. The maximum recommended capacitor is 0.01 µF.
FB	2	3	I	This pin is only available for the adjustable version. The FB pin is the input to the control-loop error amplifier, and is used to set the output voltage of the device. This pin must not be left floating.
OUT	1	1	O	This pin is the output of the regulator. A small, 2.2-µF ceramic capacitor is required from this pin to ground to assure stability. The minimum output capacitance required for stability is 2 µF.
NC	5	2, 6, 7	—	Not internally connected.
Thermal pad			—	

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6 Specifications

6.1 Absolute Maximum Ratings

at –40°C ≤ T_J and T_A ≤ +125°C (unless otherwise noted). All voltages are with respect to GND.[1]

		MIN	MAX	UNIT
V_{IN}	Voltage	–0.3	7	V
V_{EN}		–0.3	V_{IN} + 0.3	V
V_{FB}		–0.3	1.6	V
V_{OUT}		–0.3	V_{IN} + 0.3	V
I_{OUT}	Current	Internally limited		A
$P_{D(tot)}$	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed as *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		6.5	V
V_{OUT}	Output voltage	V_{FB}		6	V
I_{OUT}	Output current[1]	0		500	mA
T_A	Operating free-air temperature	–40		125	°C
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor		2		µF
C_{NR}	Noise reduction capacitor		10		nF
C_{FF}	Feed-forward capacitor [2]	3	22	1000	pF
R_2	Feedback resistor [2]		110		kΩ

(1) When operating at T_J near 125°C, $I_{OUT(min)}$ is 500 µA.
(2) Adjustable version only.

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6.4 Thermal Information

THERMAL METRIC[1]		TPS735 [2]		UNIT
		DRB (SON)	DRV (WSON)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance [3]	52.2	65.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance [4]	59.4	85.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	34.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter [5]	2	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter [6]	19.3	35.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance [7]	11.8	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 x 2 thermal via array.
ii. DRV: The exposed pad is connected to the PCB ground layer through a 2 x 2 thermal via array. Due to size limitation of thermal pad, 0.8-mm pitch array is used which is off the JEDEC standard.
(b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
ii DRV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-in × 3-in copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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6.5 Electrical Characteristics

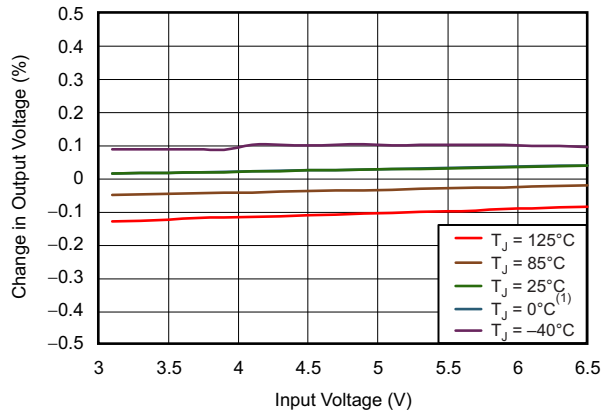
over operating temperature range (–40°C ≤ T_J ≤ 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 10 nF (unless otherwise noted). For the adjustable version (TPS73501), V_{OUT} = 3 V. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage(1)			2.7		6.5	V
V_{FB}	Internal reference (adjustable version only)	T_J = 25°C		1.196	1.208	1.220	V
V_{OUT}	Output voltage range (adjustable version only)			V_{FB}		6	V
	DC output accuracy(1)	1 mA ≤ I_{OUT} ≤ 500 mA, V_{OUT} + 0.5 V ≤ V_{IN} < 6.5 V	V_{OUT} > 2.2 V	–2%	±1%	2%	
			V_{OUT} ≤ 2.2 V	–3%	±1%	3%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	500 µA ≤ I_{OUT} ≤ 500 mA			0.005		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)	I_{OUT} = 500 mA			280	500	mV
I_{LIM}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + 0.9 V V_{IN} ≥ 2.7 V		800	1170	1900	mA
I_{GND}	Ground pin current	10 mA ≤ I_{OUT} ≤ 500 mA			45	65	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0 V			0.15	1	µA
I_{FB}	Feedback pin current (adjustable version only)	$V_{OUT(nom)}$ = 1.2 V		–0.5		0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.85 V V_{OUT} = 2.85 V C_{NR} = 0.01 µF I_{OUT} = 100 mA	f = 100 Hz		66		dB
			f = 1k Hz		68		
			f = 10 kHz		44		
			f = 100 kHz		22		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	C_{NR} = 10 nF		11 × V_{OUT}		μV_{RMS}
			C_{NR} = none		95 × V_{OUT}		
t_{STR}	Start-up time	C_{NR} = none			45		µs
		C_{NR} = 1 nF			45		
		C_{NR} = 10 nF			50		
		C_{NR} = 47 nF			50		
$V_{EN(HI)}$	Enable high (enabled)			1.2			V
$V_{EN(LO)}$	Enable low (shutdown)					0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1	µA
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		
UVLO	Undervoltage lockout	V_{IN} rising		1.9	2.2	2.65	V
V_{hys}	Hysteresis	V_{IN} falling			70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater.
(2) V_{DO} is not measured for this family of devices with $V_{OUT(nom)}$ < 2.8 V because the minimum V_{IN} = 2.7 V.

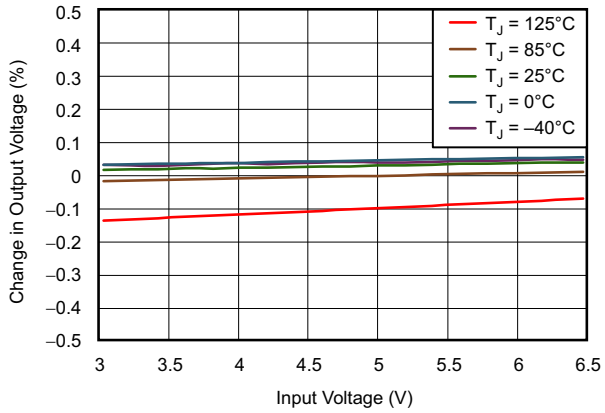
6.6 Typical Characteristics

over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN},C_{OUT} = 2.2 µF, C_{NR} = 10 nF. Typical values are at T_J = 25°C, (unless otherwise noted).



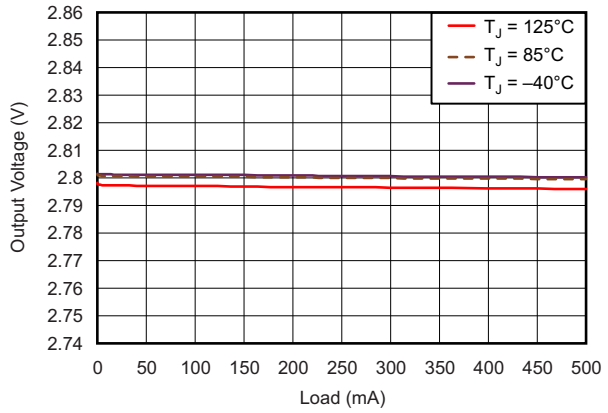
I_{OUT} = 100 mA

图 1. TPS735 Line Regulation



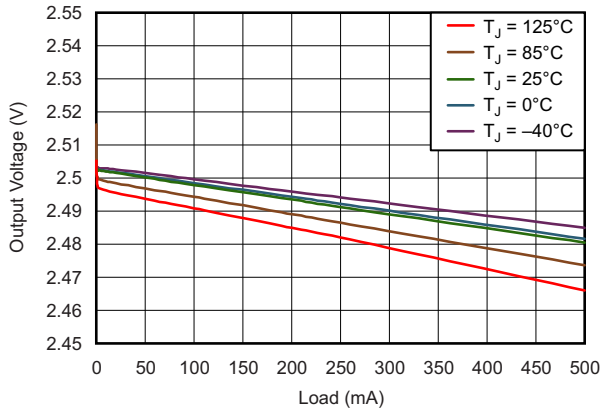
I_{OUT} = 100 mA

图 2. TPS735 Line Regulation



The y-axis range is ±2% of 2.8 V

图 3. TPS735 Load Regulation



The y-axis range is ±2% of 2.5 V

图 4. TPS735 Load Regulation

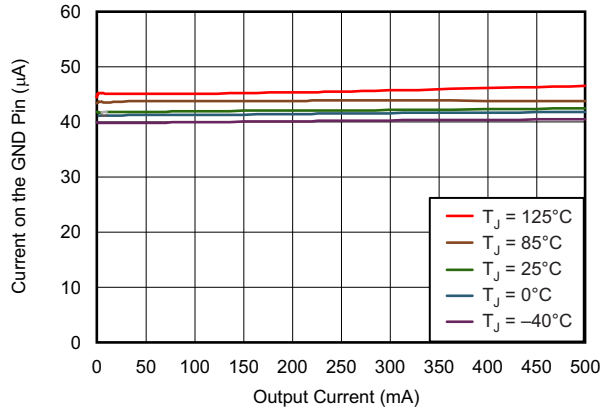


图 5. TPS735 Ground Pin Current vs Output Current

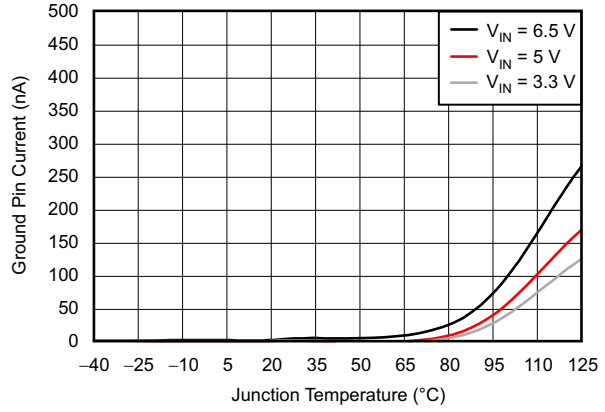


图 6. TPS735 Ground Pin Current (Disable) vs Temperature

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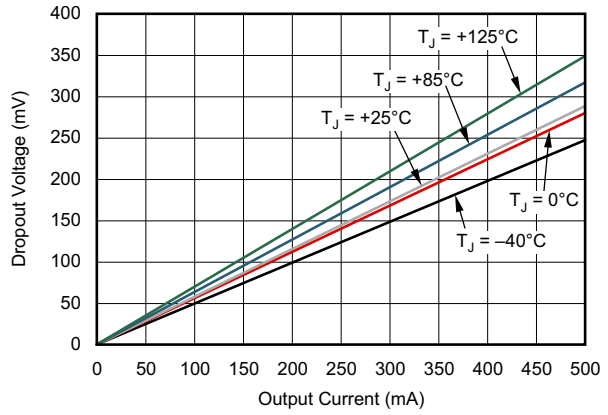
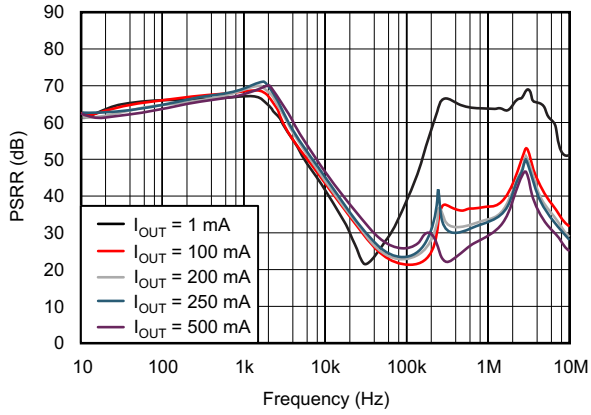
Typical Characteristics (接下页)

over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN},C_{OUT} = 2.2 µF, C_{NR} = 10 nF. Typical values are at T_J = 25°C, (unless otherwise noted).



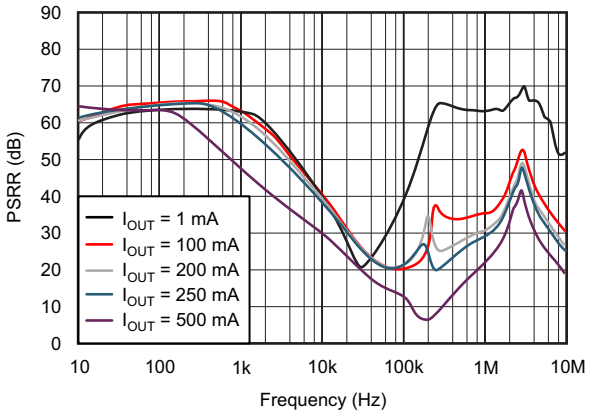
V_{EN} = 0.4 V

图 7. TPS735 Dropout Voltage vs Output Current



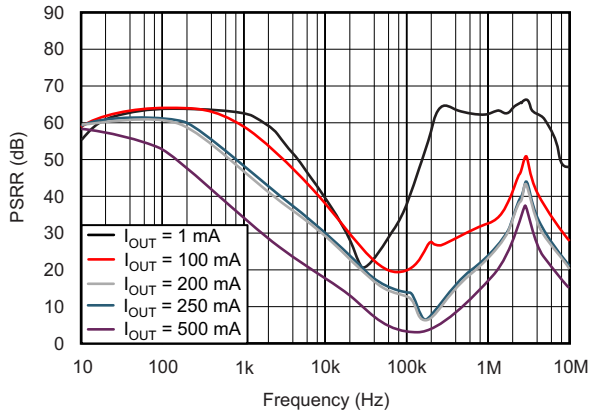
(V_{IN} – V_{OUT} = 1 V)

图 8. Power-Supply Ripple Rejection vs Frequency



(V_{IN} – V_{OUT} = 0.5 V)

图 9. Power-Supply Ripple Rejection vs Frequency



(V_{IN} – V_{OUT} = 0.3 V)

图 10. Power-Supply Ripple Rejection vs Frequency

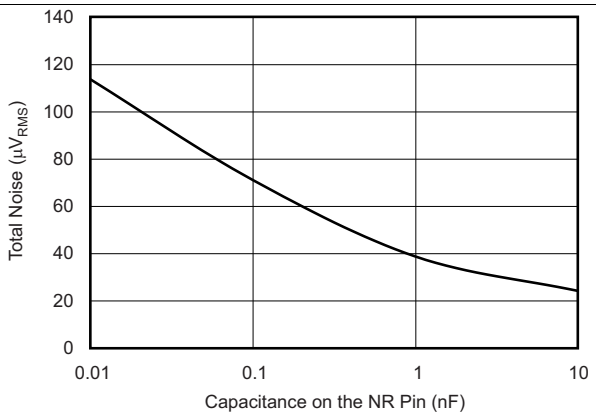
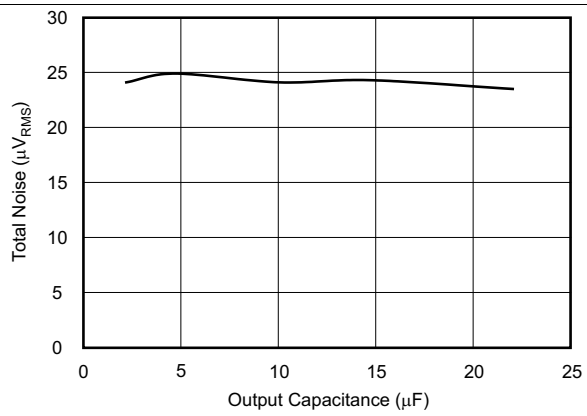


图 11. TPS73525 RMS Noise vs C_{NR}



C_{NR} = 0.01 µF, I_{OUT} = 1 mA

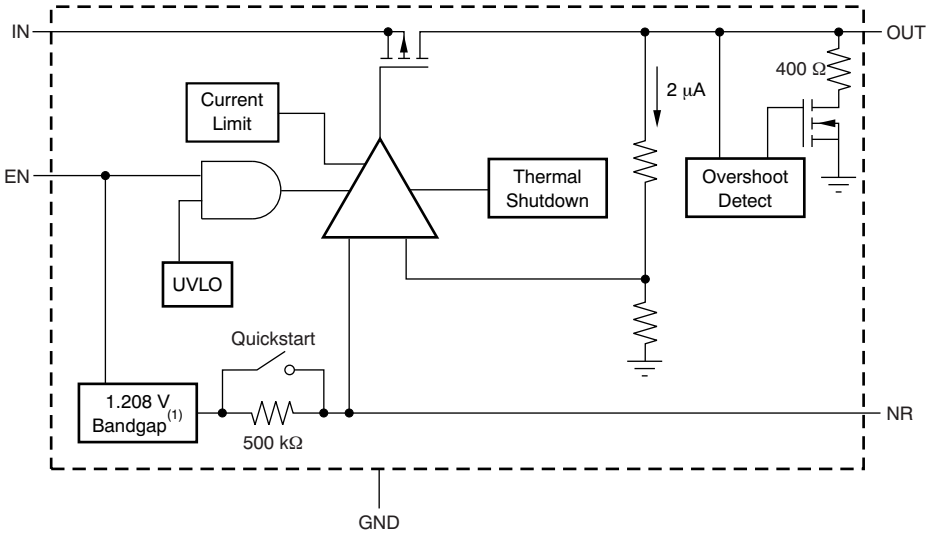
图 12. TPS735 RMS Noise vs C_{OUT}

7 Detailed Description

7.1 Overview

The TPS735 of low dropout (LDO) regulator combines the high performance required by radio frequency (RF) and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection and very low headroom ($V_{IN} – V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise that is generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at start-up. The combination of high performance and low ground current make the TPS735 device designed for portable applications. All versions have thermal and overcurrent protection and are specified from –40°C ≤ T_J ≤ +125°C.

7.2 Functional Block Diagrams



(1) The 1.2-V fixed voltage version has a 1-V band gap instead of a 1.208-V circuit.

图 13. Fixed Voltage Versions

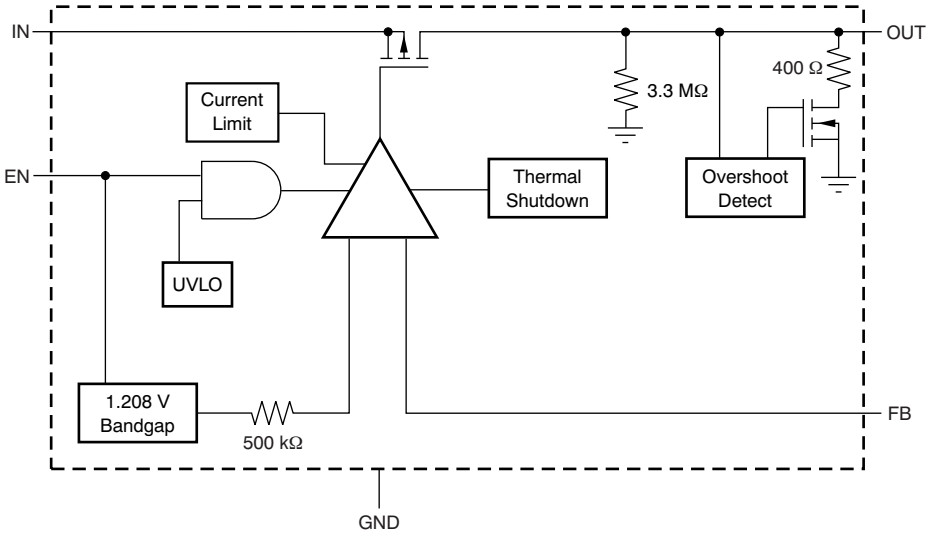


图 14. Adjustable Voltage Versions

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7.3 Feature Description

7.3.1 Internal Current Limit

The TPS735 internal current limit protects the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is independent of the output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

The PMOS pass element in the TPS735 device contains a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is expected, external limiting is appropriate.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can connect to the IN pin.

7.3.3 Dropout Voltage

The TPS735 device uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance ($R_{(IN/OUT)}$) of the PMOS pass element. V_{DO} scales with the output current because the PMOS device operates like a resistor in dropout.

As with any linear regulator, PSRR and transient response degrades as (V_{IN} – V_{OUT}) approaches dropout. *Typical Characteristics* shows this effect; (see 图 8 through 图 10).

7.3.4 Start-Up and Noise Reduction Capacitor

Fixed voltage versions of the TPS735 use a quick-start circuit to charge the noise reduction (NR) capacitor (C_{NR}) if present (see *Functional Block Diagrams*). This architecture allows the combination of low output noise and fast start-up times. The NR pin is high impedance so a low-leakage C_{NR} capacitor must be used. Most ceramic capacitors are appropriate in this configuration. A high-quality, COG-type (NPO) dielectric ceramic capacitor is recommended for C_{NR} when used in environments where abrupt changes in temperature can occur.

For the fastest start-up, first apply V_{IN} , then drive the enable (EN) pin high. If EN is tied to IN, start-up is slower. See *Typical Applications* . The quick-start switch closes for approximately 135 μs. To ensure that C_{NR} is charged during the quick-start time, use a capacitor with a value of no more than 0.01 μF.

7.3.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the transient response duration. In the adjustable version, adding C_{FF} between the OUT and FB pins improves stability and transient response performance. The transient response of the TPS735 device is enhanced by an active pulldown that engages when the output overshoots by approximately 5% or more when the device is enabled. The pull-down device operates like a 400-Ω resistor to ground when enabled.

7.3.6 Undervoltage Lockout

The TPS735 device uses an undervoltage lockout circuit to disable the output until the internal circuitry is operates properly. The UVLO circuit contains a deglitch feature so that the UVLO ignores undershoot transients on the input if the transients are less than 50 μs in duration.

7.3.7 Minimum Load

The TPS735 device is stable with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. If the output is below 500 μA and if the junction temperature is approximately 125°C, the output can increase enough to turn on the output pulldown. The output pulldown limits voltage drift to 5% (typically) but ground current can increase by approximately 50 μA. In most applications, the junction does not reach high temperatures at light loads because little power is dissipated. As a result, the specified ground current is valid at no load in most applications.

Feature Description (接下页)

7.3.8 Thermal Protection

Thermal protection disables the output when the junction temperature increases to approximately 165°C, which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit cycles on and off. This cycling limits the dissipation of the regulator and protects the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the thermal margin in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For reliable operation, trigger thermal protection at least 40°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS735 protects against overload conditions. This protection circuitry is not intended to replace proper heat sinking. Continuously running the TPS735 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage previously exceeded the UVLO voltage and did not decrease below the UVLO threshold minus V_{hys}.
- The input voltage is greater than the nominal output voltage that is added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is within the specified range.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is equal to the input voltage minus the dropout voltage. The transient performance of the device degrades because the pass device is in a triode state and the LDO operates like a resistor. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus V_{hys}, or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

表 1 lists the conditions that result in different modes of operation.

表 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUTnom} + V_{DO}$ and $V_{IN} >$ UVLO	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	UVLO $< V_{IN} < V_{OUTnom} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	—	$T_J < 165°C$
Disabled mode (any true condition disables the device)	$V_{IN} <$ UVLO $- V_{hys}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > 165°C$

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS735 LDO regulator provides a design with an ultra-low noise, high PSRR, low-dropout linear regulation with a very small ground current (5 µA, typical).

The devices are stable with ceramic capacitors and have a dropout voltage of 280 mV at the full output rating of 500 mA. The features of the TPS735 device enables the LDO regulators to be used in a wide variety of applications with minimal design complexity.

8.2 Typical Applications

图 15 shows the basic circuit connections for fixed-voltage models. 图 16 shows the connections for the adjustable output version. R_1 and R_2 can be calculated for any output voltage using the formula in 图 16.

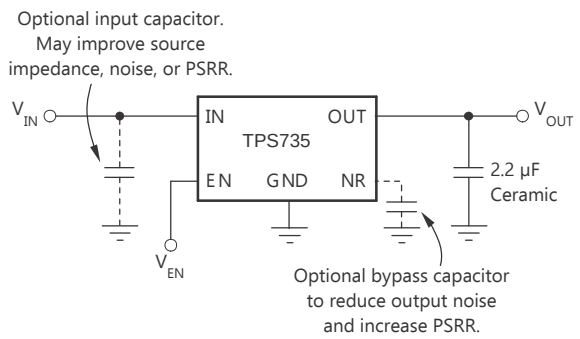

图 15. Typical Application Circuit for Fixed-Voltage Versions

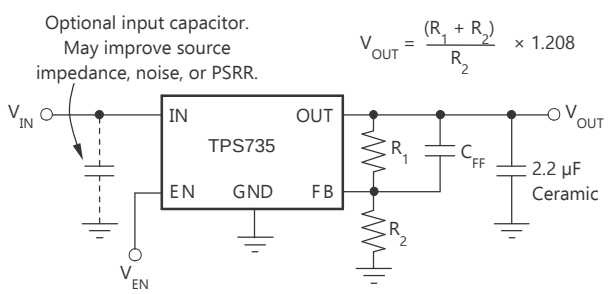

图 16. Typical Application Circuit for Adjustable-Voltage Versions

Typical Applications (接下页)

8.2.1 Design Requirements

8.2.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a 0.1-μF to 1-μF low-equivalent series-resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher-value capacitor may be required if large, fast, rise-time load transients are expected, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be required to ensure stability.

TheTPS735 device is designed to be stable with standard ceramic output capacitors of values 2 μF or larger. X5R- and X7R-type capacitors are best because these capacitors feature minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor is < 1 Ω and, therefore, the output capacitor type must be ceramic or conductive polymer electrolytic.

8.2.1.2 Feed-Forward Capacitor Requirements

The feed-forward capacitor (C_{FF}), shown in 图 16, is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value between 3 pF to 1 nF can be used. Fixed-voltage versions have an internal 30-pF feed-forward capacitor that is quick-charged at start-up. Larger value capacitors improve noise slightly. The TPS735 device is stable in unity-gain configurations (the OUT pin is tied to the FB pin) without C_{FF}.

8.2.2 Detailed Design Procedure

8.2.2.1 Output Noise

In most LDO regulators, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS735 device, the band gap does not contribute significantly to noise. Noise is dominated by the output resistor divider and the error-amplifier input. To minimize noise in a given application, use a 10-nF noise reduction capacitor. For the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that produces 2 μA of divider current has the same noise performance as a fixed voltage version with a C_{NR}. To further optimize noise, set the ESR of the output capacitor to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, which reduces the total output noise up to 10%. TI recommends a maximum capacitor value of 10 nF.

公式 1 calculates the approximate integrated output noise from 10 Hz to 100 kHz with a C_{NR} value of 10 nF.

$$V_n\ (\mu V_{RMS}) = 11\,(\mu V_{RMS} / V) \times V_{OUT}\ (V) \tag{1}$$

The TPS735adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise is minimized according to the previously listed recommendations.

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Typical Applications (接下页)

8.2.3 Application Curves

at $V_{IN} = V_{OUT(nom)} + 0.5$ V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, C_{OUT} = 2.2 µF, C_{NR} = 10 nF, and T_J = 25°C (unless otherwise noted)

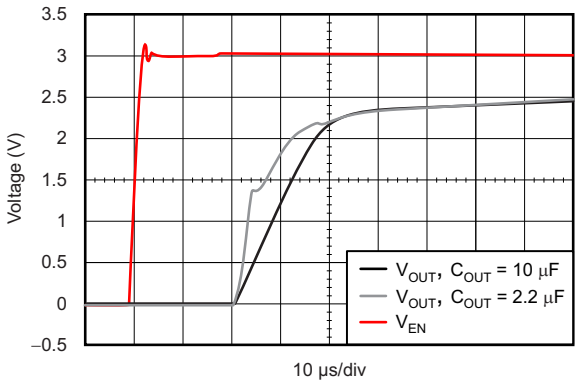


图 17. TPS735 Turnon Response ($V_{IN} = V_{EN}$)

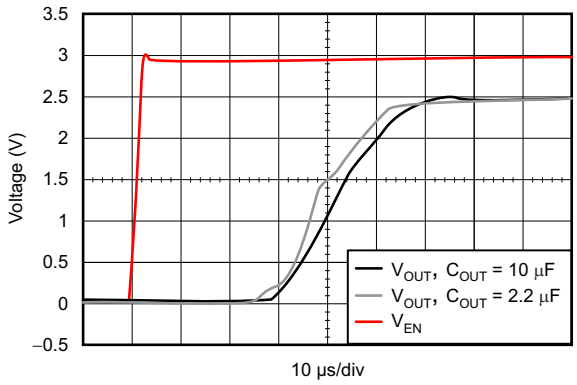


图 18. TPS735 Turnon Response Using EN

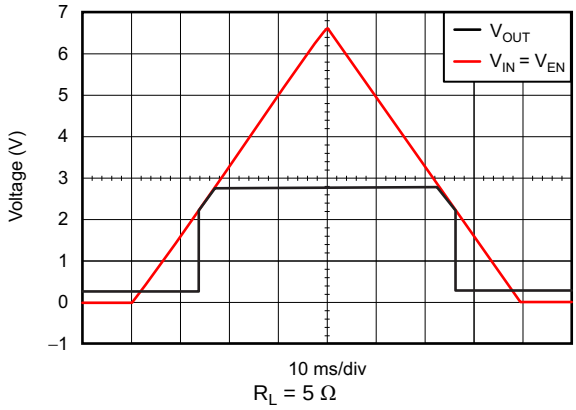


图 19. TPS73525 Power-Up and Power-Down ($V_{IN} = V_{EN}$)

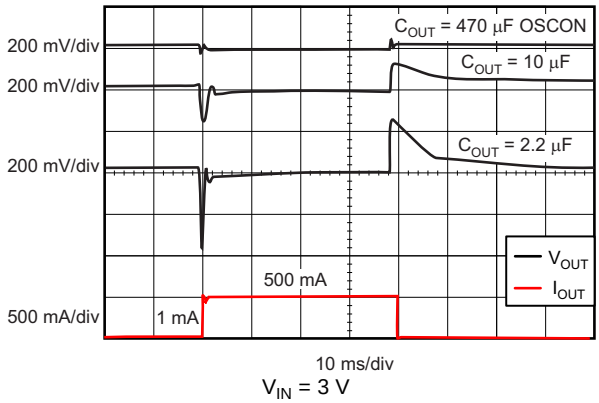


图 20. TPS735 Load Transient Response

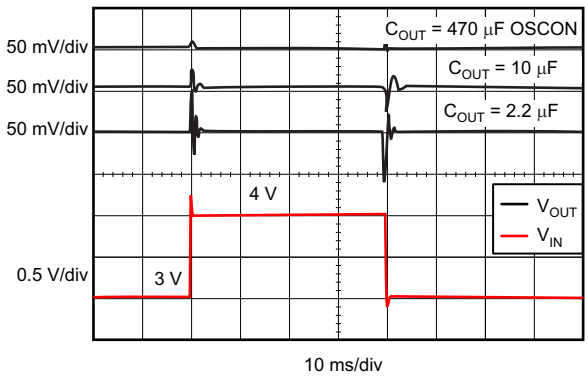


图 21. TPS735 Line Transient Response

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

10 Layout

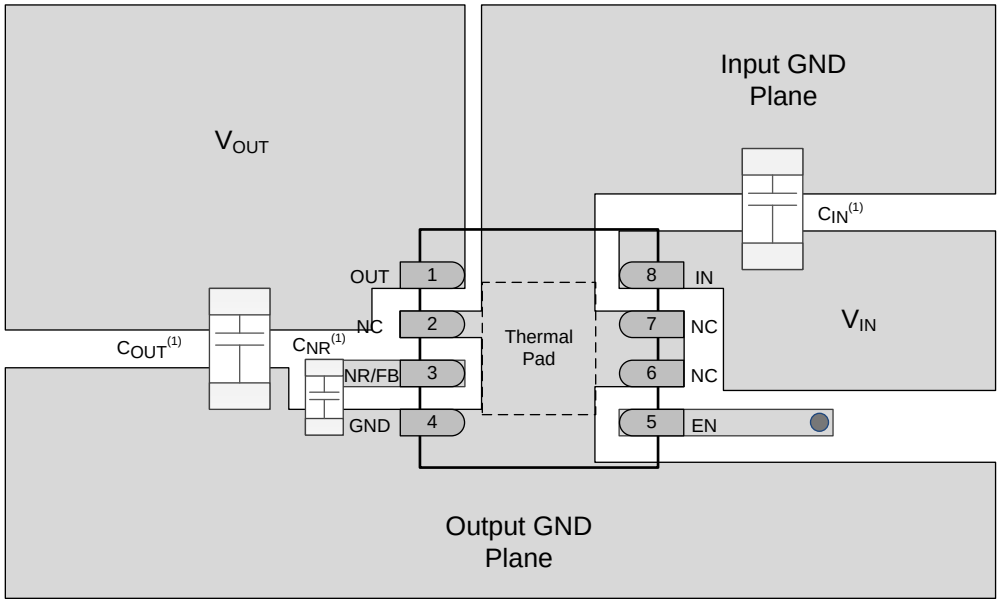
10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near to the respective LDO pin connections as possible. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and as a result, reduces load-current transients, minimizes noise, and increases circuit stability. TI recommends using a ground reference plane, and is embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane ensures accuracy of the output voltage, shields the LDO from noise, and operates similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is required to meet thermal requirements.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

10.2 Layout Example



(1) C_{IN} and C_{OUT} are 0603 capacitors and C_{NR} is a 0402 capacitor. The footprint is shown to scale with package size.

图 22. TPS735 Fixed Version Layout Reference Diagram

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10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, which presents different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* section. Heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation can be approximated by the product of the output current and the voltage drop across the output pass element, as 公式 2 shows.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{2}$$

注

When the device is used in a condition of high input and low output voltages, P_D can exceed the junction temperature rating even when the ambient temperature is at room temperature.

公式 3 is an example calculation for the power dissipation (P_D) of the DRB package.

$$P_D = (6.5\ V - 1.2\ V) \times 500\ mA = 2.65\ W \tag{3}$$

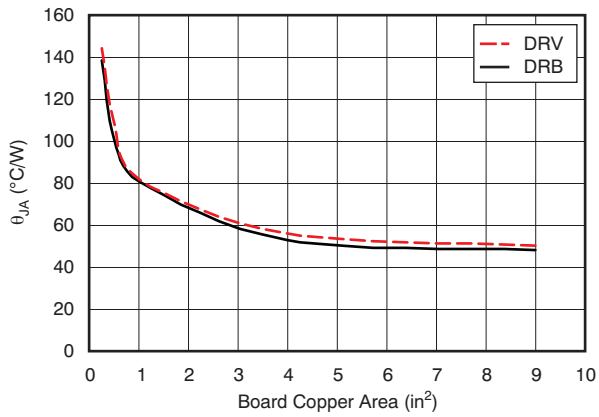
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output performance.

On the DRB package, the primary conduction path for heat is through the exposed thermal pad to the PCB. The pad can be connected to ground or left floating. The pad must be attached to an appropriate amount of copper PCB area to ensure that the device does not overheat. The maximum allowable junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. 公式 4 calculates the maximum junction-to-ambient thermal resistance.

$$R_{\theta JA} = \frac{(125°C - T_A)}{P_D} \tag{4}$$

Power Dissipation (接下页)

图 23 estimates the maximum $R_{\theta JA}$ and the minimum amount of PCB copper area required to heat sink.



Note: θ_{JA} value at board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

图 23. θ_{JA} vs Board Size

图 23 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and must not be used to estimate actual thermal performance in real application environments.

注

When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

10.4 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as the table shows, the junction temperature can be estimated with corresponding formulas (公式 5), which are more accurate than the value of T_J through calculation with θ_{JA}.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \bullet P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \bullet P_D$

where:

- P_D is the power dissipation calculated with 公式 2,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB temperature measured 1 mm away from the device package on the PCB surface (as shown in 图 25). (5)

注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see *Using New Thermal Metrics*, available for download at www.ti.com.

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Estimating Junction Temperature (接下页)

According to 图 24, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) do not depend on the copper area. Using Ψ_{JT} or Ψ_{JB} with 公式 5 can estimate T_J by measuring T_T or T_B on an application board.

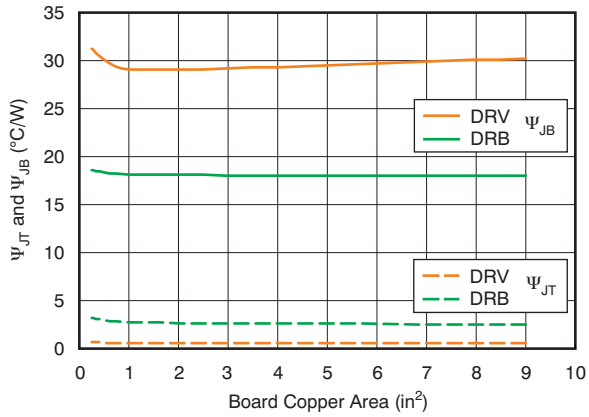
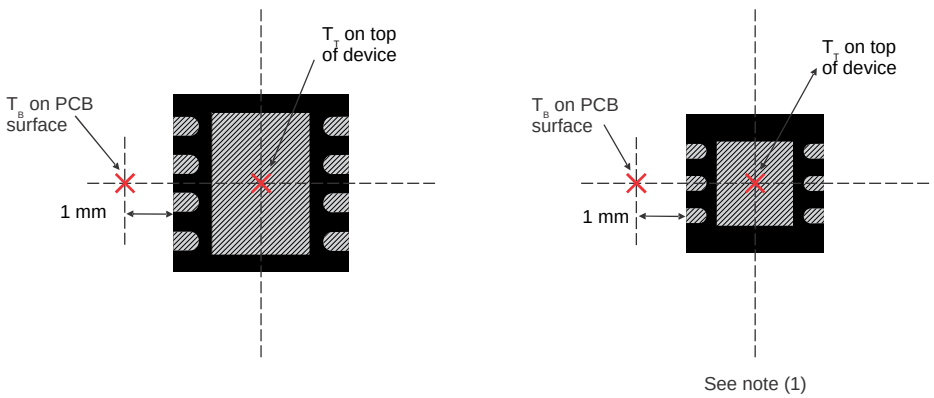


图 24. Ψ_{JT} and Ψ_{JB} vs Board Size



(a) Example DRB (SON) Package Measurement

(b) Example DRV (WSON) Package Measurement

(1) Power dissipation may limit operating range. See *Thermal Information* .

图 25. Measuring Points for T_T and T_B

10.5 Package Mounting

Solder pad footprint recommendations for the TPS735 device is available from the TI website at www.ti.com.

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

有两个评估模块 (EVM) 可与 TPS735 配套使用，帮助评估初始电路性能。TPS73501EVM-276 评估模块和 TPS73525EVM-276 评估模块（以及相关的用户指南）可在 TI 网站上的产品文件夹中获取，也可直接从 TI eStore 购买。

11.1.2 器件命名规则

表 **2.** 器件命名规则 (1)

产品	V_{OUT}
TPS735**xx(x)*yyyz***	**xx(x)** 是标称输出电压。对于分辨率为 100mV 的输出电压，订购编号中使用两位数字；否则，使用三位数字（例如，33 = 3.3V；125 = 1.25V）。 **yyy** 是封装符号。 **z** 是卷带数量（R = 3000，T = 250）。 **01** 是可调节版本。

(1) 要获得最新的封装和订购信息，请参阅本文档末尾的封装选项附录，或者访问 TI 网站 www.ti.com.cn。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《TPS735EVM-276 用户指南》*

11.3 商标

All trademarks are the property of their respective owners.

11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73501DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK	Samples
TPS73501DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK	Samples
TPS73501DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SDR	Samples
TPS73501DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SDR	Samples
TPS73512DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT	Samples
TPS73512DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT	Samples
TPS73515DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH	Samples
TPS73515DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH	Samples
TPS73525DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM	Samples
TPS73525DRBRG4	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM	Samples
TPS73525DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM	Samples
TPS73525DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NSW	Samples
TPS73525DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NSW	Samples
TPS73527DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAK	Samples
TPS73527DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAK	Samples
TPS735285DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAW	Samples
TPS735285DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAW	Samples
TPS73533DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY	Samples
TPS73533DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY	Samples
TPS73533DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVY	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73533DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVY	Samples
TPS73534DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTU	Samples
TPS73534DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

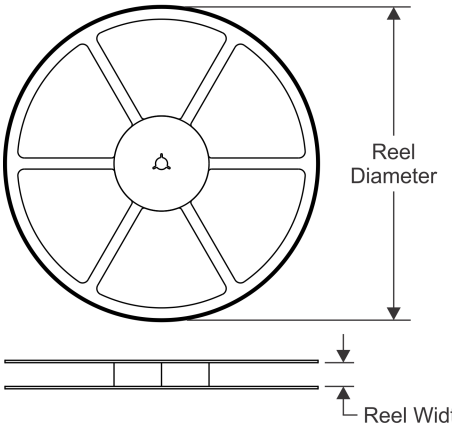
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

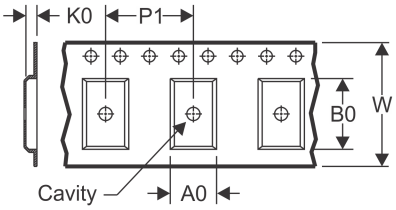
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

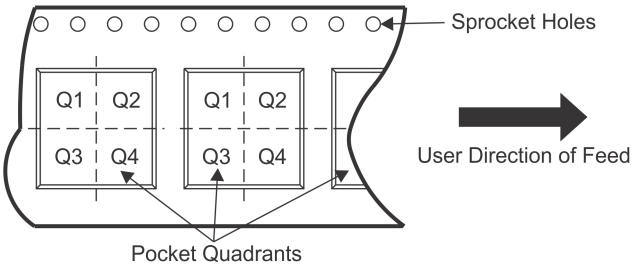


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

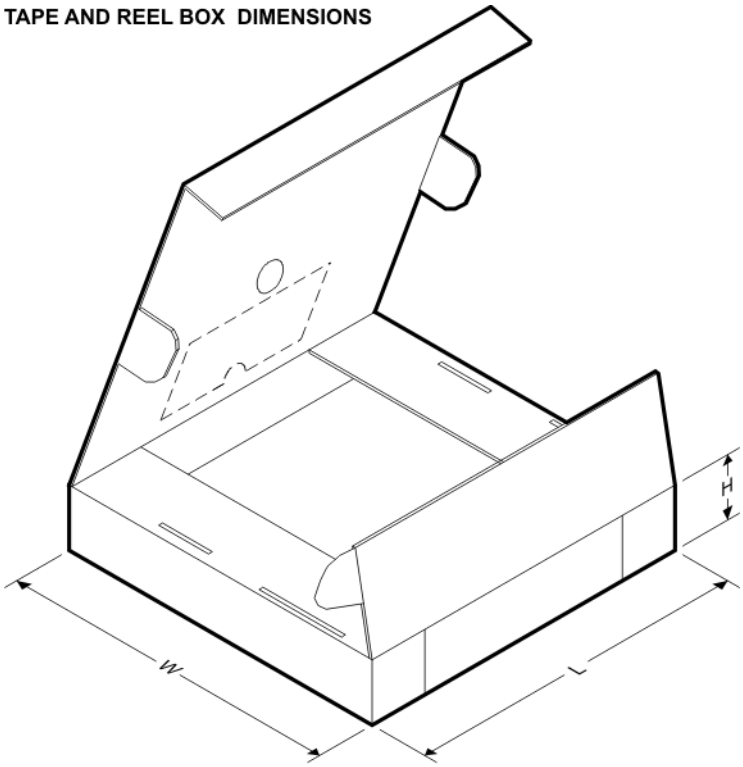


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73501DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73501DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73501DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73501DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73501DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73512DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73512DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73515DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73515DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73525DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73527DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73527DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73527DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS735285DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS735285DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73533DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73533DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73533DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73533DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73533DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73533DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73533DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73534DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73534DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



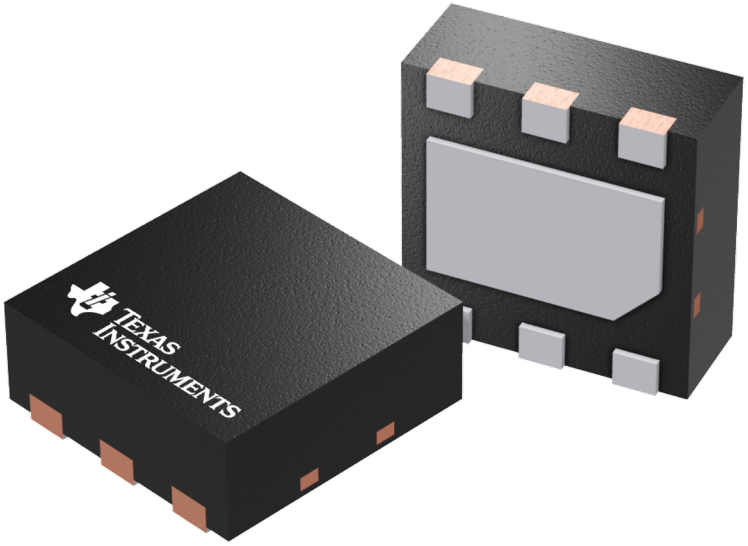
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73501DRBR	SON	DRB	8	3000	338.0	355.0	50.0
TPS73501DRBT	SON	DRB	8	250	338.0	355.0	50.0
TPS73501DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS73501DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS73501DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS73512DRBR	SON	DRB	8	3000	853.0	449.0	35.0
TPS73512DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73515DRBR	SON	DRB	8	3000	338.0	355.0	50.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73515DRBT	SON	DRB	8	250	338.0	355.0	50.0
TPS73525DRBR	SON	DRB	8	3000	338.0	355.0	50.0
TPS73525DRBT	SON	DRB	8	250	338.0	355.0	50.0
TPS73525DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS73525DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS73527DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS73527DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS73527DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS735285DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS735285DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS73533DRBR	SON	DRB	8	3000	338.0	355.0	50.0
TPS73533DRBR	SON	DRB	8	3000	853.0	449.0	35.0
TPS73533DRBT	SON	DRB	8	250	338.0	355.0	50.0
TPS73533DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS73533DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS73533DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS73533DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS73534DRBR	SON	DRB	8	3000	853.0	449.0	35.0
TPS73534DRBT	SON	DRB	8	250	210.0	185.0	35.0

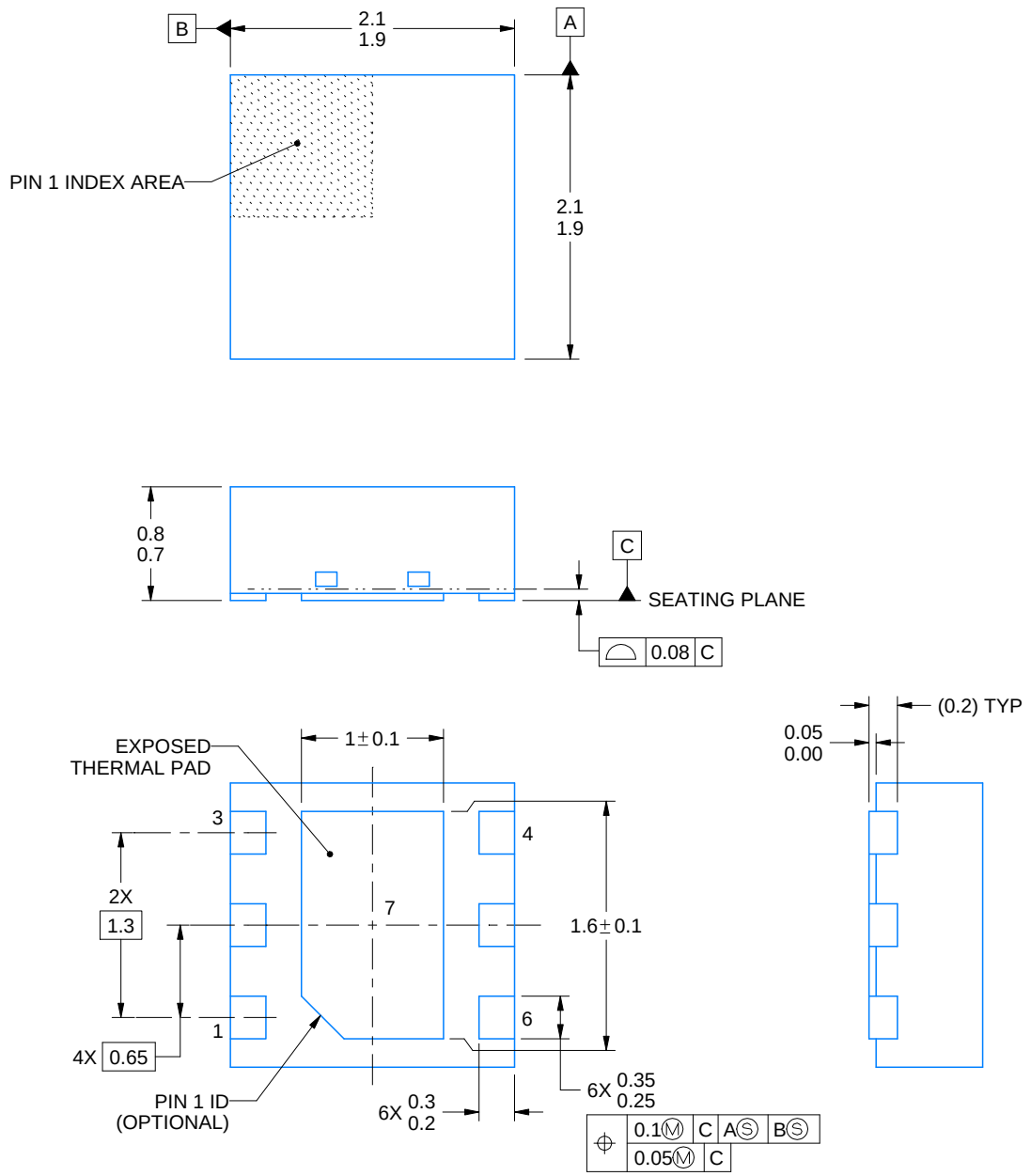
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



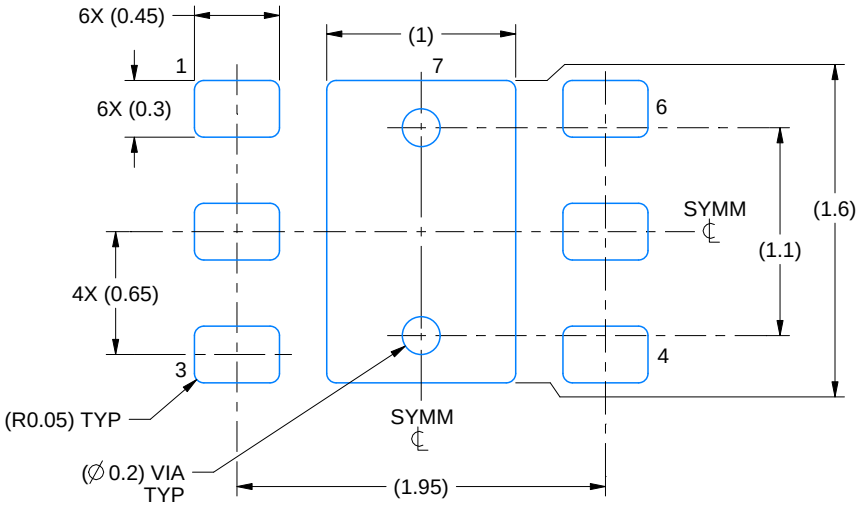
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS INSTRUMENTS

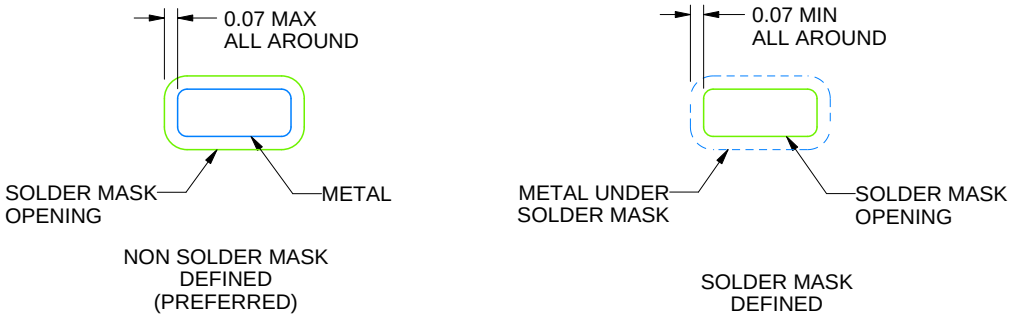


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

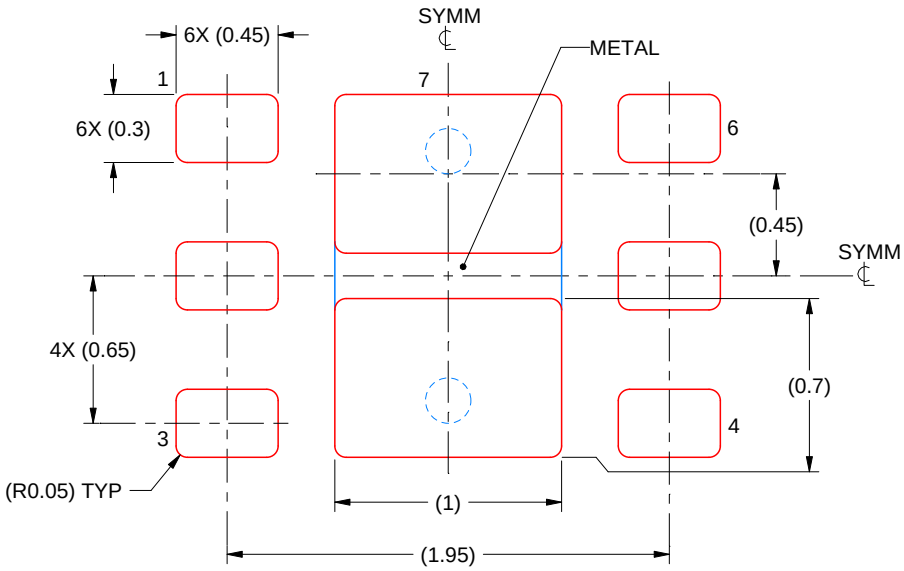


SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



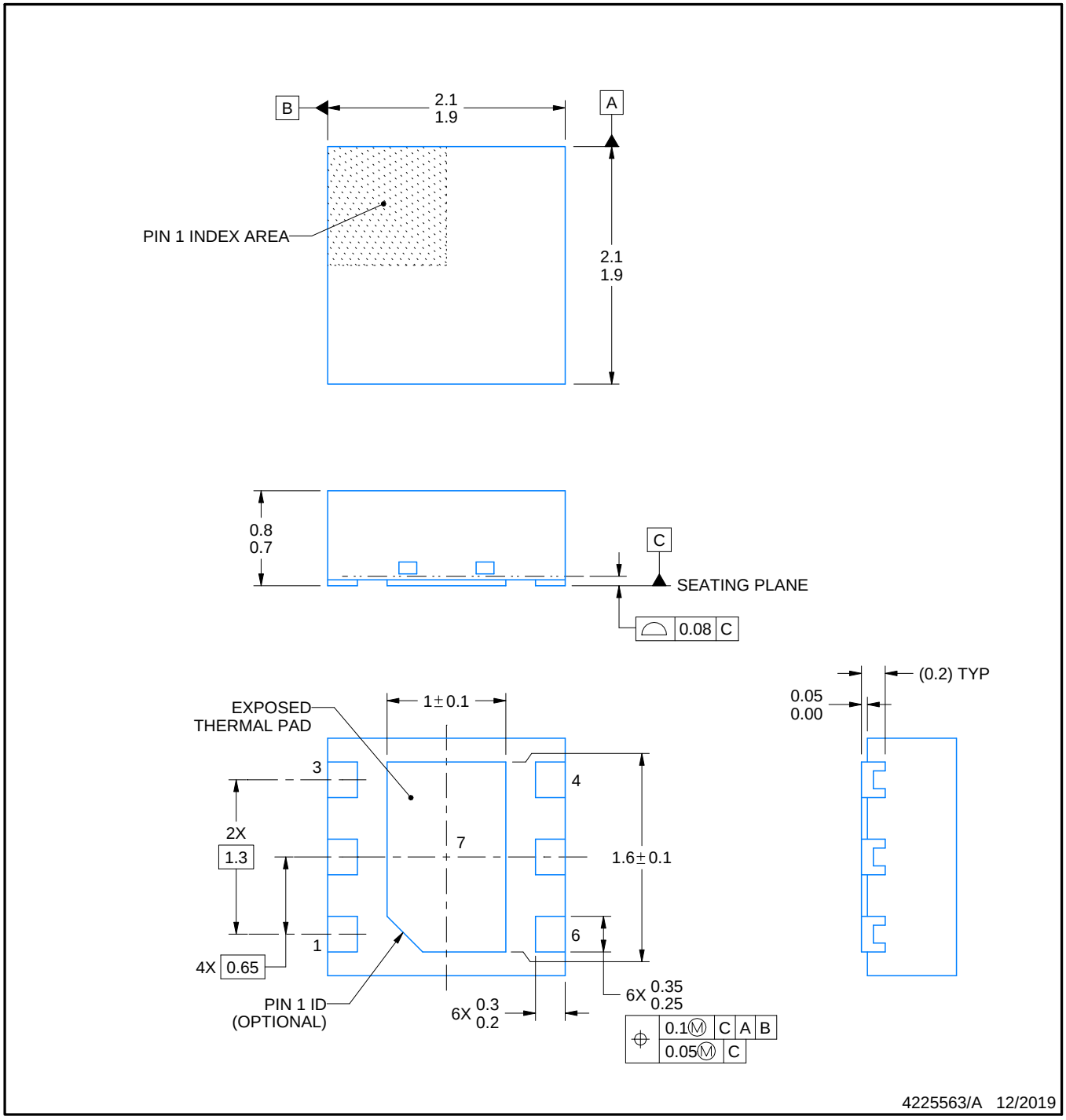
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

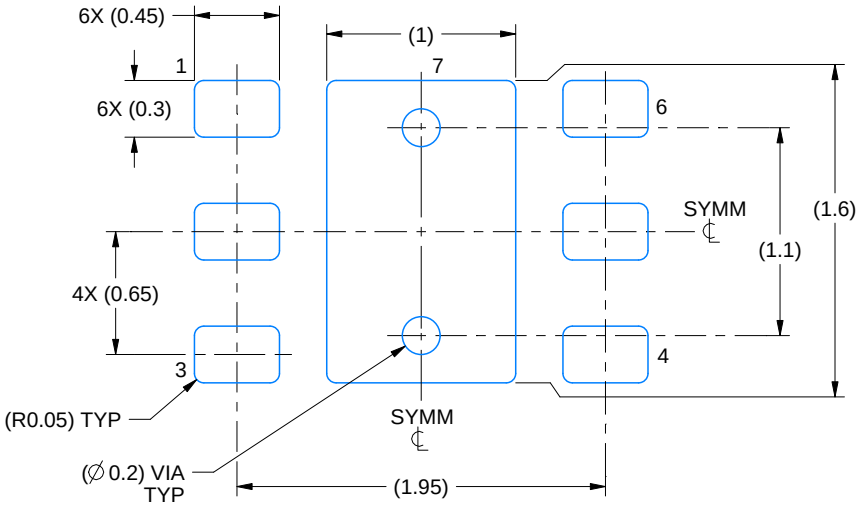
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

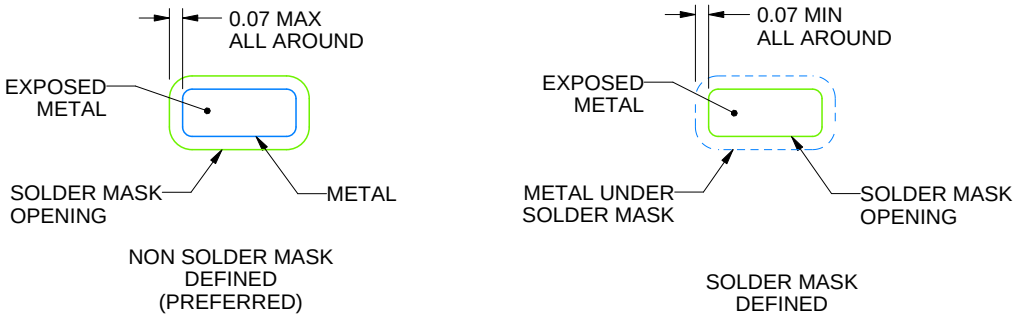


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

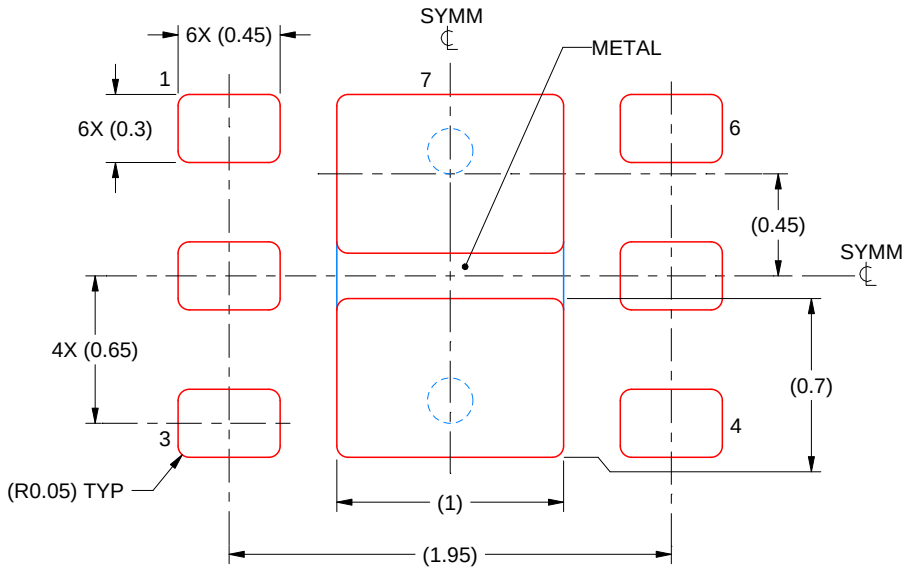


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

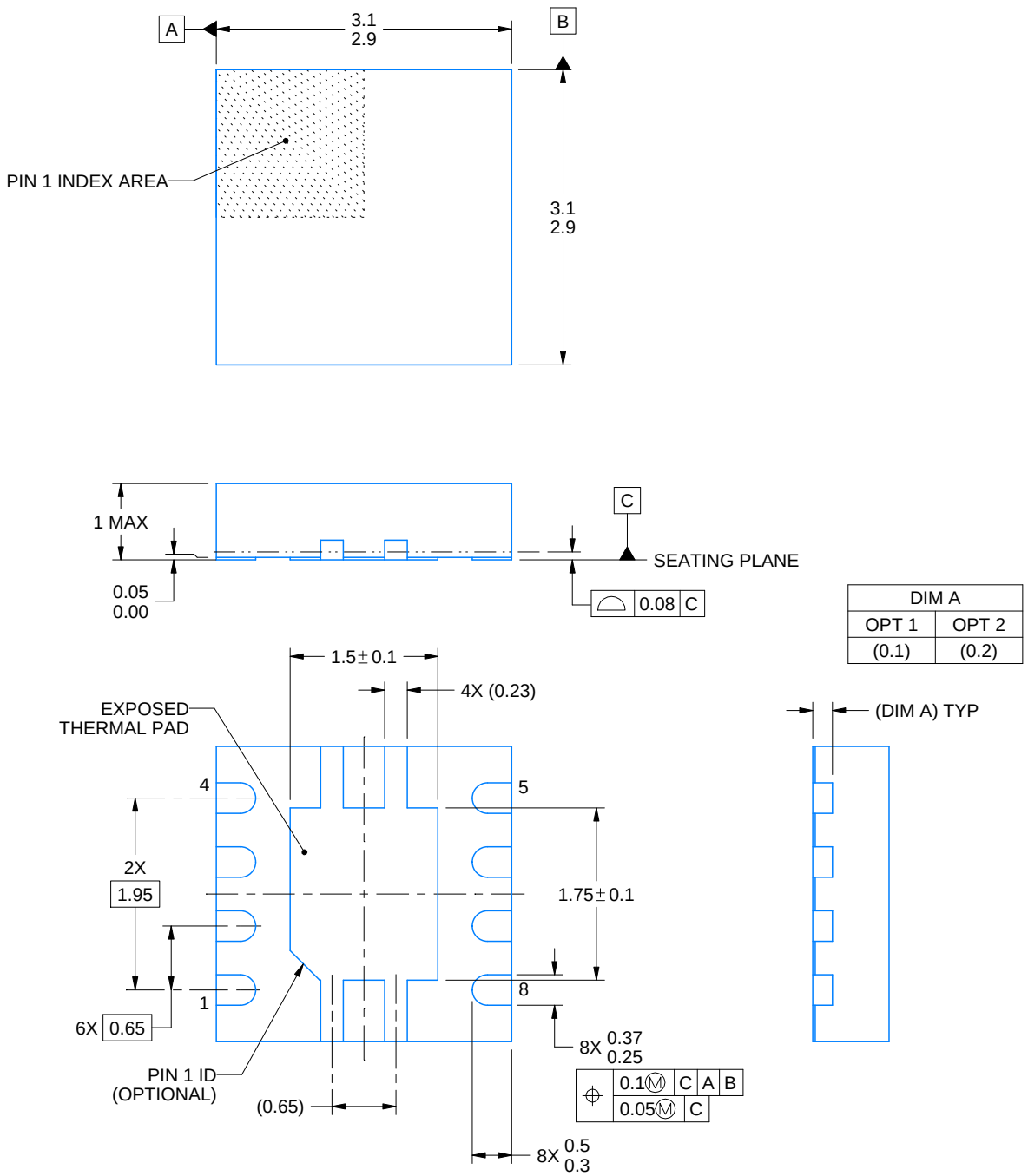
GENERIC PACKAGE VIEW

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

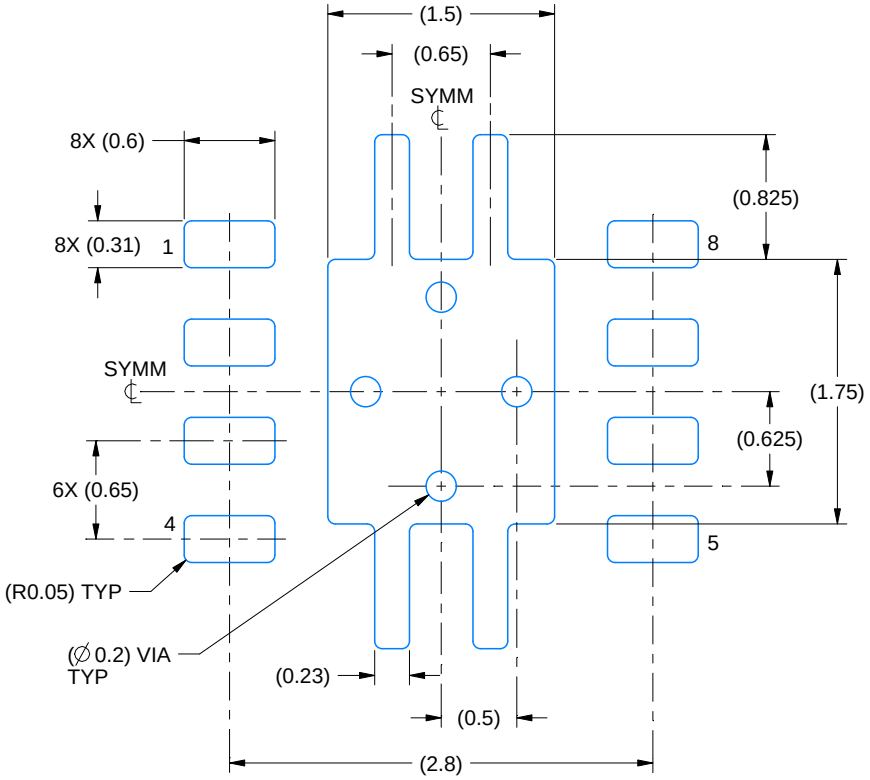
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

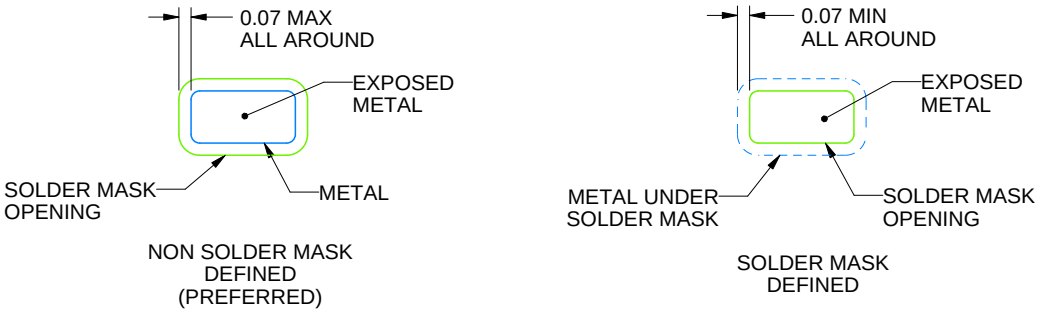


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

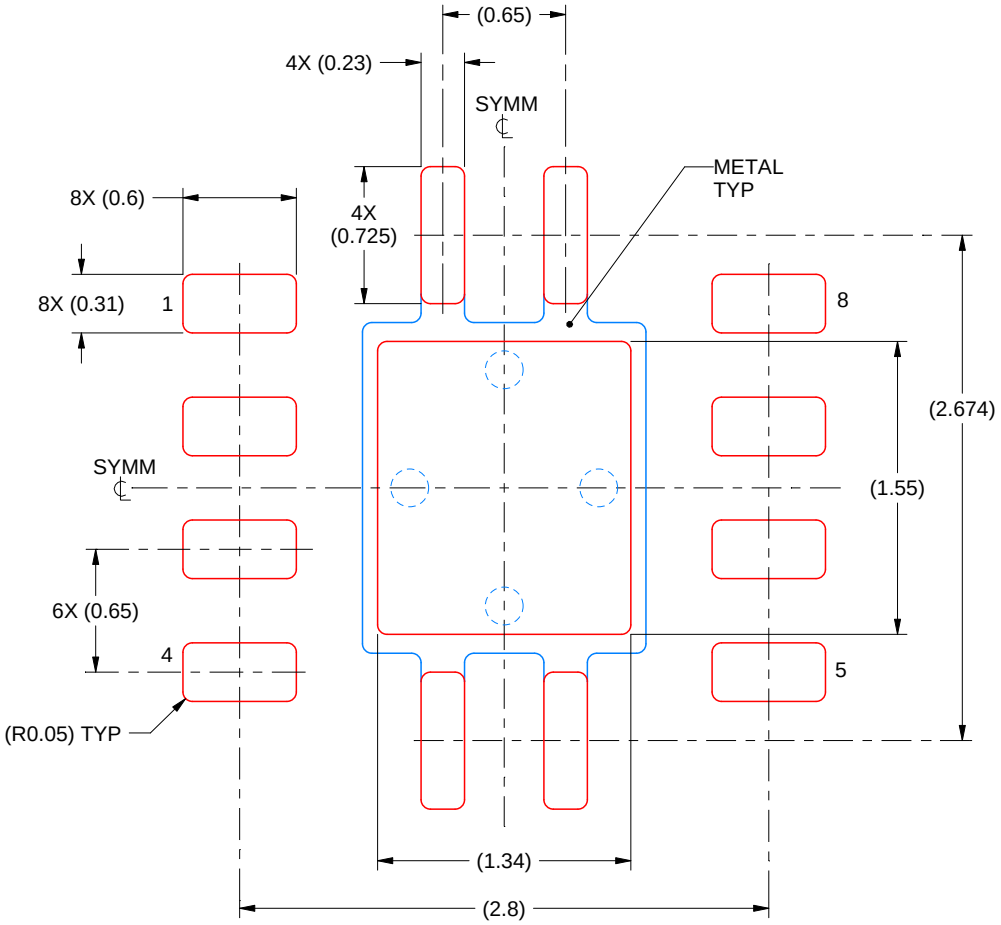


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
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