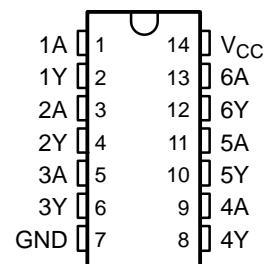


FEATURES

- Operates From 2.3 V to 3.6 V
- Max t_{pd} of 3.4 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

D, DGV, NS, OR PW PACKAGE
 (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This hex Schmitt-trigger inverter is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVC14 contains six independent inverters and performs the Boolean function $Y = \bar{A}$.

ORDERING INFORMATION

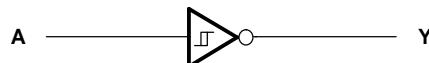
T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC - D	Tube	SN74ALVC14D	ALVC14
		Tape and reel	SN74ALVC14DR	
	SOP - NS	Tape and reel	SN74ALVC14NSR	ALVC14
	TSSOP - PW	Tape and reel	SN74ALVC14PWR	VA14
	TVSOP - DGV	Tape and reel	SN74ALVC14DGVR	VA14

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current $V_I < 0$		-50	mA
I_{OK}	Output clamp current $V_O < 0$		-50	mA
I_o	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	D package	86	°C/W
		DGV package	127	
		NS package	76	
		PW package	113	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V	-12	mA
		$V_{CC} = 2.7$ V	-12	
		$V_{CC} = 3$ V	-24	
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V	12	mA
		$V_{CC} = 2.7$ V	12	
		$V_{CC} = 3$ V	24	
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{T+} Positive-going threshold		2.3 V	0.7	1.7		V
		2.7 V	0.8	2		
		3 V	0.8	2		
		3.6 V	0.8	2		
V _{T-} Negative-going threshold		2.3 V	0.35	1.3		V
		2.7 V	0.4	1.4		
		3 V	0.6	1.5		
		3.6 V	0.8	1.8		
ΔV _T Hysteresis (V _{T+} - V _{T-})		2.3 V	0.3	1		V
		2.7 V	0.3	1.1		
		3 V	0.3	1.2		
		3.6 V	0.3	1.2		
V _{OH}	I _{OH} = 100 μA	2.3 V to 3.6 V	V _{CC} - 0.2			V
	I _{OH} = -6 mA	2.3 V	2			
	I _{OH} = -12 mA	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
V _{OL}	I _{OL} = 100 μA	2.3 V to 3.6 V		0.2		V
	I _{OL} = 6 mA	2.3 V		0.4		
	I _{OL} = 12 mA	2.3 V		0.7		
		2.7 V		0.4		
I _I	I _{OL} = 24 mA	3 V		0.55		V
	I _I = V _{CC} or GND	3.6 V		±5	μA	
	I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V		10	μA
	ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750	μA
C _i	V _I = V _{CC} or GND	3.3 V		4	pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

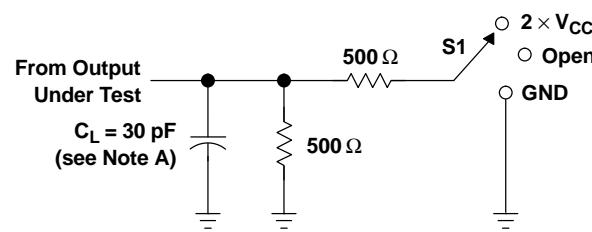
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	3.7	3.9	1	3.4	ns	

OPERATING CHARACTERISTICS

T_A = 25°C

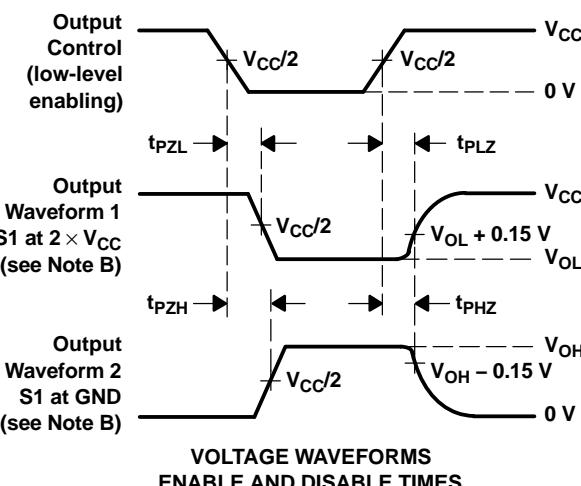
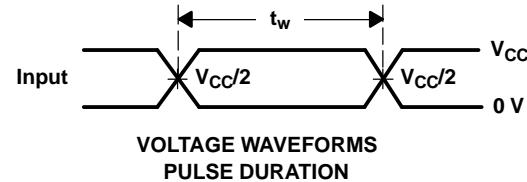
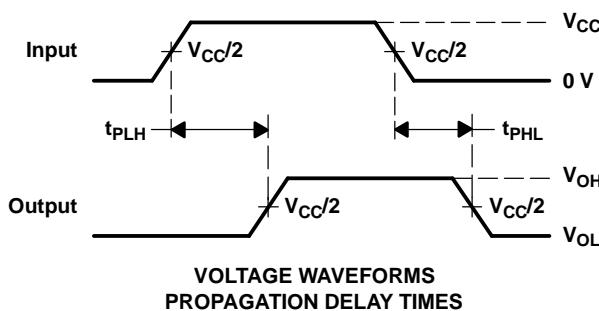
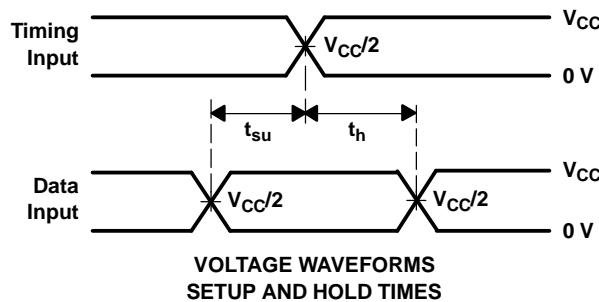
PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V		V _{CC} = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
C _{pd}	Power dissipation capacitance per inverter	C _L = 0, f = 10 MHz		27	31	pF

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

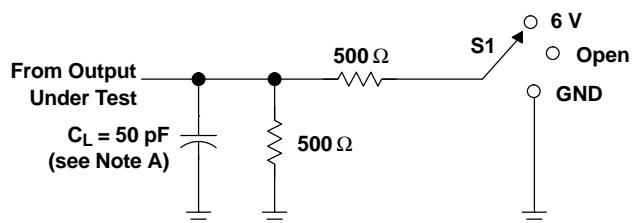


NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

Timing Input 2.7 V

0 V

Data Input 2.7 V

0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Input 2.7 V

0 V

t_{PLH}

t_{PHL}

Output V_{OH}

V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

Input 2.7 V

0 V

t_w

VOLTAGE WAVEFORMS
PULSE DURATION

Output Control (low-level enabling) 2.7 V

0 V

t_{PZL}

t_{PLZ}

Output Waveform 1 S1 at 6 V (see Note B) 3 V

0 V

t_{PZH}

t_{PHZ}

Output Waveform 2 S1 at GND (see Note B) 0 V

$V_{OH} + 0.3 \text{ V}$

V_{OL}

$V_{OH} - 0.3 \text{ V}$

V_{OL}

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVC14D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC14	Samples
SN74ALVC14DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC14	Samples
SN74ALVC14DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VA14	Samples
SN74ALVC14DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC14	Samples
SN74ALVC14DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC14	Samples
SN74ALVC14NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC14	Samples
SN74ALVC14PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VA14	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



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PACKAGE OPTION ADDENDUM

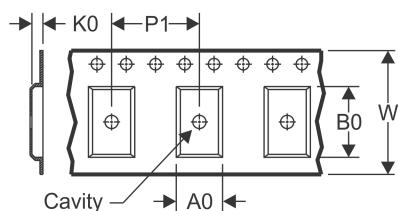
10-Dec-2020

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

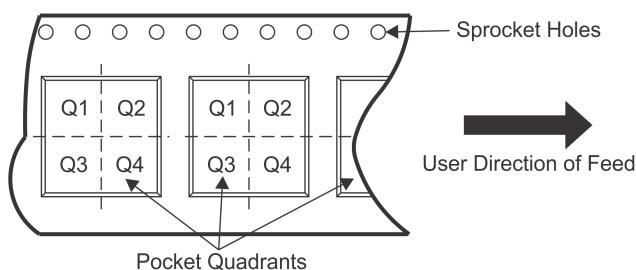
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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


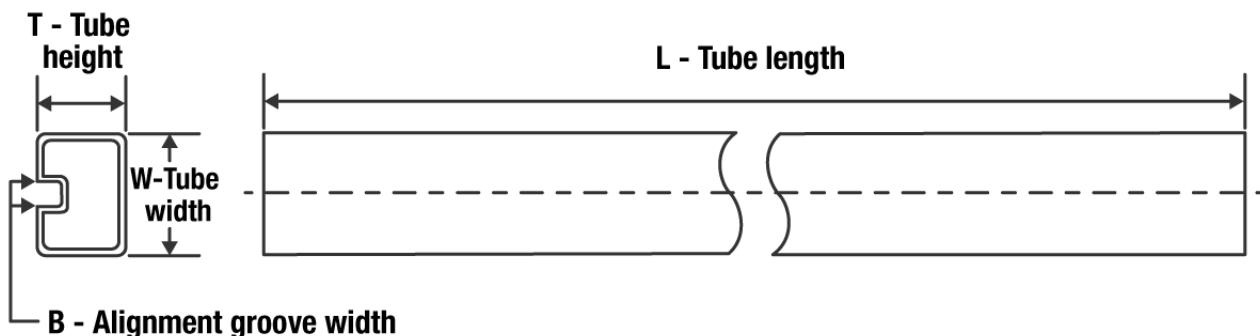
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVC14DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74ALVC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALVC14NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ALVC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVC14DGVR	TVSOP	DGV	14	2000	853.0	449.0	35.0
SN74ALVC14DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74ALVC14NSR	SO	NS	14	2000	853.0	449.0	35.0
SN74ALVC14PWR	TSSOP	PW	14	2000	853.0	449.0	35.0

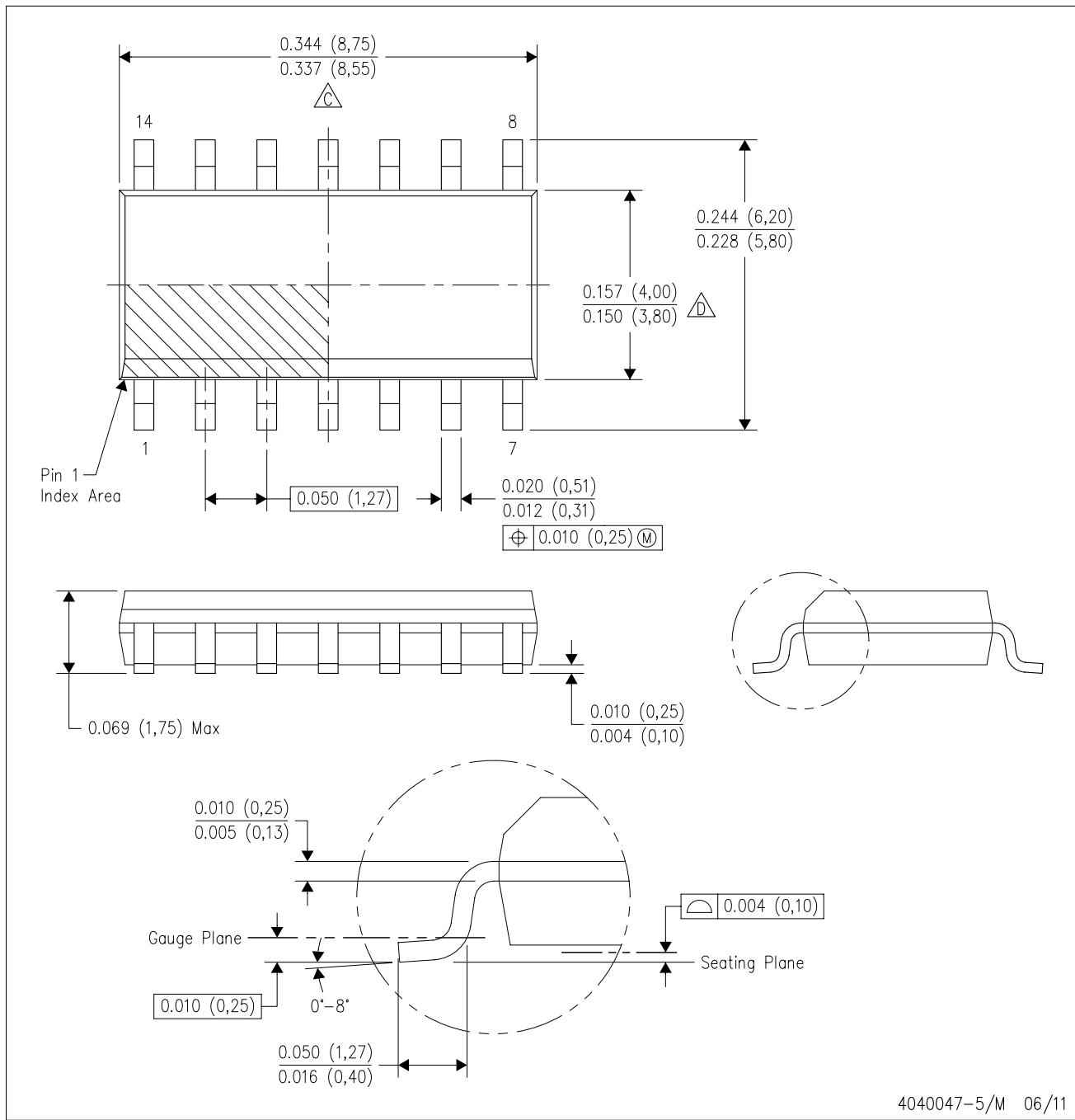
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALVC14D	D	SOIC	14	50	506.6	8	3940	4.32
SN74ALVC14DG4	D	SOIC	14	50	506.6	8	3940	4.32

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

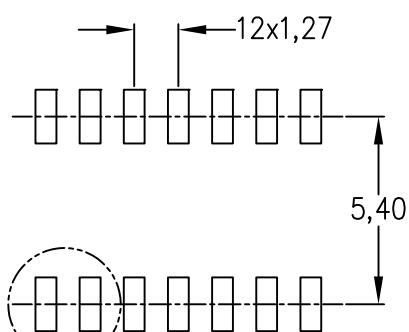
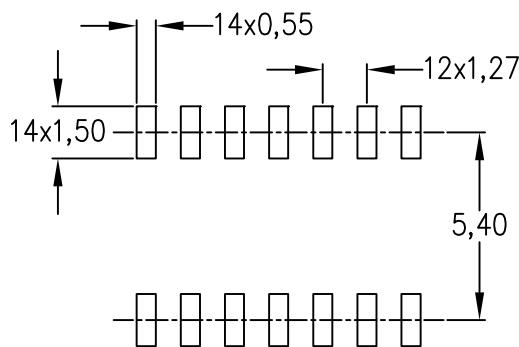
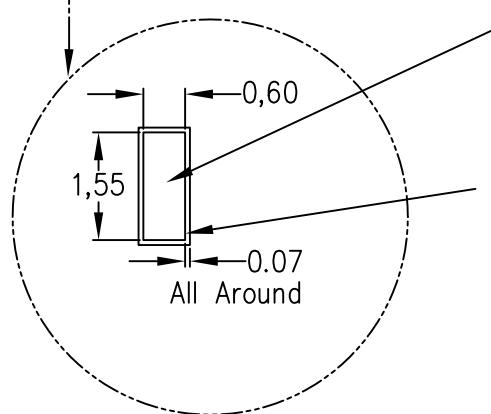
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

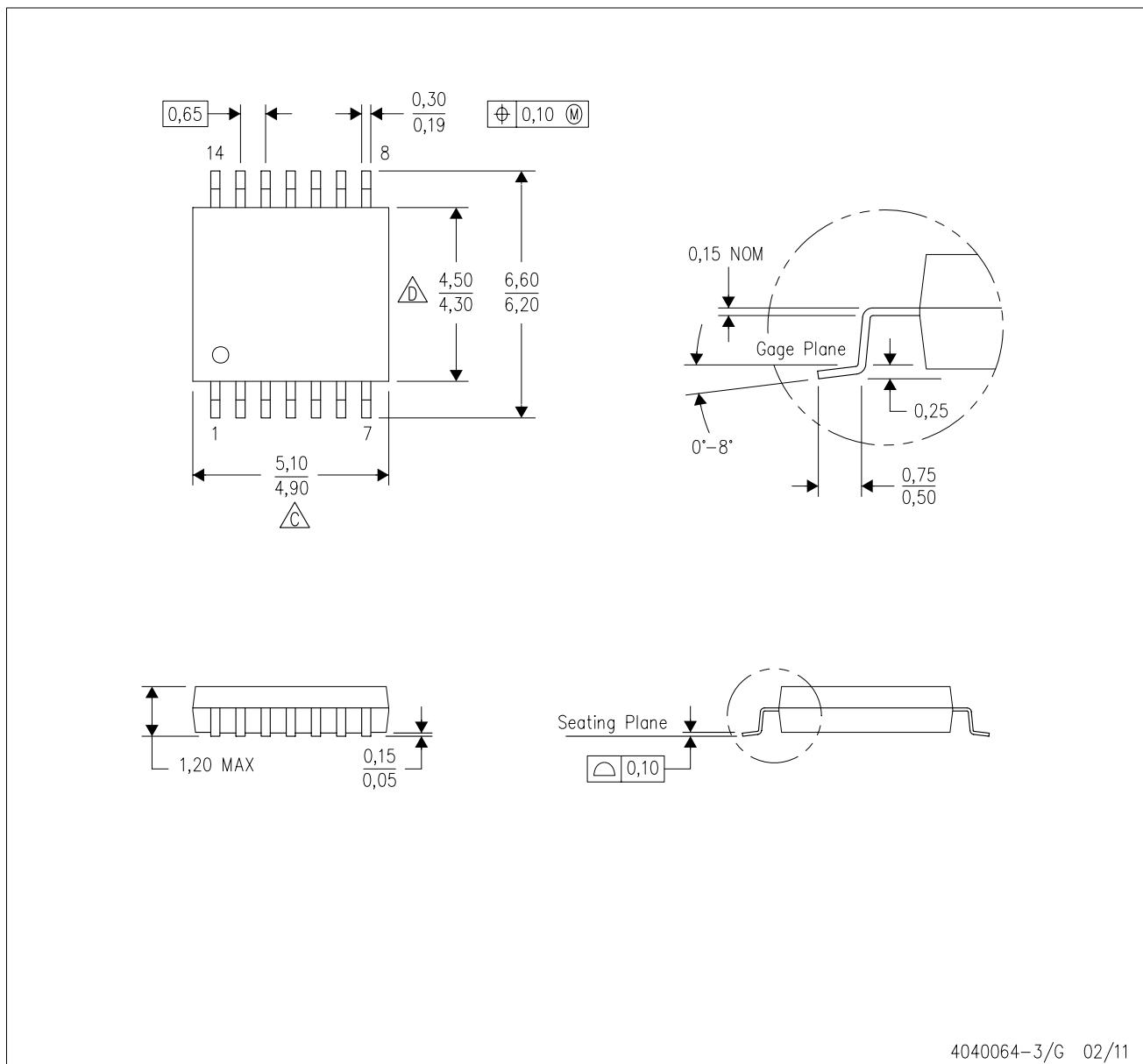
4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

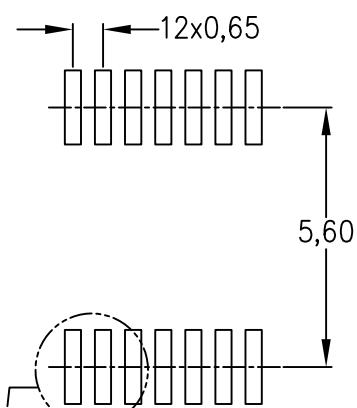
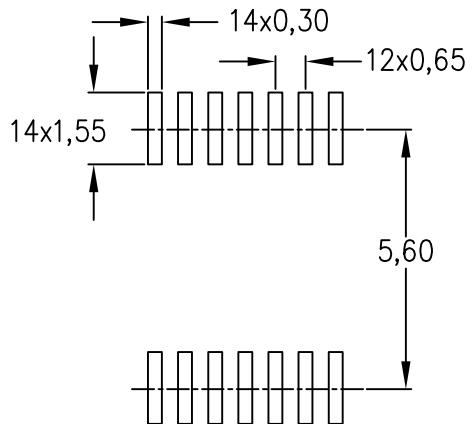
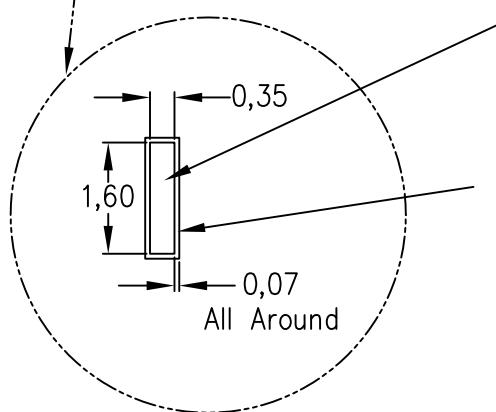
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

NOTES:

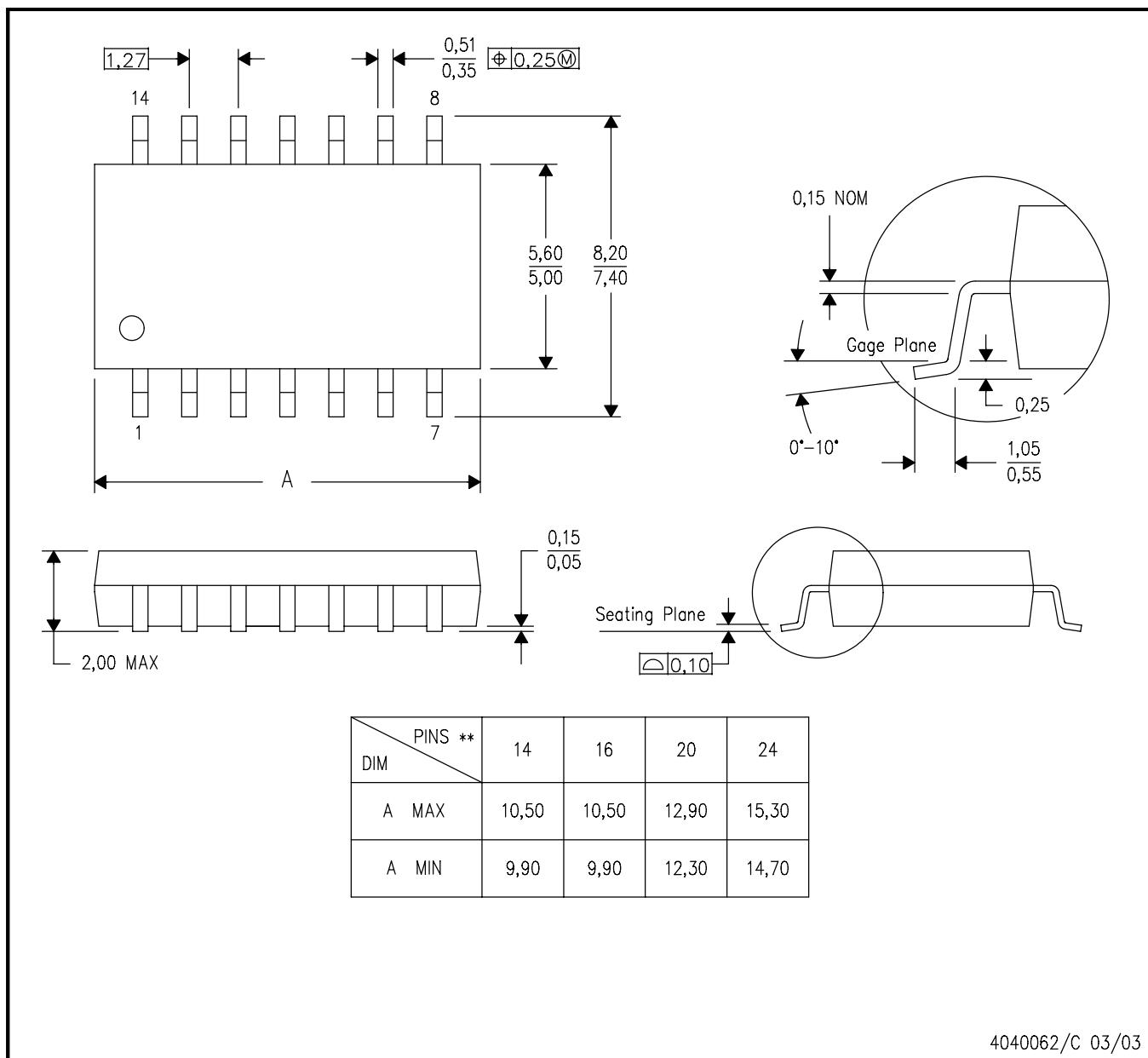
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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