

# ADC101S051/ADC101S051Q Single Channel, 200 to 500 ksps, 10-Bit A/D Converter

Check for Samples: [ADC101S051](#)

## FEATURES

- Specified Over a Range of Sample Rates.
- 6-lead WSON and SOT-23 Packages
- Variable Power Management
- Single Power Supply with 2.7V - 5.25V Range
- SPI™/QSPI™/MICROWIRE/DSP Compatible
- AECQ100 Grade 1 Qualified

## APPLICATIONS

- Portable Systems
- Remote Data Acquisition
- Instrumentation and Control Systems
- Automotive

## KEY SPECIFICATIONS

- DNL: +0.15 / -0.11 LSB (typ)
- INL: +0.15 / -0.09 LSB (typ)
- SNR: 61.6 dB (typ)
- Power Consumption
  - 3.6V Supply: 2.7 mW (typ)
  - 5.25V Supply: 9.7 mW (typ)

## DESCRIPTION

The ADC101S051 is a low-power, single channel CMOS 10-bit analog-to-digital converter with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC101S051 is fully specified over a sample rate range of 200 ksps to 500 ksps. The converter is based upon a successive-approximation register architecture with an internal track-and-hold circuit.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces.

The ADC101S051 operates with a single supply that can range from +2.7V to +5.25V. Normal power consumption using a +3.6V or +5.25V supply is 2.7 mW and 9.7 mW, respectively. The power-down feature reduces the power consumption to as low as 2.6  $\mu$ W using a +5.25V supply.

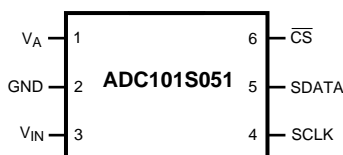
The ADC101S051 is packaged in 6-lead WSON and SOT-23 packages. Operation is specified over the temperature range of -40°C to +85°C for the ADC101S051 and -40°C to +125°C for the ADC101S051Q.

**Table 1. Pin Compatible Alternatives by Resolution and Speed<sup>(1)</sup>**

Resolution	Specified for Sample Rate Range of:		
	50 to 200 ksps	200 to 500 ksps	500 ksps to 1 Msps
12-bit	ADC121S021	ADC121S051	ADC121S101
10-bit	ADC101S021	ADC101S051	ADC101S101
8-bit	ADC081S021	ADC081S051	ADC081S101

(1) All devices are fully pin and function compatible.

## Connection Diagram



**Figure 1. WSON and SOT-23 Packages**  
See Package Numbers NGF0006A and DBV0006A



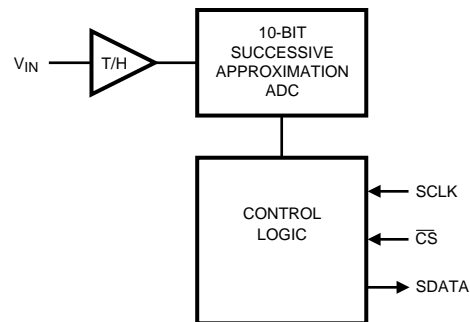
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## Block Diagram



**Figure 2.**

## Pin Descriptions and Equivalent Circuits

Pin No.	Name	Description
<b>ANALOG I/O</b>		
3	$V_{IN}$	Analog input. This signal can range from 0V to $V_A$ .
<b>DIGITAL I/O</b>		
4	SCLK	Digital clock input. This clock directly controls the conversion and readout processes.
5	SDATA	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
6	$\overline{CS}$	Chip select. On the falling edge of $\overline{CS}$ , a conversion process begins.
<b>POWER SUPPLY</b>		
1	$V_A$	Positive supply pin. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with a 1 $\mu$ F capacitor and a 0.1 $\mu$ F monolithic capacitor located within 1 cm of the power pin.
2	GND	The ground return for the supply and signals.
PAD	GND	For package suffix C1SD(X) only, it is recommended that the center pad should be connected to ground.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

Analog Supply Voltage $V_A$	–0.3V to 6.5V
Voltage on Any Analog Pin to GND	–0.3V to $(V_A + 0.3V)$
Voltage on Any Digital Pin to GND	–0.3V to 6.5V
Input Current at Any Pin <sup>(4)</sup>	±10 mA
Package Input Current <sup>(4)</sup>	±20 mA
Power Consumption at $T_A = 25^\circ\text{C}$	See <sup>(5)</sup>
ESD Susceptibility <sup>(6)</sup>	
Human Body Model	3500V
Machine Model	300V
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the [Electrical Characteristics](#). The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
- (3) If Military/Aerospace specified devices are required, please contact the TI Office/Distributors for availability and specifications.
- (4) When the input voltage at any pin exceeds the power supply (that is,  $V_{IN} < \text{GND}$  or  $V_{IN} > V_A$ ), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. The Absolute Maximum Rating specification does not apply to the  $V_A$  pin. The current into the  $V_A$  pin is limited by the Analog Supply Voltage specification.
- (5) The absolute maximum junction temperature ( $T_{Jmax}$ ) for this device is 150°C. The maximum allowable power dissipation is dictated by  $T_{Jmax}$ , the junction-to-ambient thermal resistance ( $\theta_{JA}$ ), and the ambient temperature ( $T_A$ ), and can be calculated using the formula  $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ . The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
- (6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through zero ohms.

### Operating Ratings<sup>(1)(2)</sup>

Operating Temperature Range	
ADC101S051	–40°C ≤ $T_A$ ≤ +85°C
ADC101S051Q	–40°C ≤ $T_A$ ≤ +125°C
$V_A$ Supply Voltage	+2.7V to +5.25V
Digital Input Pins Voltage Range (regardless of supply voltage)	–0.3V to 5.25V
Analog Input Pins Voltage Range	0V to $V_A$
Clock Frequency	25 kHz to 20 MHz
Sample Rate	up to 1Mps

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the [Electrical Characteristics](#). The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

### Package Thermal Resistance<sup>(1)(1)</sup>

Package	$\theta_{JA}$
6-lead WSON	94°C / W
6-lead SOT-23	265°C / W

- (1) Reflow temperature profiles are different for lead-free and non-lead-free packages.

## ADC101S051 Converter Electrical Characteristics<sup>(1)(2)</sup>

The following specifications apply for  $V_A = +2.7\text{V}$  to  $5.25\text{V}$ ,  $f_{\text{SCLK}} = 4\text{ MHz}$  to  $10\text{ MHz}$ ,  $f_{\text{SAMPLE}} = 200\text{ kps}$  to  $500\text{ kps}$ ,  $C_L = 15\text{ pF}$ , unless otherwise noted. **Boldface limits apply for  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$** ; all other limits  $T_A = 25^\circ\text{C}$ .

Parameter		Test Conditions	Typ	Limits <sup>(2)</sup>	Units
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			10	Bits
INL	Integral Non-Linearity	V <sub>A</sub> = +2.7 to +3.6V	+0.12	±0.7	LSB (max)
			−0.08		LSB (min)
		V <sub>A</sub> = +4.75 to +5.25V	+0.15	±0.7	LSB (max)
			−0.09		LSB (min)
DNL	Differential Non-Linearity	V <sub>A</sub> = +2.7 to +3.6V	+0.15	±0.6	LSB (max)
			−0.11		LSB (min)
		V <sub>A</sub> = +4.75 to +5.25V	+0.15	±0.6	LSB (max)
			−0.11		LSB (min)
V <sub>OFF</sub>	Offset Error	V <sub>A</sub> = +2.7 to +3.6V	+0.21	±0.7	LSB (max)
		V <sub>A</sub> = +4.75 to +5.25V	+0.11	±0.7	LSB (max)
GE	Gain Error	V <sub>A</sub> = +2.7 to +3.0V, ADC101S051Q	−0.2		LSB (max)
		V <sub>A</sub> = +3.0 to +3.6V, ADC101S051Q	−0.2	±1.0	LSB (max)
		V <sub>A</sub> = +2.7 to +3.6V, ADC101S051	−0.2	±1.0	LSB (max)
		V <sub>A</sub> = +4.75 to +5.25V	−0.33	±1.0	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
SINAD	Signal-to-Noise Plus Distortion Ratio	V <sub>A</sub> = +2.7 to 5.25V f <sub>IN</sub> = 100 kHz, −0.02 dBFS	61.5	60.8	dB (min)
SNR	Signal-to-Noise Ratio	V <sub>A</sub> = +2.7 to 5.25V f <sub>IN</sub> = 100 kHz, −0.02 dBFS	61.6	61.1	dB (min)
THD	Total Harmonic Distortion	V <sub>A</sub> = +2.7 to 5.25V f <sub>IN</sub> = 100 kHz, −0.02 dBFS	−79	−72.5	dB (max)
SFDR	Spurious-Free Dynamic Range	V <sub>A</sub> = +2.7 to 5.25V f <sub>IN</sub> = 100 kHz, −0.02 dBFS, ADC101S051Q	81	70	dB (min)
SFDR	Spurious-Free Dynamic Range	V <sub>A</sub> = +2.7 to 5.25V f <sub>IN</sub> = 100 kHz, −0.02 dBFS, ADC101S051	81	74	dB (min)
ENOB	Effective Number of Bits	V <sub>A</sub> = +2.7 to 5.25V f <sub>IN</sub> = 100 kHz, −0.02 dBFS	9.9	9.8	Bits (min)
IMD	Intermodulation Distortion, Second Order Terms	V <sub>A</sub> = +5.25V f <sub>a</sub> = 103.5 kHz, f <sub>b</sub> = 113.5 kHz	−83		dB
	Intermodulation Distortion, Third Order Terms	V <sub>A</sub> = +5.25V f <sub>a</sub> = 103.5 kHz, f <sub>b</sub> = 113.5 kHz	−82		dB
FPBW	−3 dB Full Power Bandwidth	V <sub>A</sub> = +5V	11		MHz
		V <sub>A</sub> = +3V	8		MHz
ANALOG INPUT CHARACTERISTICS					
V <sub>IN</sub>	Input Range		0 to V <sub>A</sub>		V
I <sub>DCL</sub>	DC Leakage Current			±1	μA (max)
C <sub>INA</sub>	Input Capacitance	Track Mode	30		pF
		Hold Mode	4		pF

(1) Tested limits are specified to Texas Instrument's AOQL (Average Outgoing Quality Level).

(2) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

## ADC101S051 Converter Electrical Characteristics<sup>(1)(2)</sup> (continued)

The following specifications apply for  $V_A = +2.7V$  to  $5.25V$ ,  $f_{SCLK} = 4\text{ MHz}$  to  $10\text{ MHz}$ ,  $f_{SAMPLE} = 200\text{ kpsps}$  to  $500\text{ kpsps}$ ,  $C_L = 15\text{ pF}$ , unless otherwise noted. **Boldface limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = 25^\circ C$ .

Parameter		Test Conditions	Typ	Limits <sup>(2)</sup>	Units
DIGITAL INPUT CHARACTERISTICS					
V <sub>IH</sub>	Input High Voltage	V <sub>A</sub> = +5.25V		2.4	V (min)
		V <sub>A</sub> = +3.6V		2.1	V (min)
V <sub>IL</sub>	Input Low Voltage	V <sub>A</sub> = +5V		0.8	V (max)
		V <sub>A</sub> = +3V		0.4	V (max)
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = 0V or V <sub>A</sub>	±0.1	±1	µA (max)
C <sub>IND</sub>	Digital Input Capacitance		2	4	pF (max)
DIGITAL OUTPUT CHARACTERISTICS					
V <sub>OH</sub>	Output High Voltage	I <sub>SOURCE</sub> = 200 µA	V <sub>A</sub> – 0.07	V <sub>A</sub> – 0.2	V (min)
		I <sub>SOURCE</sub> = 1 mA	V <sub>A</sub> – 0.1		V
V <sub>OL</sub>	Output Low Voltage	I <sub>SINK</sub> = 200 µA	0.03	0.4	V (max)
		I <sub>SINK</sub> = 1 mA	0.1		V
I <sub>OZH</sub> , I <sub>OZL</sub>	TRI-STATE Leakage Current		±0.1	±10	µA (max)
C <sub>OUT</sub>	TRI-STATE Output Capacitance		2	4	pF (max)
	Output Coding	Straight (Natural) Binary			
POWER SUPPLY CHARACTERISTICS					
V <sub>A</sub>	Supply Voltage			2.7	V (min)
				5.25	V (max)
I <sub>A</sub>	Supply Current, Normal Mode (Operational, $\overline{CS}$ low)	V <sub>A</sub> = +5.25V, f <sub>SAMPLE</sub> = 200 ksp/s	1.85	2.6	mA (max)
		V <sub>A</sub> = +3.6V, f <sub>SAMPLE</sub> = 200 ksp/s	0.75	1.2	mA (max)
	Supply Current, Shutdown ( $\overline{CS}$ high)	f <sub>SCLK</sub> = 0 MHz, V <sub>A</sub> = +5.25V f <sub>SAMPLE</sub> = 0 ksp/s	500		nA
		V <sub>A</sub> = +5.25V, f <sub>SCLK</sub> = 10 MHz, f <sub>SAMPLE</sub> = 0 ksp/s	60		µA
P <sub>D</sub>	Power Consumption, Normal Mode (Operational, $\overline{CS}$ low)	V <sub>A</sub> = +5.25V	9.7	13.7	mW (max)
		V <sub>A</sub> = +3.6V	2.7	4.3	mW (max)
	Power Consumption, Shutdown ( $\overline{CS}$ high)	f <sub>SCLK</sub> = 0 MHz, V <sub>A</sub> = +5.25V f <sub>SAMPLE</sub> = 0 ksp/s	2.6		µW
		V <sub>A</sub> = +5.25V, f <sub>SCLK</sub> = 10 MHz, f <sub>SAMPLE</sub> = 0 ksp/s	315		µW
AC ELECTRICAL CHARACTERISTICS					
f <sub>SCLK</sub>	Clock Frequency	See <sup>(3)</sup>		4	MHz (min)
				10	MHz (max)
f <sub>S</sub>	Sample Rate	See <sup>(3)</sup>		200	ksp/s (min)
				500	ksp/s (max)
DC	SCLK Duty Cycle	f <sub>SCLK</sub> = 10 MHz	50	40	% (min)
				60	% (max)
t <sub>ACQ</sub>	Minimum Time Required for Acquisition			350	ns (max)
t <sub>QUIET</sub>	See <sup>(4)</sup>			50	ns (min)
t <sub>AD</sub>	Aperture Delay		3		ns
t <sub>AJ</sub>	Aperture Jitter		30		ps

(3) This is the frequency range over which the electrical performance is specified. The device is functional over a wider range which is specified under Operating Ratings.

(4) Minimum Quiet Time required by bus relinquish and the start of the next conversion.

## ADC101S051 Timing Specifications

The following specifications apply for  $V_A = +2.7\text{V}$  to  $5.25\text{V}$ ,  $\text{GND} = 0\text{V}$ ,  $f_{\text{SCLK}} = 4\text{ MHz}$  to  $10\text{ MHz}$ ,  $C_L = 25\text{ pF}$ ,  $f_{\text{SAMPLE}} = 200\text{ kps}$  to  $500\text{ kps}$ , **Boldface limits apply for  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$** ; all other limits  $T_A = 25^\circ\text{C}$ .

Parameter		Test Conditions	Typ	Limits	Units
$t_{\text{CS}}$	Minimum $\overline{\text{CS}}$ Pulse Width			<b>10</b>	ns (min)
$t_{\text{SU}}$	$\overline{\text{CS}}$ to SCLK Setup Time			<b>10</b>	ns (min)
$t_{\text{EN}}$	Delay from $\overline{\text{CS}}$ Until SDATA TRI-STATE Disabled <sup>(1)</sup>			<b>20</b>	ns (max)
$t_{\text{ACC}}$	Data Access Time after SCLK Falling Edge <sup>(2)</sup>	$V_A = +2.7\text{V}$ to $+3.6\text{V}$		<b>40</b>	ns (max)
		$V_A = +4.75\text{V}$ to $+5.25\text{V}$		<b>20</b>	ns (max)
$t_{\text{CL}}$	SCLK Low Pulse Width			<b><math>0.4 \times t_{\text{SCLK}}</math></b>	ns (min)
$t_{\text{CH}}$	SCLK High Pulse Width			<b><math>0.4 \times t_{\text{SCLK}}</math></b>	ns (min)
$t_{\text{H}}$	SCLK to Data Valid Hold Time	$V_A = +2.7\text{V}$ to $+3.6\text{V}$		<b>7</b>	ns (min)
		$V_A = +4.75\text{V}$ to $+5.25\text{V}$		<b>5</b>	ns (min)
$t_{\text{DIS}}$	SCLK Falling Edge to SDATA High Impedance <sup>(3)</sup>	$V_A = +2.7\text{V}$ to $+3.6\text{V}$		<b>25</b>	ns (max)
				<b>5</b>	ns (min)
		$V_A = +4.75\text{V}$ to $+5.25\text{V}$		<b>25</b>	ns (max)
				<b>5</b>	ns (min)
$t_{\text{POWER-UP}}$	Power-Up Time from Full Power-Down		1		$\mu\text{s}$

- (1) Measured with the timing test circuit shown in Figure 3 and defined as the time taken by the output signal to cross  $1.0\text{V}$ .  
 (2) Measured with the timing test circuit shown in Figure 3 and defined as the time taken by the output signal to cross  $1.0\text{V}$  or  $2.0\text{V}$ .  
 (3)  $t_{\text{DIS}}$  is derived from the time taken by the outputs to change by  $0.5\text{V}$  with the timing test circuit shown in Figure 3. The measured number is then adjusted to remove the effects of charging or discharging the output capacitance. This means that  $t_{\text{DIS}}$  is the true bus relinquish time, independent of the bus loading.

## Timing Diagrams

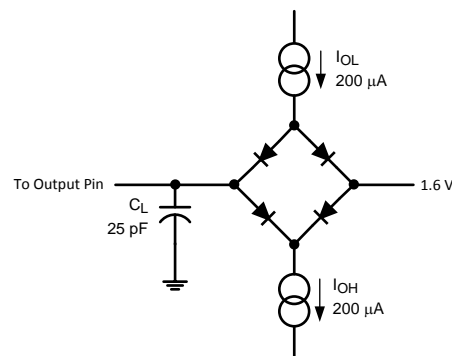
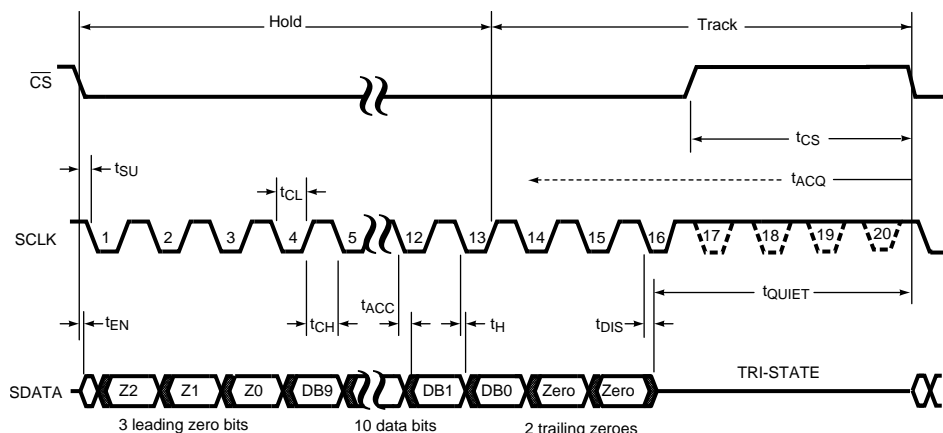


Figure 3. Timing Test Circuit



**Figure 4. ADC101S051 Serial Timing Diagram**

## Specification Definitions

**ACQUISITION TIME** is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage. Acquisition time is measured backwards from the falling edge of  $\overline{CS}$  when the signal is sampled and the part moves from track to hold. The start of the time interval that contains  $T_{ACQ}$  is the 13th rising edge of SCLK of the previous conversion when the part moves from hold to track. The user must ensure that the time between the 13th rising edge of SCLK and the falling edge of the next  $\overline{CS}$  is not less than  $T_{ACQ}$  to meet performance specifications.

**APERTURE DELAY** is the time after the falling edge of  $\overline{CS}$  to when the input signal is acquired or held for conversion.

**APERTURE JITTER (APERTURE UNCERTAINTY)** is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

**CONVERSION TIME** is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word. This is from the falling edge of  $\overline{CS}$  when the input signal is sampled to the 16th falling edge of SCLK when the SDATA output goes into TRI-STATE.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB.

**DUTY CYCLE** is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as  $(\text{SINAD} - 1.76) / 6.02$  and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

**FULL POWER BANDWIDTH** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

**GAIN ERROR** is the deviation of the last code transition (111...110) to (111...111) from the ideal ( $V_{REF} - 1.5$  LSB), after adjusting for offset error.

**INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual code from a line drawn from negative full scale ( $\frac{1}{2}$  LSB below the first code transition) through positive full scale ( $\frac{1}{2}$  LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

**INTERMODULATION DISTORTION (IMD)** is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dB.

**MISSING CODES** are those output codes that will never appear at the ADC outputs. The ADC101S051 is specified not to have any missing codes.

**OFFSET ERROR** is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

**SIGNAL TO NOISE RATIO (SNR)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

**SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD)** Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

**SPURIOUS FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

**TOTAL HARMONIC DISTORTION (THD)** is the ratio, expressed in dB or dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$\text{THD} = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \dots + A_{f6}^2}{A_{f1}^2}} \quad (1)$$

where  $A_{f1}$  is the RMS power of the input frequency at the output and  $A_{f2}$  through  $A_{f6}$  are the RMS power in the first 5 harmonic frequencies.

**THROUGHPUT TIME** is the minimum time required between the start of two successive conversion. It is the acquisition time plus the conversion time.



## Typical Performance Characteristics

$T_A = +25^\circ\text{C}$ ,  $f_{\text{SAMPLE}} = 200 \text{ kps to } 500 \text{ kps}$ ,  $f_{\text{SCLK}} = 4 \text{ MHz to } 10 \text{ MHz}$ ,  $f_{\text{IN}} = 100 \text{ kHz}$  unless otherwise stated.

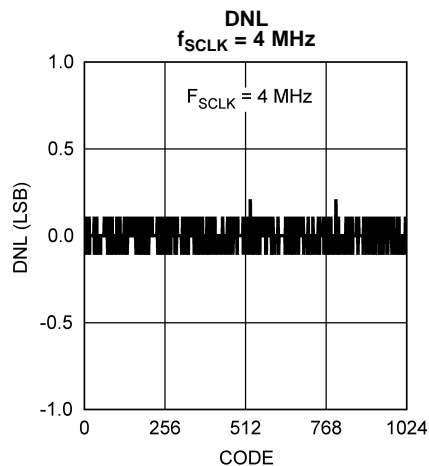


Figure 5.

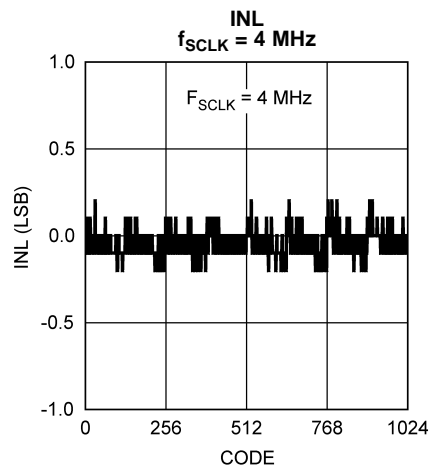


Figure 6.

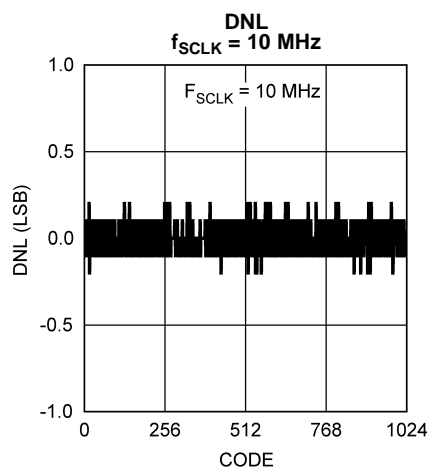


Figure 7.

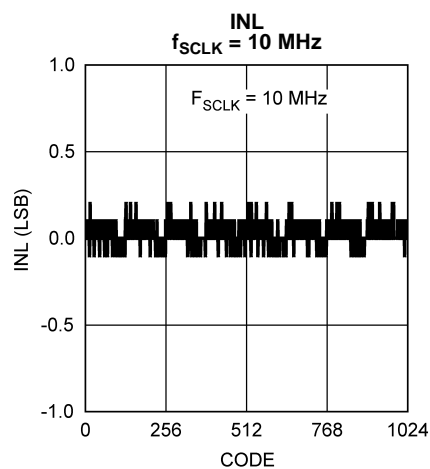


Figure 8.

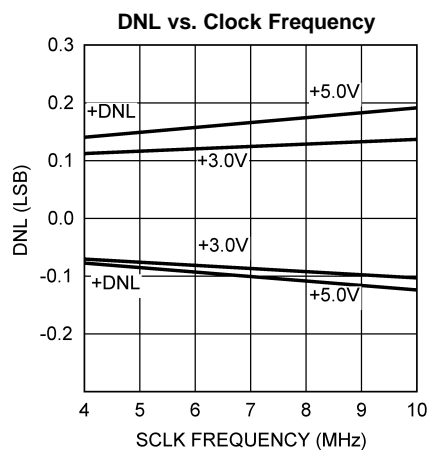


Figure 9.

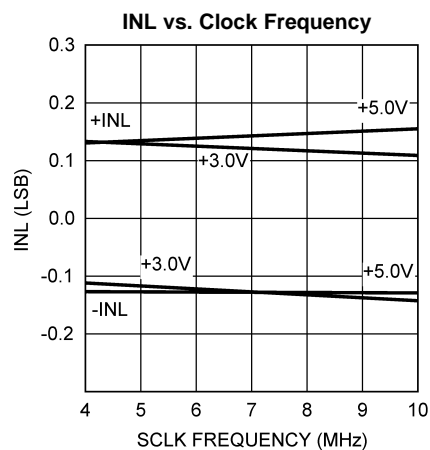
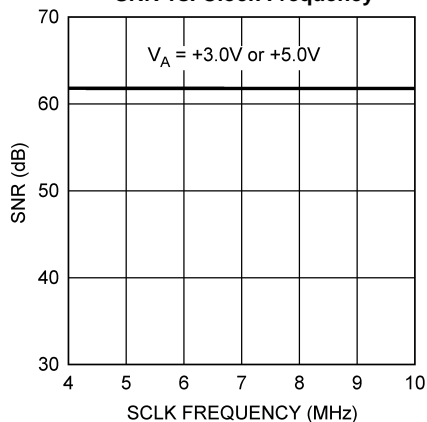


Figure 10.

### Typical Performance Characteristics (continued)

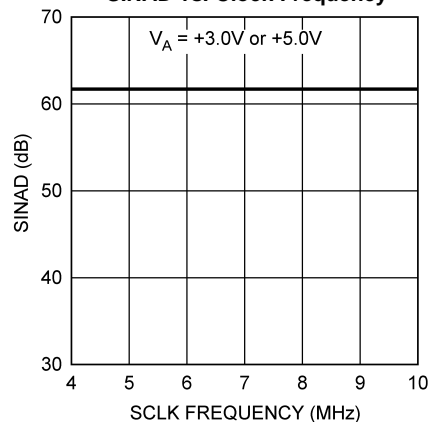
$T_A = +25^\circ\text{C}$ ,  $f_{\text{SAMPLE}} = 200 \text{ kpsps}$  to  $500 \text{ kpsps}$ ,  $f_{\text{SCLK}} = 4 \text{ MHz}$  to  $10 \text{ MHz}$ ,  $f_{\text{IN}} = 100 \text{ kHz}$  unless otherwise stated.

**SNR vs. Clock Frequency**



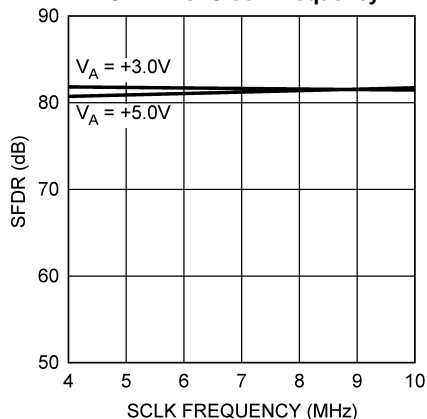
**Figure 11.**

**SINAD vs. Clock Frequency**



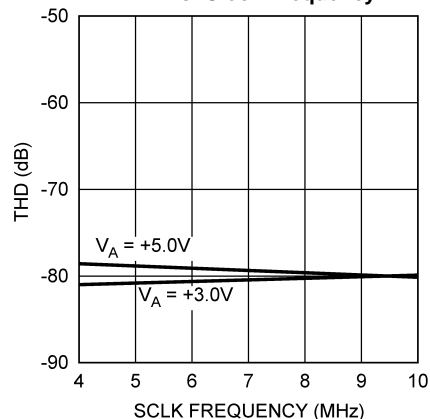
**Figure 12.**

**SFDR vs. Clock Frequency**



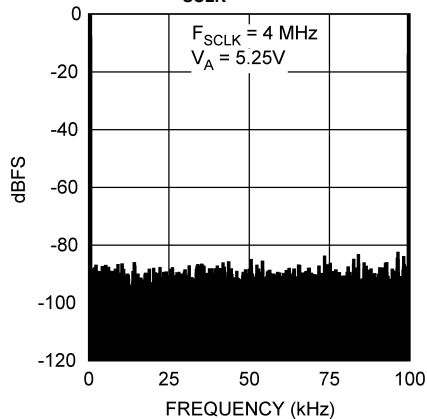
**Figure 13.**

**THD vs. Clock Frequency**



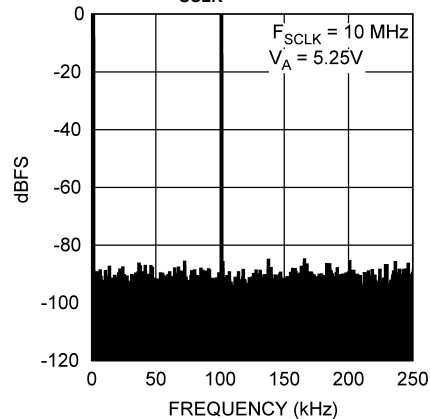
**Figure 14.**

**Spectral Response,  $V_A = 5.25\text{V}$   
 $f_{\text{SCLK}} = 4 \text{ MHz}$**



**Figure 15.**

**Spectral Response,  $V_A = 5.25\text{V}$   
 $f_{\text{SCLK}} = 10 \text{ MHz}$**

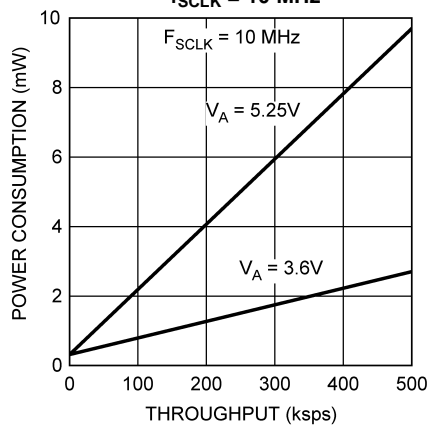


**Figure 16.**

## Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$ ,  $f_{\text{SAMPLE}} = 200 \text{ kpsps to } 500 \text{ kpsps}$ ,  $f_{\text{SCLK}} = 4 \text{ MHz to } 10 \text{ MHz}$ ,  $f_{\text{IN}} = 100 \text{ kHz}$  unless otherwise stated.

**Power Consumption vs. Throughput,  
 $f_{\text{SCLK}} = 10 \text{ MHz}$**



**Figure 17.**

## APPLICATIONS INFORMATION

### ADC101S051 OPERATION

The ADC101S051 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter core. Simplified schematics of the ADC101S051 in both track and hold modes are shown in Figure 18 and Figure 19, respectively. In Figure 18, the device is in track mode: switch SW1 connects the sampling capacitor to the input and SW2 balances the comparator inputs. The device is in this state until  $\overline{CS}$  is brought low, at which point the device moves to the hold mode.

Figure 19 shows the device in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode on the 13th rising edge of SCLK.

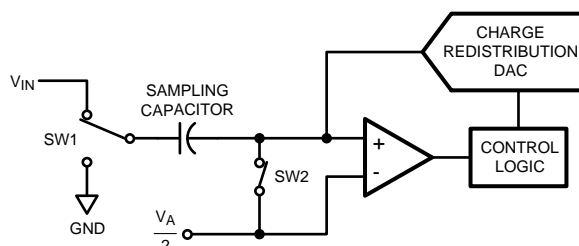


Figure 18. ADC101S051 in Track Mode

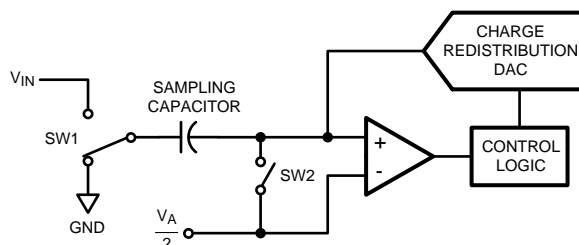


Figure 19. ADC101S051 in Hold Mode

### USING THE ADC101S051

The serial interface timing diagram for the ADC is shown in Figure 4.  $\overline{CS}$  is chip select, which initiates conversions on the ADC and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found as a serial data stream.

Basic operation of the ADC begins with  $\overline{CS}$  going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK will be labelled with reference to the falling edge of  $\overline{CS}$ ; for example, "the third falling edge of SCLK" shall refer to the third falling edge of SCLK after  $\overline{CS}$  goes low.

At the fall of  $\overline{CS}$ , the SDATA pin comes out of TRI-STATE and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion on the falling edge of  $\overline{CS}$ . The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see Figure 4). It is at this point that the interval for the  $T_{ACQ}$  specification begins. At least 350ns must pass between the 13th rising edge of SCLK and the next falling edge of  $\overline{CS}$ . The SDATA pin will be placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of  $\overline{CS}$ , whichever occurs first. After a conversion is completed, the quiet time ( $t_{QUIET}$ ) must be satisfied before bringing  $\overline{CS}$  low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the ADC. The sample bits (including leading or trailing zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent rising edges of SCLK. The ADC will produce three leading zero bits on SDATA, followed by ten data bits, most significant first. After the data bits, the ADC will clock out two trailing zeros.

If  $\overline{CS}$  goes low before the rising edge of SCLK, an additional (fourth) zero bit may be captured by the next falling edge of SCLK.

## Determining Throughput

Throughput depends on the frequency of SCLK and how much time is allowed to elapse between the end of one conversion and the start of another. At the maximum specified SCLK frequency, the maximum specified throughput is obtained by using a 20 SCLK frame. As shown in Figure 4, the minimum allowed time between  $\overline{CS}$  falling edges is determined by 1) 12.5 SCLKs for Hold mode, 2) the larger of two quantities: either the minimum required time for Track mode ( $t_{ACQ}$ ) or 2.5 SCLKs to finish reading the result and 3) 0, 1/2 or 1 SCLK padding to ensure an even number of SCLK cycles so there is a falling SCLK edge when  $\overline{CS}$  next falls. For example, at the fastest rate for this family of parts, SCLK is 20MHz and 2.5 SCLKs are 125ns, so the minimum time between  $\overline{CS}$  falling edges is calculated by

$$12.5 \cdot 50\text{ns} + 350\text{ns} + 0.5 \cdot 50\text{ns} = 1000\text{ns} \quad (2)$$

(12.5 SCLKs +  $t_{ACQ}$  + 1/2 SCLK) which corresponds to a maximum throughput of 1MSPS. At the slowest rate for this family, SCLK is 1MHz. Using a 20 cycle conversion frame as shown in Figure 4 yields a 20 $\mu$ s time between  $\overline{CS}$  falling edges for a throughput of 50KSPS. It is possible, however, to use fewer than 20 clock cycles provided the timing parameters are met. With a 1MHz SCLK, there are 2500ns in 2.5 SCLK cycles, which is greater than  $t_{ACQ}$ . After the last data bit has come out, the clock will need one full cycle to return to a falling edge. Thus the total time between falling edges of  $\overline{CS}$  is 12.5 $\mu$ s + 2.5 $\mu$ s + 1 $\mu$ s = 16 $\mu$ s which is a throughput of 62.5KSPS.

## ADC101S051 TRANSFER FUNCTION

The output format of the ADC is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC is  $V_A/1024$ . The ideal transfer characteristic is shown in Figure 20. The transition from an output code of 00 0000 0000 to a code of 00 0000 0001 is at 1/2 LSB, or a voltage of  $V_A/2048$ . Other code transitions occur at steps of one LSB.

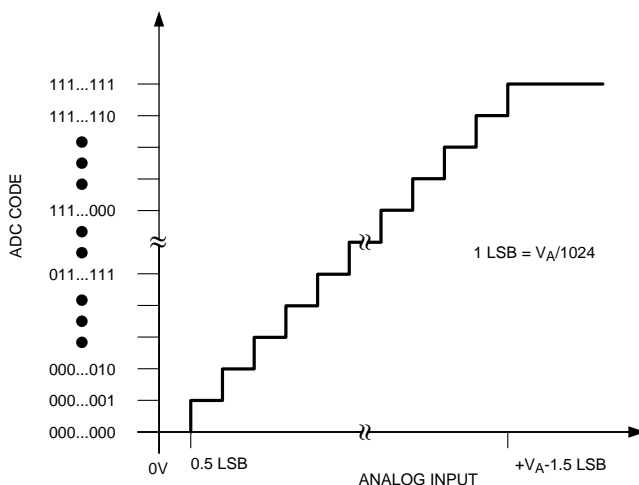


Figure 20. Ideal Transfer Characteristic

## TYPICAL APPLICATION CIRCUIT

A typical application of the ADC is shown in Figure 21. Power is provided in this example by the Texas Instruments LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network located close to the ADC. Because the reference for the ADC is the supply voltage, any noise on the supply will degrade device noise performance. To keep noise off the supply, use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC supply pin. Because of the ADC's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. The three-wire interface is shown connected to a microprocessor or DSP.

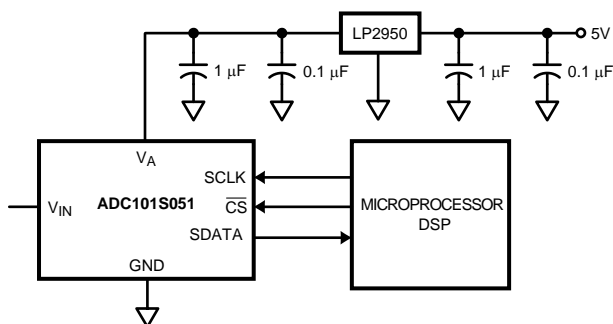


Figure 21. Typical Application Circuit

## ANALOG INPUTS

An equivalent circuit for the ADC's input is shown in Figure 22. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time should the analog input go beyond ( $V_A + 300\text{ mV}$ ) or ( $\text{GND} - 300\text{ mV}$ ), as these ESD diodes will begin conducting, which could result in erratic operation. For this reason, the ESD diodes should not be used to clamp the input signal.

The capacitor C1 in Figure 22 has a typical value of 4 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the track / hold switch, and is typically 500 ohms. Capacitor C2 is the ADC sampling capacitor and is typically 26 pF. The ADC will deliver best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC to sample AC signals. Also important when sampling dynamic signals is an anti-aliasing filter.

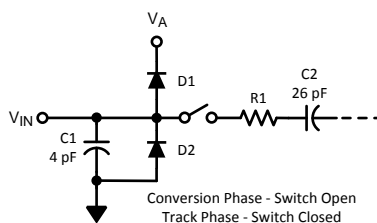


Figure 22. Equivalent Input Circuit

## DIGITAL INPUTS AND OUTPUTS

The ADC digital inputs (SCLK and  $\overline{\text{CS}}$ ) are not limited by the same maximum ratings as the analog inputs. The digital input pins are instead limited to +5.25V with respect to GND, regardless of  $V_A$ , the supply voltage. This allows the ADC to be interfaced with a wide range of logic levels, independent of the supply voltage.

## MODES OF OPERATION

The ADC has two possible modes of operation: normal mode, and shutdown mode. The ADC enters normal mode (and a conversion process is begun) when  $\overline{CS}$  is pulled low. The device will enter shutdown mode if  $\overline{CS}$  is pulled high before the tenth falling edge of SCLK after  $\overline{CS}$  is pulled low, or will stay in normal mode if  $\overline{CS}$  remains low. Once in shutdown mode, the device will stay there until  $\overline{CS}$  is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade-off throughput for power consumption, with a sample rate as low as zero.

### Normal Mode

The fastest possible throughput is obtained by leaving the ADC in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously,  $\overline{CS}$  must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing  $\overline{CS}$  low).

If  $\overline{CS}$  is brought high after the 10th falling edge, but before the 16th falling edge, the device will remain in normal mode, but the current conversion will be aborted, and SDATA will return to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed,  $\overline{CS}$  may be idled either high or low until the next conversion. If  $\overline{CS}$  is idled low, it must be brought high again before the start of the next conversion, which begins when  $\overline{CS}$  is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after  $t_{\text{QUIET}}$  has elapsed, by bringing  $\overline{CS}$  low again.

### Shutdown Mode

Shutdown mode is appropriate for applications that either do not sample continuously, or it is acceptable to trade throughput for power consumption. When the ADC is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing  $\overline{CS}$  high anytime between the second and tenth falling edges of SCLK, as shown in Figure 23. Once  $\overline{CS}$  has been brought high in this manner, the device will enter shutdown mode, the current conversion will be aborted and SDATA will enter TRI-STATE. If  $\overline{CS}$  is brought high before the second falling edge of SCLK, the device will not change mode; this is to avoid accidentally changing mode as a result of noise on the  $\overline{CS}$  line.

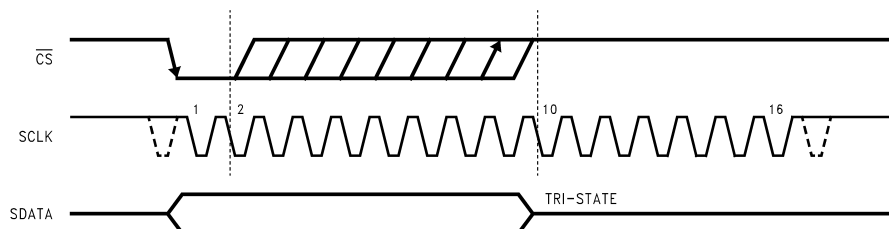


Figure 23. Entering Shutdown Mode

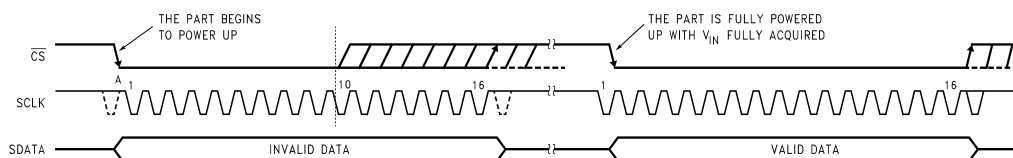


Figure 24. Entering Normal Mode

To exit shutdown mode, bring  $\overline{CS}$  back low. Upon bringing  $\overline{CS}$  low, the ADC will begin powering up (power-up time is specified in the Timing Specifications table). This power-up delay results in the first conversion result being unusable. The second conversion performed after power-up, however, is valid, as shown in Figure 24.

If  $\overline{CS}$  is brought back high before the 10th falling edge of SCLK, the device will return to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the  $\overline{CS}$  line. To exit shutdown mode and remain in normal mode,  $\overline{CS}$  must be kept low until after the 10th falling edge of SCLK. The ADC will be fully powered-up after 16 SCLK cycles.

## POWER MANAGEMENT

The ADC takes time to power-up, either after first applying  $V_A$ , or after returning to normal mode from shutdown mode. This corresponds to one "dummy" conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the ADC will perform conversions properly. Note that the  $t_{\text{QUIET}}$  time must still be included between the first dummy conversion and the second valid conversion.

When the  $V_A$  supply is first applied, the ADC may power up in either of the two modes: normal or shutdown. As such, one dummy conversion should be performed after start-up, as described in the previous paragraph. The part may then be placed into either normal mode or the shutdown mode, as described in [Normal Mode](#) and [Shutdown Mode](#).

When the ADC is operated continuously in normal mode, the maximum specified throughput is  $f_{\text{SCLK}} / 20$  at the maximum specified  $f_{\text{SCLK}}$ . Throughput may be traded for power consumption by running  $f_{\text{SCLK}}$  at its maximum specified rate and performing fewer conversions per unit time, raising the ADC  $\overline{CS}$  line after the 10th and before the 15th fall of SCLK between conversions. A plot of typical power consumption versus throughput is shown in the [Typical Performance Characteristics](#) section. To calculate the power consumption for a given throughput, multiply the fraction of time spent in the normal mode by the normal mode power consumption and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power consumption. Note that the curve of power consumption vs. throughput is essentially linear. This is because the power consumption in the shutdown mode is so small that it can be ignored for all practical purposes.

## POWER SUPPLY NOISE CONSIDERATIONS

The charging of any output load capacitance requires current from the power supply,  $V_A$ . The current pulses required from the supply to charge the output capacitance will cause voltage variations on the supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. It is good practice to use a 100  $\Omega$  series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and maintain noise performance.

## REVISION HISTORY

Changes from Revision H (March 2013) to Revision I	Page
<ul style="list-style-type: none"> <li>Changed sentence in the "Using the ADC101S051" section .....</li> </ul>	12



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**Changes from Revision G (March 2013) to Revision H****Page**

- 
- Changed layout of National Data Sheet to TI format ..... [16](#)
-

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC101S051CIMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	X14C	<a href="#">Samples</a>
ADC101S051CIMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	X14C	<a href="#">Samples</a>
ADC101S051QIMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	X14Q	<a href="#">Samples</a>
ADC101S051QIMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	X14Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF ADC101S051, ADC101S051-Q1 :**

- Catalog: [ADC101S051](#)
- Automotive: [ADC101S051-Q1](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC101S051CIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADC101S051CIMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADC101S051QIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADC101S051QIMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS

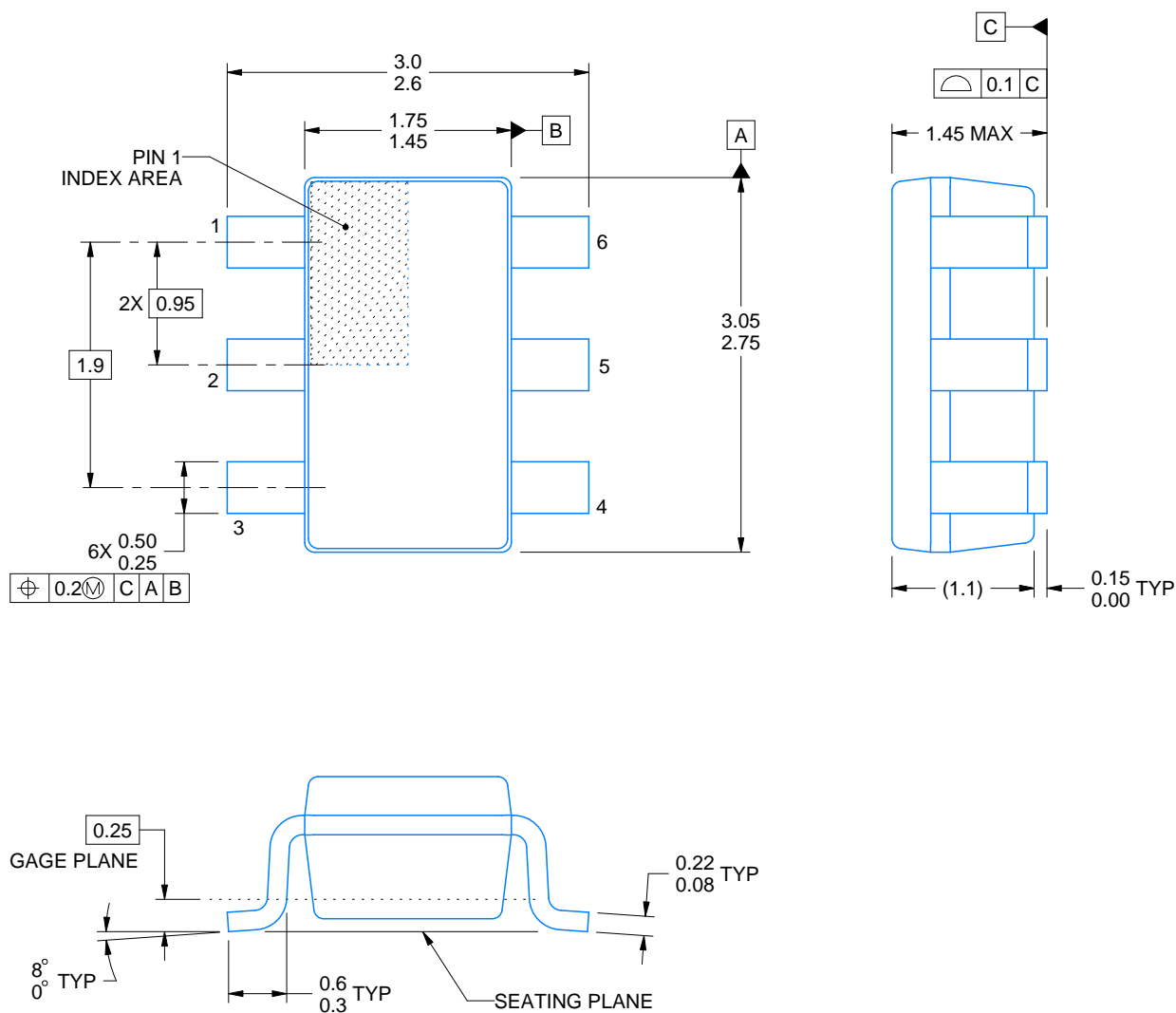


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC101S051CIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADC101S051CIMFX/NOP B	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADC101S051QIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADC101S051QIMFX/NOP B	SOT-23	DBV	6	3000	210.0	185.0	35.0

**DBV0006A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/C 06/2021

**NOTES:**

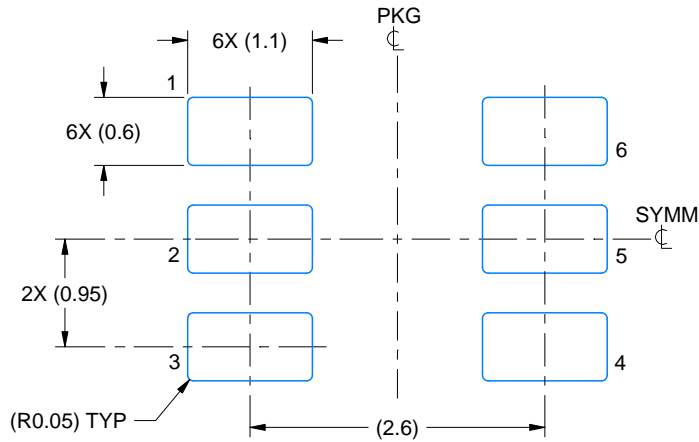
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

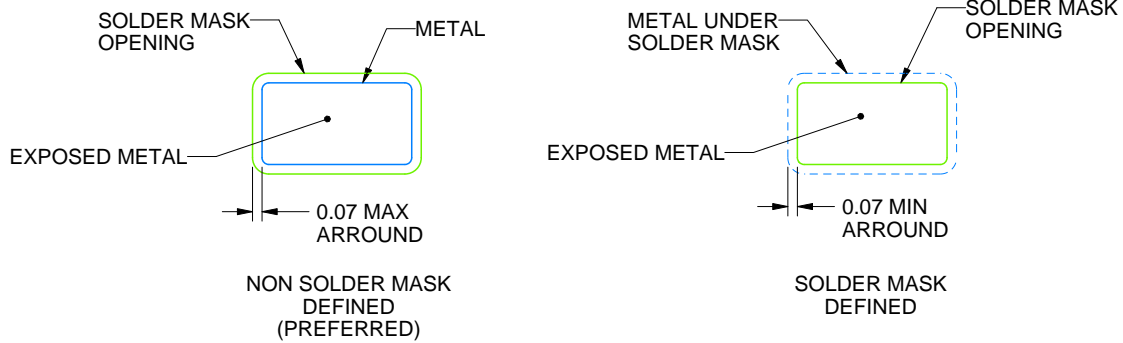
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

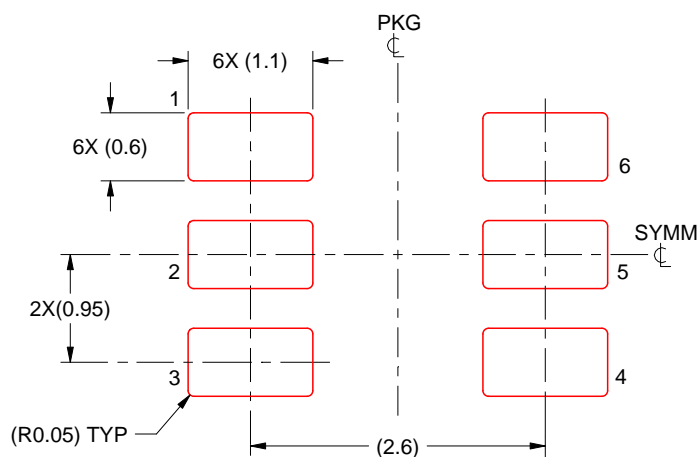
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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