

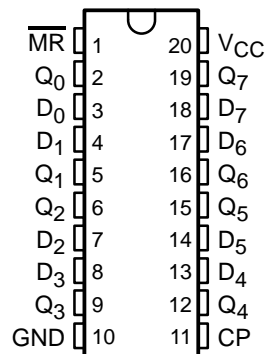
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT273T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT273T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current

description

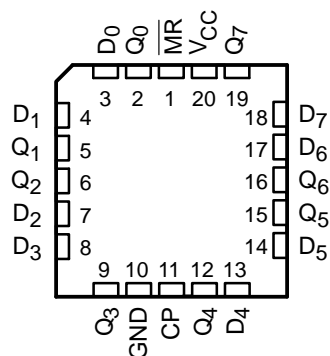
The 'FCT273T devices consist of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered-clock (CP) and master-reset (\overline{MR}) inputs load and reset all flip-flops simultaneously. These devices are edge-triggered registers. The state of each D input (one setup time before the low-to-high clock transition) is transferred to the corresponding flip-flop's Q output. All outputs are forced low by a low logic level on the \overline{MR} input.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY54FCT273T . . . D PACKAGE
CY74FCT273T . . . Q OR SO PACKAGE
(TOP VIEW)



CY54FCT273T . . . L PACKAGE
(TOP VIEW)



CY54FCT273T, CY74FCT273T
8-BIT REGISTERS

SCCS020A – MARCH 1995 – REVISED OCTOBER 2001

ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.8	CY74FCT273CTQCT	FCT273C
	SOIC – SO	Tube	5.8	CY74FCT273CTSOC	FCT273C
		Tape and reel	5.8	CY74FCT273CTSOCT	
	QSOP – Q	Tape and reel	7.2	CY74FCT273ATQCT	FCT273A
	SOIC – SO	Tube	7.2	CY74FCT273ATSOC	FCT273A
		Tape and reel	7.2	CY74FCT273ATSOCT	
	QSOP – Q	Tape and reel	13	CY74FCT273TQCT	FCT273
	SOIC – SO	Tube	13	CY74FCT273TSOC	FCT273
		Tape and reel	13	CY74FCT273TSOCT	
–55°C to 125°C	LCC – L	Tube	8.3	CY54FCT273ATLMB	

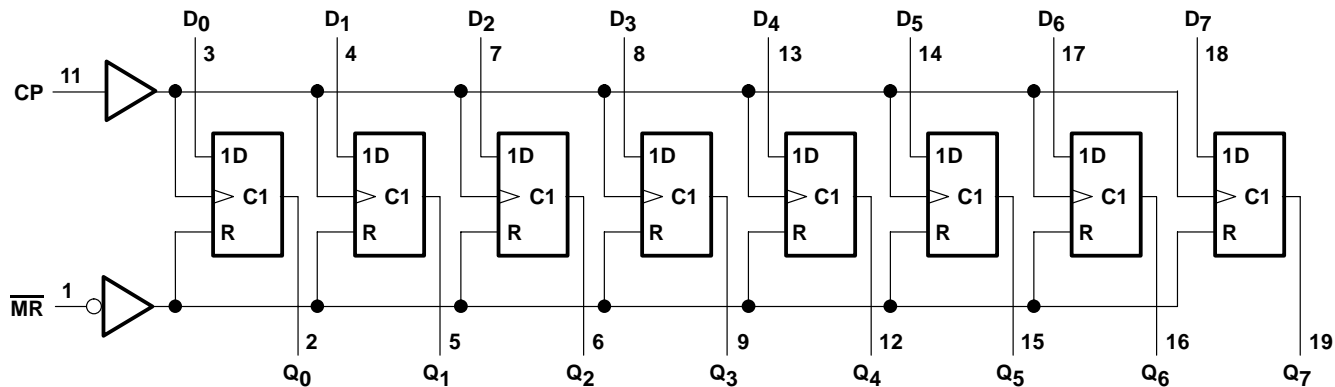
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUT Q	OPERATING MODE
MR	CP	D		
L	X	X	L	Reset (clear)
H	↑	h	H	Load '1'
H	↑	l	L	Load '0'

H = High logic level steady state, h = High logic level one setup time prior to low-to-high clock transition, L = Low logic level steady state, l = Low logic level one setup time prior to the low-to-high transition, X = Don't care, ↑ = Low-to-high clock transition

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	CY54FCT273T			CY74FCT273T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			–12			–32	mA
I_{OL} Low-level output current			32			64	mA
T_A Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

CY54FCT273T, CY74FCT273T

8-BIT REGISTERS

SCCS020A – MARCH 1995 – REVISED OCTOBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT273T			CY74FCT273T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_{IN} = -18\text{ mA}$	-0.7	-1.2					V
	$V_{CC} = 4.75\text{ V}$, $I_{IN} = -18\text{ mA}$				-0.7	-1.2		
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75\text{ V}$				2			
					2.4	3.3		
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 32\text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 64\text{ mA}$				0.3	0.55		
V_{hys}	All inputs	0.2			0.2			V
I_I	$V_{CC} = 5.5\text{ V}$, $V_{IN} = V_{CC}$			5				μA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} = V_{CC}$						5	
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 2.7\text{ V}$			± 1				μA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} = 2.7\text{ V}$						± 1	
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 0.5\text{ V}$			± 1				μA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} = 0.5\text{ V}$						± 1	
I_{off}	$V_{CC} = 0\text{ V}$, $V_{OUT} = 4.5\text{ V}$			± 1			± 1	μA
I_{OS}^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_{OUT} = 0\text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25\text{ V}$, $V_{OUT} = 0\text{ V}$				-60	-120	-225	
I_{CC}	$V_{CC} = 5.5\text{ V}$, $V_{IN} \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$				0.1	0.2		
ΔI_{CC}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 3.4\text{ V}^\S$, $f_1 = 0$, Outputs open	0.5	2					mA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} = 3.4\text{ V}^\S$, $f_1 = 0$, Outputs open				0.5	2		

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4\text{ V}$); all other inputs at V_{CC} or GND

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT273T			CY74FCT273T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I _{CCD} ¶	V _{CC} = 5.5 V, Outputs open, One bit switching at 50% duty cycle, $\overline{MR} = V_{CC}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.06	0.12					mA/ MHz
	V _{CC} = 5.25 V, Outputs open, One bit switching at 50% duty cycle, $\overline{MR} = V_{CC}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V						0.06	0.12		
I _C #	V _{CC} = 5.5 V, f ₀ = 10 MHz, Outputs open, $\overline{MR} = V_{CC}$	One bit switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4					mA
			V _{IN} = 3.4 V or GND	1.2	3.4					
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	1.6	3.2					
			V _{IN} = 3.4 V or GND	3.9	12.2					
	V _{CC} = 5.25 V, f ₀ = 10 MHz, Outputs open, $\overline{MR} = V_{CC}$	One bit switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V				0.7	1.4		
			V _{IN} = 3.4 V or GND				1.2	3.4		
		Eight bits switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V				1.6	3.2		
			V _{IN} = 3.4 V or GND				3.9	12.2		
C _i				5	10		5	10	pF	
C _o				9	12		9	12	pF	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

¶ This parameter is derived for use in total power-supply calculations.

$$\# I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4$ V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

CY54FCT273T, CY74FCT273T 8-BIT REGISTERS

SCCS020A – MARCH 1995 – REVISED OCTOBER 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

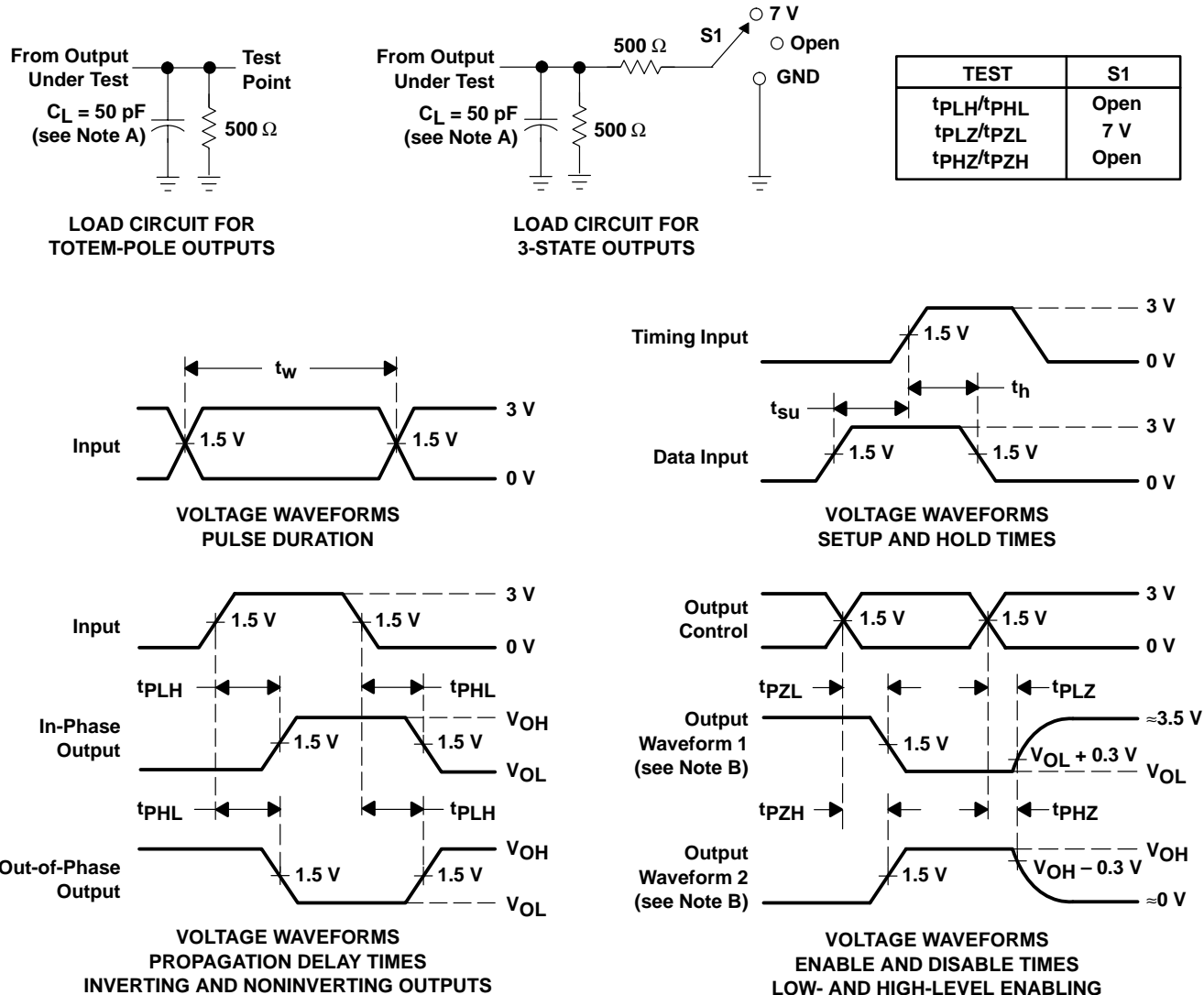
			CY74FCT273T		CY54FCT273AT		CY74FCT273AT		CY74FCT273CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, high or low	CP	6		6		6		6		ns
		\overline{MR}	6		6		6		6		
t_{su}	Setup time, high or low	D before CP \uparrow	2		2		2		2		ns
t_h	Hold time, high or low	D after CP \uparrow	1.5		1.5		1.5		1.5		ns
t_{rec}	Recovery time	\overline{MR} after CP \uparrow	2		2.5		2		2		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT273T		CY54FCT273AT		CY74FCT273AT		CY74FCT273CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CP	Q	2	13	2	8.3	2	7.2	2	5.8	ns
t_{PHL}			2	13	2	8.3	2	7.2	2	5.8	
t_{PLH}	\overline{MR}	Q	2	13	2	8.3	2	7.2	2	6.1	ns
t_{PHL}			2	13	2	8.3	2	7.2	2	6.1	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9221503M2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9221503M2A CY54FCT 273ATLMB	Samples
5962-9221503MRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9221503MR A	Samples
CY54FCT273ATLMB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9221503M2A CY54FCT 273ATLMB	Samples
CY74FCT273ATQCT	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273A	Samples
CY74FCT273ATSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273A	Samples
CY74FCT273ATSOCT	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273A	Samples
CY74FCT273CTQCT	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273C	Samples
CY74FCT273CTSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273C	Samples
CY74FCT273TQCT	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273	Samples
CY74FCT273TSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273	Samples
CY74FCT273TSOCT	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

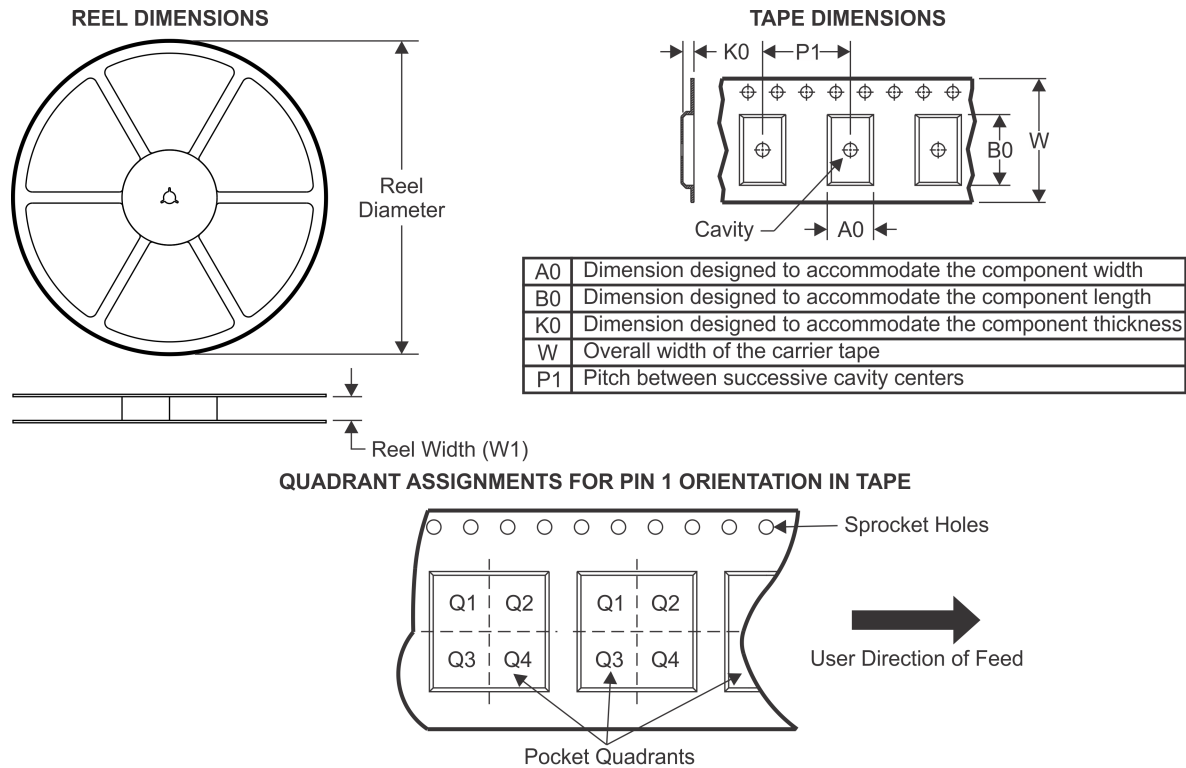
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

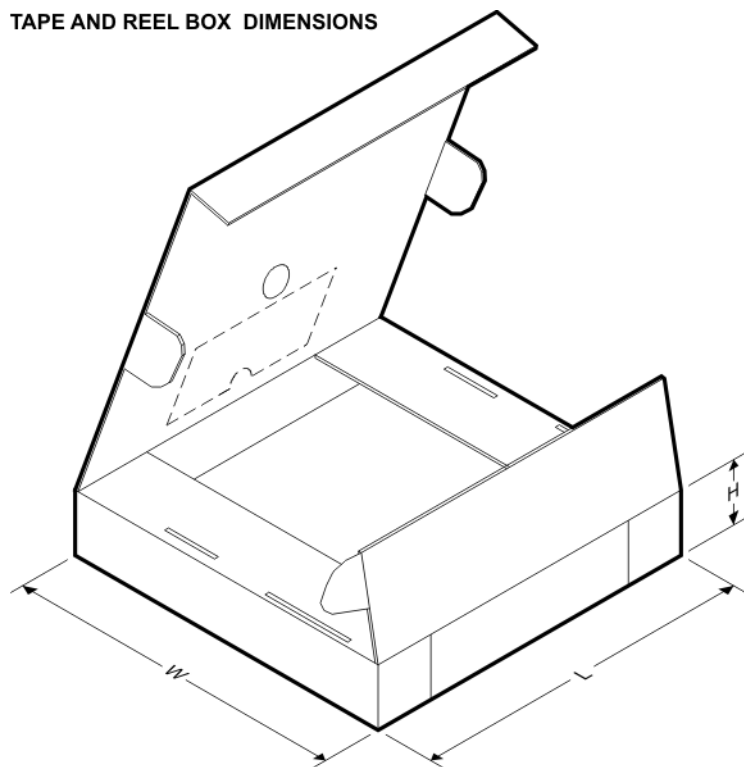
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT273ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT273ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT273CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT273TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT273TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

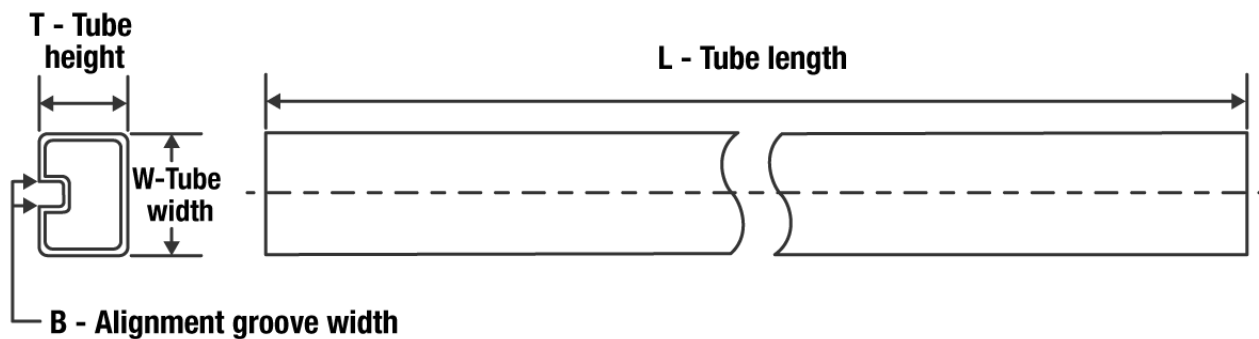
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT273ATQCT	SSOP	DBQ	20	2500	853.0	449.0	35.0
CY74FCT273ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT273CTQCT	SSOP	DBQ	20	2500	853.0	449.0	35.0
CY74FCT273TQCT	SSOP	DBQ	20	2500	853.0	449.0	35.0
CY74FCT273TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9221503M2A	FK	LCCC	20	1	506.98	12.06	2030	NA
CY54FCT273ATLMB	FK	LCCC	20	1	506.98	12.06	2030	NA
CY74FCT273ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT273CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT273TSOC	DW	SOIC	20	25	507	12.83	5080	6.6

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated