

TXB0304 具有自动方向感应的 4 位双向电平转换器/电压转换器

1 特性

- 完全对称的电源电压，A 端口和 B 端口上均为 0.9V 到 3.6V
- V_{CC} 隔离特性 – 如果任一 V_{CC} 输入接地，则所有输出处于高阻态
- 以 V_{CCA} 为基准的输出使能 (OE) 输入电路
- 低功耗，最大 $5\mu\text{A}$ (I_{CCA} 或 I_{CCB})
- I_{off} 支持局部关断模式运行
- 闩锁性能超出 JESD 78 II 类规范要求的 100mA
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
 - 8000V 人体放电模式 (A114-A)
 - 1000V 充电器件模型 (C101)

2 应用

- 个人电子产品
- 工业
- 企业
- 电信

3 说明

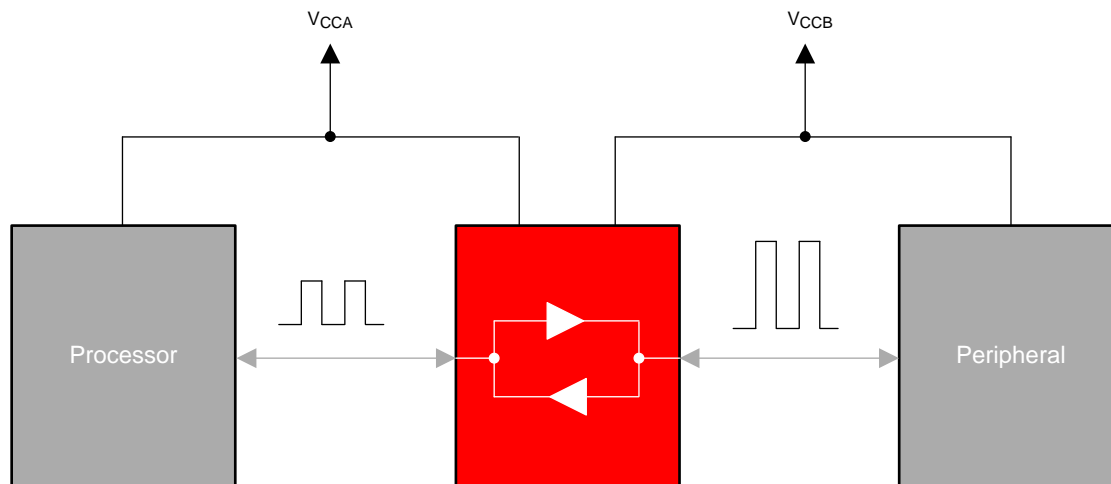
这个 4 位同相转换器使用两个独立的可配置电源轨。A 端口设计用于跟踪 V_{CCA} 。 V_{CCA} 可接受从 0.9V 到 3.6V 范围内的任意电源电压。B 端口设计用于跟踪 V_{CCB} 。 V_{CCB} 可接受 0.9V 到 3.6V 范围内的任意电源电压。这可以实现 1V、1.2V、1.5V、1.8V、2.5V 和 3V 电压节点之间的任意低压双向转换。对于 TXB0304，当输出使能 (OE) 输入为低时，所有输出均处于高阻态。为确保在上电或掉电期间均处于高阻态，应将 OE 通过下拉电阻连接至 GND；该电阻的最小值取决于驱动器的拉电流能力。OE 器件控制引脚输入电路由 V_{CCA} 供电。该器件完全适用于 I_{off} 为了部分断电的应用。 I_{off} 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。TXB0304 和 TXBN0304 唯一的区别在于 OE 信号分别为高电平有效和低电平有效。

器件信息⁽¹⁾

器件编号	封装	封装尺寸 (标称值)
TXB0304	RUT UQFN (12)	2.00mm x 1.70mm
	RSV UQFN (16)	2.60mm x 1.80mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

TCA9406 典型应用(TXB0304)



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (May 2016) to Revision G	Page
• Changed text in Power Supply Recommendations section.	13

Changes from Revision E (August 2014) to Revision F	Page
• 已更改 说明 部分	1
• 已更改 Absolute Maximum Ratings 、 Recommended Operating Conditions ⁽¹⁾⁽²⁾ 、 Switching Characteristics 和 Electrical Characteristics 表。	1

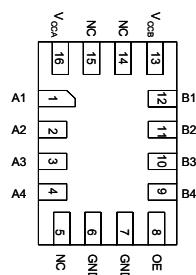
Changes from Revision D (October 2012) to Revision E	Page
• 已添加 添加了 ESD 额定值表、特性 说明部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。	1
• Changed VCCA and VCCB in the ABS MAX table to V _{CCA} and V _{CCB} in 3 places	4
• Changed in ELEC CHARAC table the 0.9 x V _{CCA} and 0.9 x V _{CCB} from MAX column into the MIN column	5
• Changed in ELEC CHARAC table 0.2 (2 places) in the MIN column to the MAX	5

Changes from Revision C (May 2012) to Revision D	Page
• Added Application Information section	12

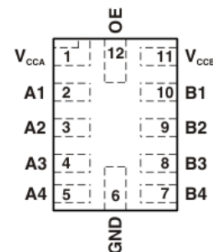
Changes from Revision B (September 2011) to Revision C	Page
• Added package pin out diagram notes	3

5 Pin Configuration and Functions

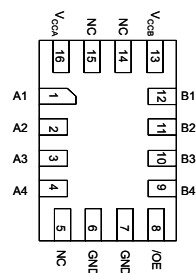
**RSV Package
16-Pin UQFN
TXB0304 Top View**



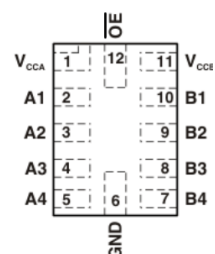
**RUT Package
12-Pin UQFN
TXB0304 Top View**



**RSV Package
16-Pin UQFN
TXBN0304 Top View**



**RUT Package
12-Pin UQFN
TXBN0304 Top View**



A. See [Layout Guidelines](#) for notes about package pin out diagrams.

Pin Functions

NAME	PIN		TYPE	DESCRIPTION			
	TXB0304	TXBN0304					
	RSV	RUT	RSV	RUT			
A1	1	2	1	2	I/O	Input/output 1	Referenced to V_{CCA}
A2	2	3	2	3	I/O	Input/output 2	
A3	3	4	3	4	I/O	Input/output 3	
A4	4	5	4	5	I/O	Input/output 4	
B1	12	10	12	10	I/O	Input/output 4	Referenced to V_{CCB}
B2	11	9	11	9	I/O	Input/output 3	
B3	10	8	10	8	I/O	Input/output 2	
B4	9	7	9	7	I/O	Input/output 1	
GND	6, 7	6	6,7	6	GND	Ground	
NC	5, 14, 15	—	5, 14, 15	—	—	No connection; not internally connected	
OE	8	12	—	—	I	3-state output-mode enable. Pull OE (TXB0304) low to place all outputs in 3-state mode. Referenced to V_{CCA} .	
\overline{OE}	—	—	8	12	I	3-state output-mode enable. Pull \overline{OE} (TXBN0304) high to place all outputs in 3-state mode. Referenced to V_{CCA} .	
V_{CCA}	16	1	16	1	—	A-port supply voltage $0.9\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$	
V_{CCB}	13	11	13	11	—	B-port supply voltage $0.9\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$	

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
V _{CCA}	Supply voltage		-0.5	4.6	V
V _{CCB}			-0.5	4.6	
V _I	Input voltage	A port	-0.5	4.6	V
		B port	-0.5	4.6	
V _O	Voltage applied to any output in the high-impedance or power-off state	A port	-0.5	4.6	V
		B port	-0.5	4.6	
V _O	Voltage applied to any output in the high or low state ⁽²⁾	A port	-0.5	V _{CCA} + 0.5	V
		B port	-0.5	V _{CCB} + 0.5	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CCA} , V _{CCB} , or GND			±100	mA
T _{stg}	Storage temperature		-65	150	°C
T _J	Junction temperature		-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾⁽²⁾

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				0.9	3.6	V
V _{CCB}							
V _{IH}	High-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	V _{CCI} × 0.65	V _{CCI}	V
		OE/ $\overline{\text{OE}}$	0.9 V to 3.6 V	0.9 V to 3.6 V	V _{CCA} × 0.65	3.6	
V _{IL}	Low-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	0	V _{CCI} × 0.35	V
		OE/ $\overline{\text{OE}}$	0.9 V to 1.2 V	0.9 V to 3.6 V	0	V _{CCA} × 0.3	
			1.2 V to 3.6 V	0.9 V to 3.6 V	0	V _{CCA} × 0.35	
V _O	Voltage range applied to any output in the high-impedance or power-off state	A-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	V
		B-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate	A-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	ns/V
		B-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	
T _A	Operating free-air temperature				-40	85	°C

- (1) The A and B sides of an unused data I/O pair must be held in the same state, such as, both at V_{CCI} or both at GND.
- (2) V_{CCI} is the supply voltage associated with the input port.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TXB0304		UNIT
		RUT (UQFN)	RSV (UQFN)	
		12 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	131.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.9	55.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.9	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}	High-level output voltage	$I_{OH} = -20 \mu A$	$T_A = 25^\circ C$	0.9 V to 3.6 V		$0.9 \times V_{CCA}$			V
V_{OLA}	Low-level output voltage	$I_{OL} = 20 \mu A$	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V				0.2	V
V_{OHB}	High-level output voltage	$I_{OH} = -20 \mu A$	$T_A = 25^\circ C$		0.9 V to 3.6 V	$0.9 \times V_{CCB}$			V
V_{OLB}	Low-level output voltage	$I_{OL} = 20 \mu A$	$-40^\circ C$ to $85^\circ C$		0.9 V to 3.6 V			0.2	V
I_I	OE	$V_I = V_{CCI}$ or GND	$T_A = 25^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			± 1	μA
			$-40^\circ C$ to $85^\circ C$					± 2	
I_{off}	A port	V_I or $V_O = 0$ to 3.6 V	$T_A = 25^\circ C$	0 V	0 V to 3.6 V			± 1	μA
	B port		$-40^\circ C$ to $85^\circ C$					± 2	
I_{OZ}		A or B port	OE = GND	$T_A = 25^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			
	$-40^\circ C$ to $85^\circ C$			± 2					
I_{CCA}		$V_I = V_{CCI}$ or GND, $I_O = 0$	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			5	μA
I_{CCB}		$V_I = V_{CCB}$ or GND, $I_O = 0$	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			5	μA
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			10	μA
I_{CCZA}	High-Z state supply current	$V_I = V_{CCI}$ or GND, $I_O = 0$, OE = GND	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			5	μA
I_{CCZB}	High-Z state supply current	$V_I = V_{CCB}$ or GND, $I_O = 0$, OE = GND	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			5	μA
C_i	OE	$T_A = 25^\circ C$		0.9 V to 3.6 V	0.9 V to 3.6 V			3	pF
C_{io}	A port	$T_A = 25^\circ C$, OE = GND		0.9 V to 3.6 V	0.9 V to 3.6 V			6.7	pF
	B port					6.7			

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	LOAD	V _{CCA}	V _{CCB}	MIN	MAX	UNIT
Data rate	C _L = 15 pF	0.9 to 3.6 V	0.9 to 3.6 V		50	Mbps
	C _L = 15 pF	1.2 to 3.6 V	1.2 to 3.6 V		100	Mbps
	C _L = 15 pF	1.8 to 3.6 V	1.8 to 3.6 V		140	Mbps
	C _L = 30 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	C _L = 30 pF	1.2 to 3.6 V	1.2 to 3.6 V		90	Mbps
	C _L = 30 pF	1.8 to 3.6 V	1.8 to 3.6 V		130	Mbps
	C _L = 50 pF	1.2 to 3.6 V	1.2 to 3.6 V		80	Mbps
	C _L = 50 pF	1.8 to 3.6 V	1.8 to 3.6 V		120	Mbps
	C _L = 100 pF	1.2 to 3.6 V	1.2 to 3.6 V		70	Mbps
C _L = 100 pF	1.8 to 3.6 V	1.8 to 3.6 V		100	Mbps	

6.7 Switching Characteristics

 over operating free-air temperature range (unless otherwise noted). (For parameter descriptions, see [Figure 2](#) and [Figure 3](#).)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V _{CCA}	V _{CCB}	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{pd}	A	B	C _L = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	A	B	C _L = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	A	B	C _L = 15	1.8-3.6	1.8-3.6		3.7	4.8	
	A	B	C _L = 30	0.9-3.6	0.9-3.6		19.5	34	
	A	B	C _L = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	A	B	C _L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	A	B	C _L = 50	1.2-3.6	1.2-3.6		8	12.3	
	A	B	C _L = 50	1.8-3.6	1.8-3.6		4	5.4	
	A	B	C _L = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	B	A	C _L = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	B	A	C _L = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	B	A	C _L = 15	1.8-3.6	1.8-3.6		3.7	5	
	B	A	C _L = 30	0.9-3.6	0.9-3.6		19.5	34	
	B	A	C _L = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	B	A	C _L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	B	A	C _L = 50	1.2-3.6	1.2-3.6		8	12.3	
	B	A	C _L = 50	1.8-3.6	1.8-3.6		4	5.4	
	B	A	C _L = 100	1.2-3.6	1.2-3.6		8.6	13.5	
t _{en}	OE	A	C _L = 15	0.9-3.6	0.9-3.6			262	ns
				1.2-3.6	1.2-3.6			64	
				1.8-3.6	1.8-3.6			37	
		B	C _L = 15	0.9-3.6	0.9-3.6			332	
				1.2-3.6	1.2-3.6			76	
				1.8-3.6	1.8-3.6			41	
t _{dis}	OE	A	C _L = 15	0.9-3.6	0.9-3.6			172	ns
		B	C _L = 15	0.9-3.6	0.9-3.6			169	ns
t _{FB} , t _{FB}	B-port rise and fall times		C _L = 15	0.9-3.6	0.9-3.6		2.95		ns
t _{SA} , t _{SA}	A-port rise and fall times		C _L = 15	0.9-3.6	0.9-3.6		3.1		ns
t _{SK(O)}	Channel-to-channel skew		C _L = 15	0.9-3.6	0.9-3.6			0.15	ns

 (1) T_A = 25°C

6.8 Operating Characteristics

C_{pd} - power dissipation capacitance measured at $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT	
C_{pdA}	A-port input, B-port output	$C_L = 0, f = 10 \text{ MHz}, t_r = t_f = 1 \text{ ns}, OE = V_{CCA}$ (outputs enabled)	34	pF	
	B-port input, A-port output		34		
C_{pdB}	A-port input, B-port output		34	pF	
	B-port input, A-port output		34		
C_{pdA}	A-port input, B-port output		$C_L = 0, f = 10 \text{ MHz}, t_r = t_f = 1 \text{ ns}, OE = \text{GND}$ (outputs disabled)	0.01	pF
	B-port input, A-port output			0.01	
C_{pdB}	A-port input, B-port output	0.01		pF	
	B-port input, A-port output	0.01			

(1) V_{CCA}, V_{CCB} 0.9 V to 3.6 V

6.9 Typical Characteristics

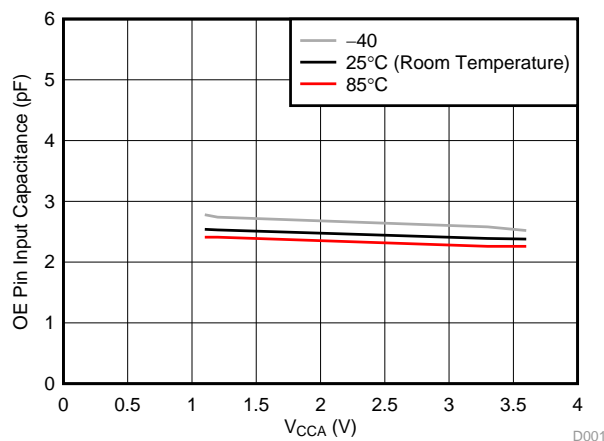
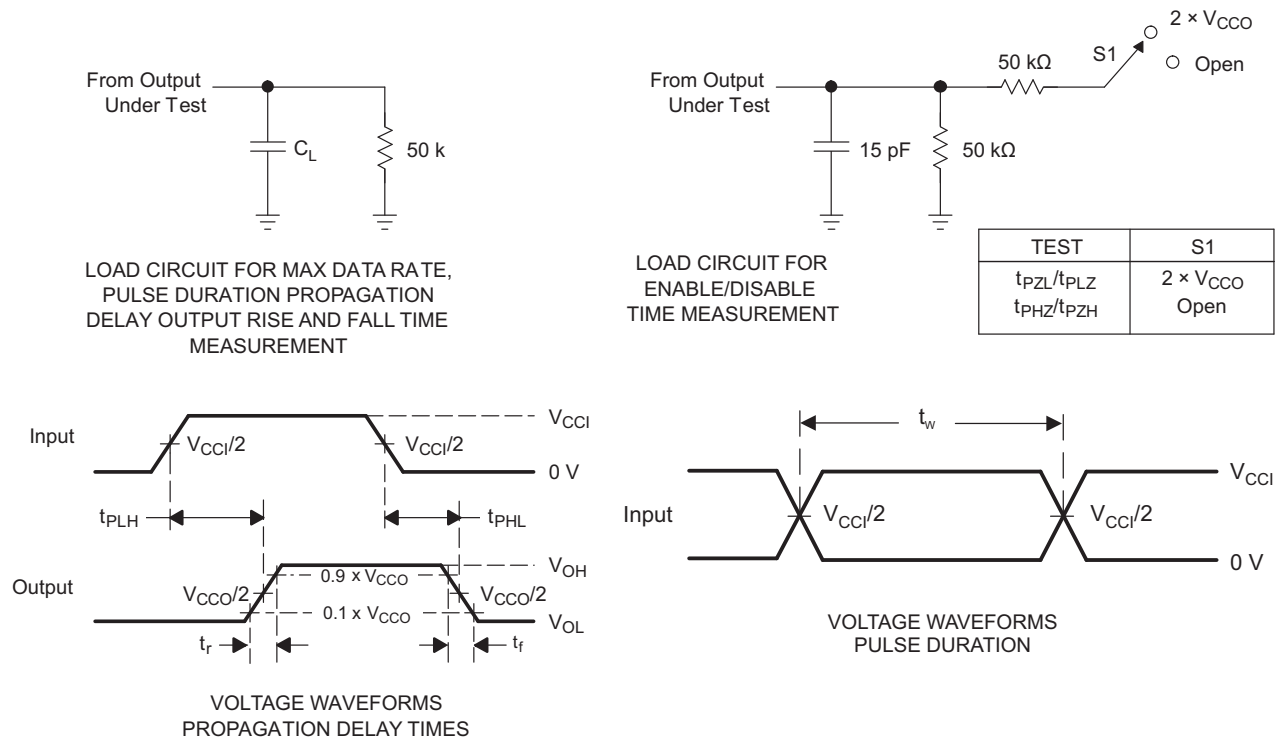


Figure 1. Input Capacitors for OE Pin (C_i) vs Power Supply (V_{CCA})

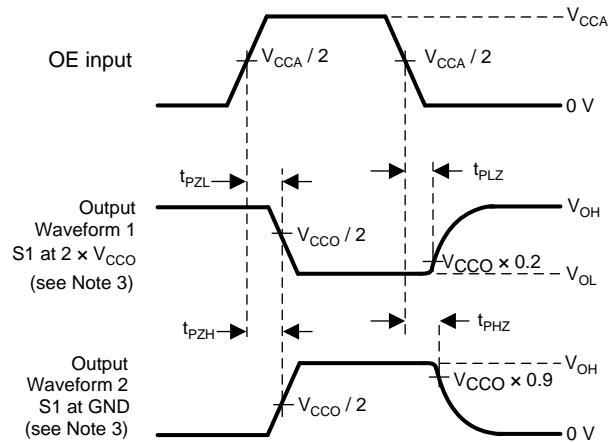
7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, $Z_0 = 50 \Omega$, $dv/dt \geq 1$ V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. V_{CCI} is the V_{CC} associated with the input port.
- F. V_{CCO} is the V_{CC} associated with output port.
- G. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuits and Voltage Waveforms

Parameter Measurement Information (continued)



- (1) t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- (2) t_{PZL} and t_{PZH} are the same as t_{en} .
- (3) Waveform 1 is for an output with internal such that the output is high, except when OE is high. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 3. Enable and Disable Times

8 Detailed Description

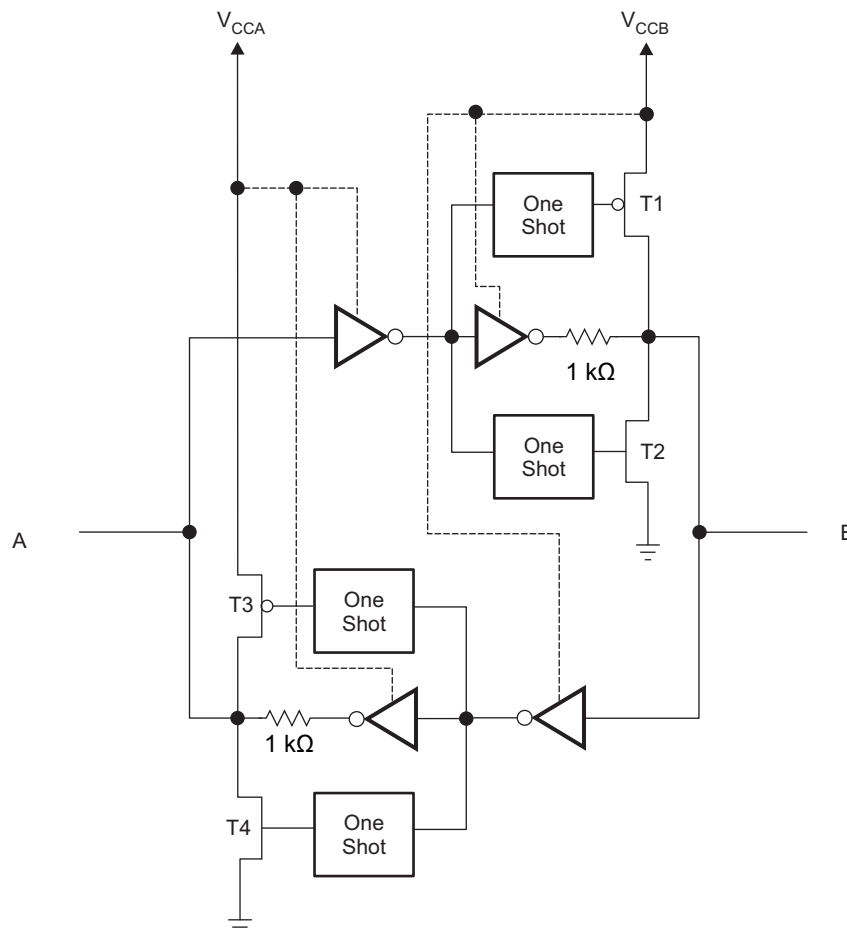
8.1 Overview

The TXB0304 and TXBN0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

8.1.1 Architecture

The TXB0304 and TXBN0304 architecture (see [Figure 4](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0304 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is $30\ \Omega$ at $V_{CC0} = 0.9\ \text{V}$ to $1\ \text{V}$, $10\ \Omega$ at $V_{CC0} = 1.1\ \text{V}$ to $1.7\ \text{V}$, and $5\ \Omega$ at $V_{CC0} = 1.8\ \text{V}$ to $3.3\ \text{V}$.

8.2 Functional Block Diagram



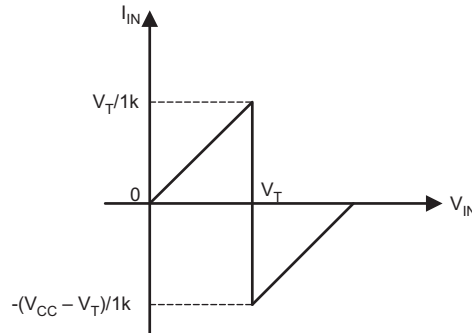
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Figure 4. Architecture of TXB0304 I/O Cell

8.3 Feature Description

8.3.1 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0304/TXBN0304 are shown in Figure 5. For proper operation, the device driving the data I/Os of the TXB0304 must have drive strength of at least ± 3 mA.



- (1) V_{CC} is power supply of TXB0304.
- (2) V_T is the input threshold voltage of TXB0304 (typically it is $V_{CC}/2$).

Figure 5. Typical I_{IN} vs V_{IN} Curve

8.4 Device Functional Modes

8.4.1 Enable and Disable

The TXB0304 has an OE input that is used to disable the device by setting OE = low (\overline{OE} = high for TXBN0304), which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is high.

8.4.2 Pullup or Pulldown Resistor on I/O Lines

The TXB0304/TXBN0304 is designed to drive capacitive loads of up to 100 pF. The output drivers of the TXB0304 have low dc drive strength. If pull-up or pull-down resistors are connected externally to the data I/Os, their values must be kept higher than 20 k Ω to ensure that they do not contend with the output drivers of the TXB0304. but if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the V_{OH} and V_{OL} .

$$V_{ol} = V_{CCout} \times \frac{1.5k\Omega}{1.5k\Omega + R_{pu}} \quad (1)$$

$$V_{oh} = V_{CCout} \times \frac{R_{pd}}{1.5k\Omega + R_{pd}}$$

where

- V_{CCOUT} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 1.5 k Ω is the counting the variation of the serial resistor 1k Ω in the I/O line. (2)

Because of this restriction on external resistors, the TXB0304 should not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI [TXS010X](#) series of level translators.

9 Application and Implementation

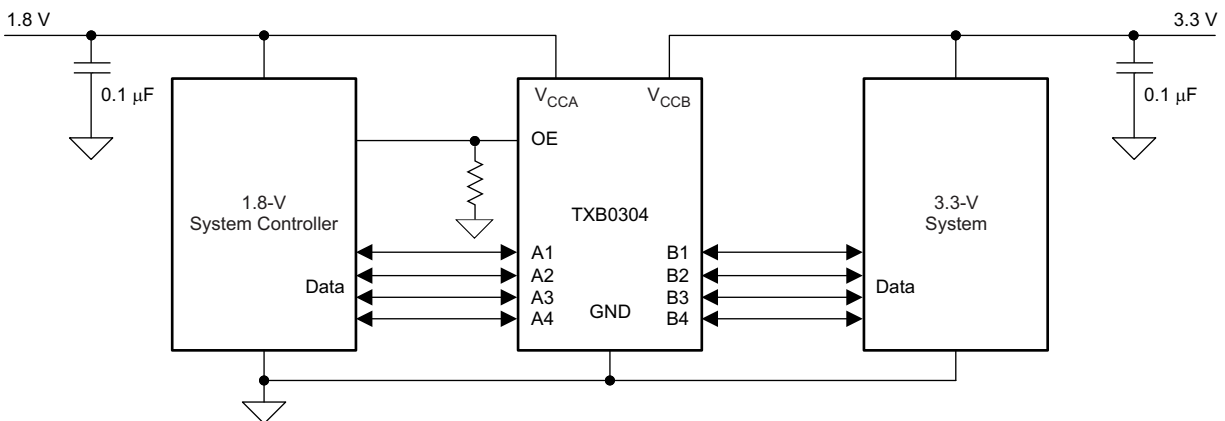
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI [TXS010X](#) products. Any external pull-down or pull-up resistors are recommended larger than 20 k Ω .

9.2 Typical Application



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Figure 6. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#).

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.9 V to 3.6 V
Output voltage range	0.9 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the TXB0304 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the TXB0304 device is driving to determine the output voltage range.
 - Don't recommend to have the external pull-up or pull-down resistors. If mandatory, it is recommended the value should be larger than 20 k Ω .

- An external pull-down or pull-up resistor decreases the output V_{OH} and V_{OL} . Use the below equations in section 8.5.2 to draft estimate the V_{OH} and V_{OL} as a result of an external pull-down and pull-up resistor.

9.2.3 Application Curve

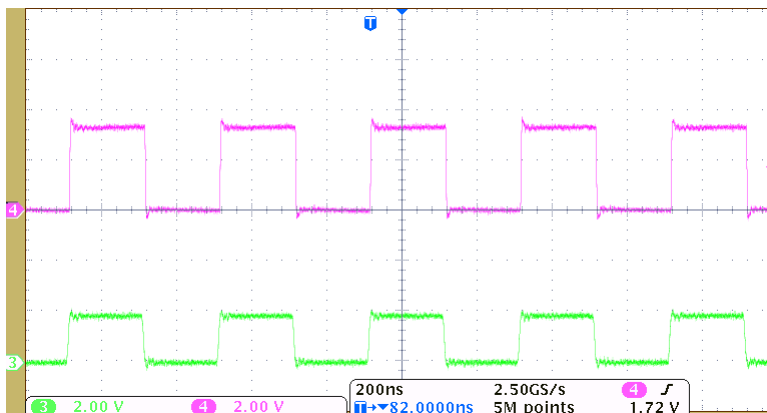


Figure 7. Level-Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

During operation, TXB0304 can work at both $V_{CCA} \leq V_{CCB}$ and $V_{CCA} \geq V_{CCB}$. During power-up sequencing, any power supply can be ramped up first. Both the supplies are recommended to be powered down together. The TXB0304 has circuitry that disables all input/output ports when either VCC is switched off ($V_{CCA/B} = 0$ V).

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the V_{CCA} , V_{CCB} pin and GND pin
- Short trace-lengths should be used to avoid excessive loading.
- For long transmission lines, place a series resistor equivalent to the impedance of the transmission lines to avoid signal integrity issues
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.
- Pullup resistors are not required on both sides for Logic I/O.
- If pullup or pulldown resistors are needed, the resistor value must be over 20 k Ω .
- 20 k Ω is a safe recommended value, if the customer can accept higher V_{ol} or lower V_{oh} , smaller pull up or pull down resistor is allowed, the draft estimation is $V_{ol} = V_{ccout} \times 1.5k / (1.5k + R_{pu})$ and $V_{oh} = V_{ccout} \times R_{pd} / (1.5k + R_{pd})$.
- If pullup resistors are needed, please refer to the TXS0104 or contact TI.
- For detailed information, refer to application note [SCEA043](#).

11.2 Layout Example

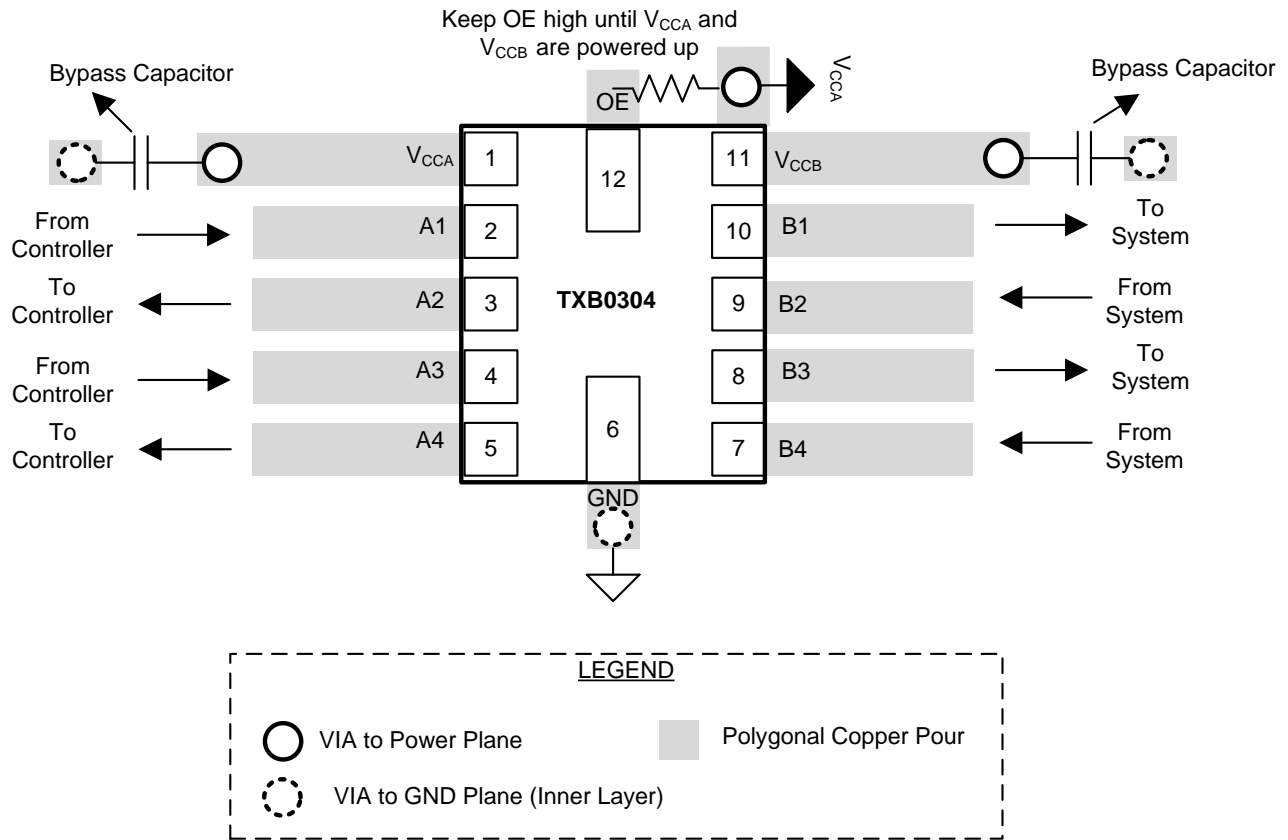


Figure 8. TXB0304 PCB Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

关于 TI TXS010X 产品, 请访问 www.ti.com.cn/product/cn/txs0101。

关于 TXB0304 IBIS 模型, 请参见 [SCEM544](#)。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档:

- 应用报告, 《使用 TXB 型转换器进行电压转换的相关指南》, [SCEA043](#)
- 用户指南, 《TXB0304 评估模块》, [SCEU003](#)

12.3 社区资源

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12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0304RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTJ	Samples
TXB0304RUTR	ACTIVE	UQFN	RUT	12	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(737, 73R, 73V)	Samples
TXBN0304RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTK	Samples
TXBN0304RUTR	ACTIVE	UQFN	RUT	12	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	74R	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

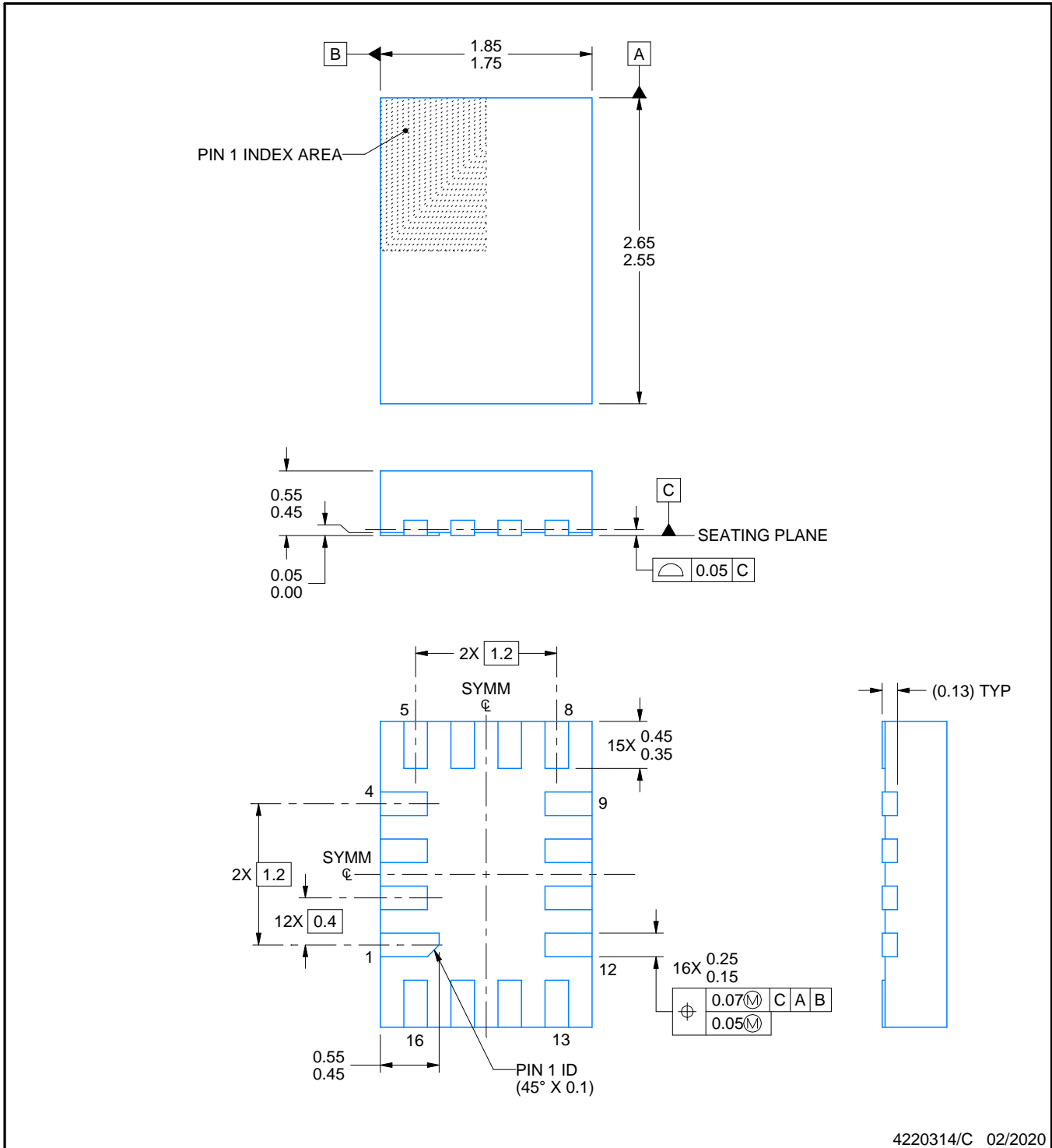
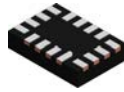

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXB0304RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	330.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXBN0304RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXB0304RUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
TXBN0304RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0
TXBN0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXBN0304RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0



4220314/C 02/2020

NOTES:

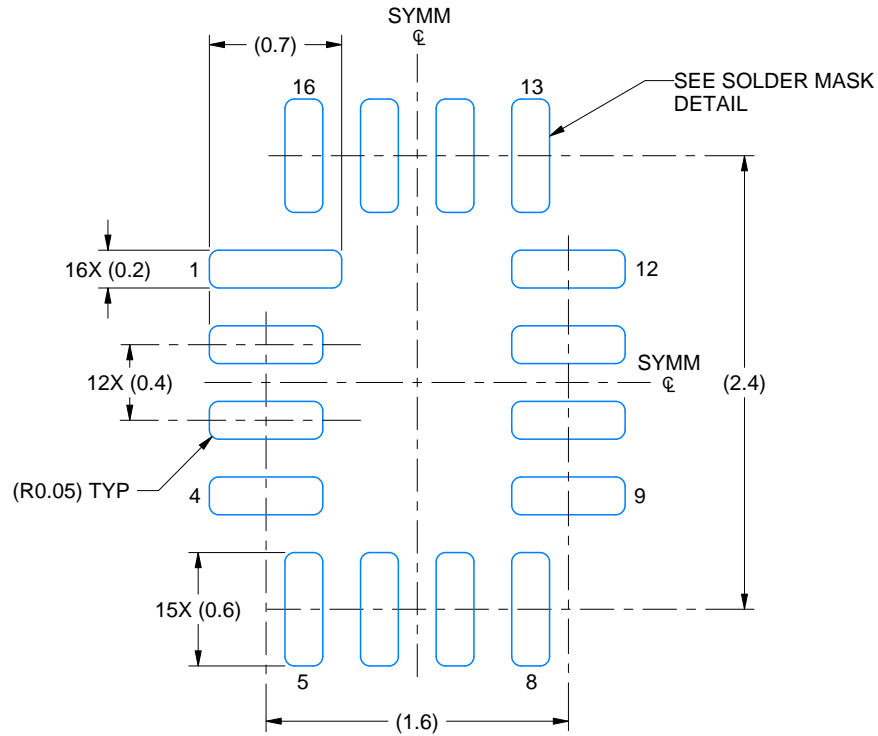
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

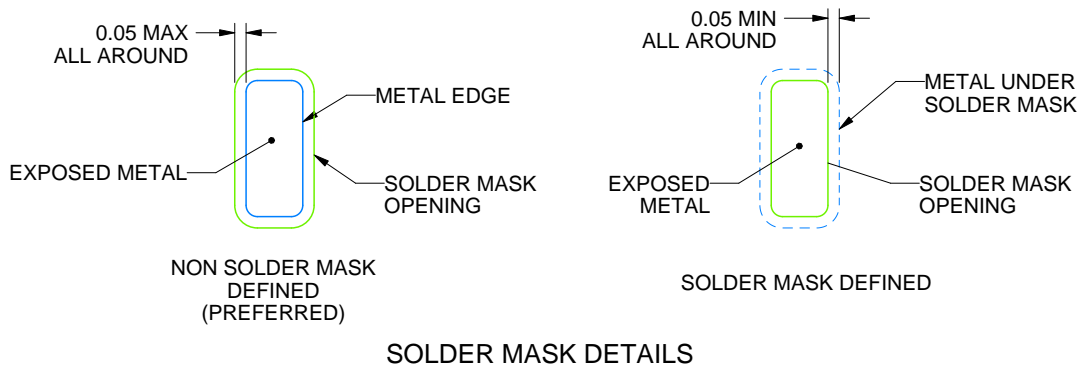
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4220314/C 02/2020

NOTES: (continued)

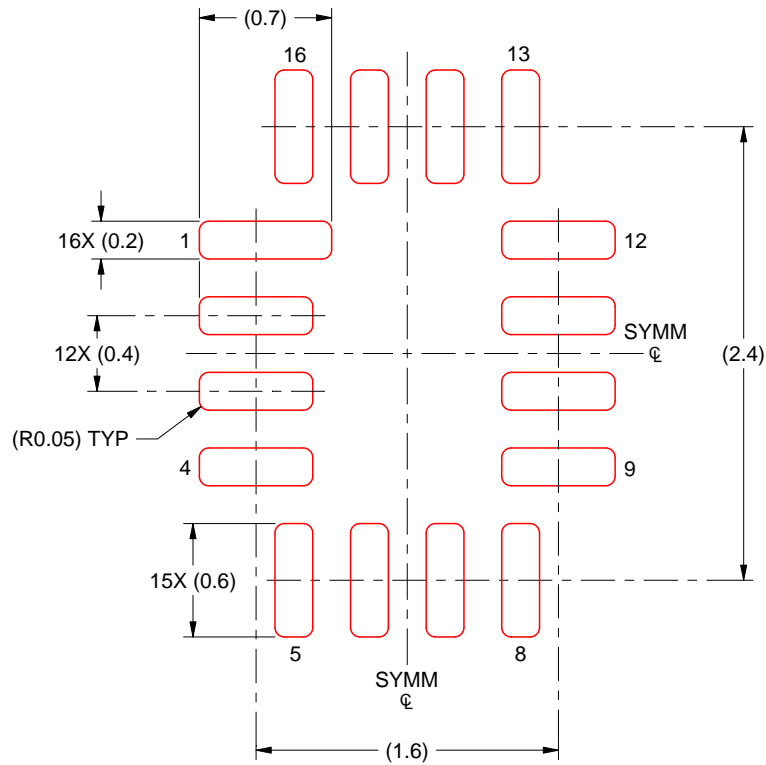
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

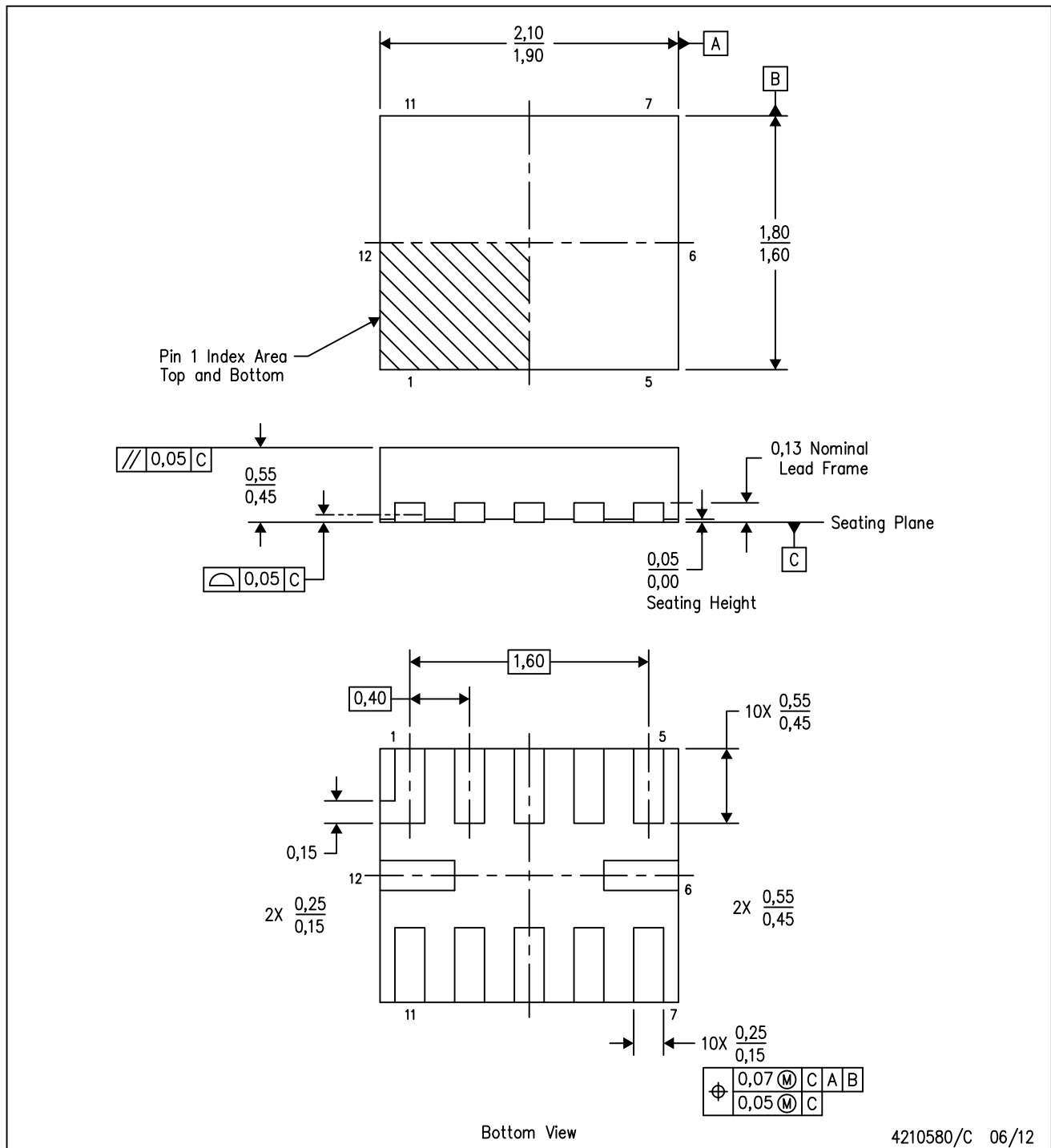
4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RUT (R-PUQFN-N12)

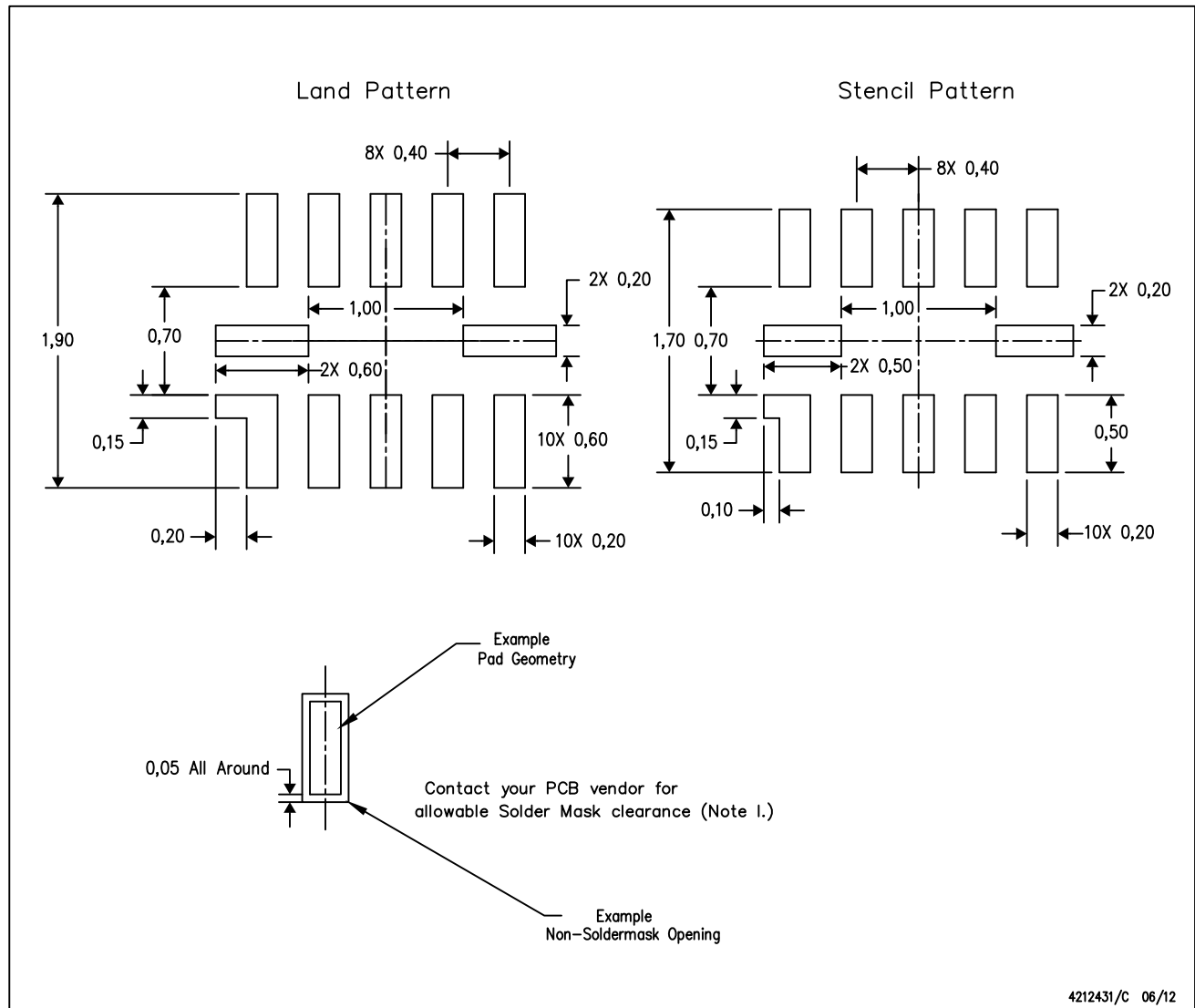
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.

RUT (R-PUQFN-N12)

PLASTIC QUAD FLATPACK NO-LEAD



4212431/C 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Over-printing land for larger area ratio is not advised due to land width and bridging potential. Exercise extreme caution.
 - H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - I. Component placement force should be minimized to prevent excessive paste block deformation.

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