LP2983 Micropower 150-mA Voltage Regulator in SOT-23 Package for Output Voltages ≤ 1.2 V*Designed for Use With Very Low-ESR Output Capacitors*

1 Features

- Operating Input Supply Voltage: 2.2 V to 16 V
- Output Current: 150 mA
- Low Z_{OUT}: 0.3 Ω Typical (10 Hz to 1 MHz)
- Stable with Low-ESR Output Capacitor
- Low Ground Pin Current at All Loads
- Output Voltage Accuracy 1% (A Grade)
- High Peak Current Capability
- Wide Supply Voltage Range (16 V Maximum)
- Overtemperature and Overcurrent Protection
- −40°C to +125°C Junction Temperature Range
- Requires Minimum External Components

2 Applications

- Cellular Phones
- Palmtop/Laptop Computers
- Personal Digital Assistants (PDA)
- Camcorders, Personal Stereos, Cameras

3 Description

The LP2983 is a 150-mA, fixed-output voltage regulator designed to provide tight voltage regulation in applications with output voltages ≤ 1.2 V.

Using an optimized vertically integrated PNP (VIP) process, the LP2983 delivers unequaled performance in all critical specifications:

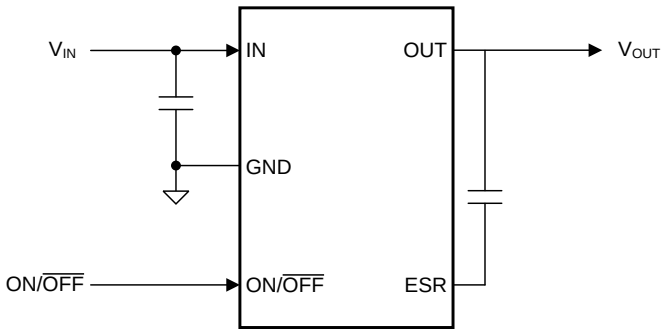
- Ground pin current: Typically 825 µA at a 150-mA load, and 75 µA at a 1-mA load.
- Enhanced stability: The LP2983 is stable with output capacitor ESR down to zero, which allows the use of ceramic capacitors on the output.
- Precision output: 1% tolerance output voltages available (A grade).
- Smallest possible size: SOT-23 package uses absolute minimum board space.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2983	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table and *Thermal Information* table with update thermal values, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; change pin names V_{OUT} and V_{IN} to OUT and IN ... 1
- Changed footnote 3 to Abs Max to replace out-of-date thetaJA temperature with general information ... 4
- Added *Thermal Information* table ... 4

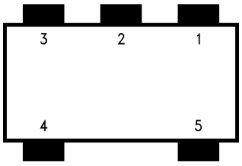
Changes from Revision B (April 2013) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format ... 11

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5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	IN	Input	Input voltage
2	GND	—	Common ground (device substrate)
3	ON/OFF	Input	Logic high enable input
4	ESR	—	Low side connection for low-ESR output capacitors
5	OUT	Output	Regulated output voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input supply voltage (survival)	−0.3	16	V
Input supply voltage (operating)	2.3	16	V
Shutdown input voltage (survival)	−0.3	16	V
Output voltage (survival)(2)	−0.3	9	V
I_{OUT} (survival)	Short-circuit protected		
Input-output voltage (survival)(3)	−0.3	16	V
Operating junction temperature	−40	125	°C
Power dissipation(4)	Internally limited		
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2983 output must be diode-clamped to ground.
(3) The output PNP structure contains a diode between the IN and OUT pins that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} turn on this diode (See *Reverse Input-Output Voltage*).
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using $P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$. The value of $R_{\theta JA}$ for the SOT-23 package varies depending on the application board — the value given in*Thermal Information* can be considered as the worstcase scenario. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator will go into thermal shutdown.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (all pins except pin 3)(1)	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (pin 3)(1)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating junction temperature	−40	125	°C
Input supply voltage (operating)	2.2	16	V

6.4 Thermal Information

THERMAL METRIC(1)		LP2983 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High-K(2)	169.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	121.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.

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6.5 Electrical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.

PARAMETER		TEST CONDITIONS	LP2981AI-XX(1)			LP2981I-XX(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_O	Output voltage tolerance		−1%		1%	−1.5%		1.5%	
		1 mA < I_L < 50 mA	–2%		2%	–2.5%		2.5	
		1 mA < I_L < 50 mA –40°C ≤ T_J ≤ 125°C	−2.5%		2.5%	−3.5%		3.5%	
		1 mA < I_L < 150 mA	−2.5%		2.5%	−3%		3%	
		1 mA < I_L < 150 mA –40°C ≤ T_J ≤ 125°C	−3.5%		3.5%	−4%		4%	
$\Delta V_O/\Delta V_{IN}$	Output voltage line regulation	$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V		0.01	0.016		0.01	0.016	%/V
		$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V –40°C ≤ T_J ≤ 125°C			0.032			0.032	
I_{GND}	Ground pin current	I_L = 0 mA		65	95		65	95	µA
		I_L = 0 mA, –40°C ≤ T_J ≤ 125°C			125			125	
		I_L = 1 mA		75	110		75	110	
		I_L = 1 mA, –40°C ≤ T_J ≤ 125°C			170			170	
		I_L = 10 mA		120	220		120	220	
		I_L = 10 mA, –40°C ≤ T_J ≤ 125°C			400			400	
		I_L = 50 mA		300	500		300	500	
		I_L = 50 mA, –40°C ≤ T_J ≤ 125°C			900			900	
		I_L = 150 mA		825	1200		825	1500	
		I_L = 150 mA, –40°C ≤ T_J ≤ 125°C			2000			2000	
		$V_{ON/\overline{OFF}}$ < 0.15 V		6	12		6	12	
		$V_{ON/\overline{OFF}}$ < 0.05 V –40°C ≤ T_J ≤ 125°C		0.2	2		0.2	2	
V_{IN} (min)	Minimum V_{IN} required to maintain output regulation			2.05					V
		–40°C ≤ T_J ≤ 125°C			2.2			2.2	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage(2)	High = O/P ON		1.4			1.4		V
		High = O/P ON –40°C ≤ T_J ≤ 125°C	1.6			1.6			
		Low = O/P OFF		0.1			0.1		
		Low = O/P OFF –40°C ≤ T_J ≤ 125°C			0.05			0.05	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}}$ = 0 V		0.01			0.01		µA
		$V_{ON/\overline{OFF}}$ = 0 V –40°C ≤ T_J ≤ 125°C			–2			–2	
		$V_{ON/\overline{OFF}}$ = 5 V		5			5		
		$V_{ON/\overline{OFF}}$ = 5 V –40°C ≤ T_J ≤ 125°C			15			15	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Average Outgoing Quality Level (AOQL).

(2) The ON/$\overline{OFF}$ inputs must be properly driven to prevent misoperation. For details, see *Operation With ON/$\overline{OFF}$ Control*.

Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.

PARAMETER		TEST CONDITIONS	LP2981AI-XX(1)			LP2981I-XX(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
e_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz V_{OUT} = 1.2 V, C_{OUT} = 10 µF		60			60		µV
$\Delta V_O/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, C_{OUT} = 2.2 µF		65			65		dB
$I_{O(MAX)}$	Short-circuit current	R_L = 0 Ω (steady state)(3)		400			400		mA
$I_{O(PK)}$	Peak output current	$V_{OUT} \geq V_{O(NOM)}$ − 5%		250			250		mA

(3) The LP2983 has foldback current limiting which allows a high peak current when V_{OUT} > 0.5 V, and then reduces the maximum output current as V_{OUT} is forced down to ground. See related curve(s) in *Typical Characteristics* section.

6.6 Typical Characteristics

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = V_{OUT}(NOM) + 1, T_A = 25°C, ON/OFF pin is tied to V_{IN}.

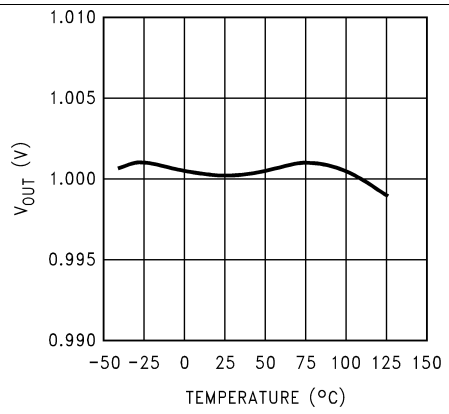


Figure 1. LP2983 Tempco

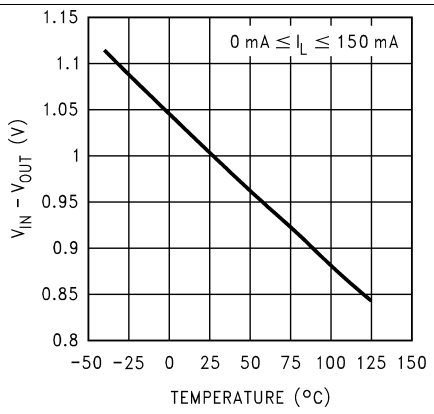
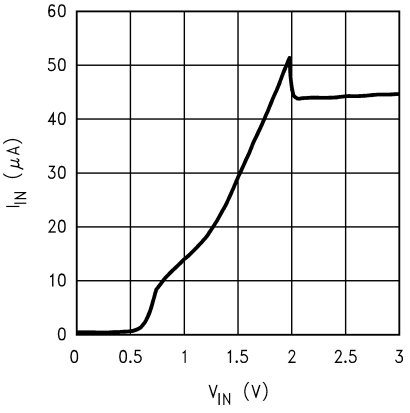
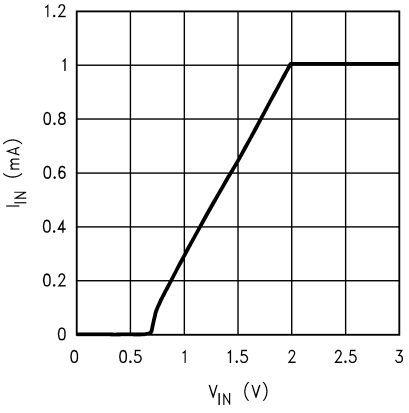


Figure 2. Minimum Input Voltage vs Temperature



Load = 0 mA

Figure 3. Input Current vs V_{IN}



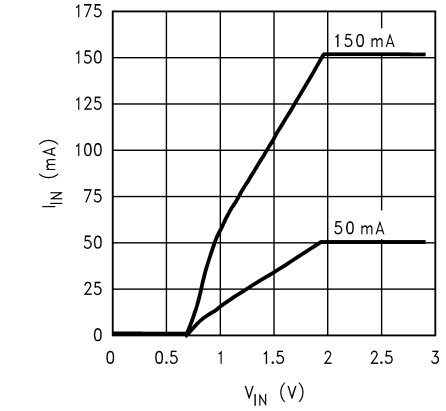
Load = 1 mA

Figure 4. Input Current vs V_{IN}

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Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = V_{OUT}(NOM) + 1, T_A = 25°C, ON/OFF pin is tied to V_{IN}.



Load = 50 mA and 150 mA

Figure 5. Input Current vs V_{IN}

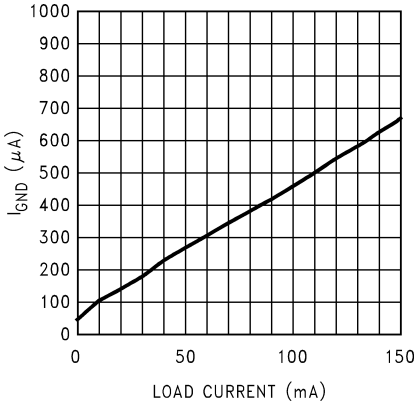


Figure 6. GND Pin vs Load Current

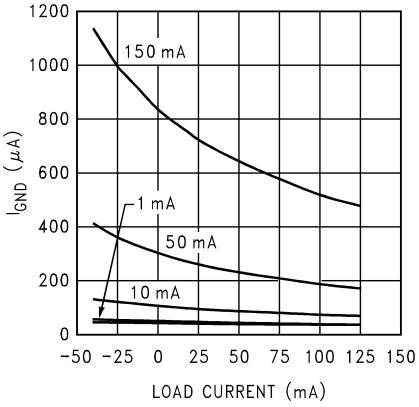
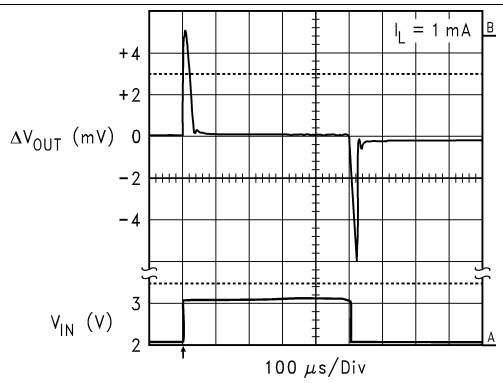
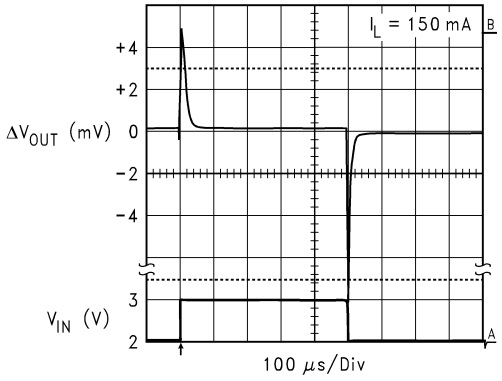


Figure 7. GND Pin vs Temperature and Load



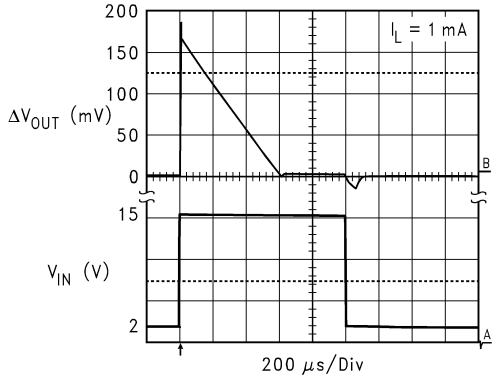
Load = 1 mA ΔV_{IN} = 1 V

Figure 8. Line Transient Response



Load = 150 mA ΔV_{IN} = 1 V

Figure 9. Line Transient Response

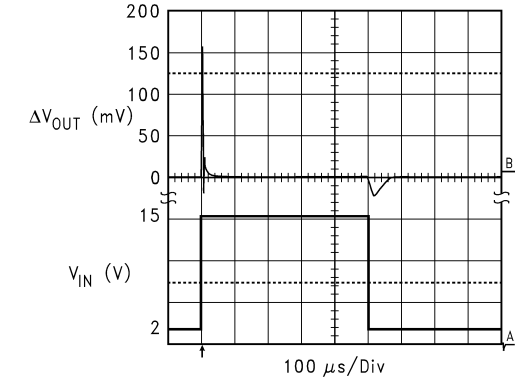


Load = 1 mA ΔV_{IN} = 13.8 V

Figure 10. Line Transient Response

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = V_{OUT}(NOM) + 1, T_A = 25°C, ON/OFF pin is tied to V_{IN}.



Load = 150 mA ΔVIN = 13.8 V

Figure 11. Line Transient Response

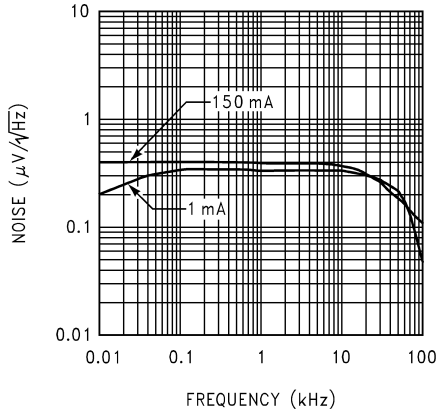
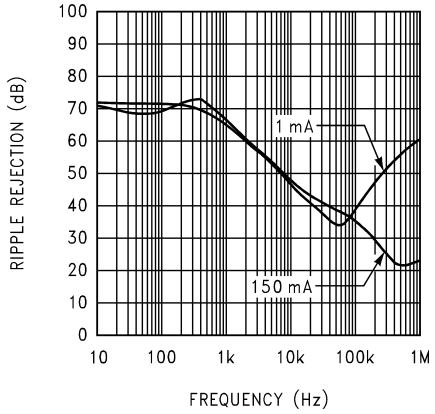


Figure 12. Noise Density



COUT = 2.2 µF

Figure 13. Ripple Rejection

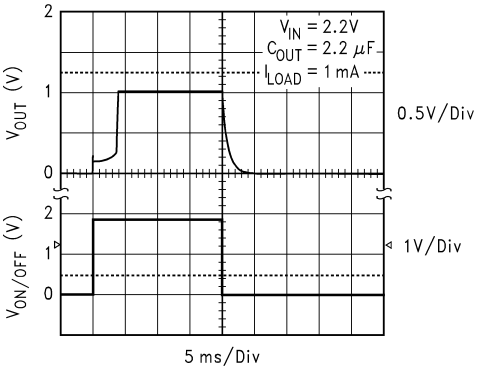


Figure 14. Turnon Time

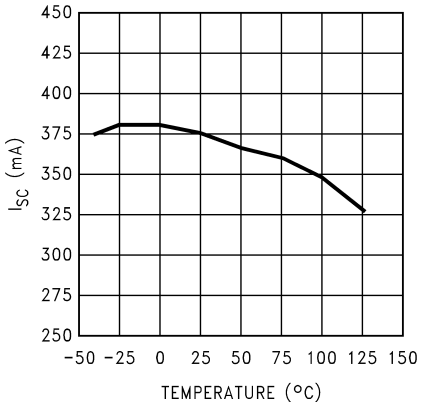
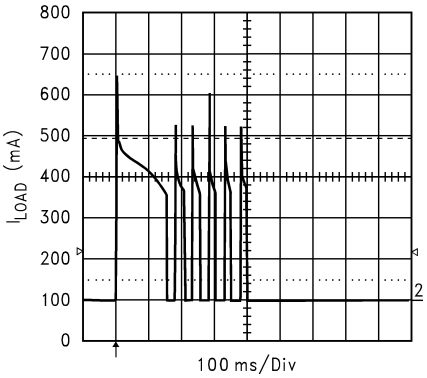


Figure 15. Short-Circuit Current vs Temperature



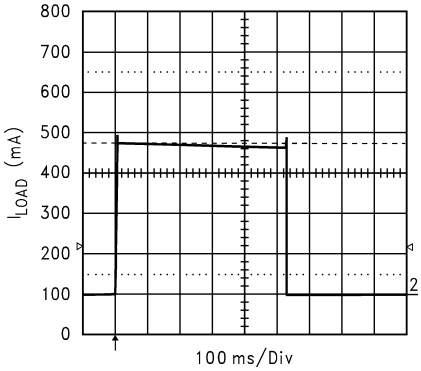
VIN = 16 V

Figure 16. Short-Circuit Current

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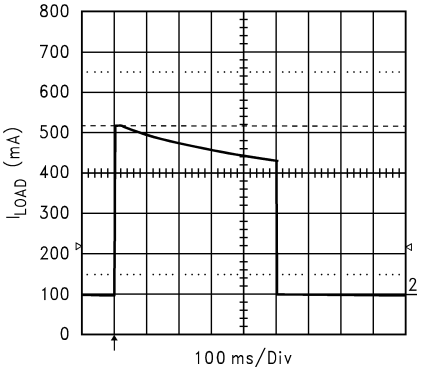
Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = V_{OUT}(NOM) + 1, T_A = 25°C, ON/OFF pin is tied to V_{IN}.



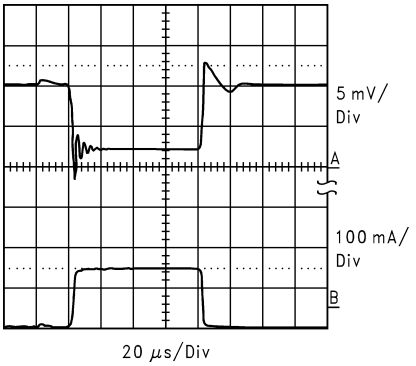
V_{IN} = 2.8 V

Figure 17. Short-Circuit Current



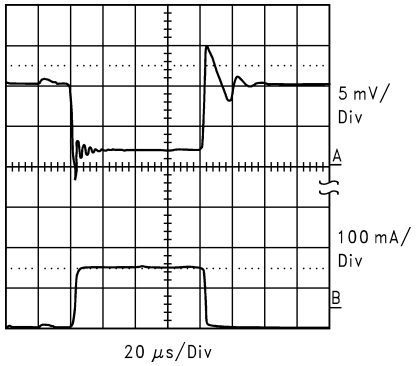
V_{IN} = 6 V

Figure 18. Short-Circuit Current



C_{OUT} = 4.7 µF

Figure 19. Load Transient Response



C_{OUT} = 2.2 µF

Figure 20. Load Transient Response

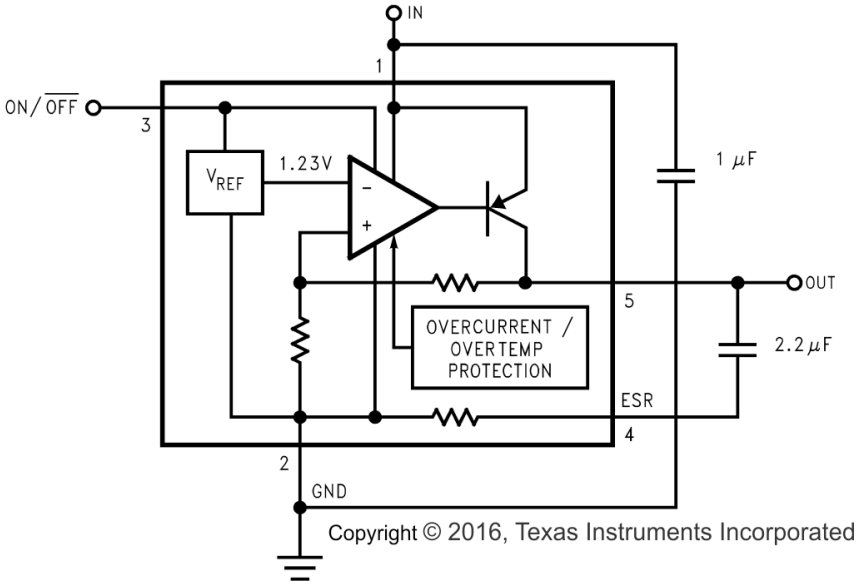
7 Detailed Description

7.1 Overview

The LP2983 is a voltage regulator with optimized vertically integrated PNP designed for use with very low ESR output capacitors, excellent for low noise applications that require a clean voltage supply. The LP2983 has a wide input voltage range (16 V maximum), high accuracy (A grade 1%), and a fixed output voltage supply capable of delivering 150 mA. In addition the LP2983 device provides the following features:

- High accuracy output voltage
- Low ground current, typically 825 µA at 150-mA load and 75 µA at 1-mA load
- A sleep mode feature is available, allowing the regulator to consume only 1 µA (typical) when the ON/$\overline{\text{OFF}}$ pin is pulled low.
- Overtemperature protection and overcurrent protection circuitry designed to safeguard the device during unexpected conditions.
- Thermal protection

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Accuracy Output Voltage

With special careful design to minimize all contributions to the output voltage error, the LP2983 distinguishes itself as a very high-accuracy output voltage micropower LDO. This includes a tight initial tolerance (typically 1.5% at 50 mA, 25°C junction temperature; also available in A grade with an accuracy of 1% under the same conditions), extremely good line regulation (0.01%/V typical), and a very low output-voltage temperature coefficient, making the part an ideal low-power voltage reference.

7.3.2 Low Ground Current

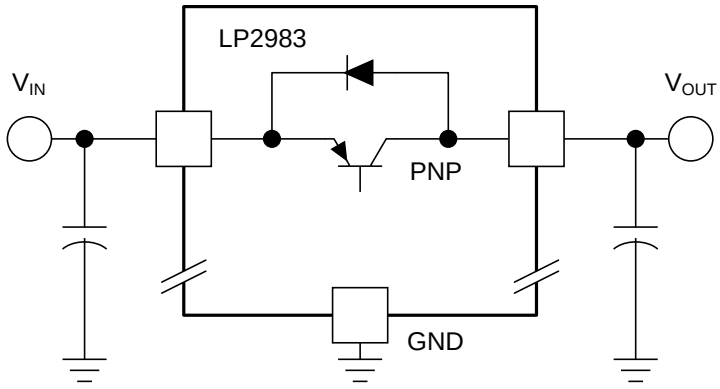
The LP2983 device uses a vertical PNP process which allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators, typically 825 µA at 150-mA load and 75 µA at 1-mA load.

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Feature Description (continued)

7.3.3 Reverse Input-Output Voltage

The internal PNP power transistor used as the pass element in the LP2983 has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse biased (See Figure 21).



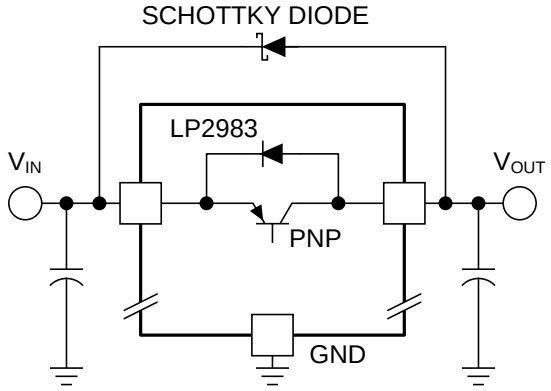
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Figure 21. LP2983 Reverse Current Path

However, if the input voltage is more than a V_{BE} below the output voltage, this diode turns ON and current flows into the regulator output. In such cases, a parasitic SCR can latch which allows a high current to flow into the V_{IN} pin and out the ground pin, which can damage the part.

The internal diode can also be turned on if the input voltage is abruptly stepped down to a voltage which is a V_{BE} below the output voltage.

In any application where the output voltage may be higher than the input voltage, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT} — see Figure 22), to limit the reverse voltage across the LP2983 to 0.3 V (see *Absolute Maximum Ratings*).



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Figure 22. Adding External Schottky Diode Protection

Feature Description (continued)

7.3.4 ON/OFF Input Operation

The LP2983 is shut off by driving the ON/OFF input low, and turned on by pulling it high. If this feature is not to be used, the ON/OFF input must be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in *Typical Characteristics* under $V_{ON/OFF}$. To prevent mis-operation, the turnon (and turnoff) voltage signals applied to the ON/OFF input must have a slew rate which is ≥ 40 mV/µs.

CAUTION

The regulator output voltage can not be ensured if a slow-moving AC (or DC) signal is applied that is in the range between the specified turn-on and turn-off voltages listed under the electrical specification $V_{ON/OFF}$ (see *Electrical Characteristics*).

7.3.5 Thermal Protection

The LP2983 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced. The internal protection circuitry of the LM2983 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

7.4 Device Functional Modes

7.4.1 Operation With $V_{O(NOM)}$ + 1 V ≤ V_{IN} < 16 V

The device operates if the input voltage is equal to, or exceeds, $V_{OUT(TARGET)}$ + 1 V. If the previous condition is not met, the device will not operate correctly, and the output voltage may not reach target value.

7.4.2 Operation With ON/$\overline{\text{OFF}}$ Control

If the voltage on the ON/$\overline{\text{OFF}}$ pin is less than 0.1 V at room temperature and less than 0.05 V over the full operating temperature range, the device output is disabled, and the shutdown current (I_{GND}) will not exceed 12 µA. Raising ON/$\overline{\text{OFF}}$ above 1.4 V at room temperature and above 1.6 V over the full operating temperature range initiates the start-up sequence of the device.

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8 Application and Implementation

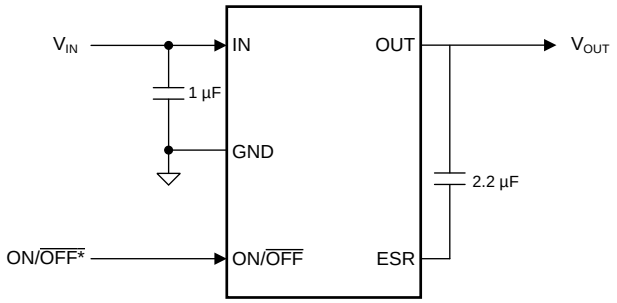
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2983 is a linear voltage regulator operating from 2.2 V to 16 V on the input and regulates voltages between ≤ 1.2 V with high accuracy and a 150-mA maximum output current. To achieve high efficiency, the dropout voltage (V_{IN} – V_{OUT}) must be as small as possible. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure performance.

8.2 Typical Application



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*ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not to be used.
**Minimum capacitance is shown to ensure stability (may be increased without limit). A ceramic capacitor is required for output (see *External Capacitors*).

Figure 23. LP2983 Typical Application

8.2.1 Design Requirements

For typical voltage regulator applications, use the parameters listed in Table 1:

Table 1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.2 V to 16 V
Output voltage	1V or 1.2 V
Output current	0 mA to 150 mA
Output tolerance (1 mA ≤ I_L ≤ 50 mA at 25°C)	±1.5% (±1% with A-grade version)

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, the LP2983 requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

8.2.2.1.1 Input Capacitor

An input capacitor whose capacitance is ≥ 1 µF is required between the LP2983 input and ground (the amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failure due to surge current when connected to a low-impedance source of power (like a battery or very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance is ≥ 1 µF over the entire operating temperature range.

8.2.2.1.2 Output Capacitors

The LP2983 is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 0 Ω.

The ceramic output capacitor must be connected between the OUT pin (device pin 5) and the ESR pin (device pin 4) (see Figure 24).

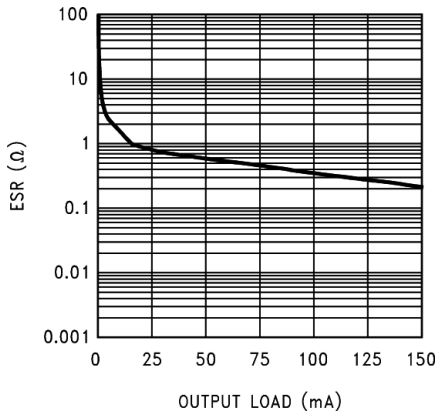


Figure 24. Ceramic to ESR Pin (C_{OUT} = 2.2 µF)

The LP2983 requires a minimum of 2.2 µF on the output (output capacitor size can be increased without limit).

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. Note that ceramic capacitors can exhibit large changes in capacitance with temperature (see *Capacitor Characteristics*).

The output capacitor must be located not more than 1 cm from the output pin and returned to a clean analog ground via the ESR pin.

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8.2.2.2 Capacitor Characteristics

The LP2983 was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 2.2-µF to 4.7-µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise).

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 2.2-µF capacitor were used on the output since it will drop down to approximately 1 µF at high ambient temperatures (which could cause the LP2983 to oscillate). If Z5U or Y5V capacitors are used on the output, a minimum capacitance value of 4.7 µF must be observed.

A better choice for temperature coefficient in ceramic capacitors is X7R, which holds the capacitance within ±15%. Unfortunately, the larger values of capacitance are not offered by all manufacturers in the X7R dielectric.

8.2.2.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the SOT-23 (DBV) package, the primary conduction path for heat is through the pins to the PCB. The maximum allowable junction temperature ($T_{J(MAX}$))determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 3:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_D = T_{J(MAX)} - T_{A(MAX)} / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

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8.2.2.4 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 3
- T_{TOP} is the temperature measured at the center-top of the device package. (4)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 3.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (5)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics* (SPRA953); for more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics* (SBVA025); and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017). These application notes are available at www.ti.com.

8.2.3 Application Curves

Unless otherwise specified, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/OFF pin is tied to VIN..

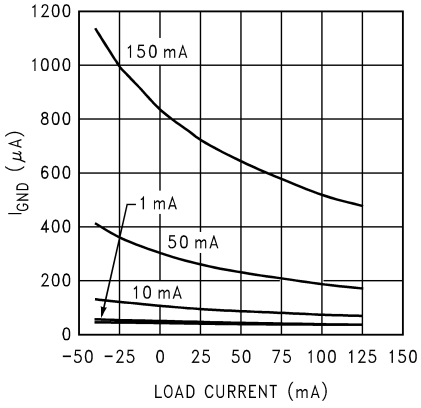


Figure 25. Line Transient Response

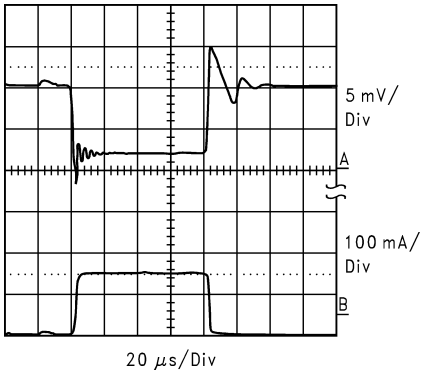


Figure 26. Load Transient Response

9 Power Supply Recommendations

The LP2983 is designed to operate from an input voltage supply range between 2.2 V and 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise and transient performance.

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10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. TI also recommends a ground reference plane, either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

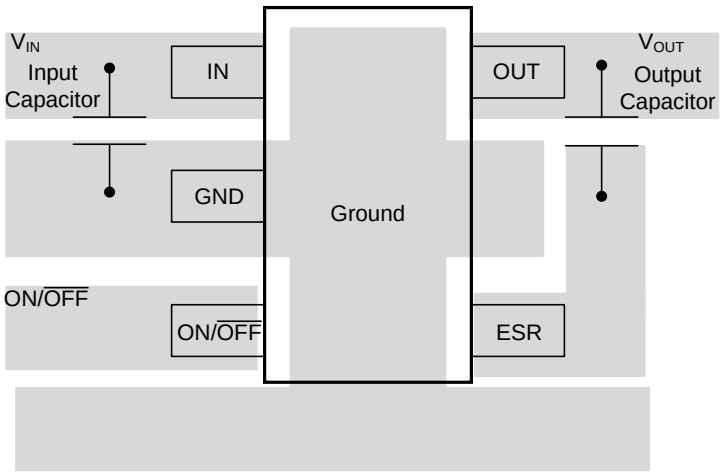


Figure 27. LP2983 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following:

- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Using New Thermal Metrics* (SBVA025)
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2983AIM5-1.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LENA	Samples
LP2983AIM5-1.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LELA	Samples
LP2983AIM5X-1.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LENA	Samples
LP2983AIM5X-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LELA	Samples
LP2983IM5-1.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LENB	Samples
LP2983IM5-1.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LELB	Samples
LP2983IM5X-1.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LENB	Samples
LP2983IM5X-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LELB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

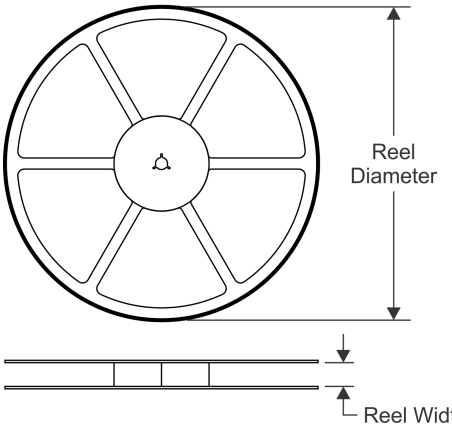
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

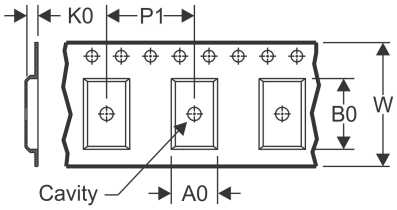
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

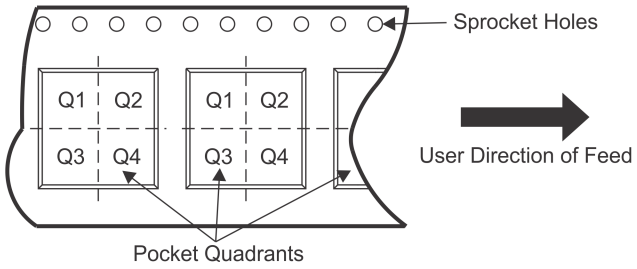


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

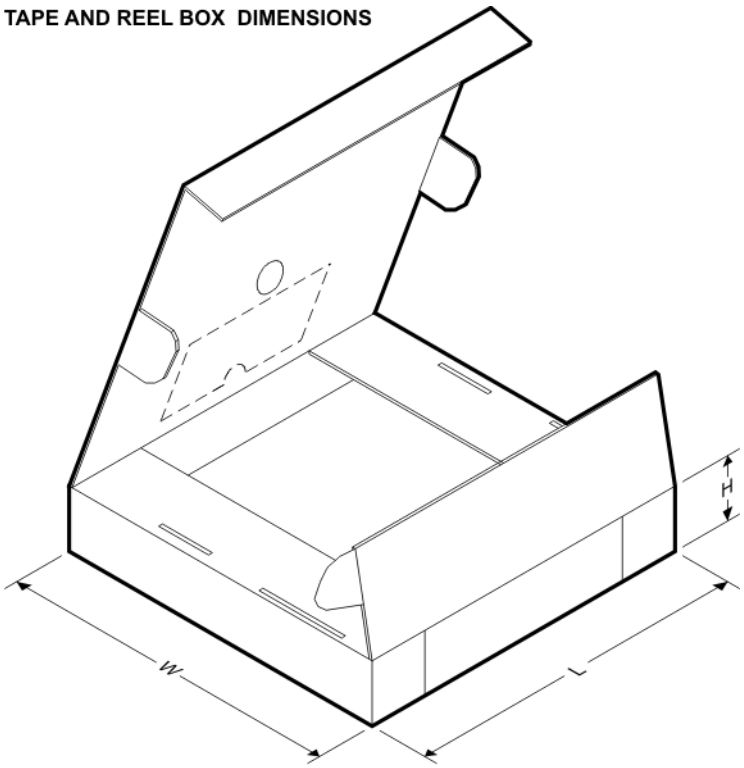
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2983AIM5-1.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2983AIM5-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2983AIM5X-1.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2983AIM5X-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2983IM5-1.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2983IM5-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2983IM5X-1.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2983IM5X-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

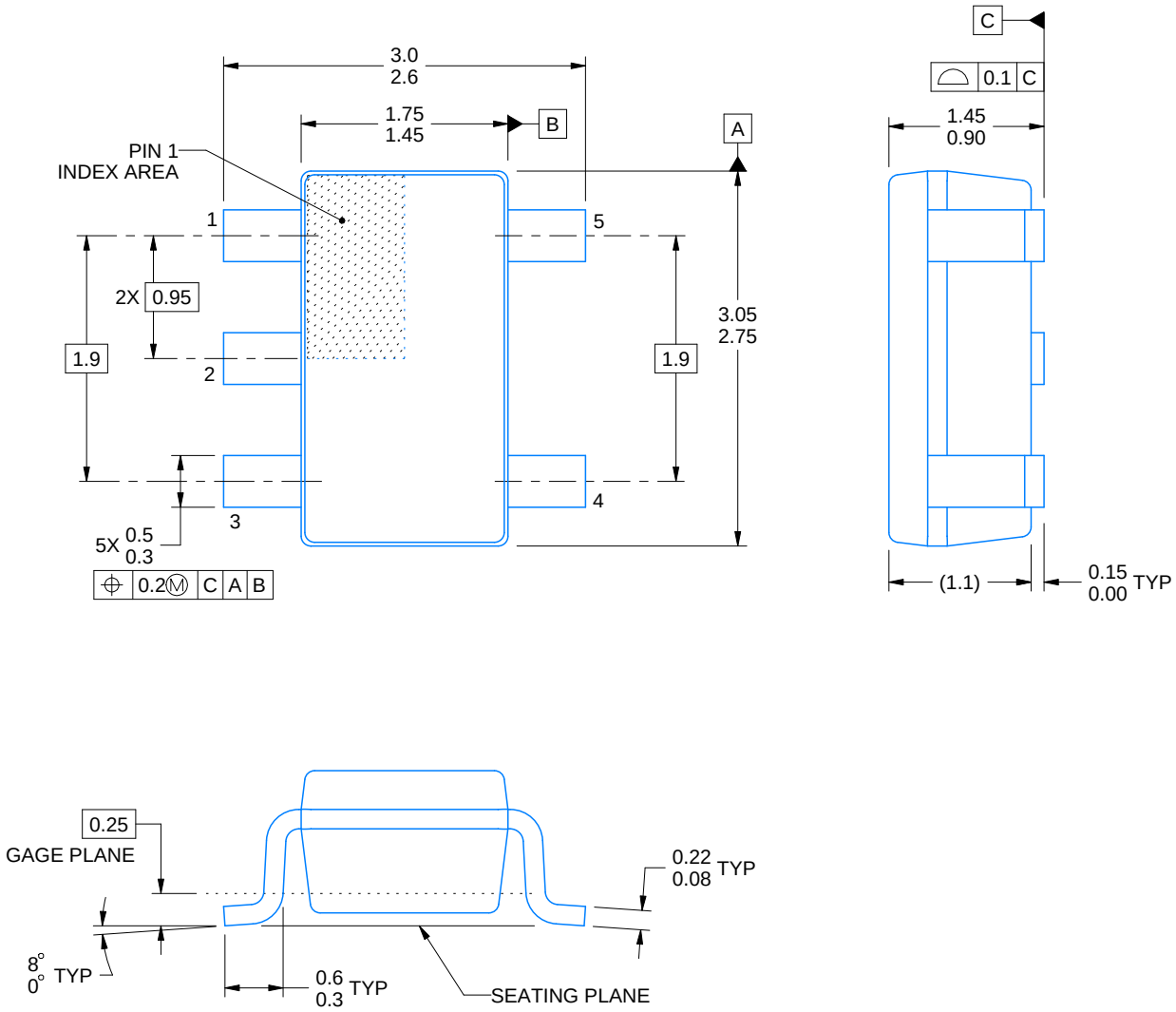
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2983AIM5-1.0/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2983AIM5-1.2/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2983AIM5X-1.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2983AIM5X-1.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2983IM5-1.0/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2983IM5-1.2/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2983IM5X-1.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2983IM5X-1.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

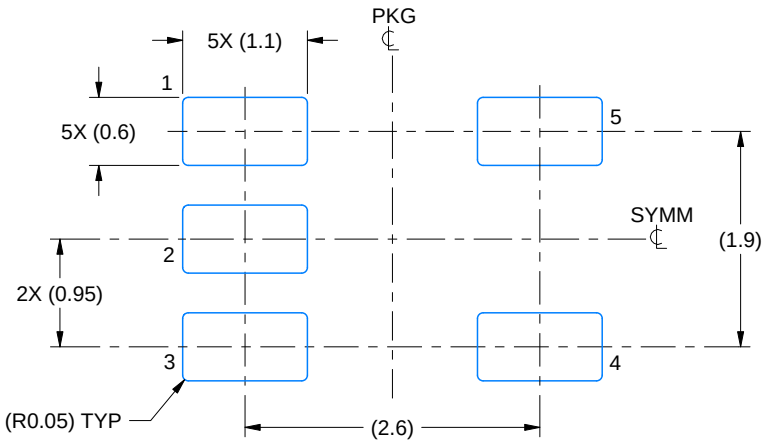
SMALL OUTLINE TRANSISTOR



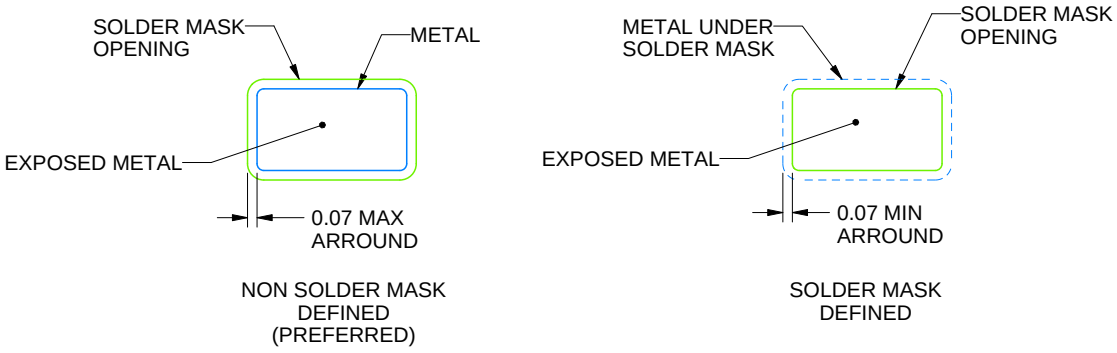
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

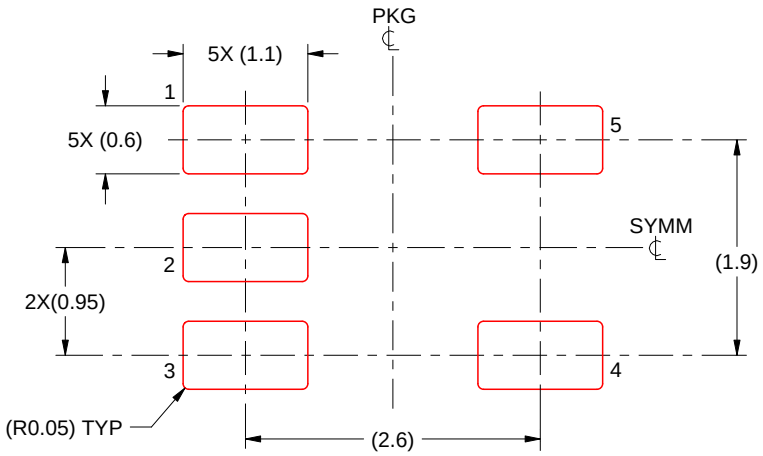


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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