TLV1702-Q1 2.2V 至 36V 微功耗比较器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体模型 (HBM) 分类等级 1C
  - 器件充电器器件模型 (CDM) 分类等级 C6
- 电源电压范围：2.2V 至 36V 或 ±1.1V 至 ±18V
- 低静态电流：每个比较器 55µA
- 输入共模范围包括两个电源轨
- 低传播延迟：560ns
- 低输入偏移电压：300µV
- 集电极开路输出：
  - 最多可高出负电源电压 36V 且不受电源电压影响
- 工业温度范围：-40°C 至 +125°C
- 小型封装：
  - 双列：超薄小外形尺寸 (VSSOP)-8

2 应用范围

- 过压和欠压检测器
- 窗口比较器
- 过流检测器
- 零交叉检测器
- 针对以下应用的系统监控：
  - 电源
  - 白色家电
  - 工业传感器
  - 汽车
  - 医疗

3 说明

TLV1702-Q1 器件可提供宽电源电压范围、轨到轨输入、低静态电流和低传播延迟。 凭借符合行业标准且在极小型封装内集成的上述特性，此类器件成为当前市场中的最佳通用比较器。

集电极开路输出具有能够将输出拉至任意电压轨（最多可高出负电源 36 V）且不受 TLV1702-Q1 电源电压影响的优势。

该器件是一款双通道微功耗比较器。 低输入偏移电压、低输入偏置电流、低电源电流和集电极开路配置使 TLV1702-Q1 器件能够灵活处理从简单电压检测到驱动单个继电器的多数应用。

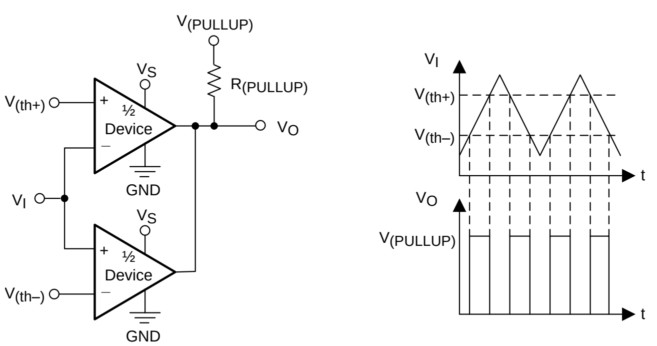
该器件在 –40°C 至 +125°C 的扩展级工业温度范围内额定运行。

器件信息[(1)]

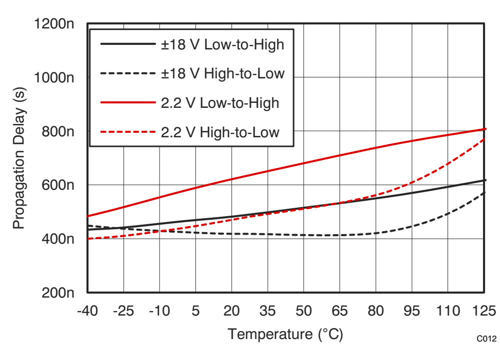
部件号	封装	封装尺寸（标称值）
TLV1702-Q1	超薄小外形尺寸封装 (VSSOP) (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

TLV1702-Q1 用作窗口比较器



稳定传播延迟与温度



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

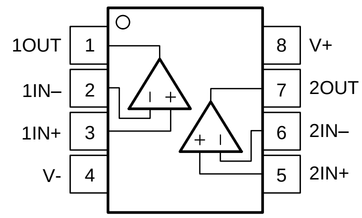
日期	修订版本	注释
2015 年 11 月	*	最初发布版本。

5 Related Products

DEVICE	FEATURES
TLC3702-Q1	Push-Pull, 20 µA, 20 mA drive
TLC3704-Q1	
TLV3012-Q1	Push-Pull, 5 µA, Integrated 1.242-V Reference
TLV3501-Q1	Push-Pull, 3.2 mA, 4.5-ns Propagation Delay
TLV3502-Q1	
TLV3701-Q1	Push-Pull, 560 nA, Reverse Battery to 16 V
TLV3702-Q1	
REF50xx-Q1	Series Reference, 0.1% Tolerance, 8 ppm/°C
TL4050xx-Q1	Shunt Reference, 0.1% Tolerance, 50 ppm/°C
TLVH431-Q1	Adjustable Shunt Reference 1.24 to 18 V

6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input, channel 1
2IN+	5	I	Noninverting input, channel 2
1IN–	2	I	Inverting input, channel 1
2IN–	6	I	Inverting input, channel 2
1OUT	1	O	Output, channel 1
2OUT	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage			40 (±20)	V
Signal input pins	Voltage(2)	$(V_S–) – 0.5$	$(V_S+) + 0.5$	V
	Current(2)		±10	mA
Output short-circuit(3)		Continuous		mA
Operating temperature		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground; one comparator per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage $V_S = (V_S+) – (V_S–)$	2.2 (±1.1)		36 (±18)	V
Specified temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV1702-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	199	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	89.5	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	120.4	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	22	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	118.7	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = 2.2 V to 36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C, V_S = 2.2 V		±0.5	±3.5	mV
		T_A = 25°C, V_S = 36 V		±0.3	±2.5	mV
		T_A = –40°C to +125°C			±5.5	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±4	±20	µV/°C
PSRR	Power-supply rejection ratio	T_A = 25°C		15	100	µV/V
		T_A = –40°C to +125°C		20		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C	(V–)		(V+)	V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		5	15	nA
		T_A = –40°C to +125°C			20	nA
I_{OS}	Input offset current			0.5		nA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			
OUTPUT						
V_O	Voltage output swing from rail	I_O ≤ 4 mA, input overdrive = 100 mV, V_S = 36 V			900	mV
		I_O = 0 mA, input overdrive = 100 mV, V_S = 36 V			600	mV
I_{SC}	Short circuit sink current			20		mA
	Output leakage current	V_{IN+} > V_{IN-}		70		nA
POWER SUPPLY						
V_S	Specified voltage range		2.2		36	V
I_Q	Quiescent current (per channel)	I_O = 0 A		55	75	µA
		I_O = 0 A, T_A = –40°C to +125°C			100	µA

7.6 Switching Characteristics

at T_A = 25°C, V_S = +2.2 V to +36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL}	Propagation delay time, high-to-low	Input overdrive = 100 mV		460		ns
t_{pLH}	Propagation delay time, low-to-high	Input overdrive = 100 mV		560		ns
t_R	Rise time	Input overdrive = 100 mV		365		ns
t_F	Fall time	Input overdrive = 100 mV		240		ns

7.7 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)

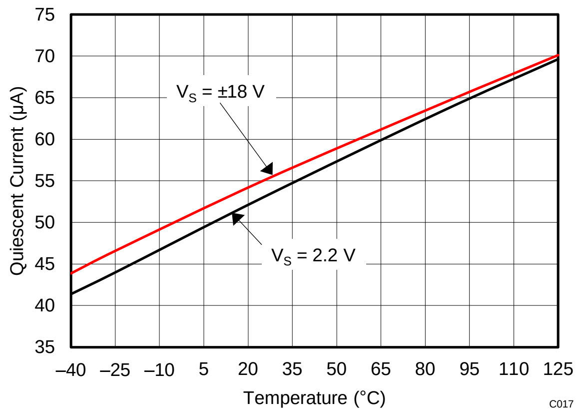


Figure 1. Quiescent Current vs Temperature

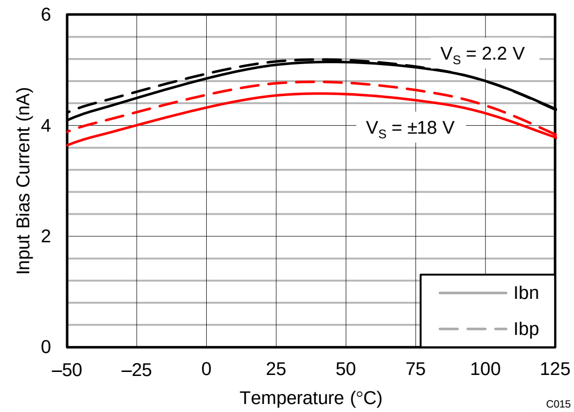


Figure 2. Input Bias Current vs Temperature

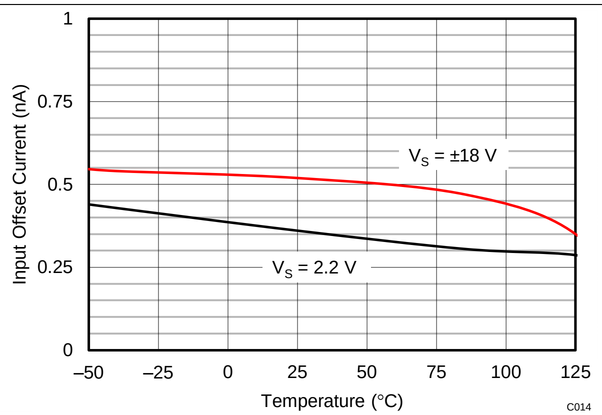


Figure 3. Input Offset Current vs Temperature

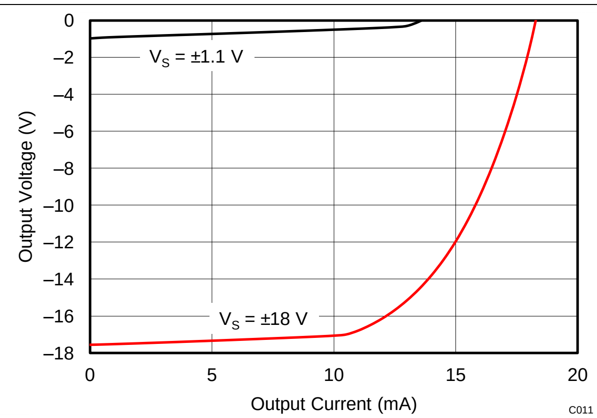


Figure 4. Output Voltage vs Output Current

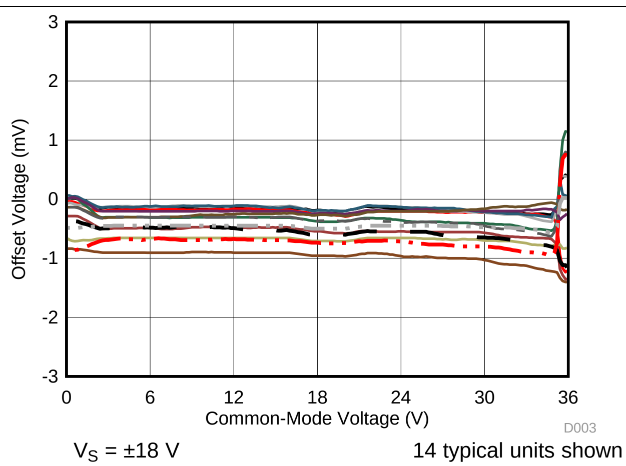


Figure 5. Offset Voltage vs Common-Mode Voltage

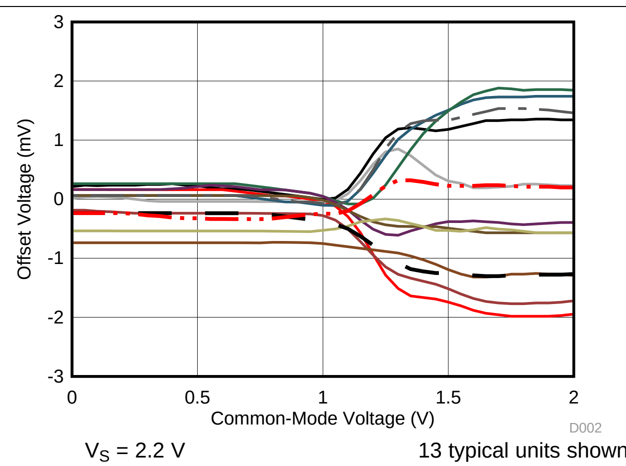
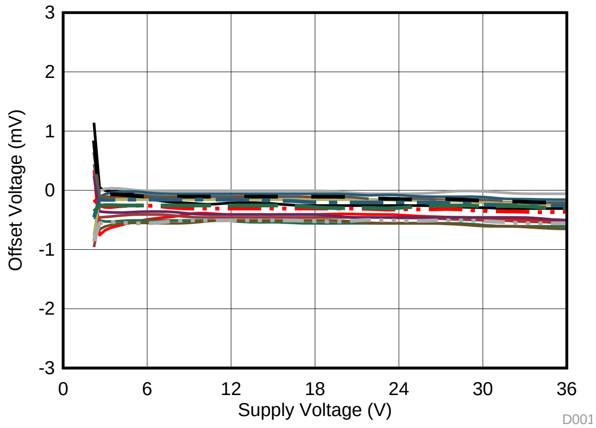


Figure 6. Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)



16 typical units shown

Figure 7. Offset Voltage vs Supply Voltage

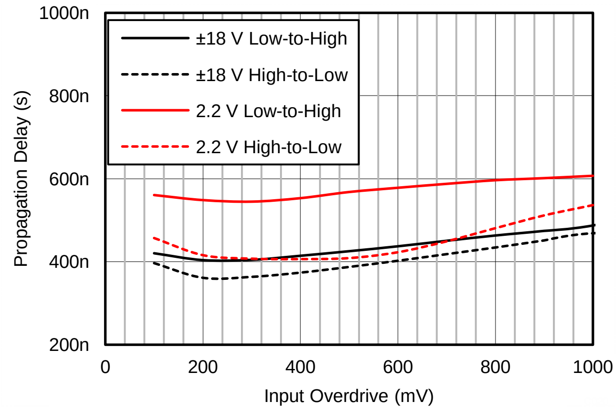


Figure 8. Propagation Delay vs Input Overdrive

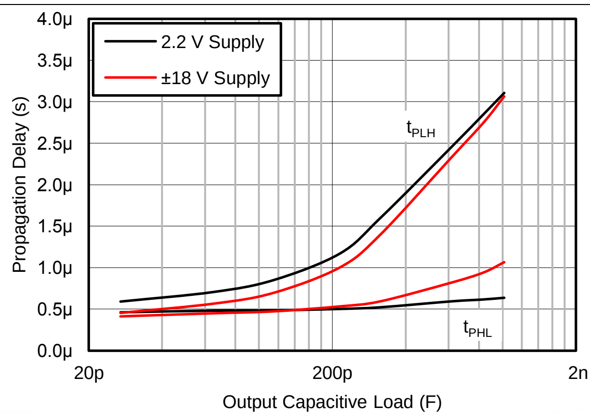
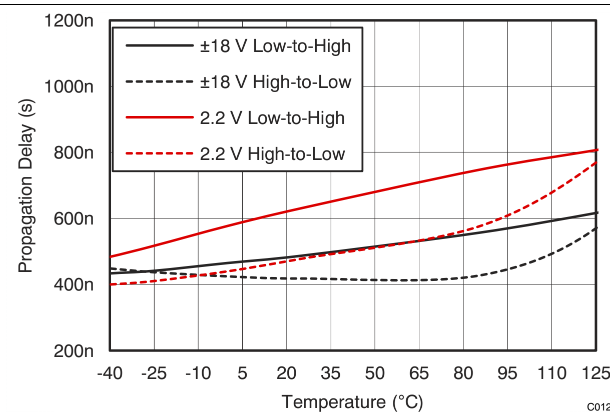
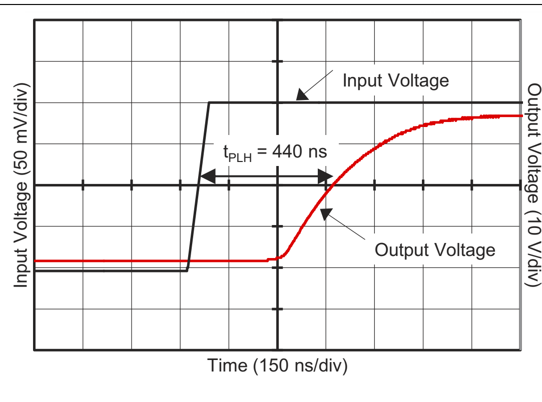


Figure 9. Propagation Delay vs Capacitive Load



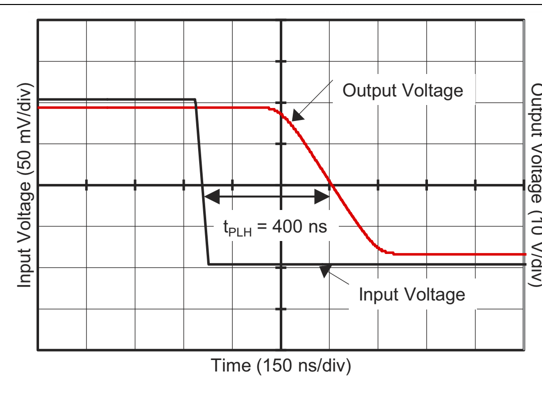
V_{OD} = 100 mV

Figure 10. Propagation Delay vs Temperature



V_S = 36 V Overdrive = 100 mV

Figure 11. Propagation Delay (T_{pLH})

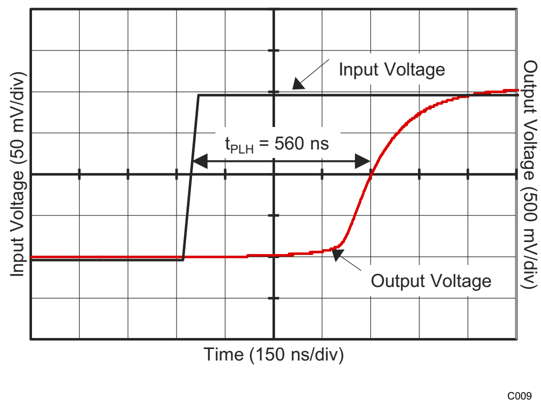


V_S = 36 V Overdrive = 100 mV

Figure 12. Propagation Delay (T_{pHL})

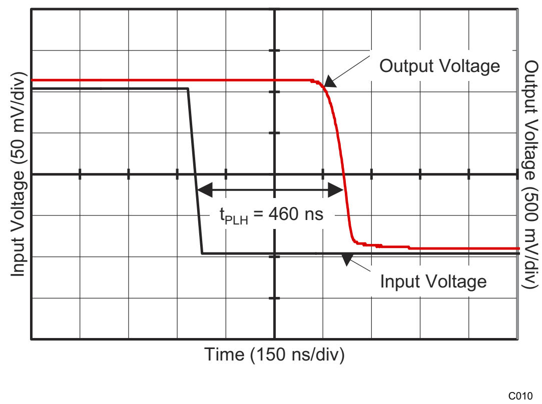
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)



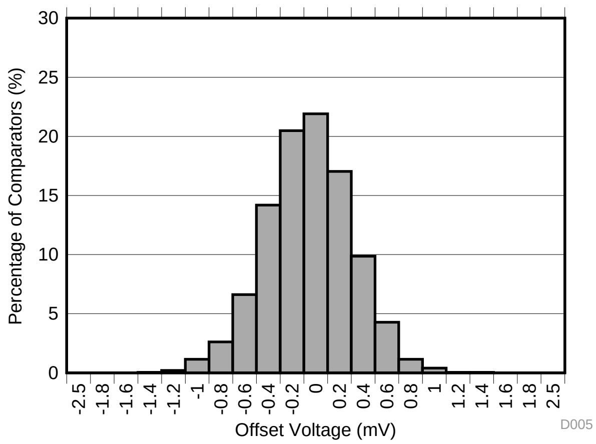
V_S = 2.2 V Overdrive = 100 mV

Figure 13. Propagation Delay (T_{pLH})



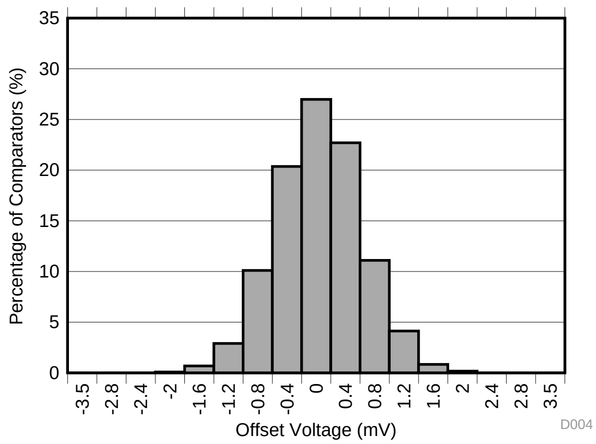
V_S = 2.2 V Overdrive = 100 mV

Figure 14. Propagation Delay (T_{pHL})



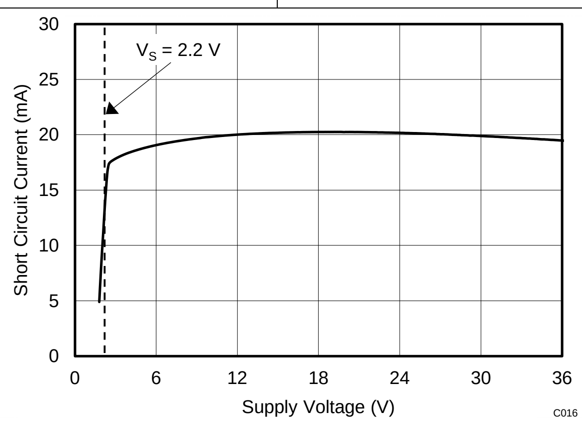
V_S = ±18 V Distribution taken from 2524 comparators

Figure 15. Offset Voltage Production Distribution



V_S = 2.2 V Distribution taken from 2524 comparators

Figure 16. Offset Voltage Production Distribution



Sink current

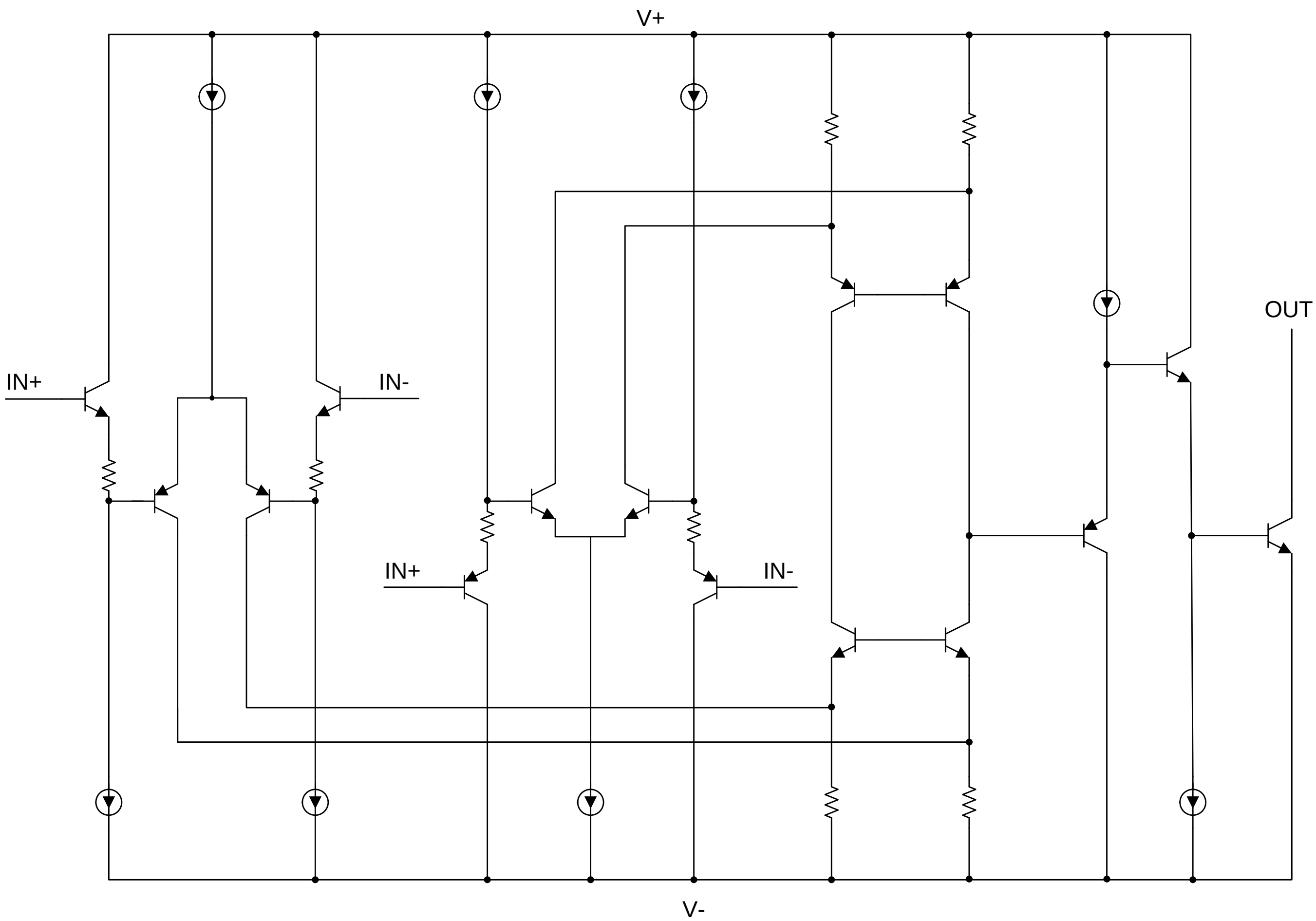
Figure 17. Short-Circuit Current vs Supply Voltage

8 Detailed Description

8.1 Overview

The TLV1702-Q1 comparator features rail-to-rail input and output on supply voltages as high as 36 V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55 µA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Comparator Inputs

The TLV1702-Q1 device is a rail-to-rail input comparator, with an input common-mode range that includes the supply rails. The TLV1702-Q1 device is designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 18 shows the TLV1702-Q1 device response when input voltages exceed the supply, resulting in no phase inversion.

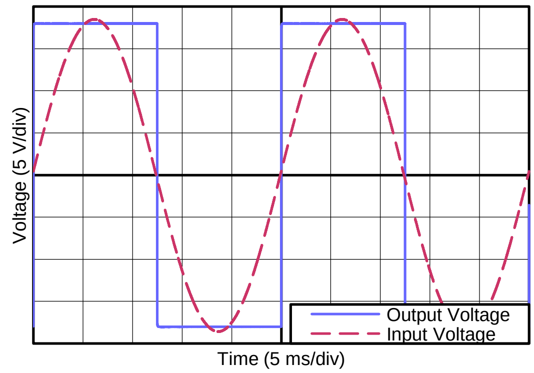


Figure 18. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

8.4 Device Functional Modes

8.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV1702-Q1 device. The REF3333, as shown in Figure 19, provides a 3.3-V reference voltage with low drift and only 3.9 µA of quiescent current.

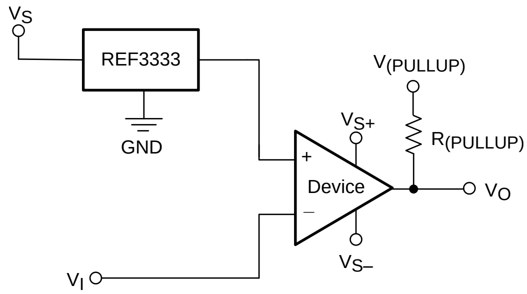


Figure 19. Reference Voltage for the TLV1702-Q1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV1702-Q1 device can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

9.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

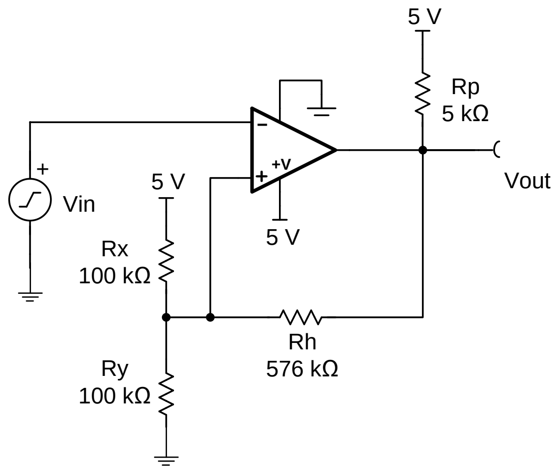


Figure 20. Comparator Schematic with Hysteresis

9.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V
- Input: 0 V to 5 V
- Lower threshold (VL) = 2.3 V ±0.1 V
- Upper threshold (VH) = 2.7 V ±0.1 V
- VH – VL = 2.4 V ±0.1 V
- Low-power consumption

Typical Application (continued)

9.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

Figure 20 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if Rh > 100 Rp.

When the output is at a logic high (5 V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7 V. The input signal must drive above VH = 2.7 V to cause the output to transition to logic low (0 V).

When the output is at logic low (0 V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3 V. The input signal must drive below VL = 2.3 V to cause the output to transition to logic high (5 V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design TIPD144, *Comparator with Hysteresis Reference Design*.

9.2.3 Application Curve

Figure 21 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76 V and the lower threshold is 2.34 V, both of which are close to the design target.

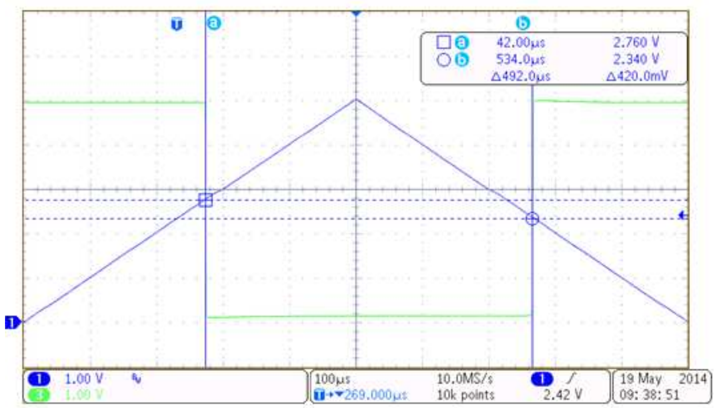


Figure 21. TLV1701 Upper and Lower Threshold with Hysteresis

10 Power Supply Recommendations

The TLV1702-Q1 device is specified for operation from 2.2 V to 36 V (±1.1 to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *Layout Guidelines* section.

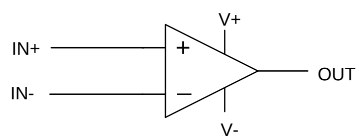
11 Layout

11.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV1702-Q1 device.
- To minimize supply noise, place a decoupling capacitor (0.1-μF ceramic, surface-mount capacitor) as close as possible to V_S as shown in Figure 22.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

11.2 Layout Example



(Schematic Representation)

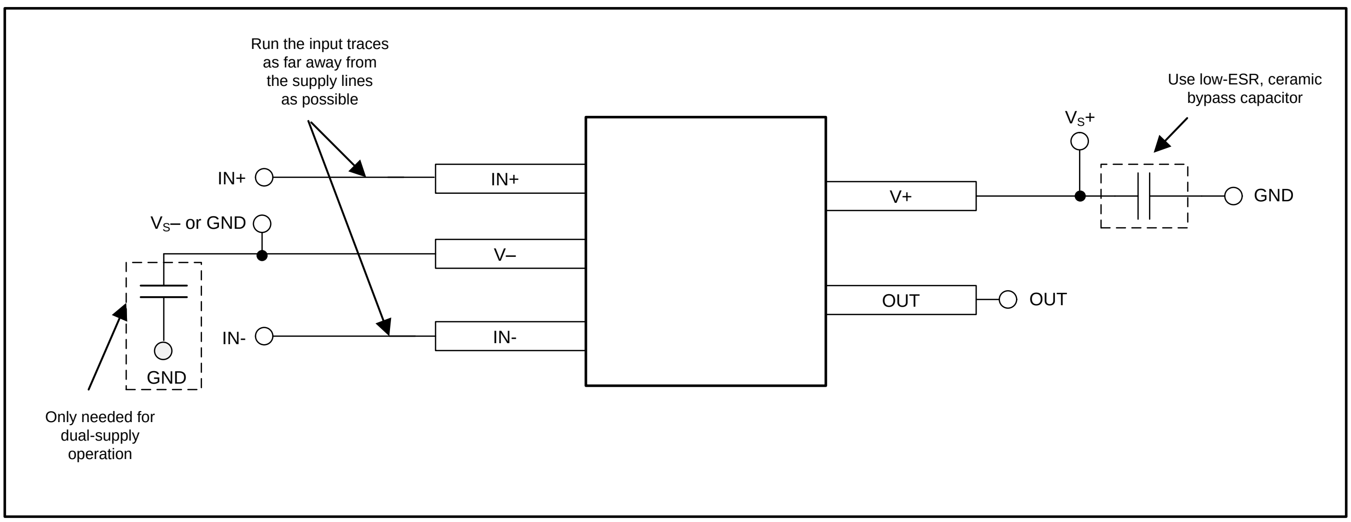


Figure 22. Comparator Board Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *《高精度设计，采用滞后参考设计的比较器》*，TIDU020
- *《REF33xx 3.9μA，SC70-3、SOT-23-3 和 UQFN-8，30ppm/°C 漂移电压基准》*，SBOS392

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

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12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
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RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1702AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1702Q	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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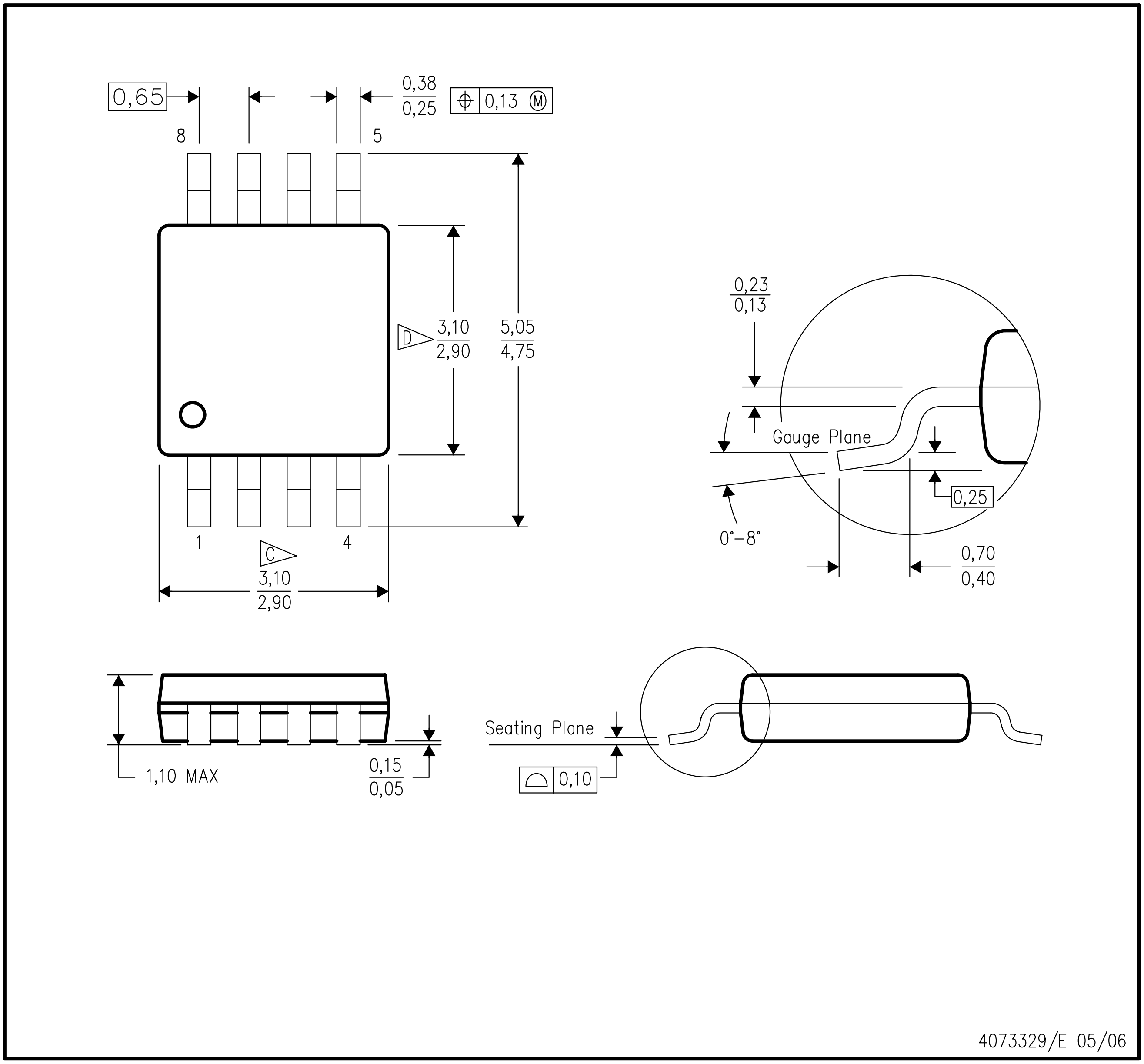
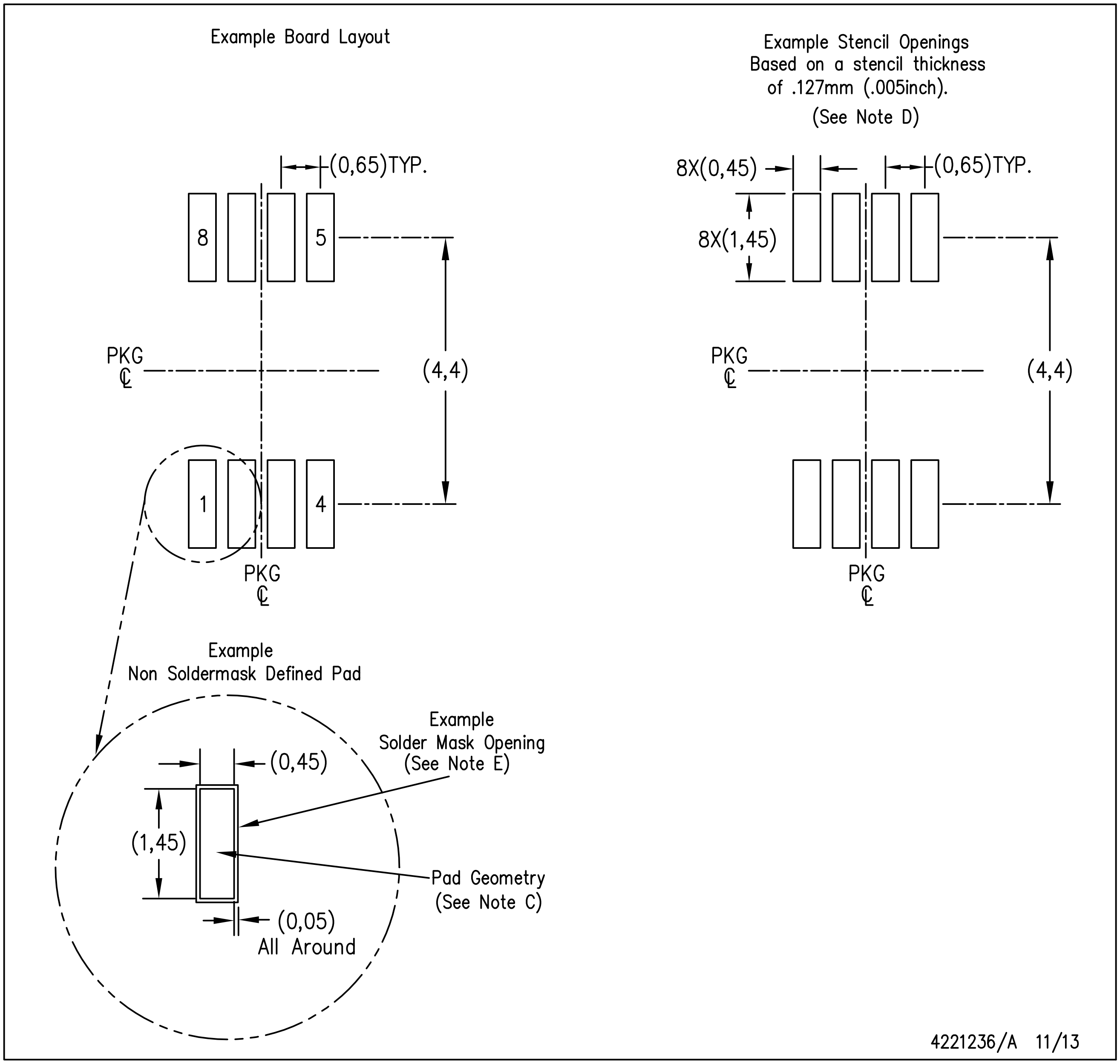
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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