

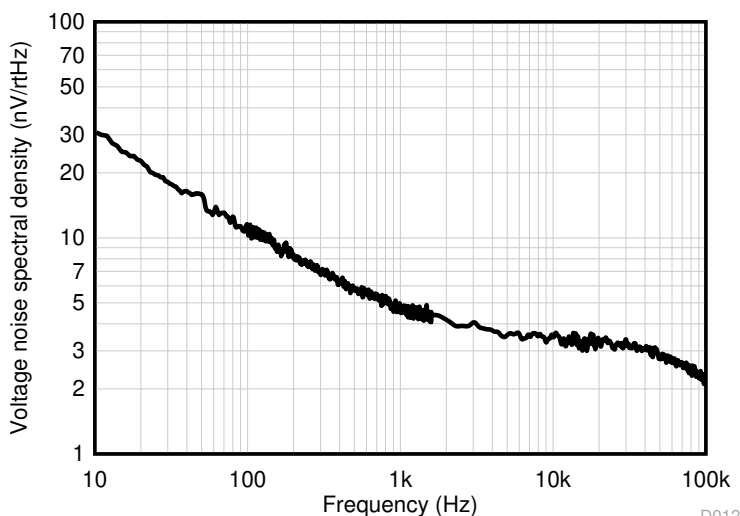
## TLV6741、TLV6742、TLV6744 10MHz 低宽带噪声 RRO 运算放大器

### 1 特性

- 低宽带噪声： $3.5\text{nV}/\sqrt{\text{Hz}}$
- 增益带宽：10MHz
- 低输入偏置电流： $\pm 3\text{pA}$
- 低失调电压：0.15mV
- 低失调电压漂移： $\pm 0.2\mu\text{V}/^\circ\text{C}$
- 轨到轨输出
- 单位增益稳定
- 低  $I_Q$ ：
  - TLV6741：890 $\mu\text{A}$ /通道
  - TLV6742/4：990 $\mu\text{A}$ /通道
- 宽电源电压范围：
  - TLV6741：2.25V 至 5.5V
  - TLV6742/4：1.7V 至 5.5V
- 强大的 EMIRR 性能：2.4GHz 时为 71dB

### 2 应用

- 固态硬盘
- 可穿戴设备（非医用）
- 专业音频放大器（机架式）
- 跨阻放大器电路
- 测试和测量
- 电机驱动器
- 压力变送器
- 实验室和现场仪表
- 桥式放大器电路
- 游戏应用



噪声频谱密度与频率间的关系

### 3 说明

TLV674x 系列包括单通道 (TLV6741)、双通道 (TLV6742) 和四通道 (TLV6744) 通用 CMOS 运算放大器，这些运算放大器提供  $3.5\text{nV}/\sqrt{\text{Hz}}$  的低噪声系数和 10MHz 的高带宽。TLV674x 系列器件凭借低噪声和高带宽特性，适用于要求在成本和性能之间达到良好平衡的各种高精度应用。此外，TLV674x 系列的输入偏置电流支持具有高源阻抗的应用。

TLV674x 系列器件采用稳健耐用的设计，方便电路设计人员使用；这得益于该器件具有单位增益稳定性、集成的 RFI/EMI 抑制滤波器、在过驱条件下不会出现反相并且具有高静电放电 (ESD) 保护功能 (2kV HBM)。另外，电阻式开环输出阻抗使其易于在超高的容性负载下保持稳定。

该运算放大器系列经过优化，可在低电压下运行，TLV6741 的工作电压低至 2.25V ( $\pm 1.125\text{V}$ )，TLV6742 和 TLV6744 的工作电压可低至 1.7V ( $\pm 0.85\text{V}$ )。所有器件的最高工作电压均为 5.5V ( $\pm 2.75\text{V}$ )，额定温度范围为  $-40^\circ\text{C}$  至  $125^\circ\text{C}$ 。

单通道 TLV6741 采用小尺寸的 SC70-5 封装。双通道 TLV6742 可采用多种封装选项，其中包括 1.5mm  $\times$  2.0mm X2QFN 微型封装。

#### 器件信息

器件型号 <sup>(1)</sup>	封装	封装尺寸 (标称值)
TLV6741	SC70 (5)	1.25mm $\times$ 2.00mm
TLV6742	SOIC (8)	3.91mm $\times$ 4.90mm
	TSSOP (8)	3.00mm $\times$ 4.40mm
	VSSOP (8)	3.00mm $\times$ 3.00mm
	SOT-23 (8)	1.60mm $\times$ 2.90mm
	WSON (8)	2.00mm $\times$ 2.00mm
TLV6742S	X2QFN (10)	1.50mm $\times$ 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

### Changes from Revision H (February 2021) to Revision I (August 2021) Page

• 删除了 <i>器件信息</i> 部分中 TLV6742 VSSOP 的预发布标签.....	1
• Removed preview tag to VSSOP (DGK) in <i>Device Comparison Table</i> section.....	4

### Changes from Revision G (April 2020) to Revision H (February 2021) Page

• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 删除了 <i>器件信息</i> 部分中 TLV6742S X2QFN 的预发布标签.....	1
• Removed preview note from X2QFN for TLV6742S in <i>Pin Configuration and Functions</i> section.....	5
• Removed Table of TLV6741 Graphs and Table of TLV6742 Graphs tables from the <i>Specifications</i> section....	12
• Removed <i>Related Links</i> section from the <i>Device and Documentation Support</i> section.....	39

### Changes from Revision F (January 2020) to Revision G (April 2020) Page

• 向 <i>应用</i> 部分添加了终端设备链接.....	1
• 删除了 <i>器件信息</i> 部分中 TSSOP、SOT-23、WSON 和 X2QFN 封装的预发布标签.....	1
• 删除了 <i>器件信息</i> 部分中的 VSSOP (8) 封装.....	1
• 在 <i>器件信息</i> 部分中添加了 TLV6742S X2QFN 的预发布标签.....	1
• Deleted VSSOP (DGK) in <i>Device Comparison Table</i> section.....	4
• Added preview tag to X2QFN (RUG) in <i>Device Comparison Table</i> section.....	4
• Deleted DGK package in pinout drawing for TLV6742 package in <i>Pin Configuration and Functions</i> section....	5
• Deleted DGK VSSOP in <i>Thermal Information for Dual Channel</i> section.....	7
• Added shutdown electrical characteristic information.....	9
• Deleted example layout for VSSOP-8 (DGK) package in <i>Layout Example</i> section.....	37

### Changes from Revision E (December 2019) to Revision F (January 2020) Page

• 删除了数据表页眉中的 TLV6744 产品文件夹链接.....	1
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**Changes from Revision D (January 2019) to Revision E (December 2019) Page**

- 在特性部分中添加了 TLV6742 和 TLV744 的  $I_Q$  定义..... 1
- 在特性部分中添加了 EMIRR、电源电压范围、 $I_Q$  和失调电压漂移..... 1
- 将首页上的噪声频谱密度与频率间的关系图更改为 TLV6742 和 TLV6744 噪声图..... 1
- 更改了说明部分的措辞以包含 TLV6742 和 TLV6744 器件的发布..... 1
- 更改了器件信息中的 TLV6742 封装..... 1
- Added *Device Comparison Table* section..... 4
- Added note regarding single supply operation to Pin Functions: TLV6741 table..... 5
- Added pin out drawings for TLV6742 packages in *Pin Configuration and Functions* section..... 5
- Added pin functions for TLV6742 packages..... 5
- Added X2QFN Package Drawing and Pin Functions for TLV6742S in *Pin Configuration and Functions* section..... 5
- Added TLV6742 typical characteristic graphs in the *Specifications* section..... 12
- Changed wording throughout *Detailed Description* section to incorporate addition of TLV6742 and TLV6744 devices..... 26
- Added *EMI Rejection* section with description information to *Detailed Description* section..... 27
- Added *Electrical Overstress* section and diagram to *Detailed Description* section..... 28
- Added *Typical Specification and Distributions* section to *Detailed Description* section..... 29
- Added *Shutdown Function* section with description for TLV6742S to *Detailed Description* section..... 30
- Added *Packages With an Exposed Thermal Pad* section to *Detailed Description* section..... 30
- Changed wording in *Application and Implementation* section to include the addition of TLV6742 and TLV6744..... 32
- Added TLV6742 and TLV6744 information to *Power Supply Recommendations* section..... 35
- Added dual channel layout example in the *Layout* section..... 37

**Changes from Revision C (October 2017) to Revision D (January 2019) Page**

- Changed Operating temperature from 125 to 150 in *Absolute Maximum Ratings* ..... 7
- Added Junction temperature spec to *Absolute Maximum Ratings* ..... 7

**Changes from Revision B (October 2017) to Revision C (October 2017) Page**

- Added test conditions to input offset voltage parameter in *Electrical Characteristics* table..... 9
- Changed typical input current noise density value from 2 fA  $\sqrt{\text{Hz}}$  to 23 fA  $\sqrt{\text{Hz}}$ ..... 9
- Changed total supply voltage total from 5V to 5.5V in *Electrical Characteristics* condition statement..... 9
- Deleted "Vs = 2.25 V to 5.5 V" test conditions for common-mode rejection ratio parameter in *Electrical Characteristics* ..... 9
- Deleted "C<sub>L</sub> = 0" test condition from 图 7-25 和 图 7-26, 图 7-27 和 图 7-28 ..... 12
- Changed voltage step from 5 V to 2 V in 图 7-32 ..... 12

**Changes from Revision A (September 2017) to Revision B (October 2017) Page**

- Changed Human-body model (HBM) value from:  $\pm 1000$  to  $\pm 3000$  and Charged-device mode (CDM) value from  $\pm 250$  to  $\pm 1000$ ..... 7

**Changes from Revision \* (June 2017) to Revision A (September 2017) Page**

- 将器件文档状态从“预告信息”更改为“量产数据” ..... 1

## 5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS						
		SOIC D	SC-70 DCK	VSSOP DGK	WSON DSG	TSSOP PW	SOT-23 DDF	X2QFN RUG
TLV6741	1	—	5	—	—	—	—	—
TLV6742	2	8	—	8	8	8	8	—
TLV6742S		—	—	—	—	—	—	10

## 6 Pin Configuration and Functions

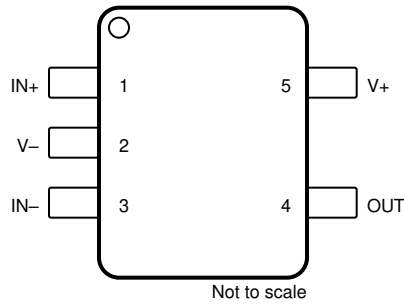


图 6-1. TLV6741 DCK Package  
5-Pin SC70  
Top View

表 6-1. Pin Functions: TLV6741

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	1	I	Noninverting input
IN -	3	I	Inverting input
OUT	4	O	Output
V+	5	—	Positive (highest) supply
V -	2	—	Negative (lowest) supply or ground (for single-supply operation)

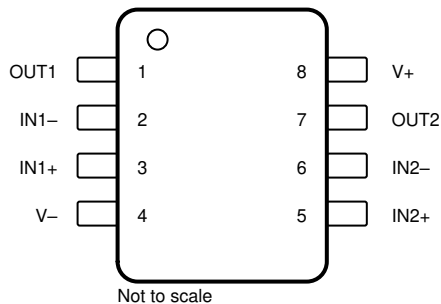
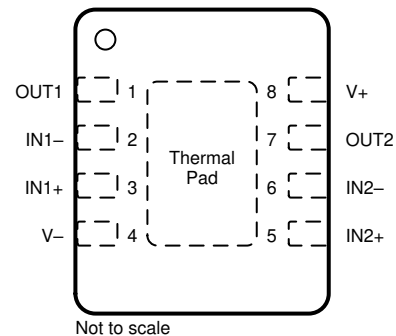


图 6-2. TLV6742 D, DGK, PW, and DDF Package  
8-Pin SOIC, VSSOP, TSSOP, and SOT-23  
Top View



Connect thermal pad to V -. See 节 8.3.8 for more information.

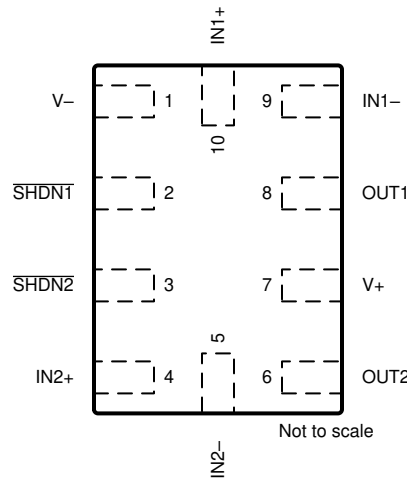
图 6-3. TLV6742 DSG Package  
8-Pin WSON With Exposed Thermal Pad  
Top View

表 6-2. Pin Functions: TLV6742

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 -	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 -	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V -	4	—	Negative (lowest) supply or ground (for single-supply operation)

**表 6-2. Pin Functions: TLV6742 (continued)**

PIN		I/O	DESCRIPTION
NAME	NO.		
V+	8	—	Positive (highest) supply



**图 6-4. TLV6742S RUG Package  
10-Pin X2QFN  
Top View**

**表 6-3. Pin Functions: TLV6742S**

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 -	9	I	Inverting input, channel 1
IN1+	10	I	Noninverting input, channel 1
IN2 -	5	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	8	O	Output, channel 1
OUT2	6	O	Output, channel 2
SHDN1	2	I	Shutdown: low = amp disabled, high = amp enabled. Channel 1. See <a href="#">节 8.3.7</a> for more information.
SHDN2	3	I	Shutdown: low = amp disabled, high = amp enabled. Channel 2. See <a href="#">节 8.3.7</a> for more information.
V -	1	I or —	Negative (lowest) supply or ground (for single-supply operation)
V+	7	I	Positive (highest) supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	6	V
Signal input pins	Common-mode voltage <sup>(3)</sup>	$(V-) - 0.5$	$(V+) + 0.5$	V
	Differential voltage <sup>(3) (4)</sup>		$V_S + 0.2$	V
	Current <sup>(3)</sup>	- 10	10	mA
Output short-circuit <sup>(2)</sup>		Continuous		
Operating ambient temperature, $T_A$		- 55	150	°C
Junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		- 65	150	°C

- (1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
- (2) Short-circuit to ground, one amplifier per package.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (4) Differential input voltages greater than 0.25 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	TLV6741: Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000	V
		TLV6742: Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
		All Devices: Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_S$	Supply voltage, $(V+) - (V-)$ , for TLV6742 and TLV6744	1.7 <sup>(1)</sup>	5.5	V
$V_S$	Supply voltage, $(V+) - (V-)$ , for TLV6741 only	2.25	5.5	V
$V_I$	Input voltage range	$(V-) -$	$(V+) - 1.2$	V
$T_A$	Specified temperature	- 40	125	°C

- (1) Operation between 1.7V and 1.8V is only recommended for  $T_A = 0 - 85$  °C

### 7.4 Thermal Information for Single Channel

THERMAL METRIC <sup>(1)</sup>		TLV6741	UNIT
		DCK (SC70)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	240.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	34.8	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	63.3	°C/W

## 7.4 Thermal Information for Single Channel (continued)

THERMAL METRIC <sup>(1)</sup>		TLV6741	UNIT
		DCK (SC70)	
		5 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report [SPRA953C](#).

## 7.5 Thermal Information for Dual Channel

THERMAL METRIC <sup>(1)</sup>		TLV6742, TLV6742S						UNIT
		D (SOIC)	DDF (SOT-23-8)	DSG (WSON)	PW (TSSOP)	DGK (VSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.1	153.8	78.2	185.6	177.0	140.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.2	80.2	97.5	74.5	68.6	52.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.5	73.1	44.6	116.3	98.7	69.7	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	24.4	6.6	4.7	12.6	12.4	1.0	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	73.3	72.7	44.6	114.6	97.1	67.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	19.8	n/a	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953C](#).

## 7.6 Electrical Characteristics

**TLV6742/4 Specifications:**  $V_S = (V+) - (V-) = 1.8\text{ V to }5.5\text{ V}$  ( $\pm 0.9\text{ V to } \pm 2.75\text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

**TLV6741 Specifications:**  $V_S = (V+) - (V-) = 5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_S = 5.0\text{ V}$		$\pm 0.15$	$\pm 1.0$	mV
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$	TLV6742/4(3)		
$dV_{OS}/dT$	Input offset voltage drift			$\pm 0.35$		$\mu\text{V}/^\circ\text{C}$
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$	TLV6741(2) TLV6742/4(3)		
PSRR	Input offset voltage versus power supply	$V_{CM} = V_-$	TLV6741(2)	$\pm 0.32$	$\pm 6.3$	$\mu\text{V/V}$
		$V_{CM} = V_+$	TLV6742/4(3)	$\pm 0.7$	$\pm 5.8$	
	Channel separation	$f = 20\text{ kHz}$		130		dB
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current		TLV6741(2)	$\pm 10$		pA
			TLV6742/4(3)	$\pm 3$		
$I_{OS}$	Input offset current		TLV6741(2)	$\pm 10$		pA
			TLV6742/4(3)	$\pm 0.5$		
<b>NOISE</b>						
$E_N$	Input voltage noise	$f = 0.1\text{ to }10\text{ Hz}$		1.2		$\mu\text{V}_{PP}$
				0.227		$\mu\text{V}_{RMS}$
$e_N$	Input voltage noise density	$f = 10\text{ Hz}$	TLV6742/4(3)	30		$\text{nV}/\sqrt{\text{Hz}}$
			TLV6741(2)	5.0		
			TLV6742/4(3)	4.6		
			TLV6741(2)	3.7		
		$f = 10\text{ kHz}$	TLV6742/4(3)	3.5		
$i_N$	Input current noise	$f = 1\text{ kHz}$		23		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range			(V -)	(V+) -1.2	V
CMRR	Common-mode rejection ratio	$(V_-) < V_{CM} < (V_+) - 1.2\text{ V}$	TLV6741(2)	95	120	dB
		$V_S = 1.8\text{ V}, (V_-) < V_{CM} < (V_+) - 1.2\text{ V}$	TLV6742/4(3)	87	100	
		$V_S = 5.5\text{ V}, (V_-) < V_{CM} < (V_+) - 1.2\text{ V}$		94	110	
<b>INPUT CAPACITANCE</b>						
$Z_{ID}$	Differential			$10 \parallel 6$		$\text{M}\Omega \parallel \text{pF}$
$Z_{ICM}$	Common-mode			$10 \parallel 6$		$\text{G}\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$(V_-) + 40\text{ mV} < V_O < (V_+) - 40\text{ mV}, R_L = 10\text{ k}\Omega$ to $V_S/2$	TLV6741(2)	125		dB
		$(V_-) + 150\text{ mV} < V_O < (V_+) - 150\text{ mV}, R_L = 2\text{ k}\Omega$ to $V_S/2$		110	130	
		$V_S = 1.8\text{ V}, (V_-) + 150\text{ mV} < V_O < (V_+) - 150\text{ mV}, R_L = 2\text{ k}\Omega$ to $V_S/2$	TLV6742/4(3)	107	120	
		$V_S = 5.5\text{ V}, (V_-) + 150\text{ mV} < V_O < (V_+) - 150\text{ mV}, R_L = 2\text{ k}\Omega$ to $V_S/2$		140		
		$V_S = 1.8\text{ V}, (V_-) + 40\text{ mV} < V_O < (V_+) - 40\text{ mV}, R_L = 10\text{ k}\Omega$ to $V_S/2$		110	120	
		$V_S = 5.5\text{ V}, (V_-) + 40\text{ mV} < V_O < (V_+) - 40\text{ mV}, R_L = 10\text{ k}\Omega$ to $V_S/2$		140		

## 7.6 Electrical Characteristics (continued)

**TLV6742/4 Specifications:**  $V_S = (V+) - (V-) = 1.8\text{ V to }5.5\text{ V}$  ( $\pm 0.9\text{ V to } \pm 2.75\text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{O\ UT} = V_S / 2$ , unless otherwise noted.

**TLV6741 Specifications:**  $V_S = (V+) - (V-) = 5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{O\ UT} = V_S / 2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
<b>FREQUENCY RESPONSE</b>								
GBW	Gain-bandwidth product				10		MHz	
SR	Slew rate	$V_S = 5.5\text{ V}$ , $G = +1$ , $C_L = 20\text{ pF}$			4.5		V/ $\mu\text{s}$	
$t_S$	Settling time	To 0.1%, $V_S = 5.5\text{ V}$ , $V_{STEP} = 2\text{ V}$ , $G = +1$ , $C_L = 20\text{ pF}$			0.65		$\mu\text{s}$	
		To 0.01%, $V_S = 5.5\text{ V}$ , $V_{STEP} = 2\text{ V}$ , $G = +1$ , $C_L = 20\text{ pF}$			1.2			
	Phase margin	$G = +1$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$			55		°	
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			0.2		$\mu\text{s}$	
THD+N	Total harmonic distortion + noise	$V_S = 5.5\text{ V}$ , $V_{CM} = 2.5\text{ V}$ , $V_O = 1\text{ V}_{RMS}$ , $G = +1$ , $f = 1\text{ kHz}$ , $R_L = 10\text{ k}\Omega$		TLV6741 <sup>(2)</sup>	0.00035%			
				TLV6742/4 <sup>(3)</sup>	0.00015%			
EMIRR	Electro-magnetic interference rejection ratio	$f = 1\text{ GHz}$		TLV6742/4 <sup>(3)</sup>	51		dB	
<b>OUTPUT</b>								
	Voltage output swing from rail	Positive/Negative rail headroom	$V_S = 5.5\text{ V}$ , $R_L = 10\text{ k}$	TLV6741 <sup>(2)</sup>	8	10	mV	
			$V_S = 5.5\text{ V}$ , $R_L = \text{no load}$			7		
		Positive rail headroom	$V_S = 5.5\text{ V}$ , $R_L = 2\text{ k}\Omega$	TLV6742/4 <sup>(3)</sup>				35
			$V_S = 5.5\text{ V}$ , $R_L = 10\text{ k}\Omega$					5
		Negative rail headroom	$V_S = 5.5\text{ V}$ , $R_L = \text{no load}$					7
			$V_S = 5.5\text{ V}$ , $R_L = 2\text{ k}\Omega$					35
$V_S = 5.5\text{ V}$ , $R_L = 10\text{ k}\Omega$					5	14		
$I_{SC}$	Short-circuit current				TLV6742/4 <sup>(3)</sup>	$\pm 68$		mA
$C_{LOAD}$	Capacitive load drive				See <a href="#">Fig 7-58</a>			
$Z_O$	Open-loop output impedance	$f = 10\text{ MHz}$ , $I_O = 0\text{ A}$		TLV6741 <sup>(2)</sup>	160		$\Omega$	
		$f = 2\text{ MHz}$ , $I_O = 0\text{ A}$		TLV6742/4 <sup>(3)</sup>	165			
<b>POWER SUPPLY</b>								
$I_Q$	Quiescent current per amplifier	$V_S = 5.5\text{ V}$ , $I_O = 0\text{ A}$		TLV6741 <sup>(2)</sup>	890		$\mu\text{A}$	
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$			1100		
				TLV6742/4 <sup>(3)</sup>	990	1200		
$T_A = -40^\circ\text{C to }125^\circ\text{C}$		1250						
	Turn-On Time	At $T_A = 25^\circ\text{C}$ , $V_S = 5.5\text{ V}$ , $V_S$ ramp rate $> 0.3\text{ V}/\mu\text{s}$		TLV6742/4 <sup>(3)</sup>	10		$\mu\text{s}$	

## 7.6 Electrical Characteristics (continued)

**TLV6742/4 Specifications:**  $V_S = (V+) - (V-) = 1.8\text{ V to }5.5\text{ V } (\pm 0.9\text{ V to } \pm 2.75\text{ V})$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

**TLV6741 Specifications:**  $V_S = (V+) - (V-) = 5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SHUTDOWN</b>						
$I_{QSD}$	Quiescent current per amplifier	All amplifiers disabled, $\overline{\text{SHDN}} = V-$		1	3.5	$\mu\text{A}$
$Z_{SHDN}$	Output impedance during shutdown	Amplifier disabled		10    6		$\text{G}\Omega \parallel \text{pF}$
$V_{IH}$	Logic high threshold voltage (amplifier enabled)		$(V-) + 1.1\text{ V}$			V
$V_{IL}$	Logic low threshold voltage (amplifier disabled)			$(V-) + 0.2\text{ V}$		
$t_{ON}$	Amplifier enable time (full shutdown) <sup>(1)</sup>	$G = +1, V_{CM} = V-, V_O = 0.1 \times V_S/2$		15		$\mu\text{s}$
	Amplifier enable time (partial shutdown) <sup>(1)</sup>	$G = +1, V_{CM} = V-, V_O = 0.1 \times V_S/2$		8		
$t_{OFF}$	Amplifier disable time <sup>(1)</sup>	$V_{CM} = V-, V_O = V_S/2$		3		
	$\overline{\text{SHDN}}$ pin input bias current (per pin)	$(V+) \geq \overline{\text{SHDN}} \geq (V-) + 0.9\text{ V}$		0.4		$\mu\text{A}$
		$(V-) \leq \overline{\text{SHDN}} \leq (V-) + 0.7\text{ V}$		0.25		

- (1) Disable time ( $t_{OFF}$ ) and enable time ( $t_{ON}$ ) are defined as the time interval between the 50% point of the signal applied to the  $\overline{\text{SHDN}}$  pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
- (2) This electrical characteristic only applies to the single-channel, TLV6741
- (3) This electrical characteristic only applies to the dual-channel TLV6742 and quad-channel TLV6744

### 7.7 TLV6741: Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

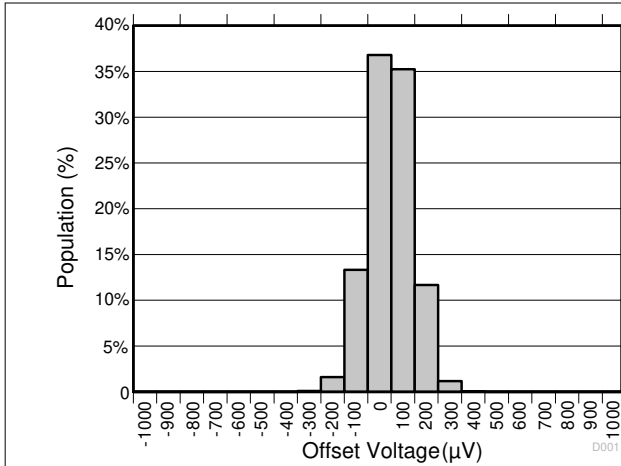


图 7-1. Offset Voltage Production Distribution

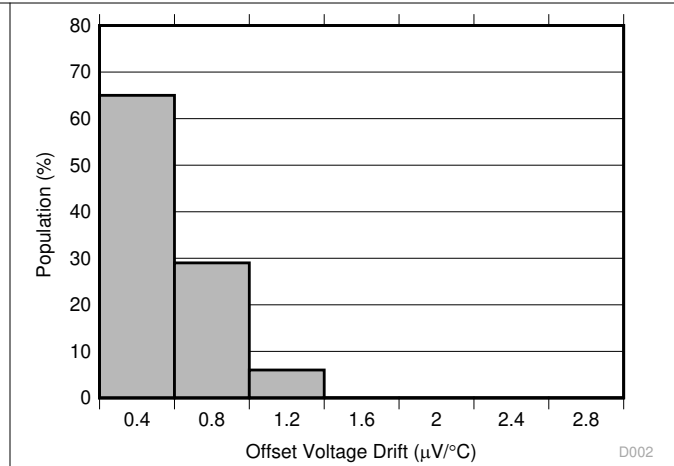


图 7-2. Offset Voltage Drift Distribution

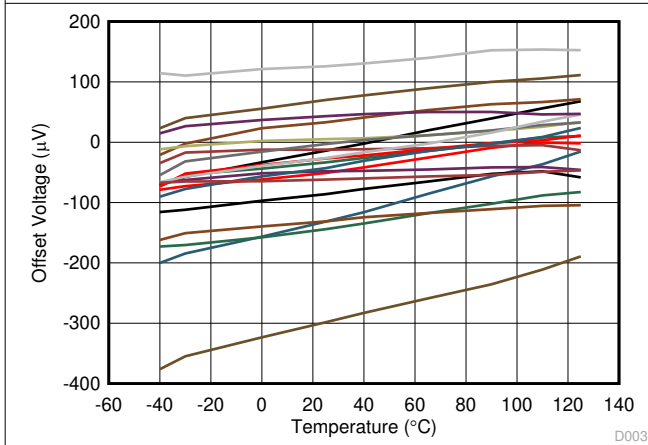


图 7-3. Offset Voltage vs Temperature

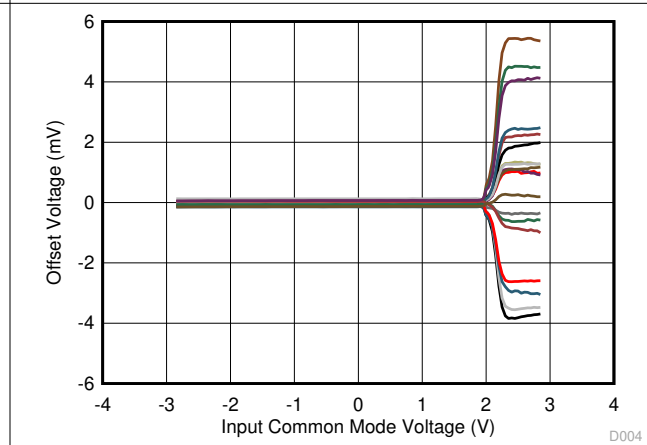


图 7-4. Offset Voltage vs Common-Mode Voltage

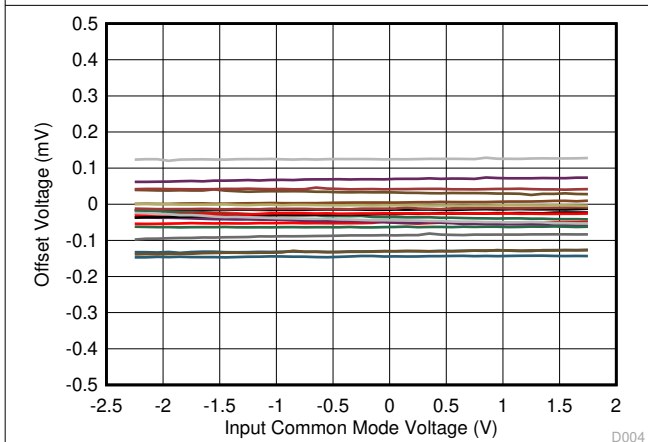


图 7-5. Offset Voltage vs Common-Mode Voltage

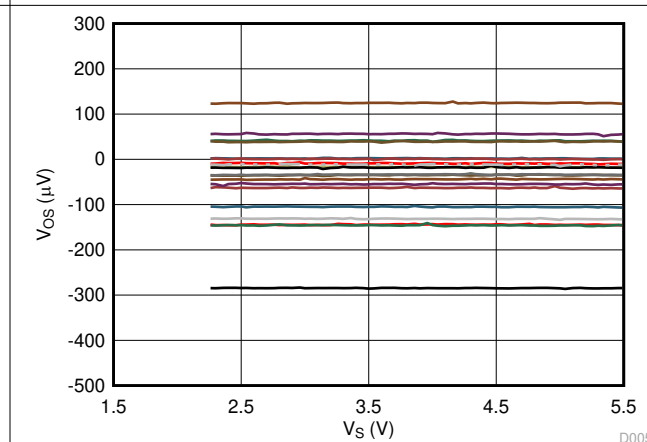


图 7-6. Offset Voltage vs Power Supply

### 7.7 TLV6741: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

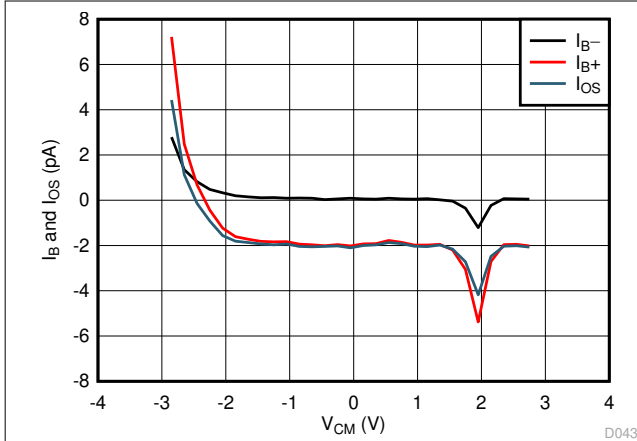


图 7-7.  $I_B$  and  $I_{OS}$  vs Common-Mode Voltage

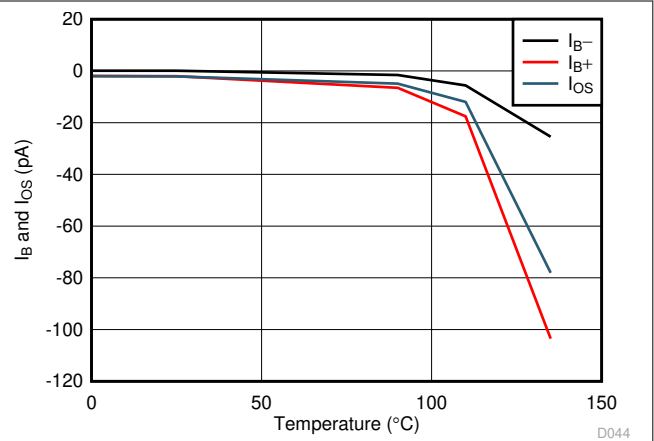


图 7-8.  $I_B$  and  $I_{OS}$  vs Temperature

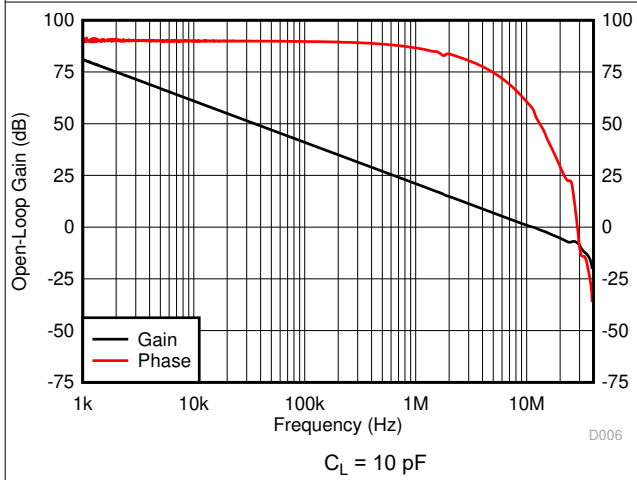


图 7-9. Open-Loop Gain and Phase vs Frequency

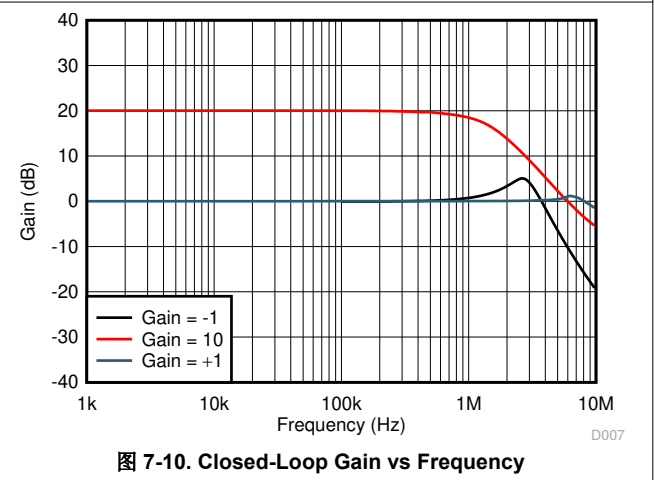


图 7-10. Closed-Loop Gain vs Frequency

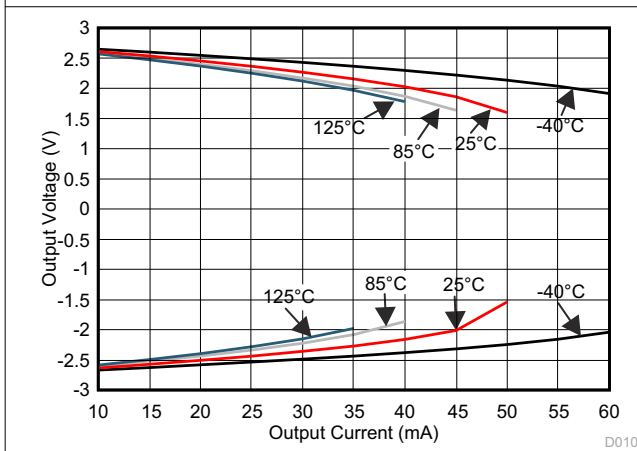


图 7-11.  $V_O$  vs  $I$  Sourcing and Sinking

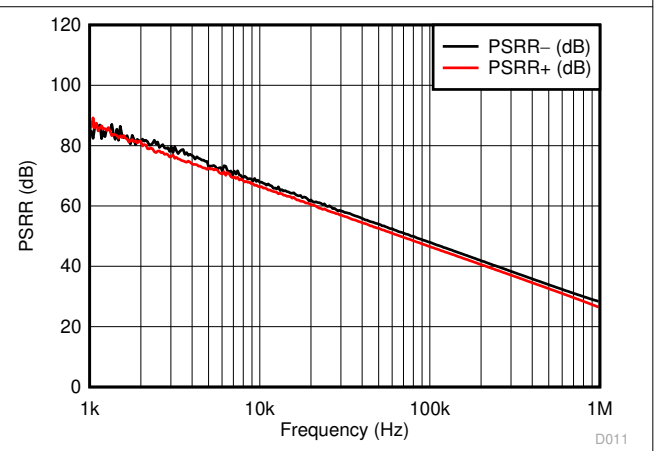


图 7-12. PSRR vs Frequency (Referred to Input)

### 7.7 TLV6741: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

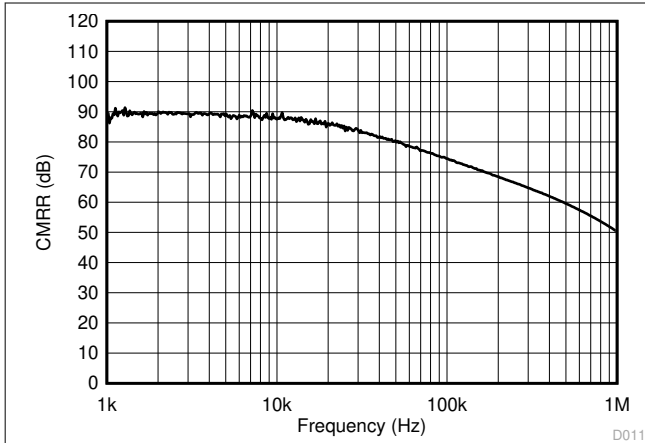
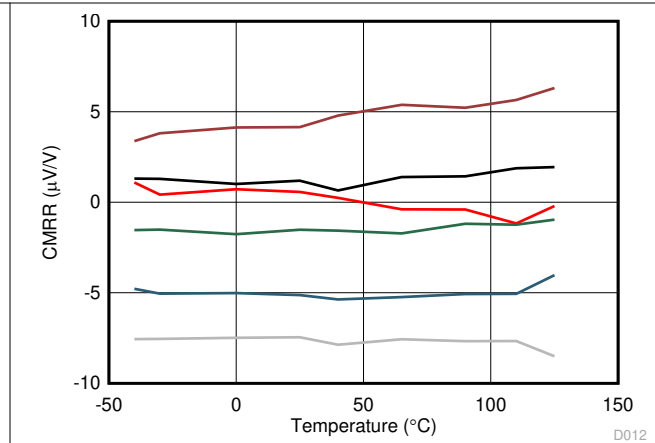


图 7-13. CMRR vs Frequency (Referred to Input)



$V_S = 5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CM} = 0\text{ V}$  to  $4.3\text{ V}$

图 7-14. CMRR vs Temperature

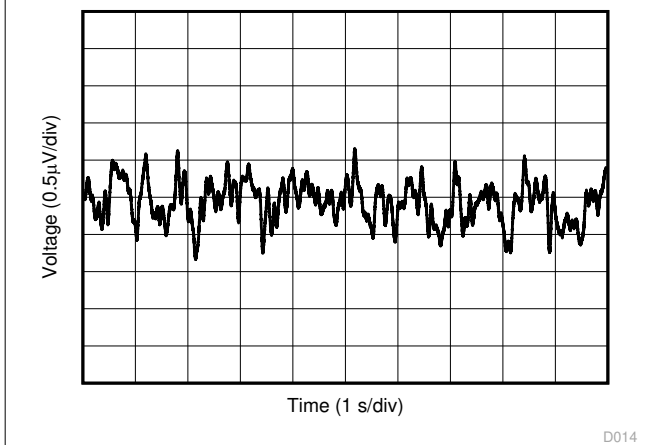


图 7-15. 0.1-Hz to 10-Hz Flicker Noise

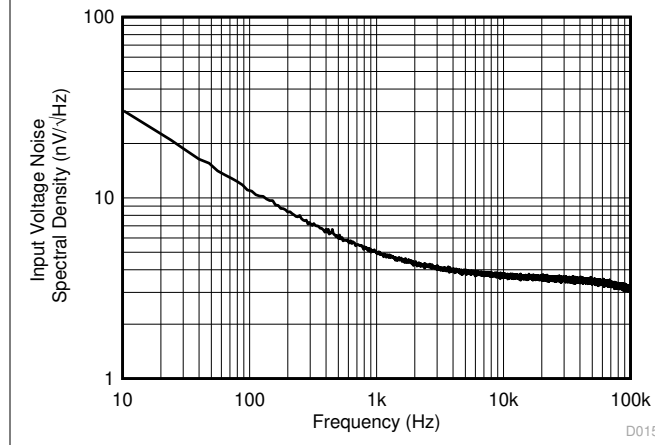
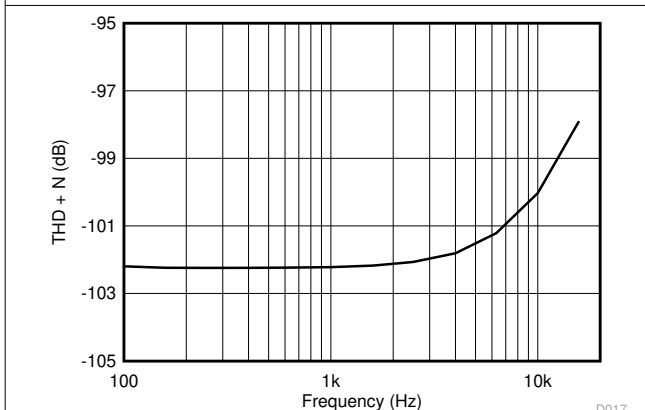
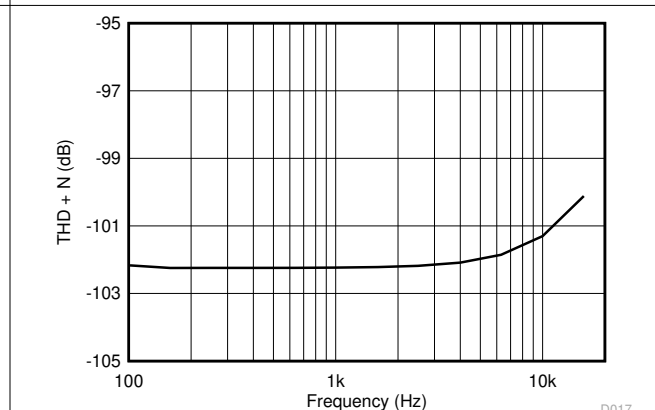


图 7-16. Input Voltage Noise Spectral Density vs Frequency



$V_S = 5.5\text{ V}$ ,  $V_{ICM} = 2.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  
Gain = 1, BW = 80 kHz,  $V_{OUT} = 0.5\text{ Vrms}$

图 7-17. THD + N vs Frequency

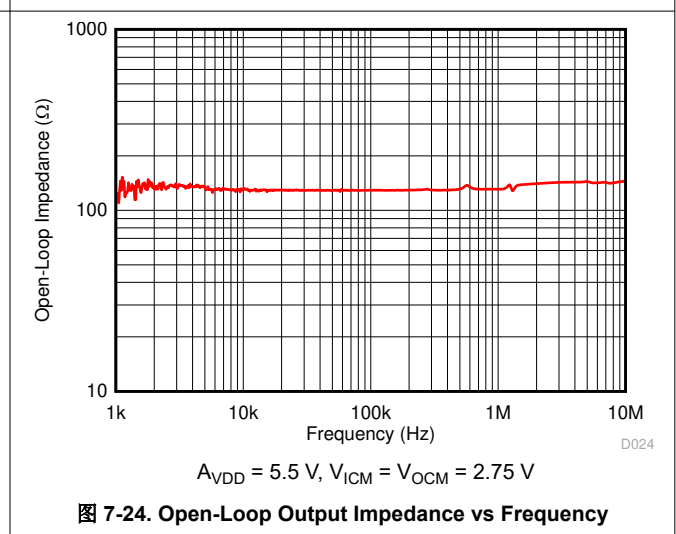
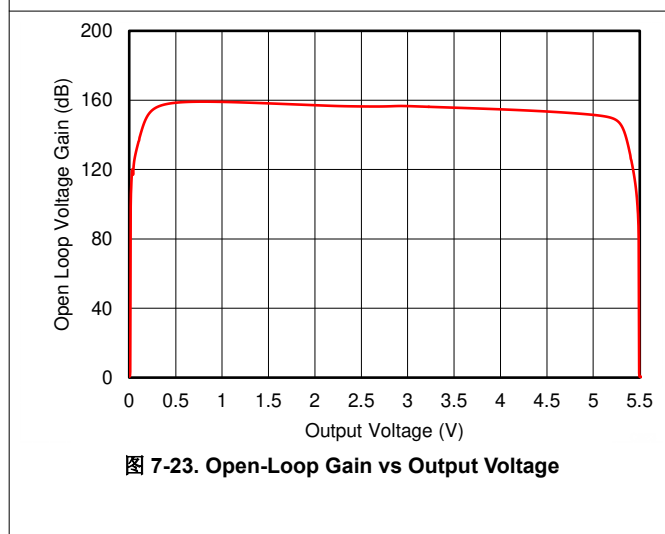
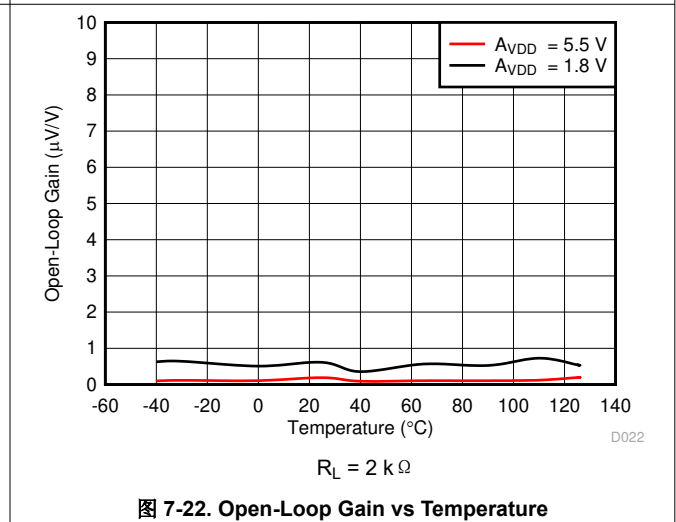
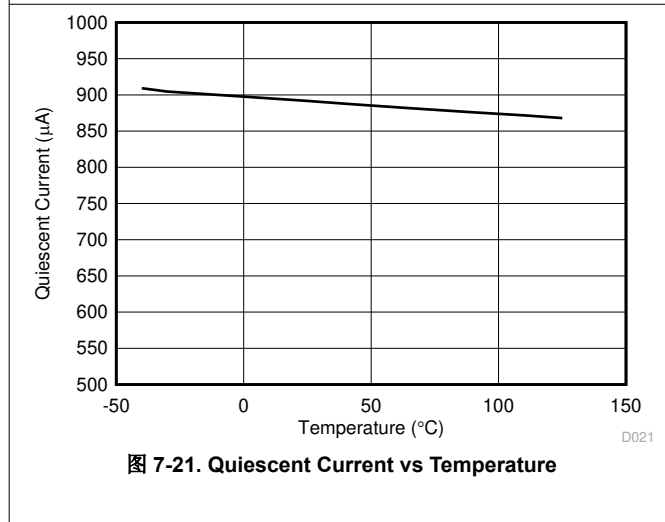
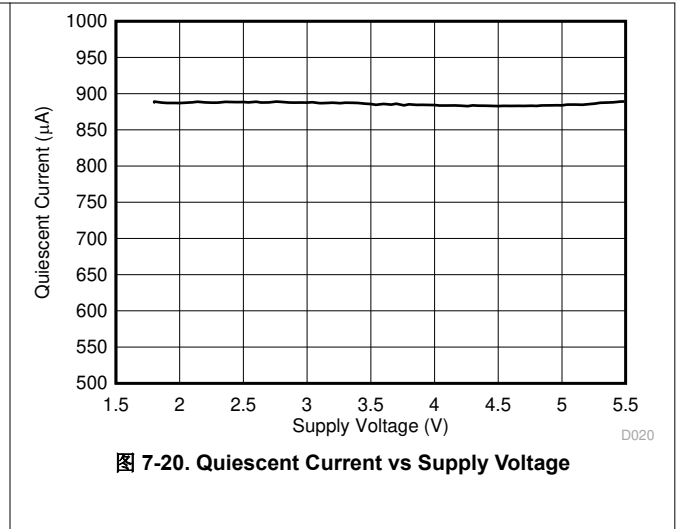
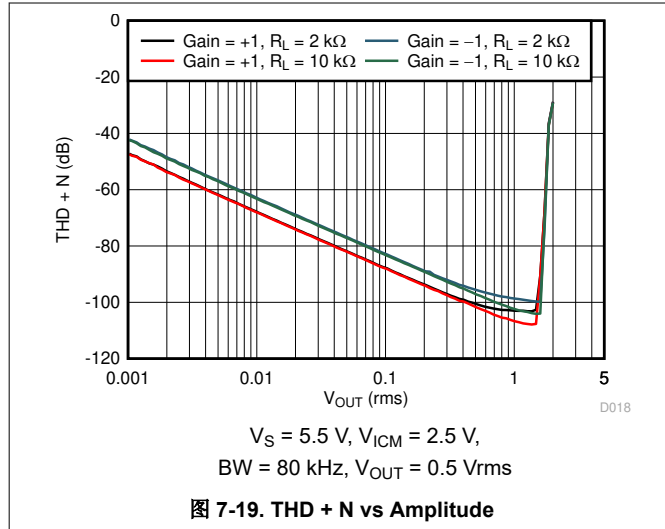


$V_S = 5.5\text{ V}$ ,  $V_{ICM} = 2.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  
Gain = 1, BW = 80 kHz,  $V_{OUT} = 0.5\text{ Vrms}$

图 7-18. THD + N vs Frequency

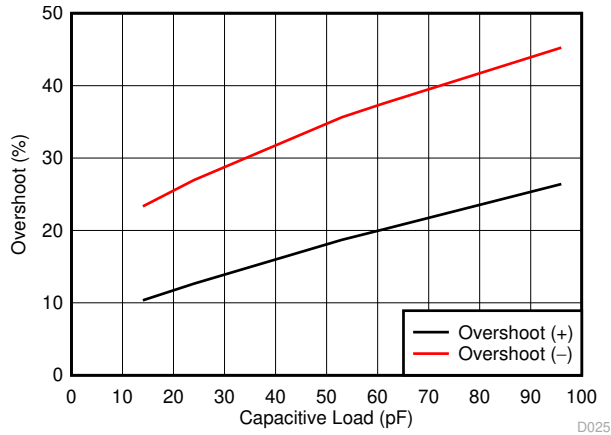
### 7.7 TLV6741: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.



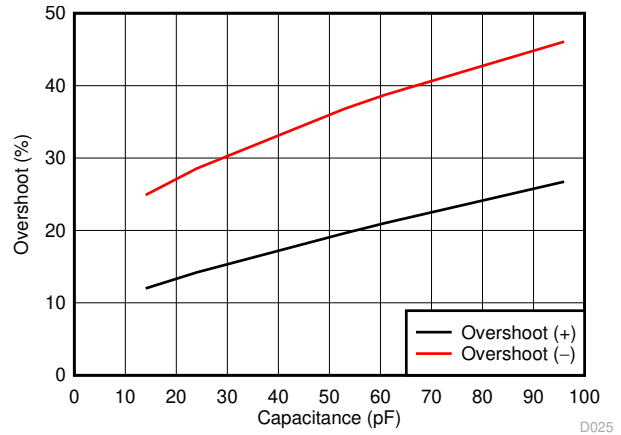
### 7.7 TLV6741: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.



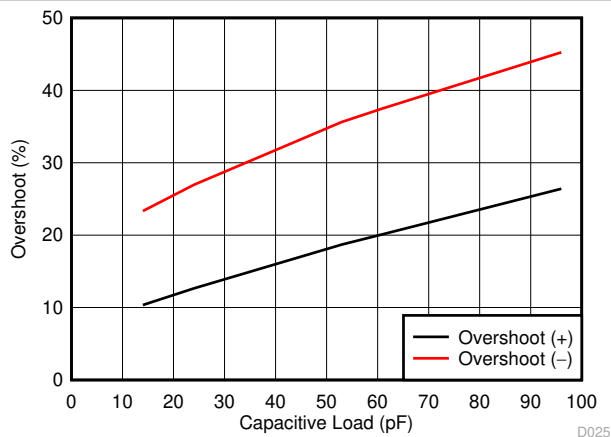
$V_S = 5.5\text{ V}$ ,  $V_{ICM} = 2.75\text{ V}$ ,  
 $V_{OCM} = 2.75\text{ V}$ ,  $G = 1$ , 100-mV output step

图 7-25. Small-Signal Overshoot vs Load Capacitance



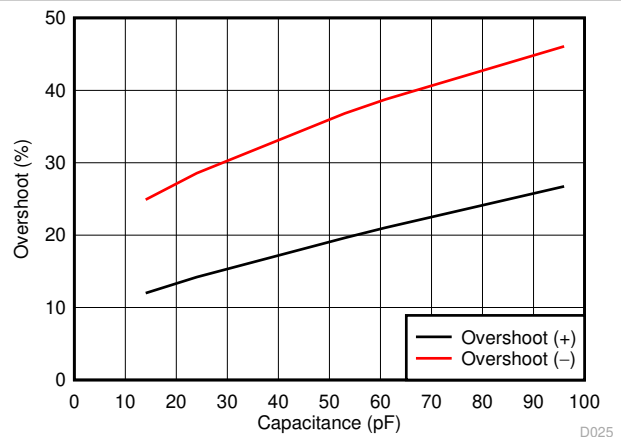
$V_S = 1.8\text{ V}$ ,  $V_{ICM} = 0.9\text{ V}$   
 $V_{OCM} = 0.9\text{ V}$ ,  $G = 1$ , 100-mV output step

图 7-26. Small-Signal Overshoot vs Load Capacitance



$V_S = 5.5\text{ V}$ ,  $V_{ICM} = 2.75\text{ V}$ ,  
 $V_{OCM} = 2.75\text{ V}$ , Gain = -1, 100-mV output step

图 7-27. Small-Signal Overshoot vs Load Capacitance



$V_S = 1.8\text{ V}$ ,  $V_{ICM} = 0.9\text{ V}$   
 $V_{OCM} = 0.9\text{ V}$ , Gain = -1, 100-mV output step

图 7-28. Small-Signal Overshoot vs Load Capacitance

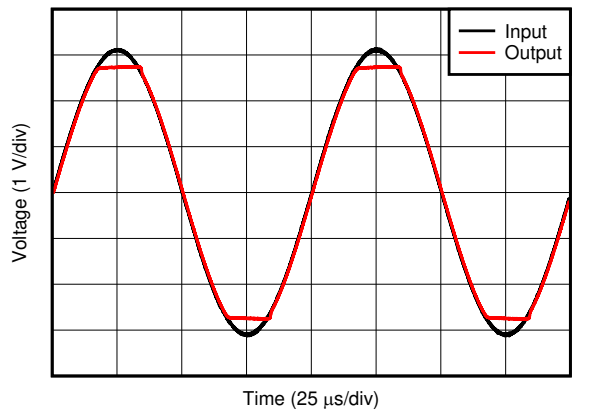


图 7-29. No Phase Reversal

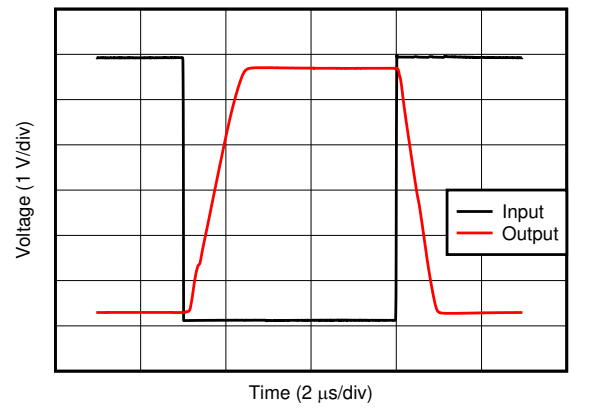
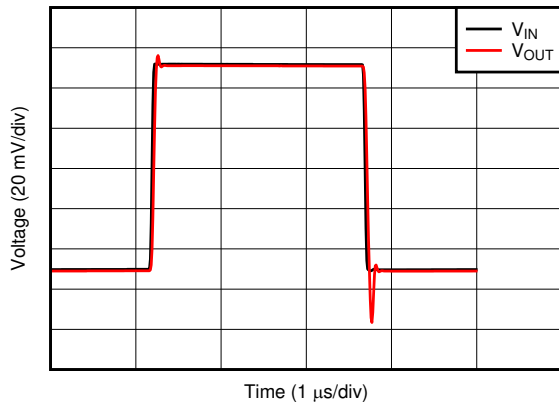


图 7-30. Overload Recovery

## 7.7 TLV6741: Typical Characteristics (continued)

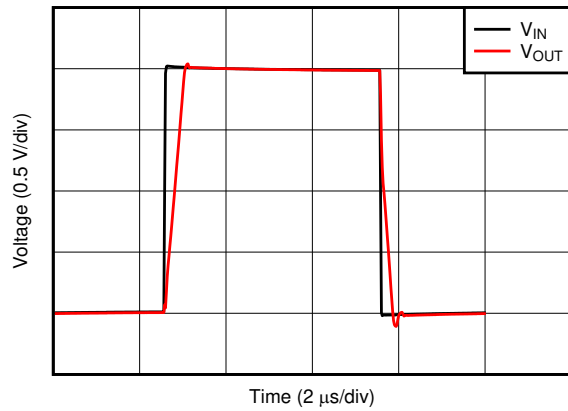
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.



D030

$V_S = 1.8\text{ V}$ ,  $V_{ICM} = 0.9\text{ V}$ ,  $V_{OCM} = 0.9\text{ V}$   
 $C_L = 30\text{ pF}$ , Gain = 1,  $V_{IN} = 100\text{-mVpp}$

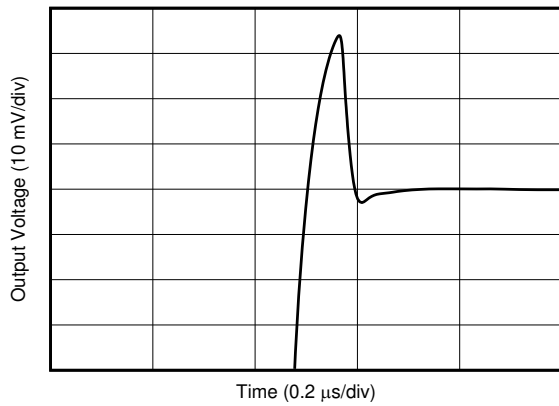
图 7-31. Small-Signal Step Response



D031

$V_S = 5.5\text{ V}$ ,  $V_{OCM} = 2.75\text{ V}$ ,  $C_L = 10\text{ pF}$   
 $V_{ICM} = 2.75\text{ V}$ , Gain = 1, 2-V step

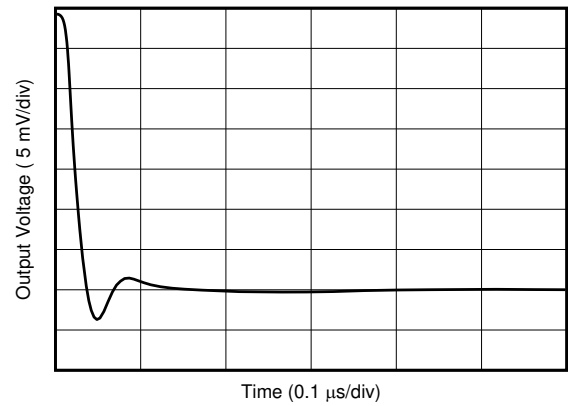
图 7-32. Large Signal Step Response



D032

$V_S = 5.5\text{ V}$ ,  $V_{ICM} = 2.75\text{ V}$ ,  $V_{OCM} = 2.75\text{ V}$   
 $C_L = 0$ , Gain = 1, 5-V step

图 7-33. Large Signal Settling Time (Positive)



D033

$V_S = 5.5\text{ V}$ ,  $V_{ICM} = 2.75\text{ V}$ ,  $V_{OCM} = 2.75\text{ V}$   
 $C_L = 0$ , Gain = 1, 5-V step

图 7-34. Large Signal Settling Time (Negative)

### 7.7 TLV6741: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

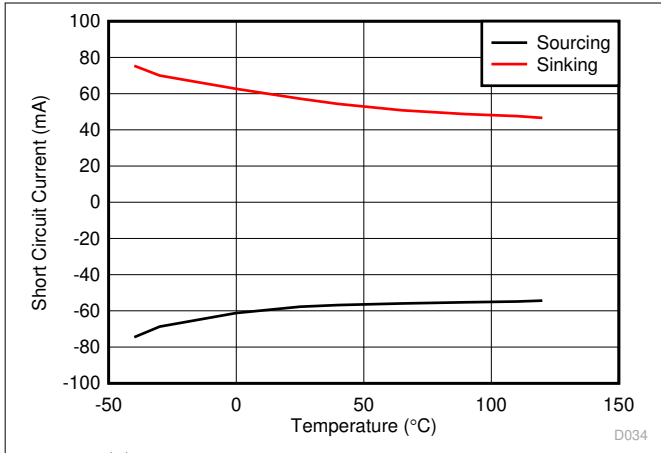
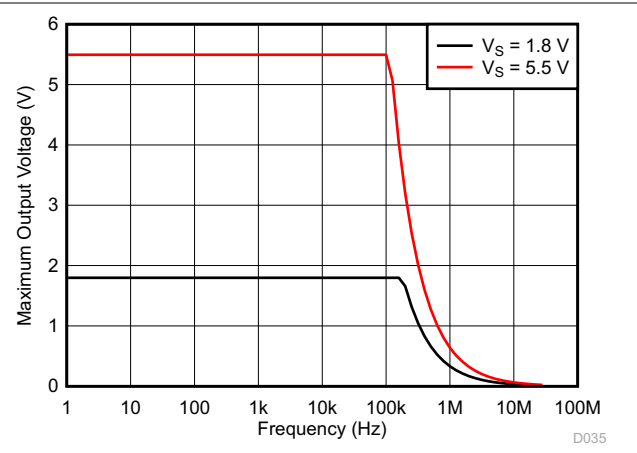


图 7-35. Short-Circuit Current vs Temperature



$V_{ICM} = V_S / 2$ ,  $V_{OCM} = V_S / 2$ ,  
 $C_L = 10\text{ pF}$ , Gain = 1

图 7-36. Maximum Output Voltage vs Frequency

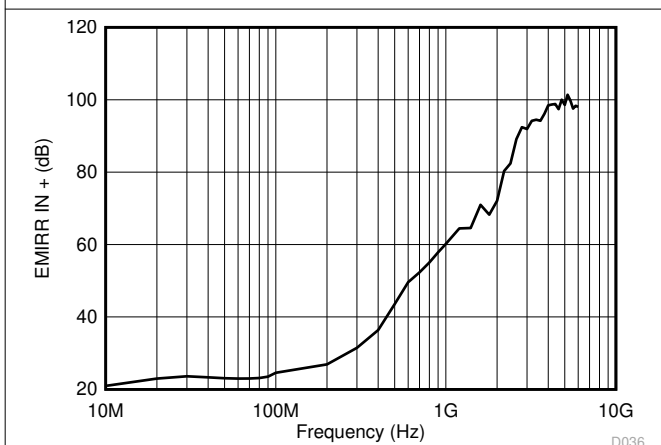
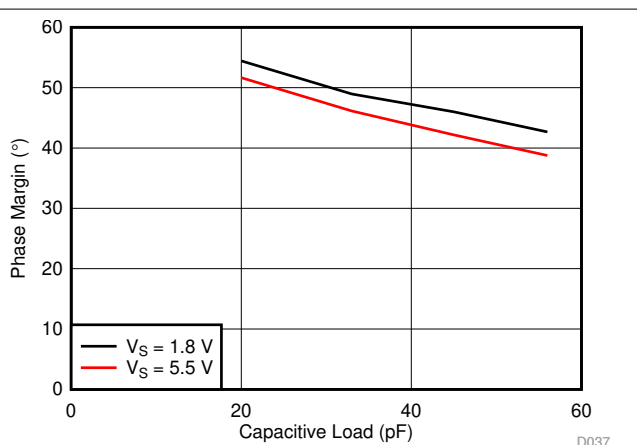


图 7-37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



$V_{ICM} = V_{OCM} = V_S / 2$

图 7-38. Phase Margin vs Capacitive Load

## 7.8 TLV6742: Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.75\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

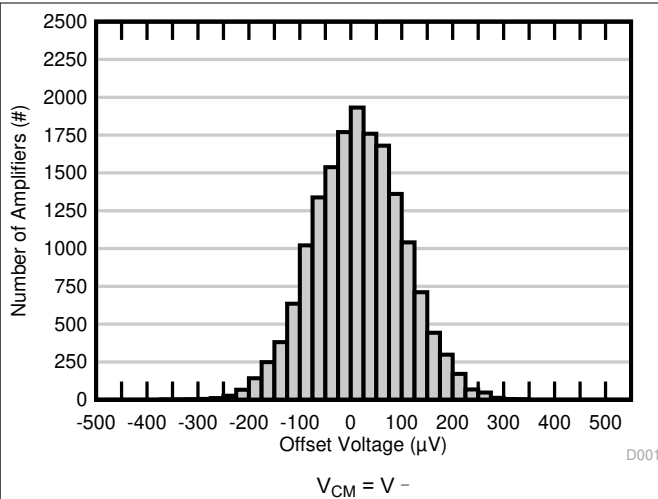


图 7-39. Offset Voltage Production Distribution

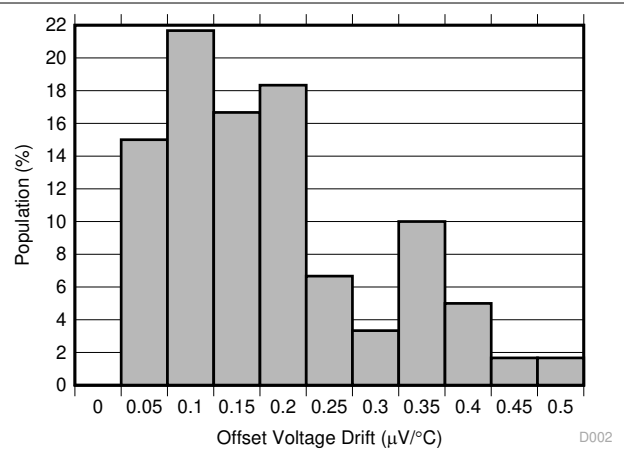


图 7-40. Offset Voltage Drift Distribution

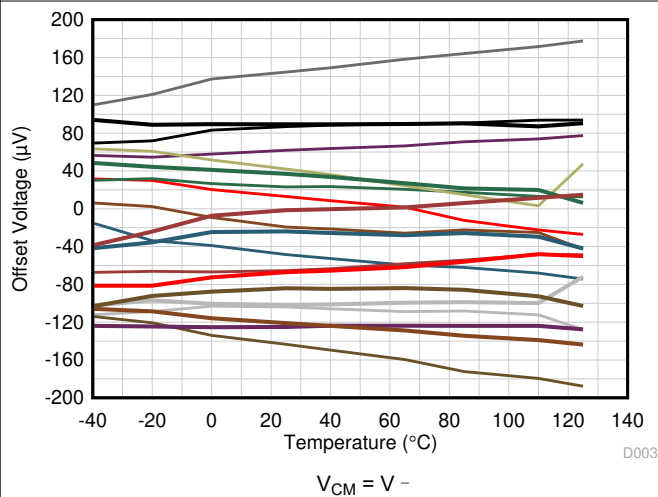


图 7-41. Offset Voltage vs Temperature (PMOS Input Pair)

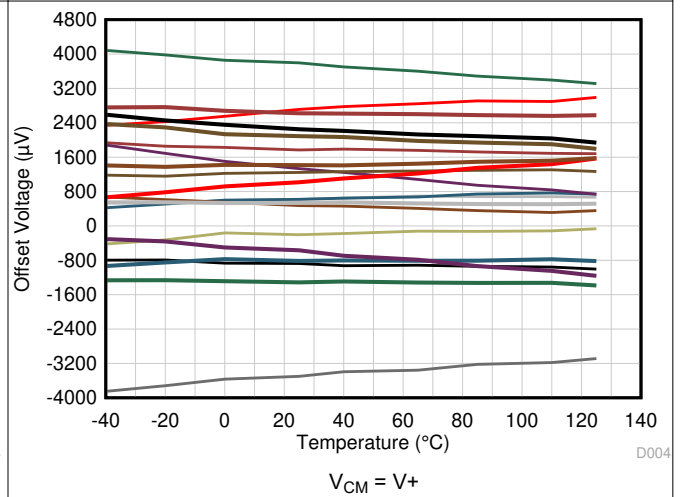


图 7-42. Offset Voltage vs Temperature (NMOS Input Pair)

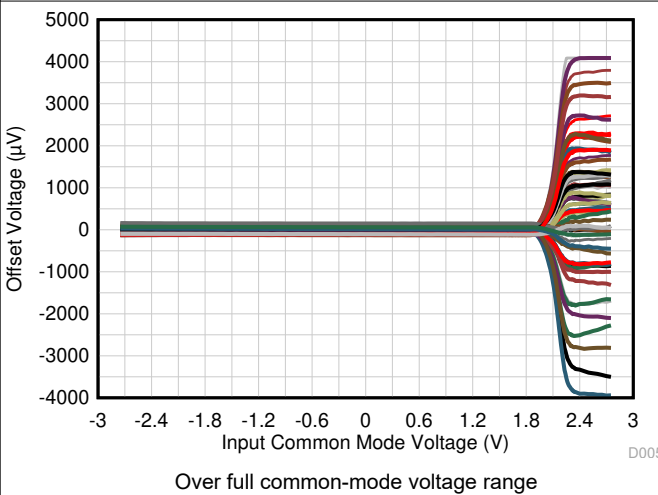


图 7-43. Offset Voltage vs Common-Mode Voltage (Full Range)

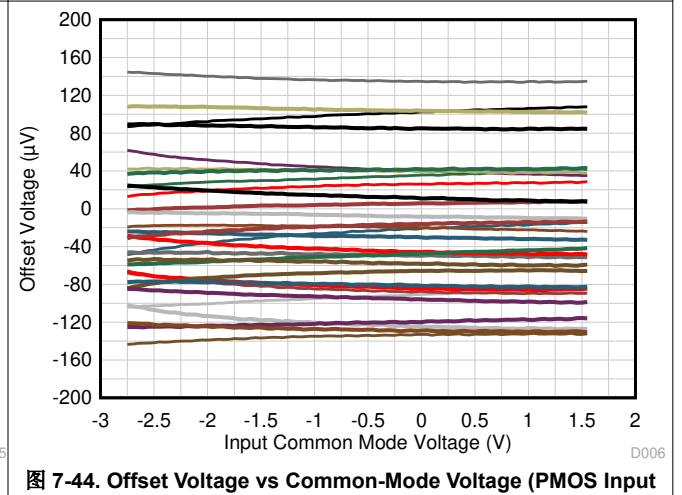


图 7-44. Offset Voltage vs Common-Mode Voltage (PMOS Input Pair)

### 7.8 TLV6742: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.75\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

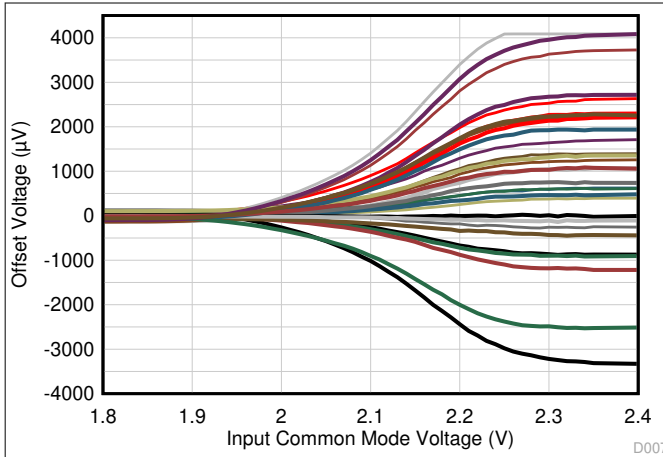


图 7-45. Offset Voltage vs Common-Mode Voltage (Transition Region)

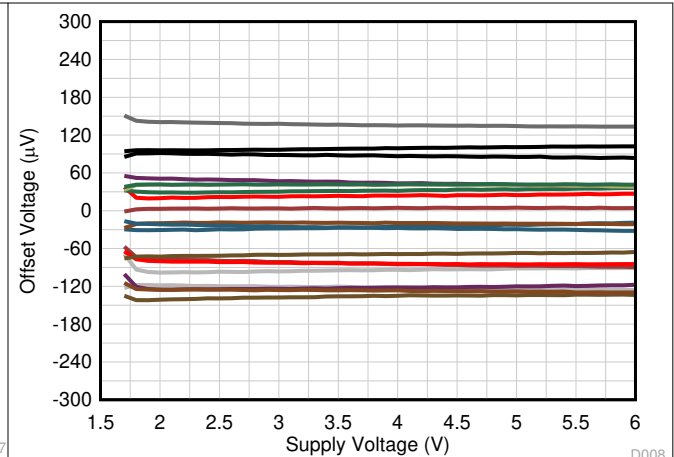


图 7-46. Offset Voltage vs Power Supply

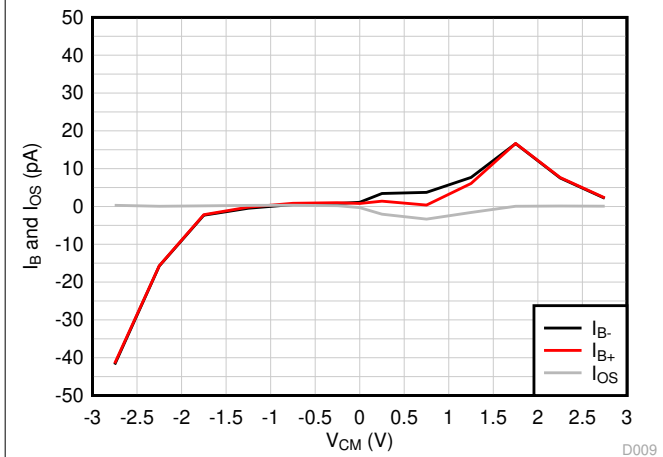


图 7-47.  $I_B$  and  $I_{OS}$  vs Common-Mode Voltage

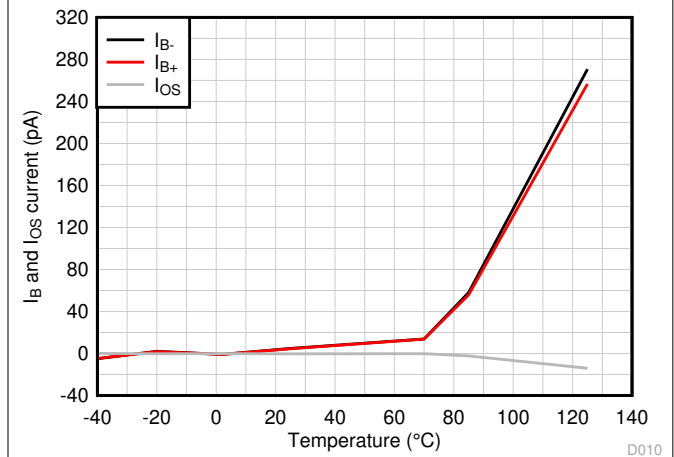


图 7-48.  $I_B$  and  $I_{OS}$  vs Temperature

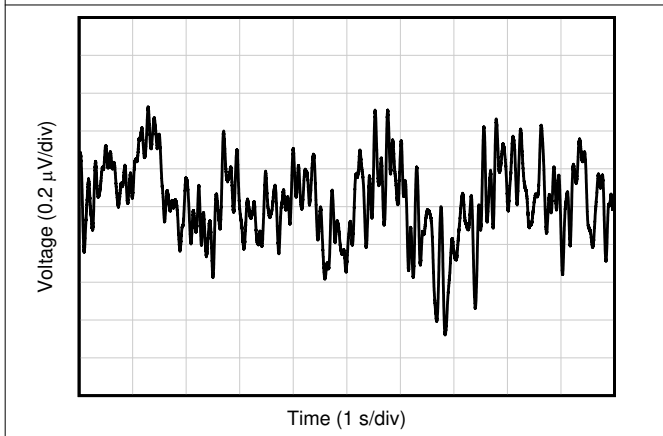


图 7-49. 0.1-Hz to 10-Hz Flicker Noise

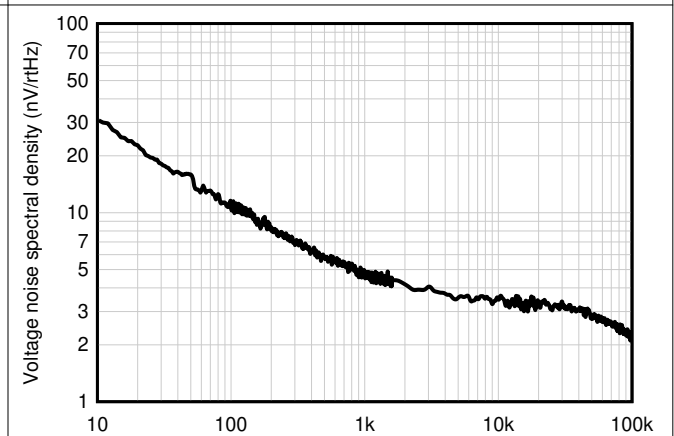


图 7-50. Input Voltage Noise Spectral Density vs Frequency

### 7.8 TLV6742: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.75\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

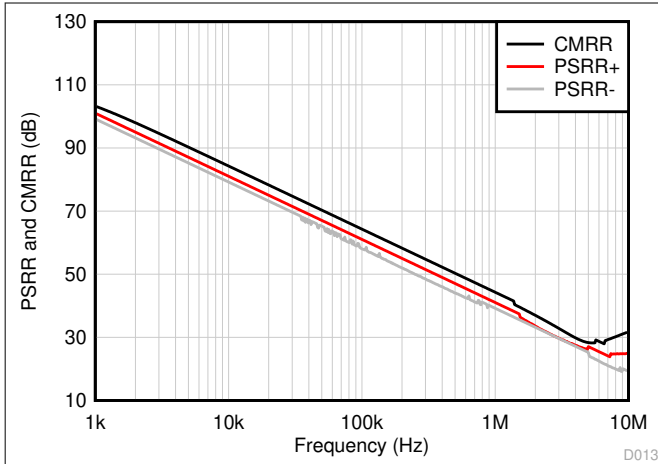
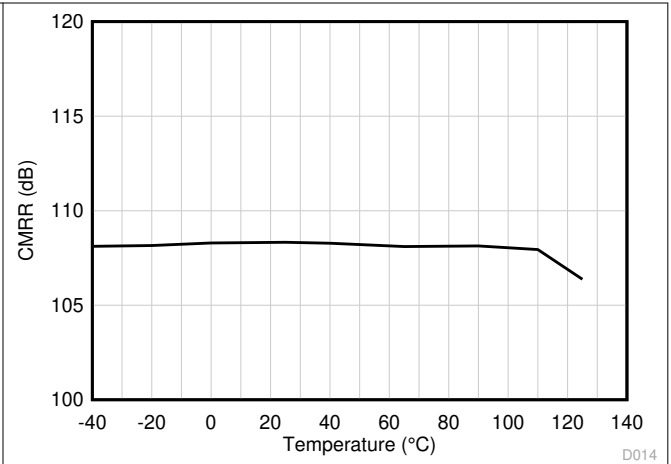
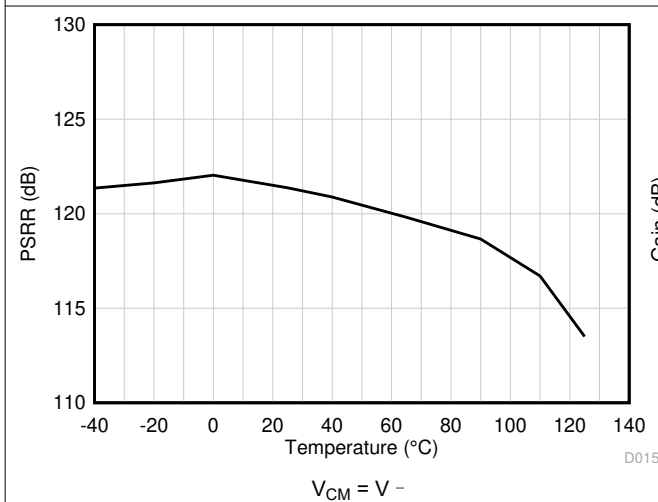


图 7-51. CMRR and PSRR vs Frequency (Referred to Input)



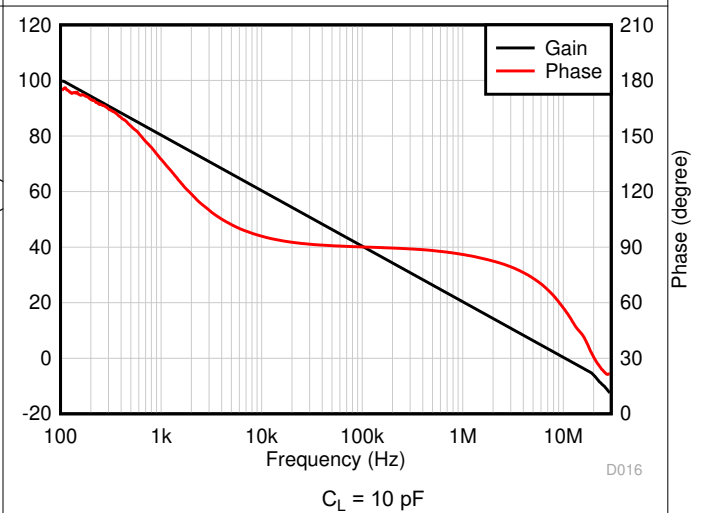
$V_S = 5.5\text{ V}$ ,  $V_{CM} = V^-$  to  $(V^+) - 1.2\text{ V}$

图 7-52. CMRR vs Temperature



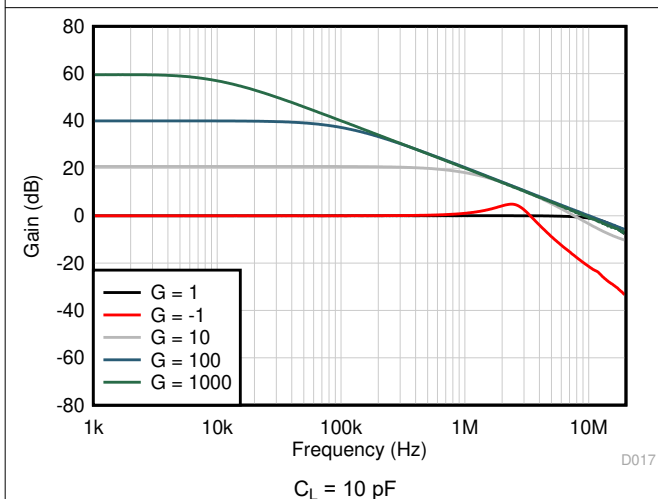
$V_{CM} = V^-$

图 7-53. PSRR vs Temperature



$C_L = 10\text{ pF}$

图 7-54. Open-Loop Gain and Phase vs Frequency



$C_L = 10\text{ pF}$

图 7-55. Closed-Loop Gain vs Frequency

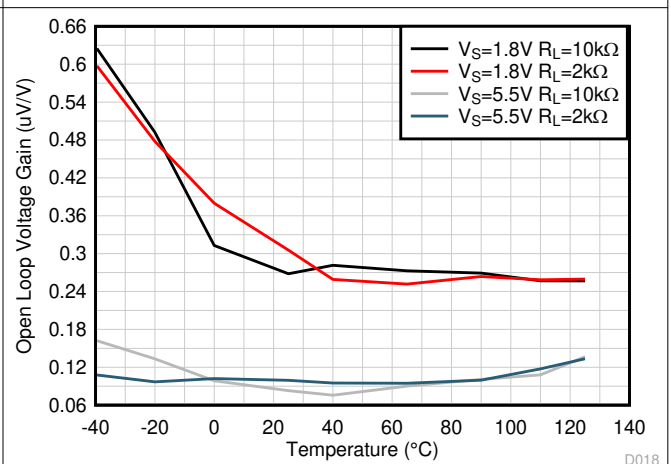


图 7-56. Open-Loop Gain vs Temperature

### 7.8 TLV6742: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.75\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

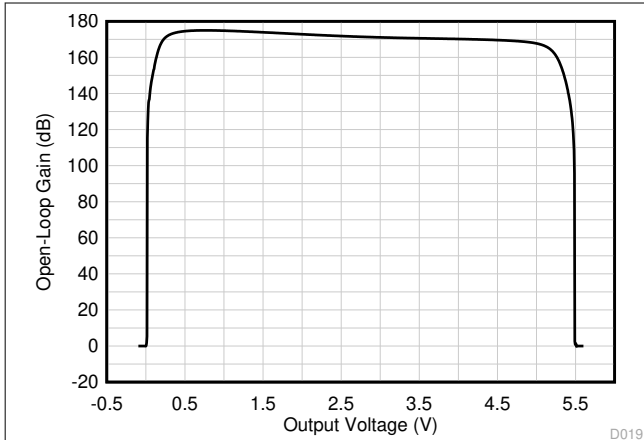


图 7-57. Open-Loop Gain vs Output Voltage

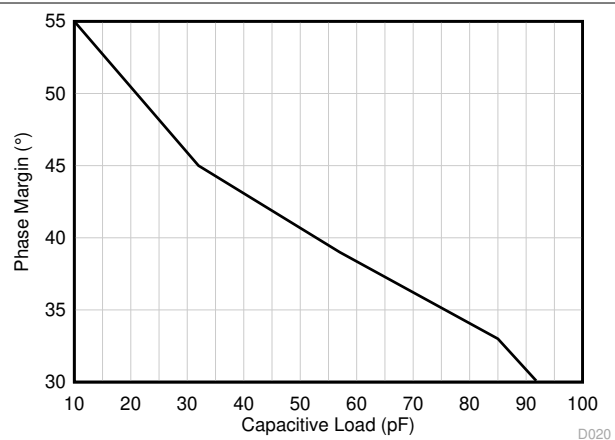


图 7-58. Phase Margin vs Capacitive Load

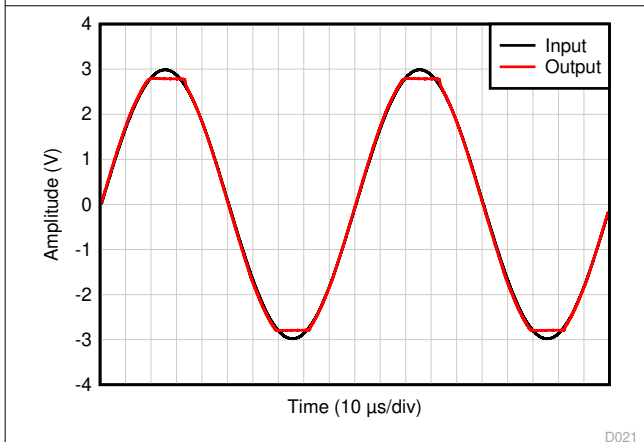
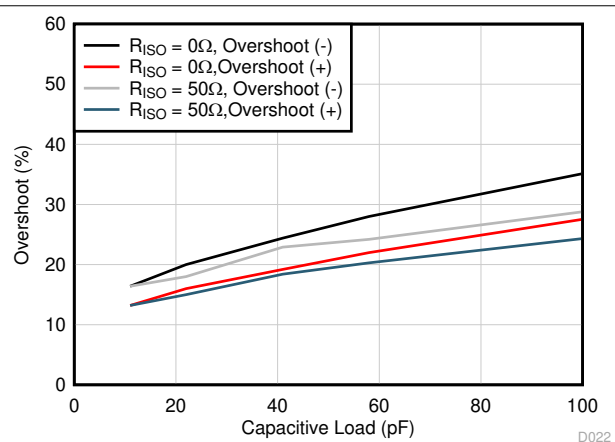
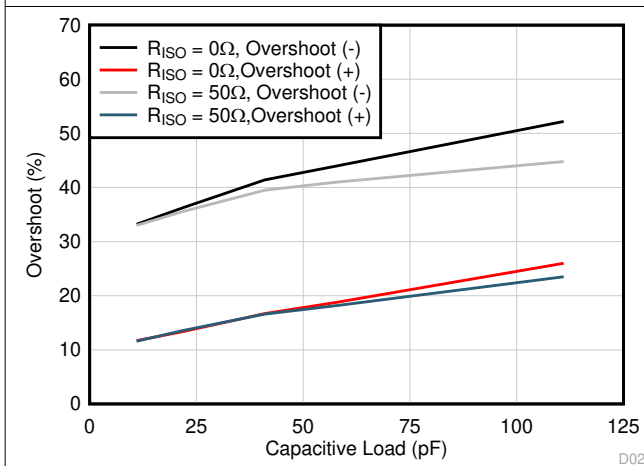


图 7-59. No Phase Reversal



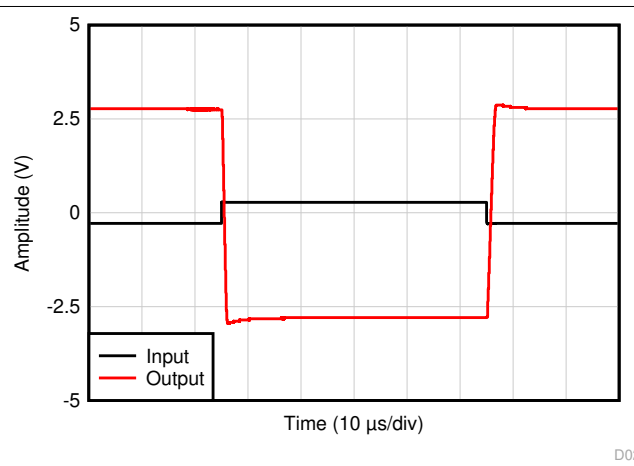
$V_{CM} = V_S / 2$ ,  $R_L = 1\text{ k}\Omega$   
Gain = -1, 100-mV output step

图 7-60. Small-Signal Overshoot vs Load Capacitance



$V_{CM} = V_S / 2$ ,  $R_L = 1\text{ k}\Omega$   
Gain = +1, 100-mV output step

图 7-61. Small-Signal Overshoot vs Load Capacitance

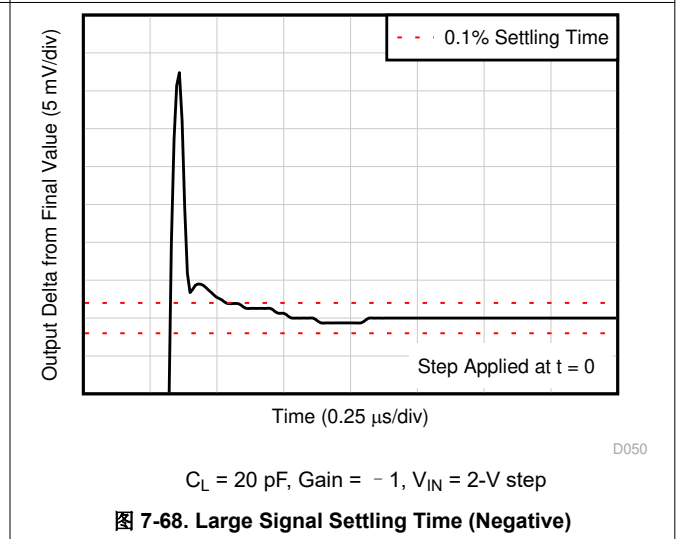
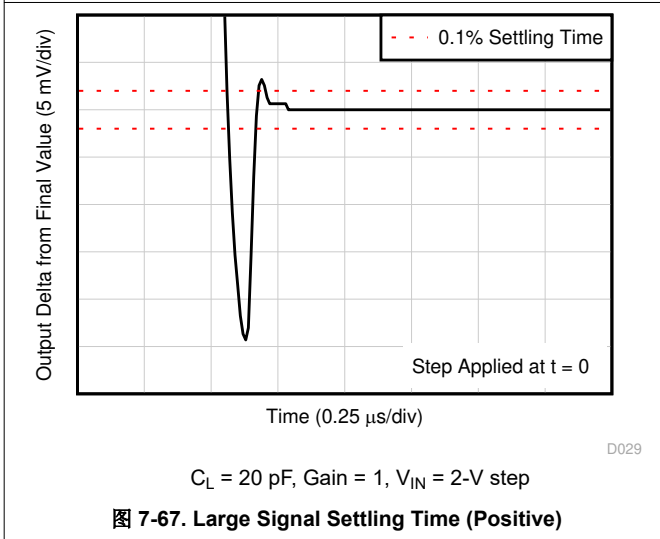
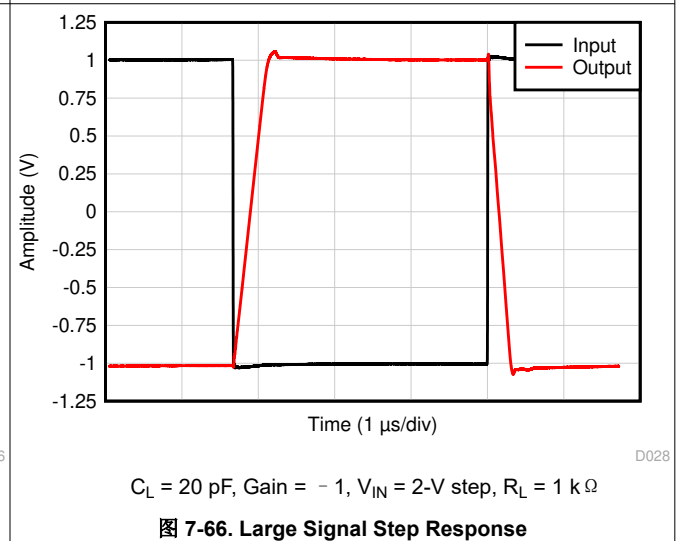
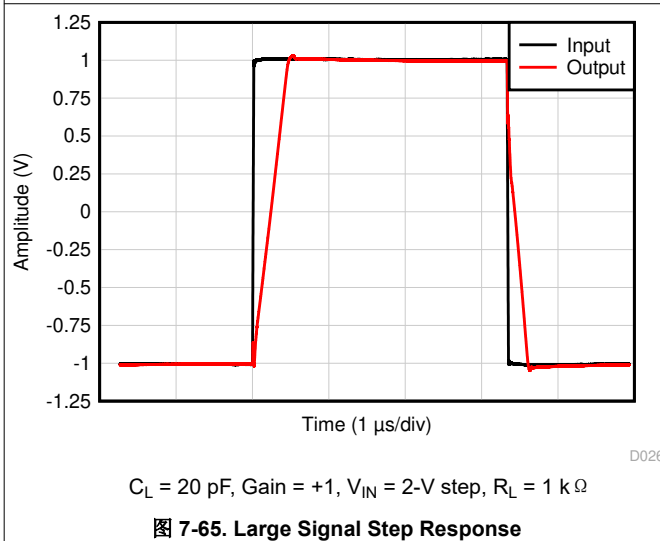
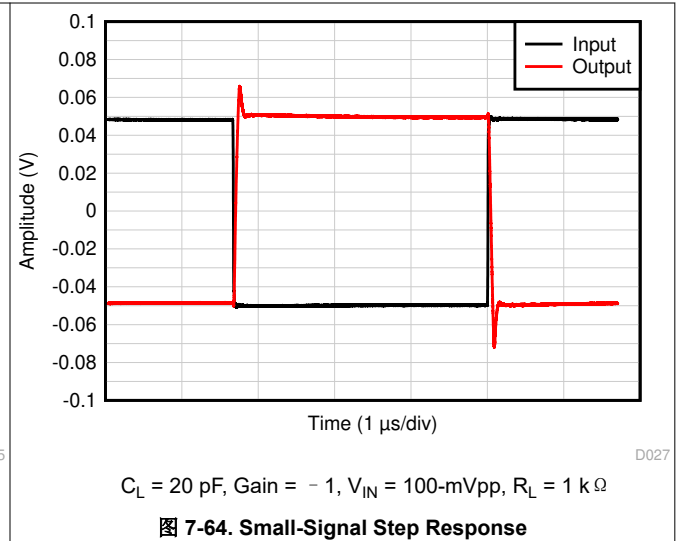
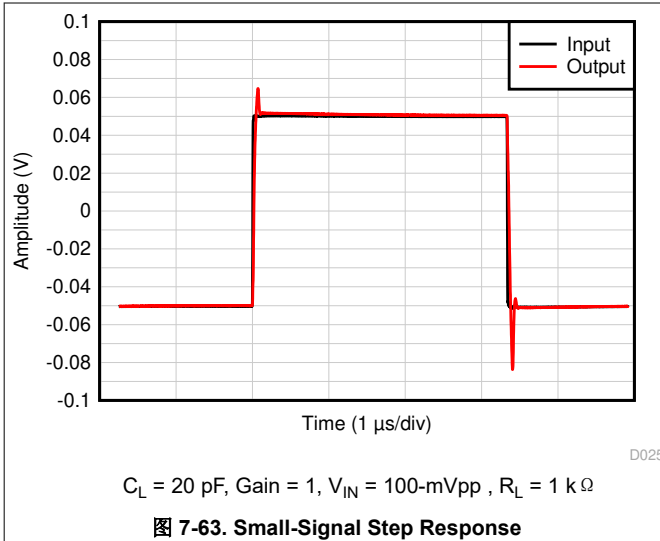


$V_{IN} = 0.6\text{ Vpp}$ ,  $G = -10$ ,  $V_{IN} \times \text{gain} > V_S$

图 7-62. Overload Recovery

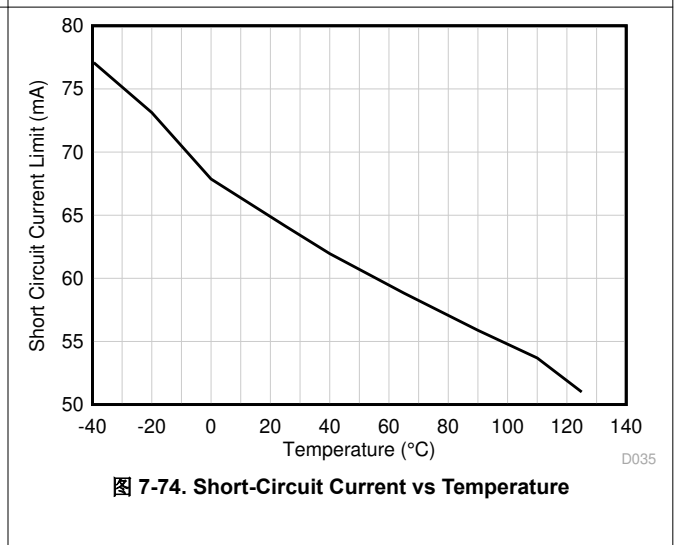
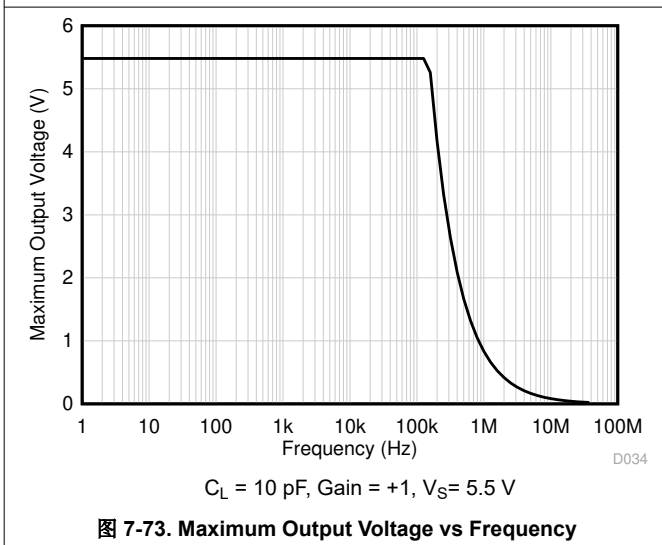
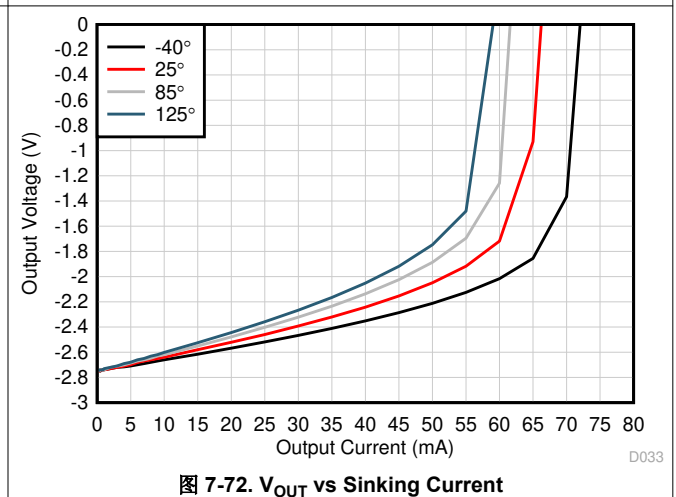
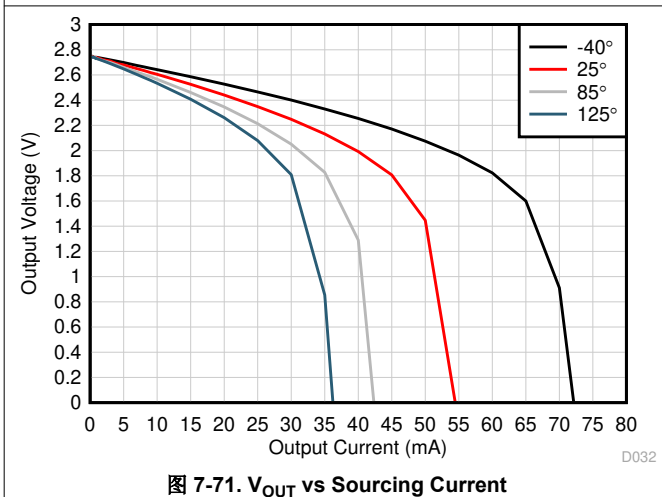
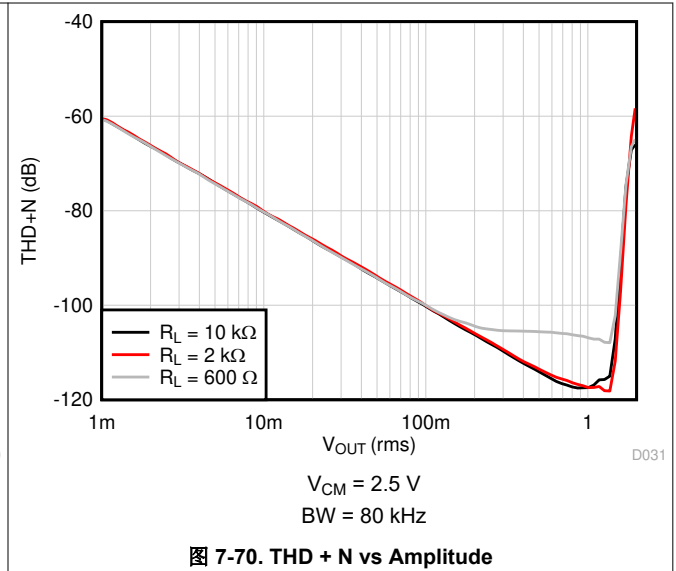
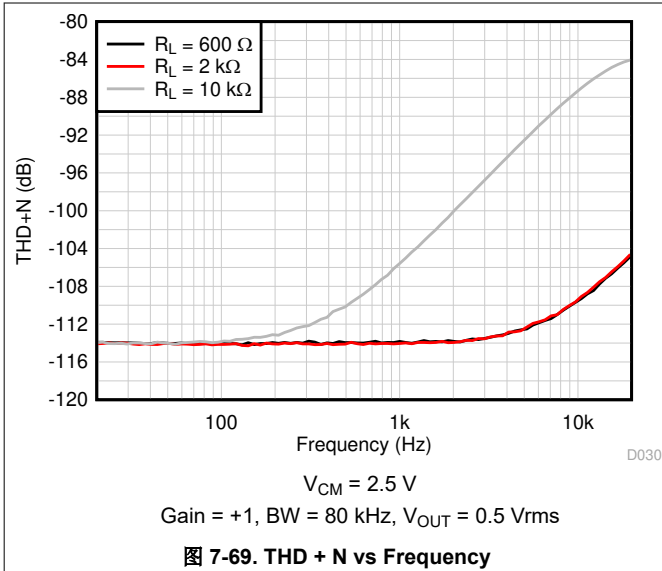
## 7.8 TLV6742: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.75\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.



### 7.8 TLV6742: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.75\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.



### 7.8 TLV6742: Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.75\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

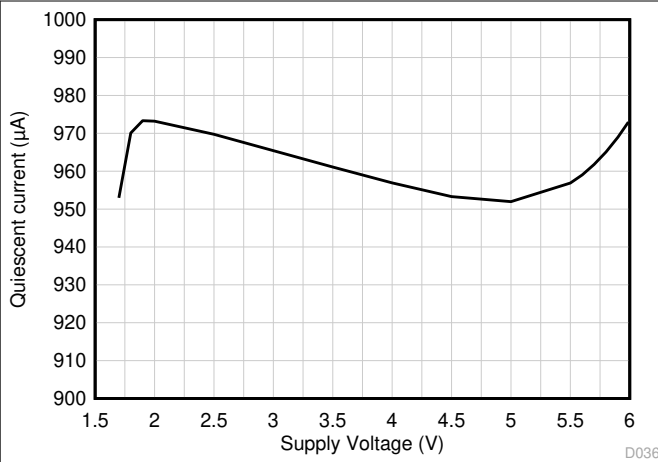


图 7-75. Quiescent Current vs Supply Voltage

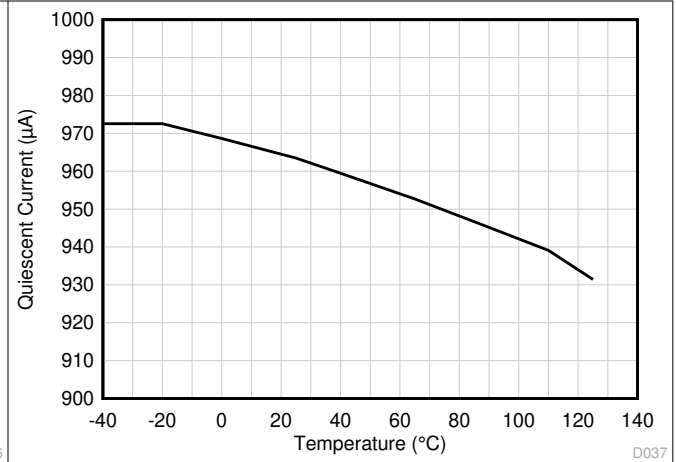


图 7-76. Quiescent Current vs Temperature

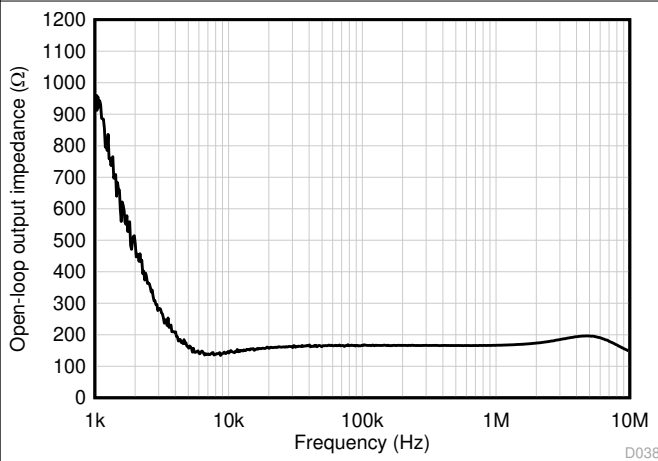
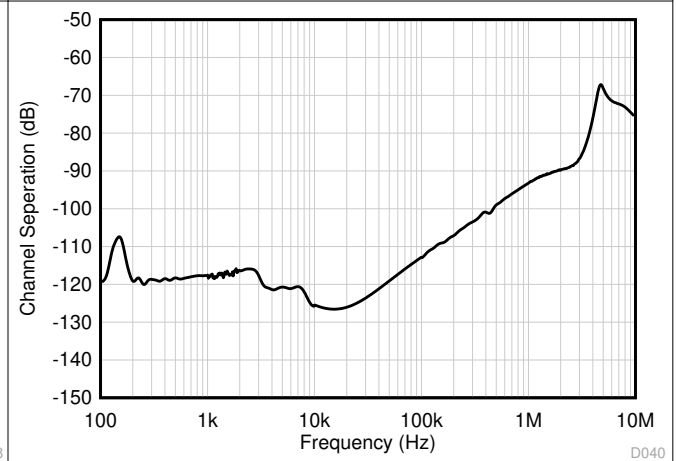


图 7-77. Open-Loop Output Impedance vs Frequency



$A_{VDD} = 5.5\text{ V}$ ,  $V_{ICM} = V_{OCM} = 2.75\text{ V}$

图 7-78. Channel Separation vs Frequency

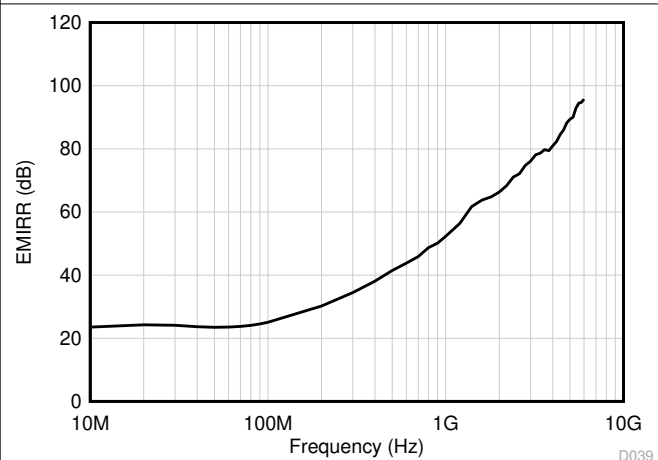
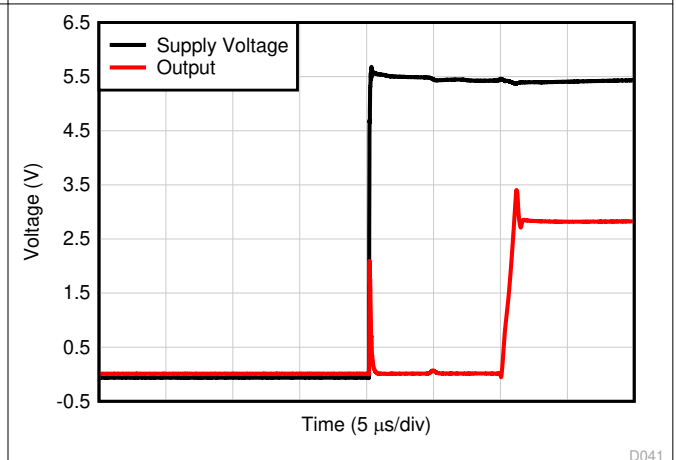


图 7-79. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



$V_S = 0\text{ to }5.5\text{ V}$ ,  $V_{OUT} = 0\text{ to }2.75\text{ V}$

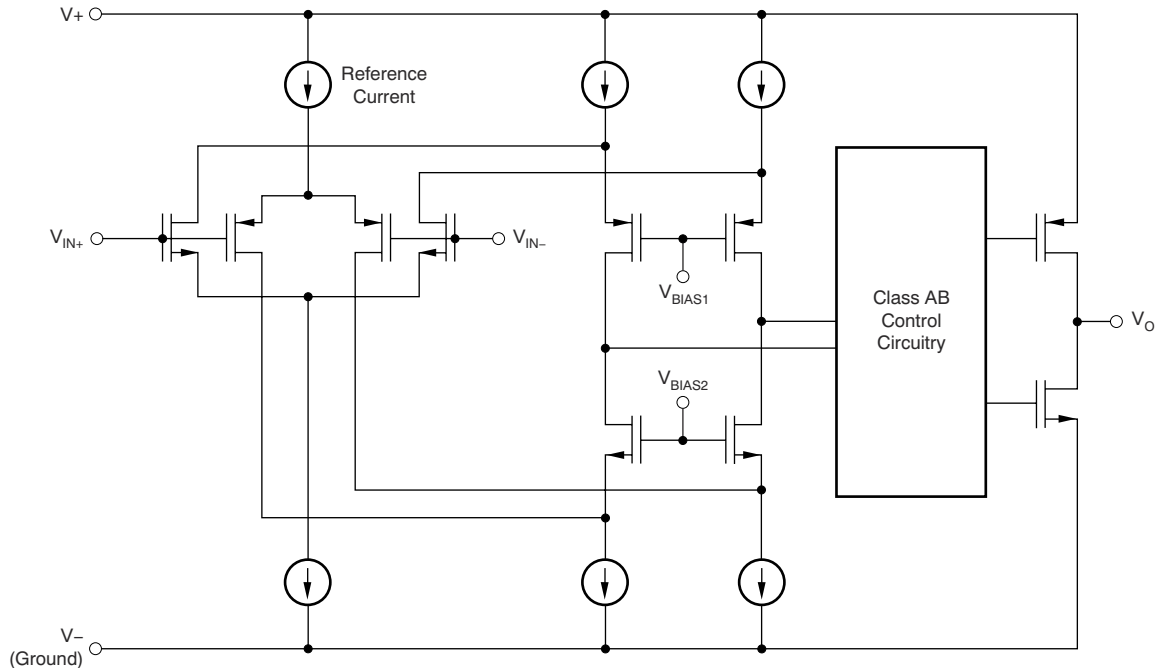
图 7-80. Turn-On Time

## 8 Detailed Description

### 8.1 Overview

The TLV674x family is an ultra low-noise, rail-to-rail output operational amplifier family. These devices operate from a supply voltage of 2.25 V to 5.5 V (TLV6741) and 1.7 V to 5.5 V (TLV6742 and TLV6744), are unity-gain stable, and suitable for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail and allows the TLV674x op amp family to be used in most single-supply applications. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications, and makes it suitable for many audio applications as well as driving sampling analog-to-digital converters (ADCs).

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 THD+ Noise Performance

TLV674x operational amplifier family has excellent distortion characteristics. TLV6742 and TLV6744 THD + Noise is below 0.00015% ( $G = +1$ ,  $V_O = 1 V_{RMS}$ ,  $V_{CM} = 1.8 V$ ,  $V_S = 5.5 V$ ) throughout the audio frequency range, 20 Hz to 20 kHz with a 10-k $\Omega$  load. TLV6741 THD + Noise is below 0.00035% ( $G = +1$ ,  $V_O = 1 V_{RMS}$ ,  $V_{CM} = 2.5 V$ ,  $V_S = 5.5 V$ ) throughout the audio frequency range, 20 Hz to 20 kHz, with a 10-k $\Omega$  load. Broadband noise of 3.5 nV/ $\sqrt{Hz}$  (TLV6742/4) and 3.7 nV/ $\sqrt{Hz}$  (TLV6741) is extremely low for a 10-MHz general purpose amplifier.

#### 8.3.2 Operating Voltage

The TLV674x operational amplifier family is fully specified and assured for operation from 1.7 V to 5.5 V (TLV6742/4) and 2.25 V to 5.5 V (TLV6741). In addition, many specifications apply from  $-40^\circ C$  to  $125^\circ C$ . Power-supply pins should be bypassed with 0.1- $\mu F$  ceramic capacitors.

#### 8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV674x devices deliver a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-k $\Omega$ , the output swings to within a few mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails, see [图 7-11](#).

### 8.3.4 EMI Rejection

The TLV674x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV674x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 8-1 shows the results of this testing on the TLV674x. 表 8-1 shows the EMIRR IN+ values for the TLV674x at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational Amplifiers](#) application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from [www.ti.com](http://www.ti.com).

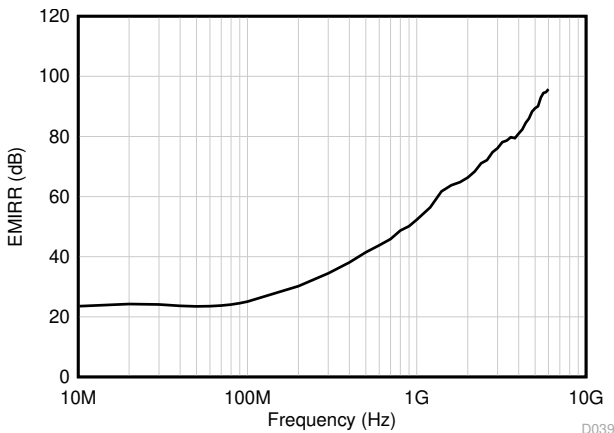


图 8-1. EMIRR Testing

表 8-1. TLV674x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

### 8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 8-2 shows an illustration of the ESD circuits contained in the TLV674x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

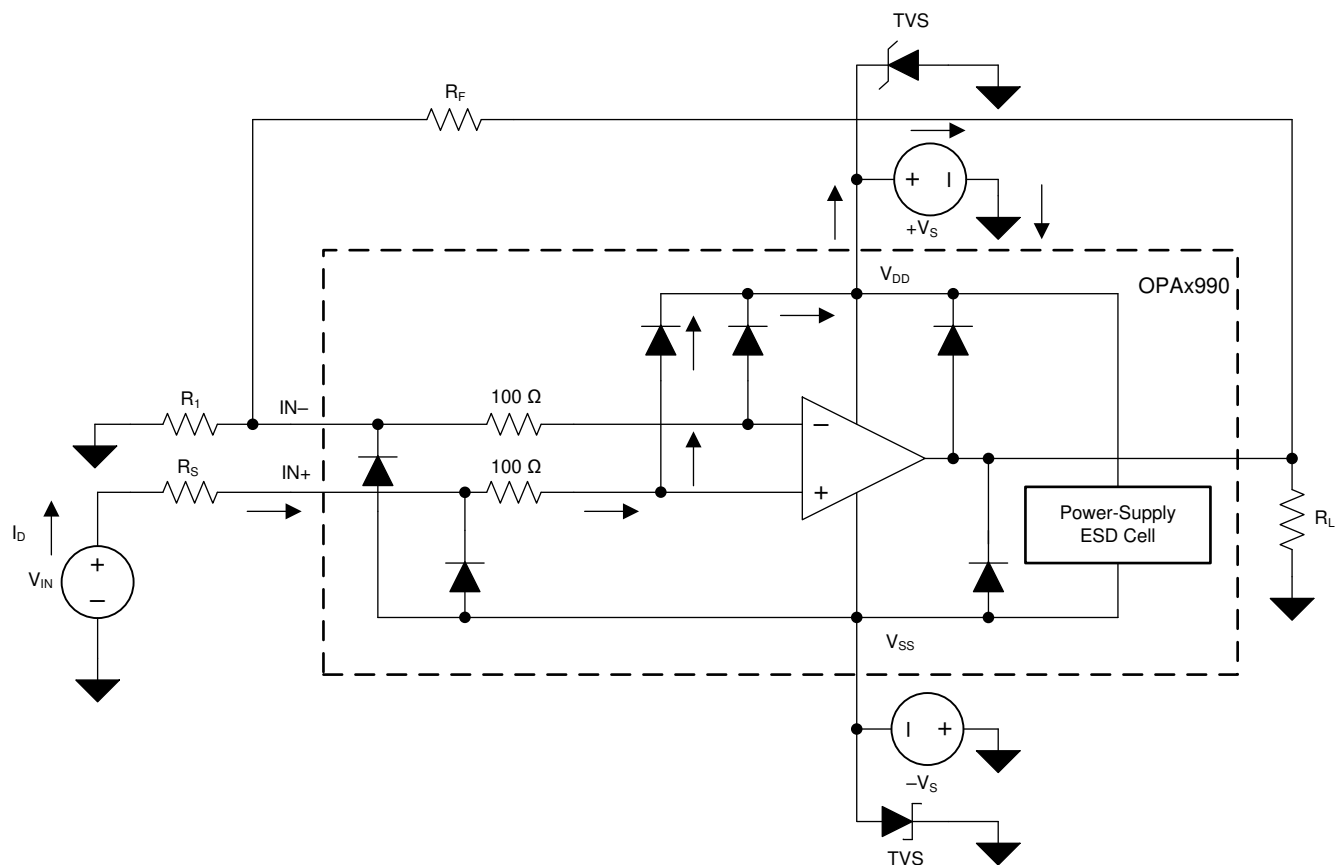


图 8-2. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long in duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressor (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

The TLV674x family incorporates internal electrostatic discharge (ESD) protection circuits on all pins, as shown above. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in 节 7.1. 图 8-3 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

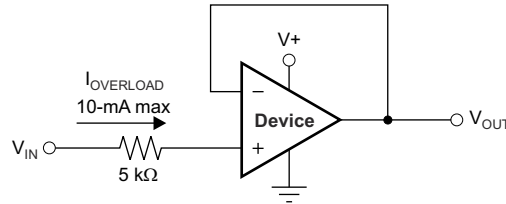


图 8-3. Input Current Protection

### 8.3.6 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal*, distributions and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in 节 7.6.

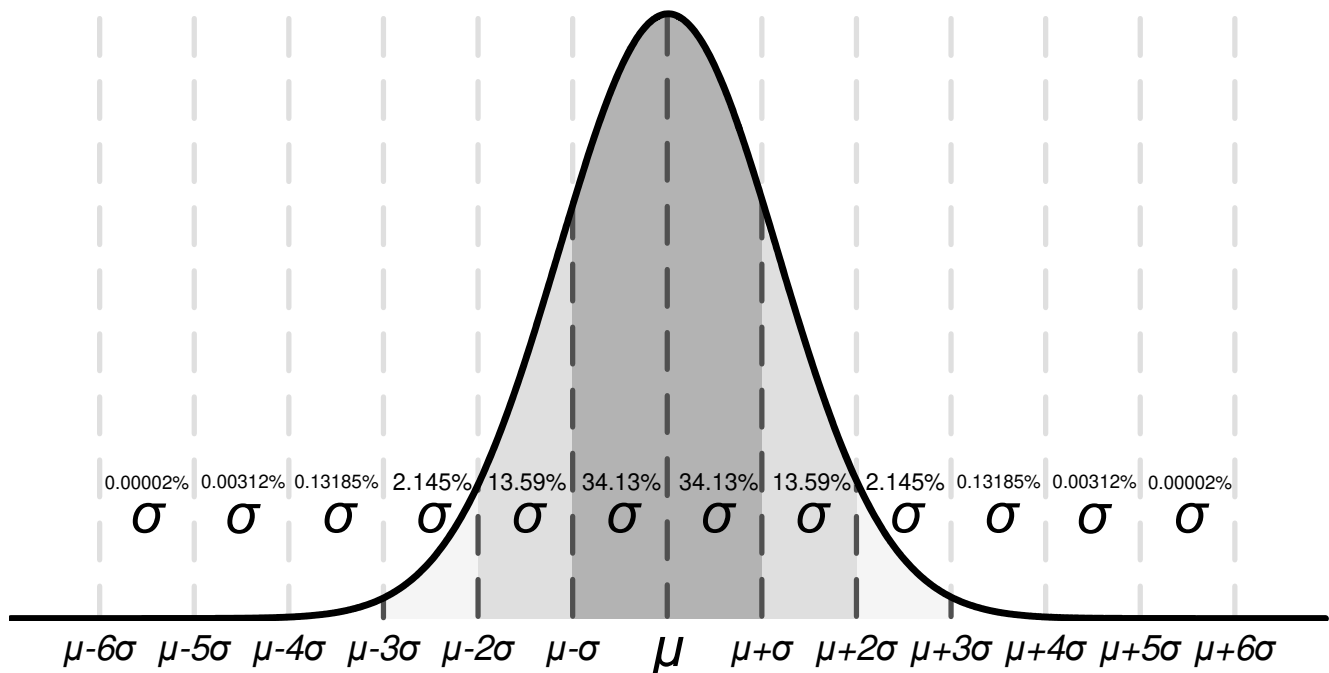


图 8-4. Ideal Gaussian Distribution

图 8-4 shows an example distribution, where  $\mu$ , or *mu*, is the mean of the distribution, and where  $\sigma$ , or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from  $\mu - \sigma$  to  $\mu + \sigma$ ).

Depending on the specification, values listed in the *typical* column of 节 7.6 are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean ( $\mu$ ). However, if a specification naturally has a mean near zero (like input

offset voltage), then the typical value is equal to the mean plus one standard deviation ( $\mu + \sigma$ ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV6742, the typical input voltage offset is 150  $\mu\text{V}$ , so 68.2% of all TLV6742 devices are expected to have an offset from -150  $\mu\text{V}$  to 150  $\mu\text{V}$ .

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV6742 device has a maximum offset voltage of 1.0 mV at 25°C, and even though this corresponds to 5  $\sigma$  ( $\approx 1$  in 1.7 million units), which is extremely unlikely, TI assures that any unit with a larger offset than 1.0 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6  $\sigma$  value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV6742 does not have a maximum or minimum for offset voltage drift, but based on [Figure 7-40](#) and the typical value of 0.2  $\mu\text{V}/^\circ\text{C}$  in [Section 7.6](#), it can be calculated that the 6- $\sigma$  value for offset voltage drift is about 1.0  $\mu\text{V}/^\circ\text{C}$ . When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

### 8.3.7 Shutdown Function

The TLV674xS devices feature  $\overline{\text{SHDN}}$  pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1  $\mu\text{A}$ . The  $\overline{\text{SHDN}}$  pins are active-low, meaning that shutdown mode is enabled when the input to the  $\overline{\text{SHDN}}$  pin is a valid logic low.

The  $\overline{\text{SHDN}}$  pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) above the negative rail. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the  $\overline{\text{SHDN}}$  pins should be driven with valid logic signals. A valid logic low is defined as a voltage between  $V^-$  and  $V^- + 0.2\text{ V}$ . A valid logic high is defined as a voltage between  $V^- + 1.2\text{ V}$  and  $V^+$ . The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit. There is **no** internal pull-up to enable the amplifier.

The  $\overline{\text{SHDN}}$  pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 15  $\mu\text{s}$  for full shutdown of all channels; disable time is 3  $\mu\text{s}$ . When disabled, the output assumes a high-impedance state. This architecture allows the TLV674xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time ( $t_{\text{OFF}}$ ) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-k  $\Omega$  load to midsupply ( $V_S / 2$ ) is required. If using the TLV674xS without a load, the resulting turnoff time is significantly increased.

### 8.3.8 Packages With an Exposed Thermal Pad

The TLV674x family is available in packages such as the WSON-8 (DSG) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to  $V^-$  or left floating. Attaching the thermal pad to a potential other than  $V^-$  is not allowed, and performance of the device is not assured when doing so.

## 8.4 Device Functional Modes

The TLV674x family has a single functional mode. The TLV6742 and TLV6744 are powered on as long as the power-supply voltage is between 1.7 V ( $\pm 0.85$  V) and 5.5 V ( $\pm 2.75$  V). The TLV6741 is powered on as long as the power-supply voltage is between 2.25 V ( $\pm 1.125$  V) and 5.5 V ( $\pm 2.75$  V).

## 9 Application and Implementation

### Note

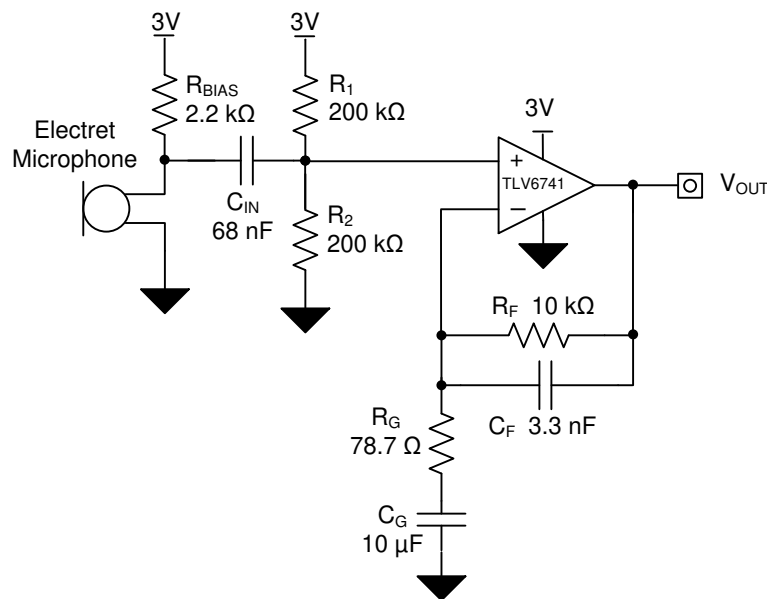
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TLV674x family features 10-MHz bandwidth and 4.5-V/ $\mu$ s slew rate with only 890- $\mu$ A (TLV6741), 990- $\mu$ A (TLV6742/4) of supply current per channel, providing good AC performance at very-low-power consumption. DC applications are well served with a very-low input noise voltage of 3.5 nV / $\sqrt{\text{Hz}}$  (TLV6742/4), 3.7 nV /  $\sqrt{\text{Hz}}$  (TLV6741) at 10 kHz, low input bias current, and a typical input offset voltage of 0.15 mV.

### 9.2 Single-Supply Electret Microphone Preamp with Speech Filter

Electret microphones are commonly used in portable electronics because of their small size, low cost, and relatively good signal-to-noise ratio (SNR). The small package size, low operating voltage and excellent AC performance of the TLV674x family make it an excellent choice for preamplifier circuits for electret microphones. The circuit shown in [Figure 9-1](#) is a single-supply preamplifier circuit for electret microphones, highlighting the TLV6741 device.



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**Figure 9-1. Microphone Preamplifier**

#### 9.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 3 V
- Input: 7.93 mV<sub>RMS</sub> (0.63 Pa with a -38 dB SPL microphone)
- Output: 1 V<sub>RMS</sub>
- Bandwidth: 300 Hz to 3 kHz

#### 9.2.2 Detailed Design Procedure

The transfer function defining the relationship between  $V_{OUT}$  and the AC input signal is shown in [Equation 1](#):

$$V_{OUT} = V_{IN\_AC} \times \left( 1 + \frac{R_F}{R_G} \right) \quad (1)$$

The required gain can be calculated based on the expected input signal level and desired output level as shown in [方程式 2](#):

$$G_{OPA} = \frac{V_{OUT}}{V_{IN\_AC}} = \frac{1V_{RMS}}{7.93mV_{RMS}} = 126 \frac{V}{V} \quad (2)$$

Select a standard 10-k  $\Omega$  feedback resistor and calculate  $R_G$ .

$$R_G = \frac{R_F}{G_{OPA} - 1} = \frac{10k\Omega}{126 \frac{V}{V} - 1} = 80\Omega \rightarrow 78.7\Omega \text{ (closest standard value)} \quad (3)$$

To minimize the attenuation in the desired passband from 300 Hz to 3 kHz, set the upper ( $f_H$ ) and lower ( $f_L$ ) cutoff frequencies outside of the desired bandwidth as:

$$f_L = 200 \text{ Hz} \quad (4)$$

and

$$f_H = 5 \text{ kHz} \quad (5)$$

Select  $C_G$  to set the  $f_L$  cutoff frequency using [方程式 6](#):

$$C_G = \frac{1}{2 \times \pi \times R_G \times f_L} = \frac{1}{2 \times \pi \times 78.7\Omega \times 200\text{Hz}} = 10.11\mu F \rightarrow 10\mu F \quad (6)$$

Select  $C_F$  to set the  $f_H$  cutoff frequency using [方程式 7](#):

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_H} = \frac{1}{2 \times \pi \times 10k\Omega \times 5k\text{Hz}} = 3.18nF \rightarrow 3.3nF \text{ (Standard Value)} \quad (7)$$

The input signal cutoff frequency should be set low enough such that low-frequency sound waves still pass through. Therefore select  $C_{IN}$  to achieve a 30-Hz cutoff frequency ( $f_{IN}$ ) using [方程式 8](#):

$$C_{IN} = \frac{1}{2 \times \pi \times (R_1 \parallel R_2) \times f_{IN}} = \frac{1}{2 \times \pi \times 100k\Omega \times 30\text{Hz}} = 53nF \rightarrow 68nF \text{ (Standard Value)} \quad (8)$$

The measured transfer function for the microphone preamplifier circuit is shown in [图 9-2](#) and the measured THD+N performance of the microphone preamplifier circuit is shown in [图 9-3](#).

### 9.2.3 Application Curves

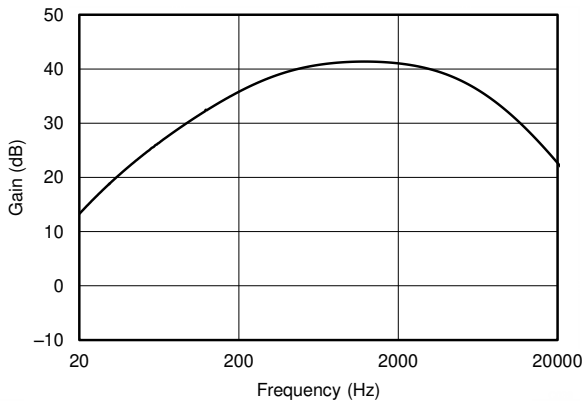


图 9-2. Gain vs Frequency

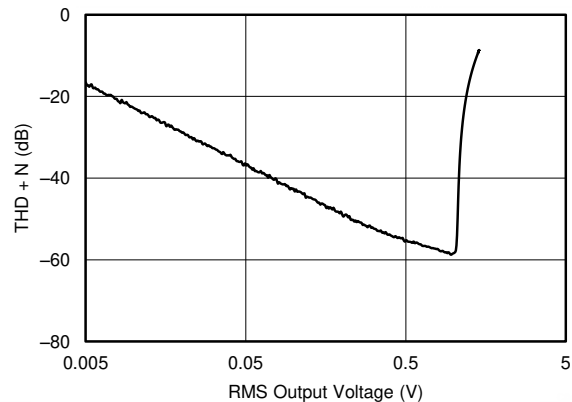


图 9-3. THD + N vs RMS Output Voltage

## 10 Power Supply Recommendations

The TLV6742 and TLV6744 devices are specified for operation from 1.7 V to 5.5 V ( $\pm 0.85$  V to  $\pm 2.75$  V). The TLV6741 device is specified for operation from 2.25 V to 5.5 V ( $\pm 1.125$  V to  $\pm 2.75$  V). Many specifications of the TLV674x family apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### CAUTION

Supply voltages larger than 7 V can permanently damage the device (see [节 7.1](#)).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [节 11.1](#).

## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Figure 11-1](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Example

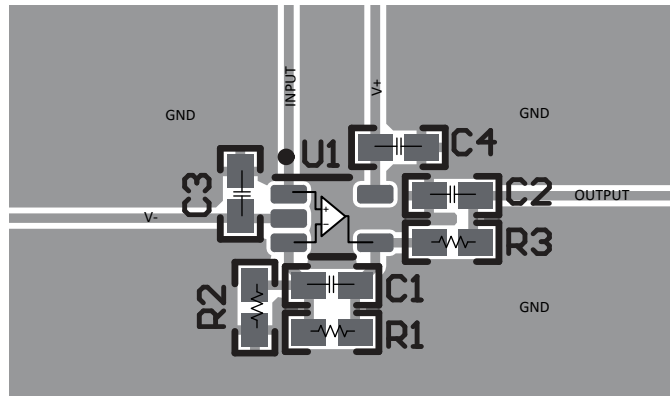
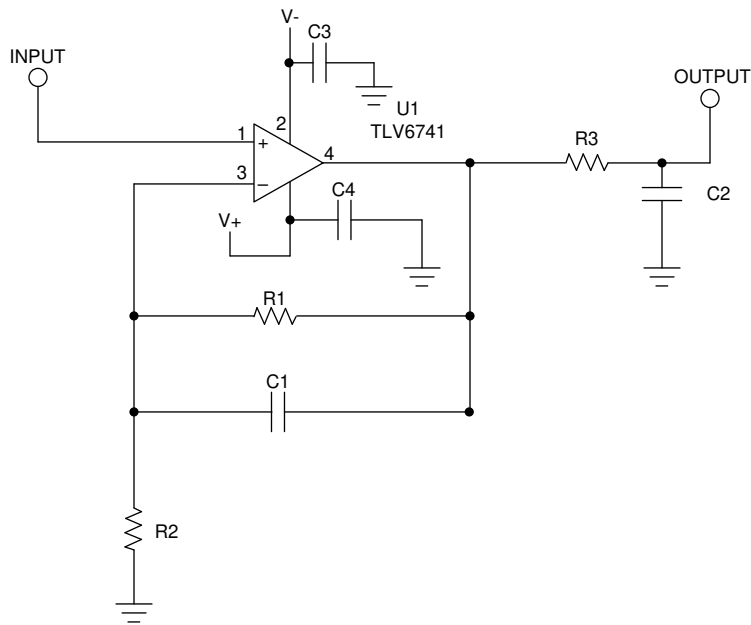


图 11-1. Operational Amplifier Board Layout for Noninverting Configuration



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图 11-2. Schematic Used for Layout Example

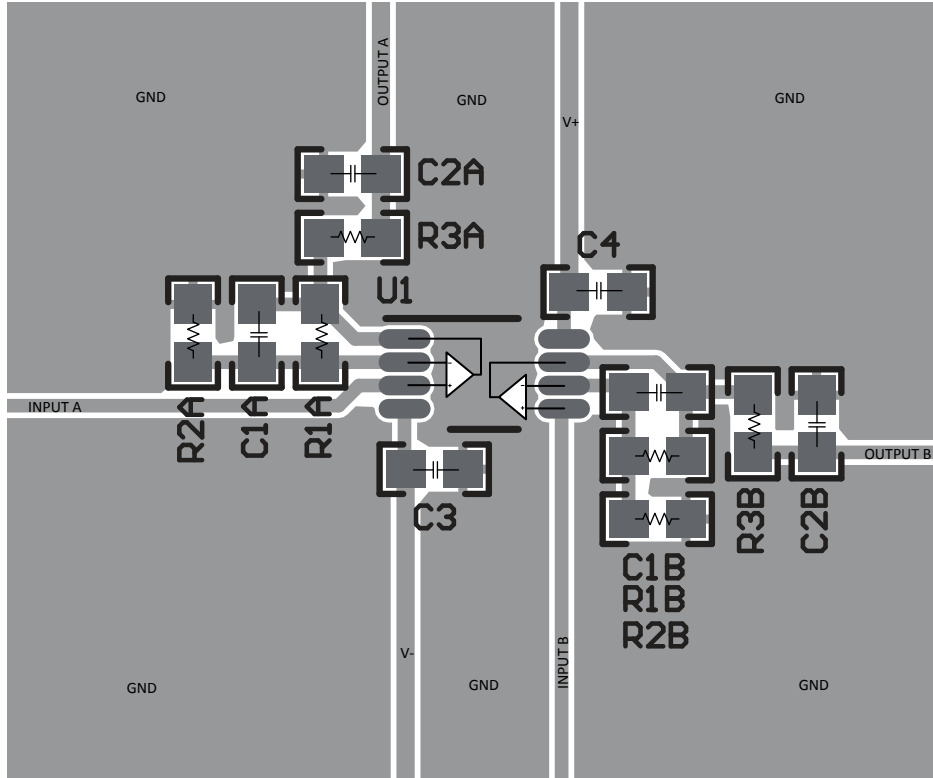


图 11-3. Example Layout for VSSOP-8 (DGK) Package

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [QFN/SON PCB Attachment.](#)
- [Quad Flatpack No-Lead Logic Packages.](#)
- [EMI Rejection Ratio of Operational Amplifiers.](#)

### 12.2 接收文档更新通知

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### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV6741DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18E	<a href="#">Samples</a>
TLV6741DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18E	<a href="#">Samples</a>
TLV6742IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42D	<a href="#">Samples</a>
TLV6742IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2H8T	<a href="#">Samples</a>
TLV6742IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T6742D	<a href="#">Samples</a>
TLV6742IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D42S	<a href="#">Samples</a>
TLV6742IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T6742P	<a href="#">Samples</a>
TLV6742SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	HHF	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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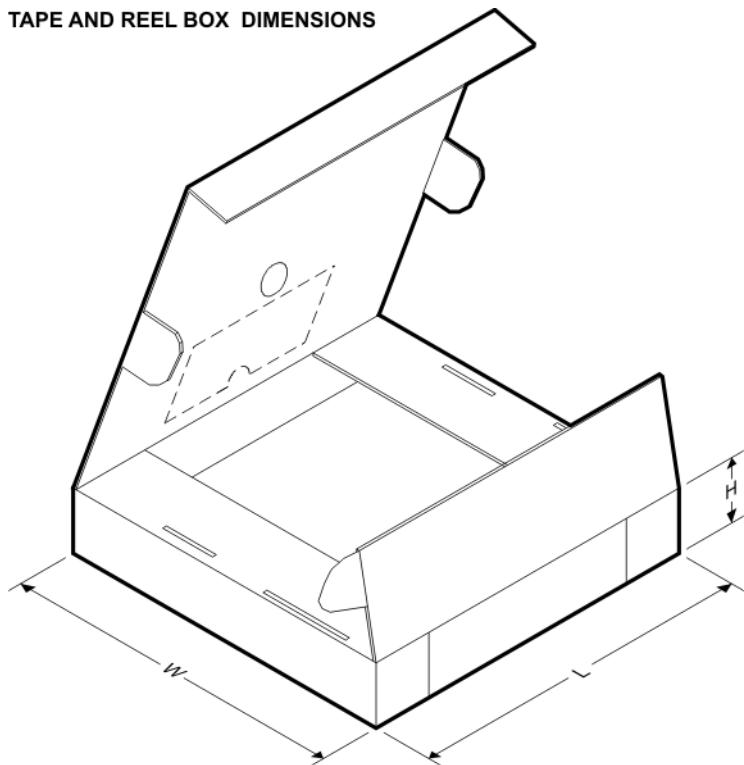
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6741DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV6741DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV6742IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6742IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV6742IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV6742IDSGR	WSO8	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV6742IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV6742SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1

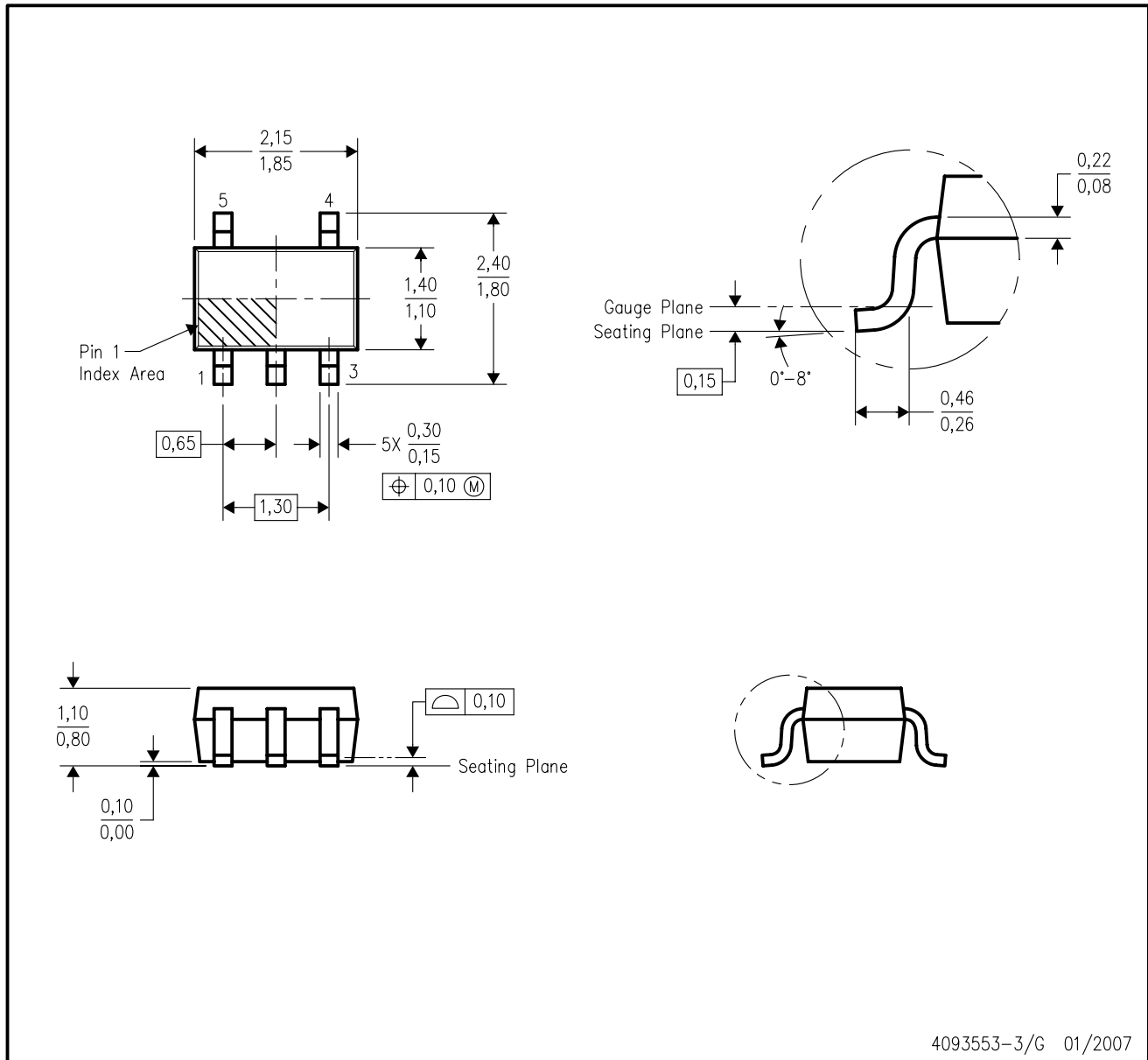
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6741DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV6741DCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV6742IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV6742IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV6742IDR	SOIC	D	8	2500	853.0	449.0	35.0
TLV6742IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV6742IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV6742SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0

DCK (R-PDSO-G5)

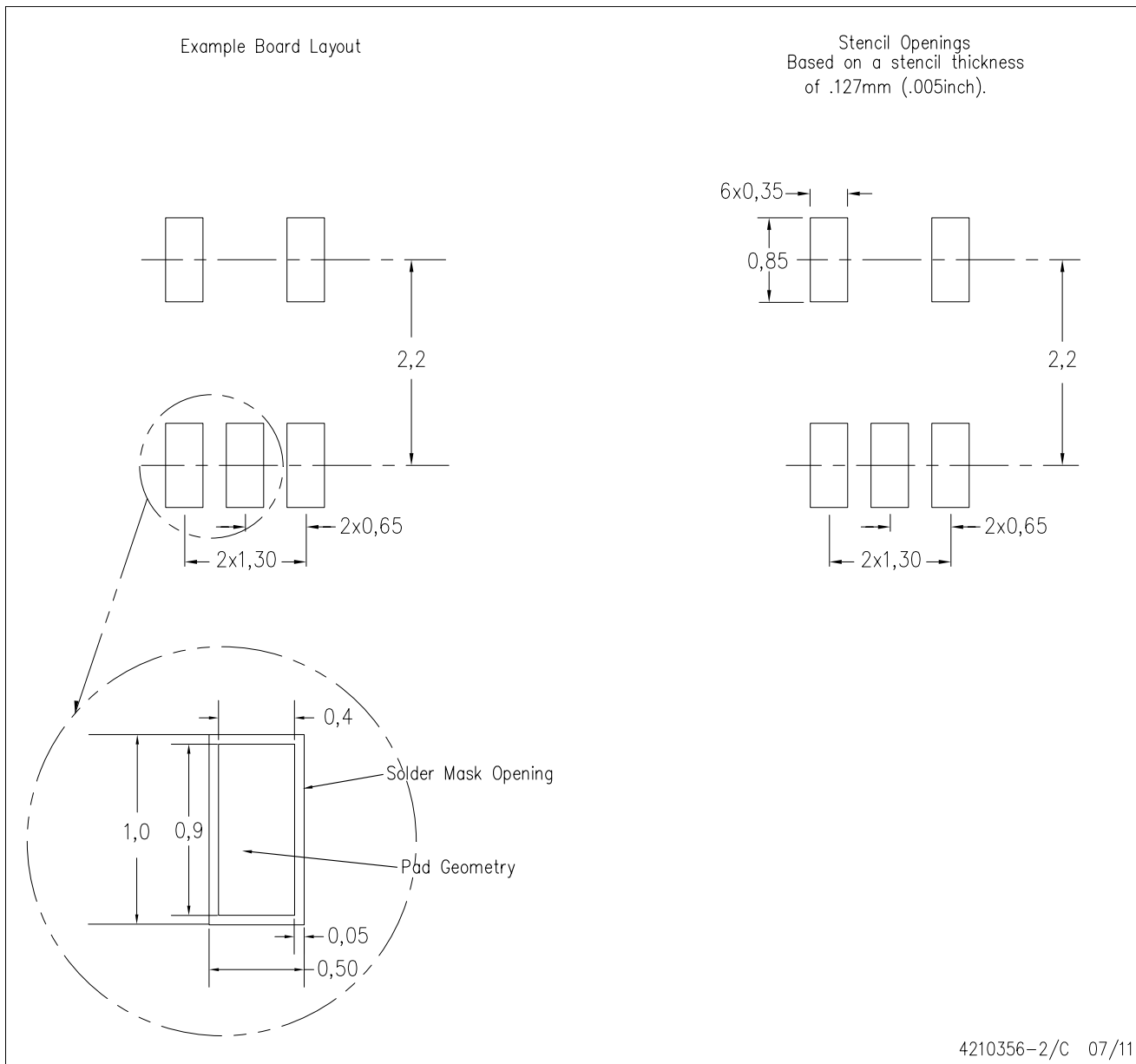
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

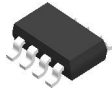
DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

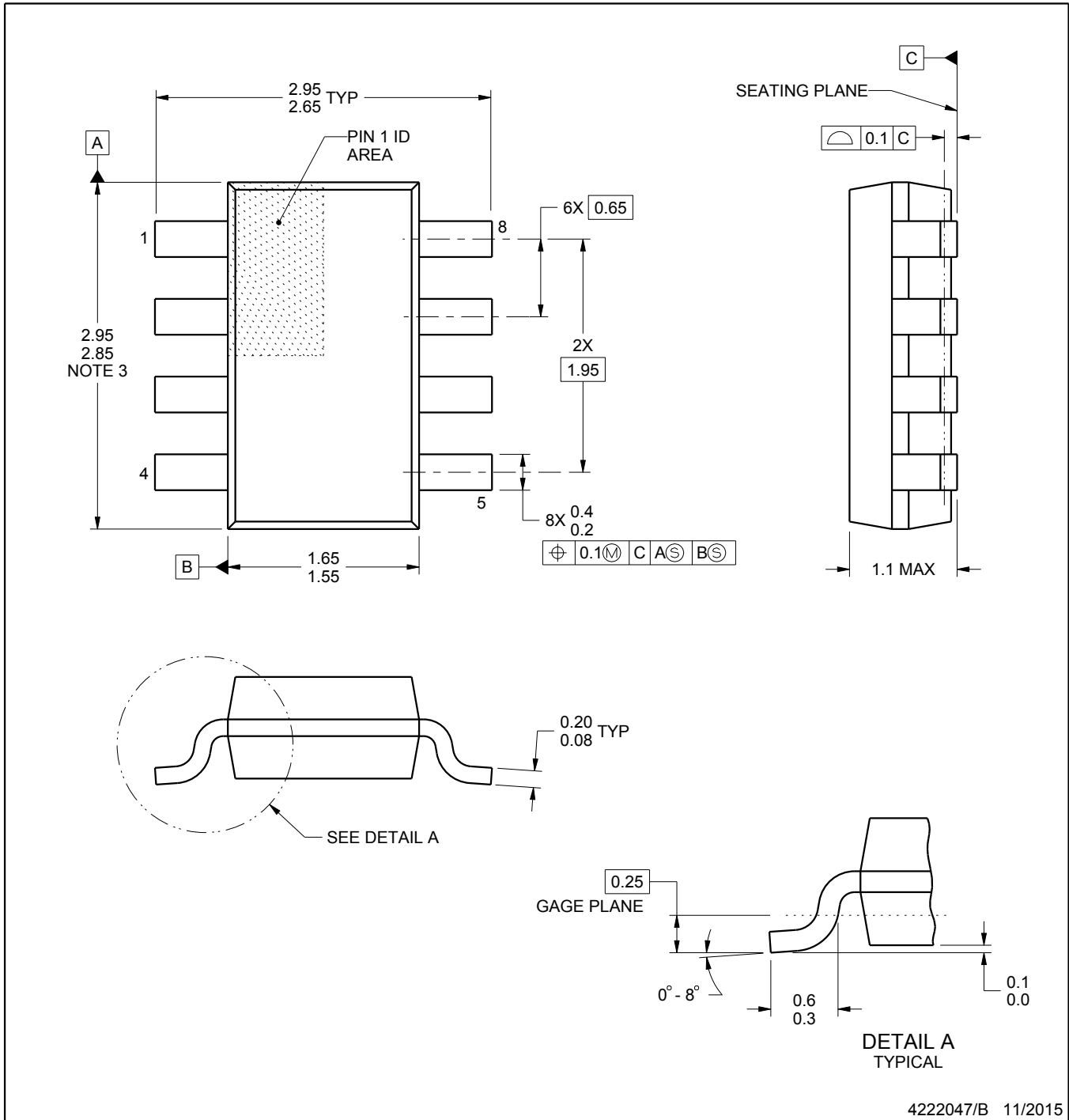
# DDF0008A



# PACKAGE OUTLINE

## SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



**NOTES:**

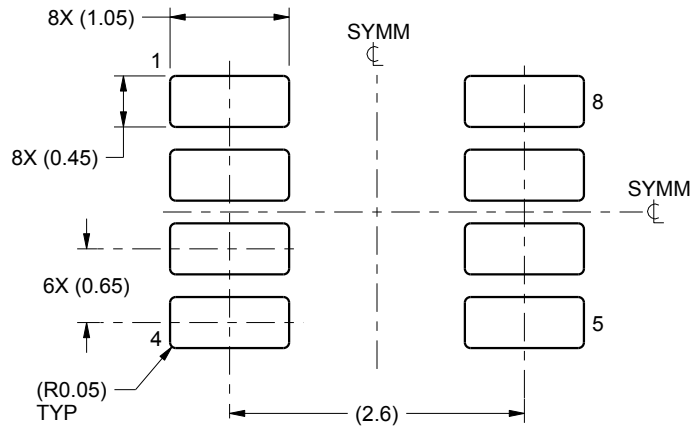
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

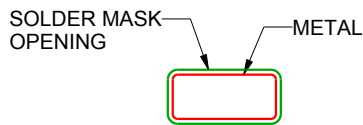
DDF0008A

SOT-23 - 1.1 mm max height

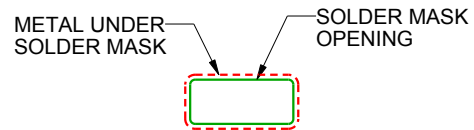
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

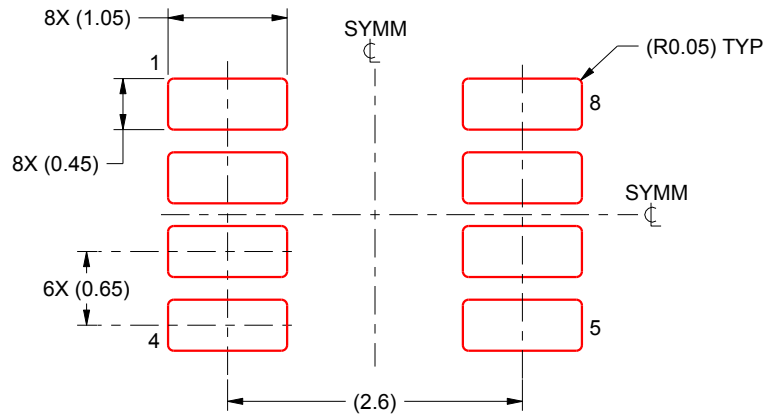
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

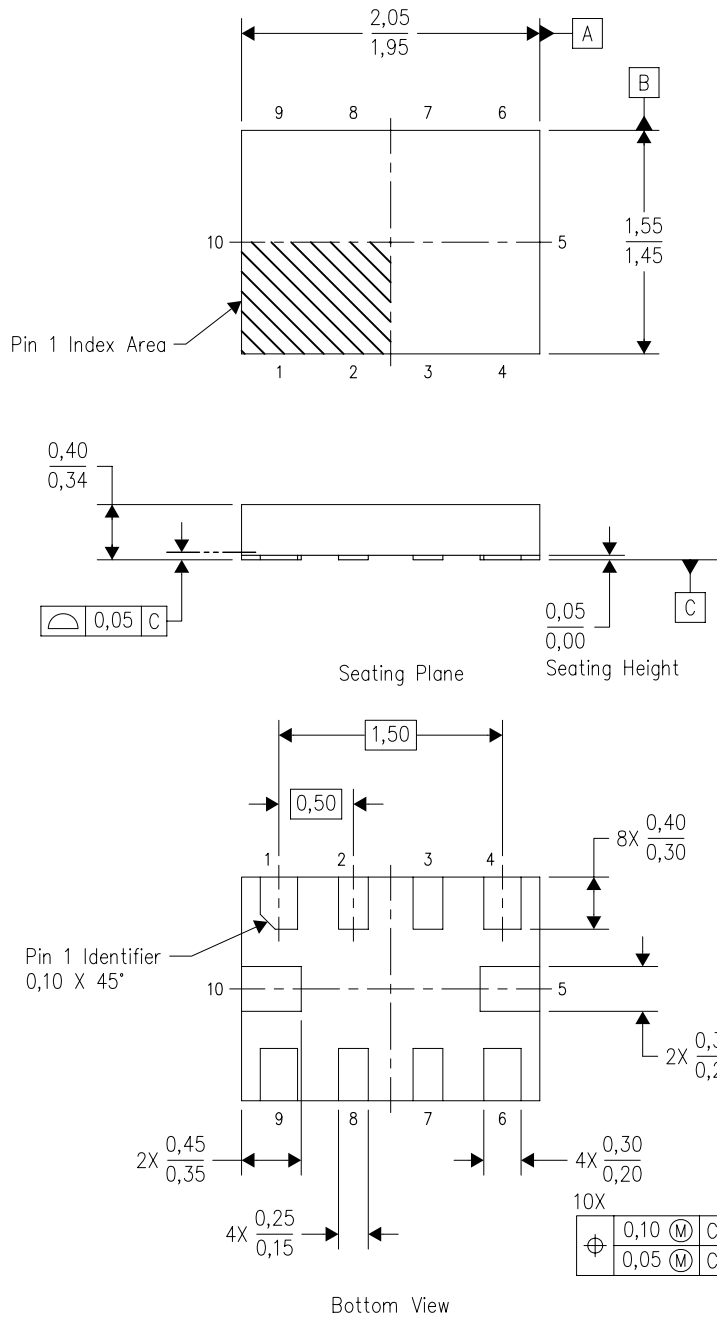
4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

RUG (R-PQFP-N10)

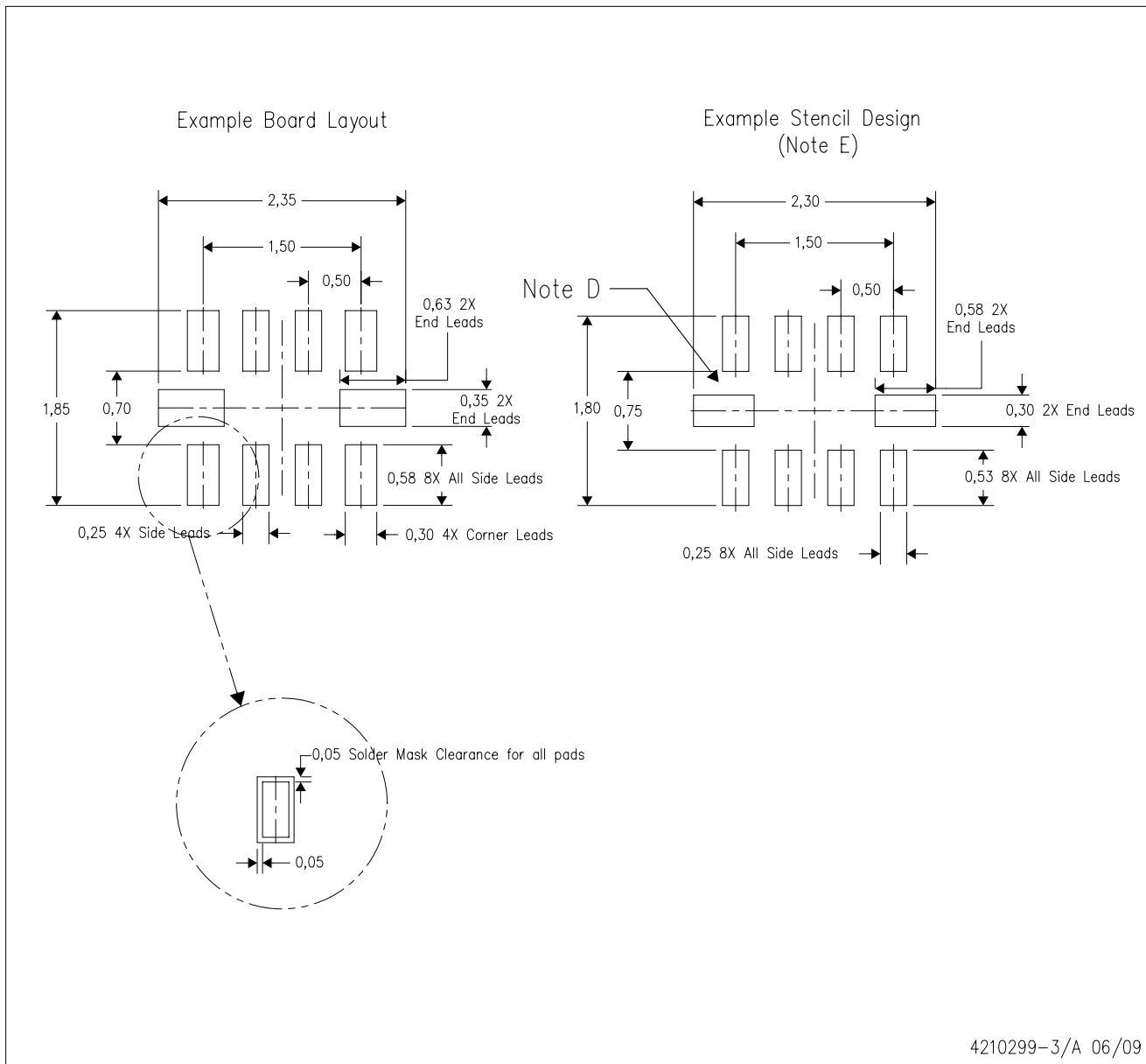
PLASTIC QUAD FLATPACK



4208528-3/B 04/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R-PQFP-N10)



4210299-3/A 06/09

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



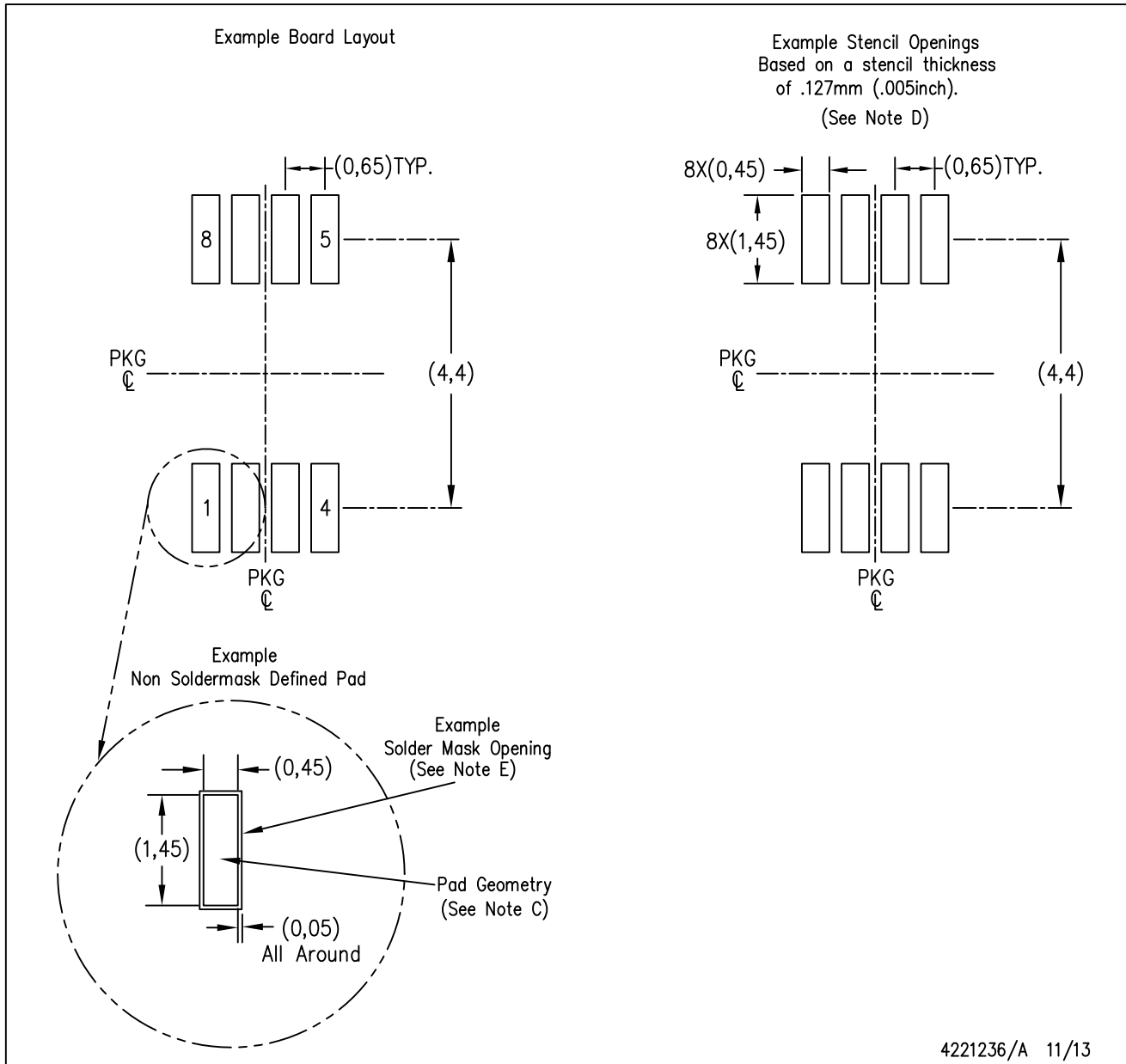
SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.





- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## GENERIC PACKAGE VIEW

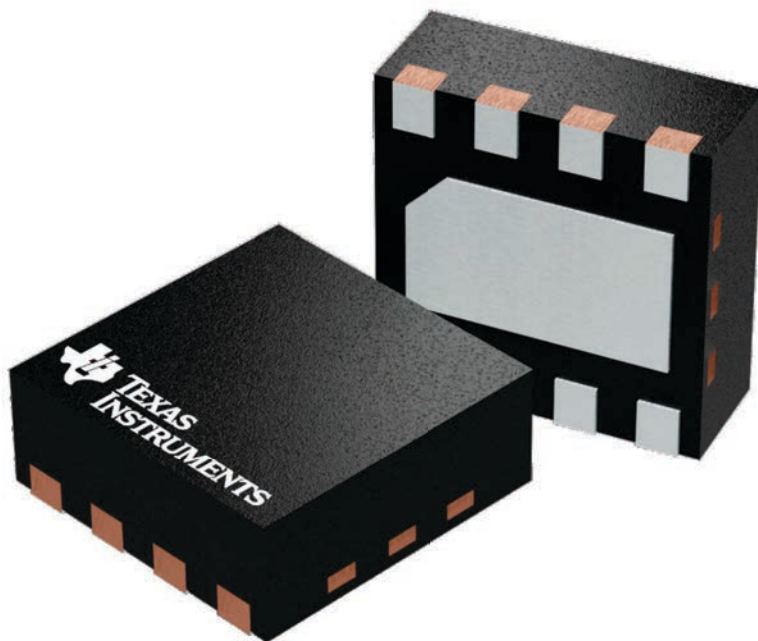
**DSG 8**

**WSON - 0.8 mm max height**

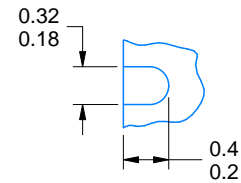
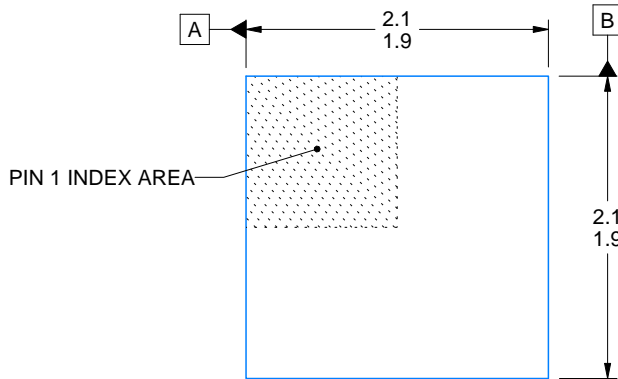
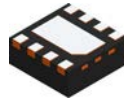
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

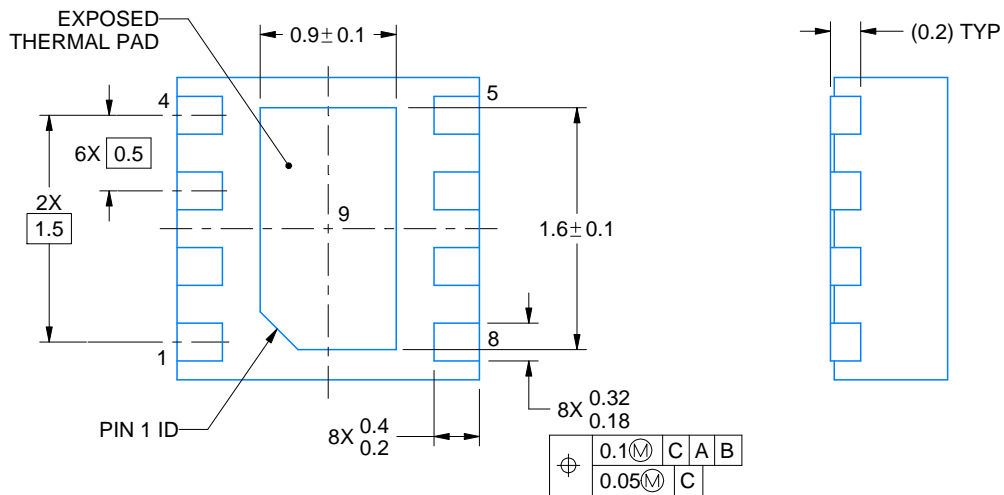
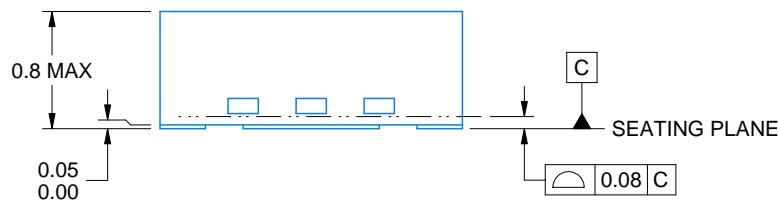
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A



ALTERNATIVE TERMINAL SHAPE  
TYPICAL



4218900/D 04/2020

NOTES:

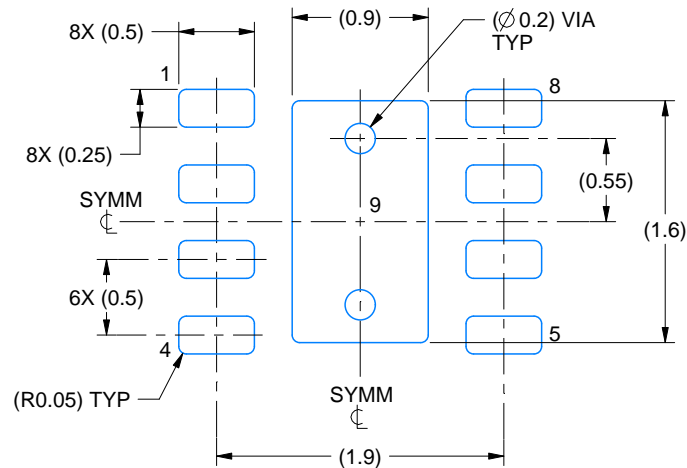
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

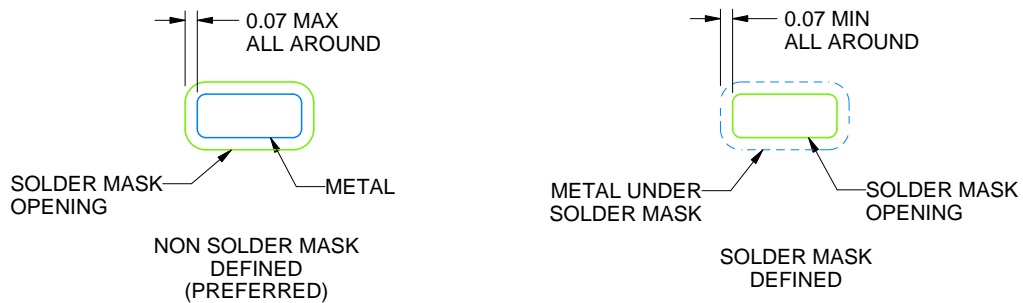
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

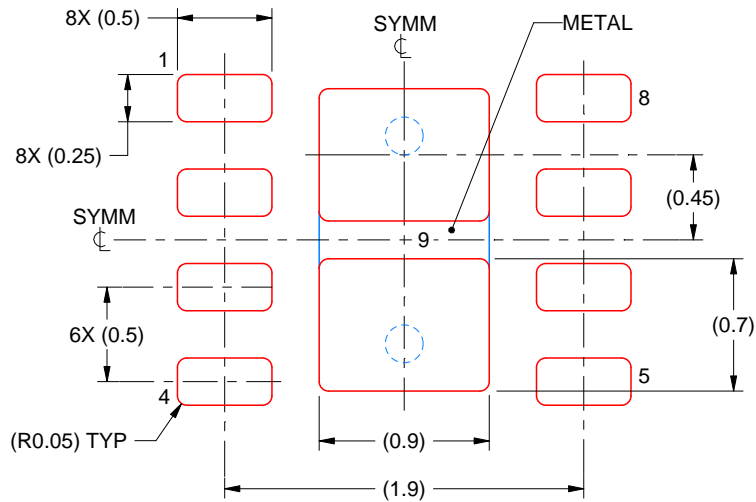
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

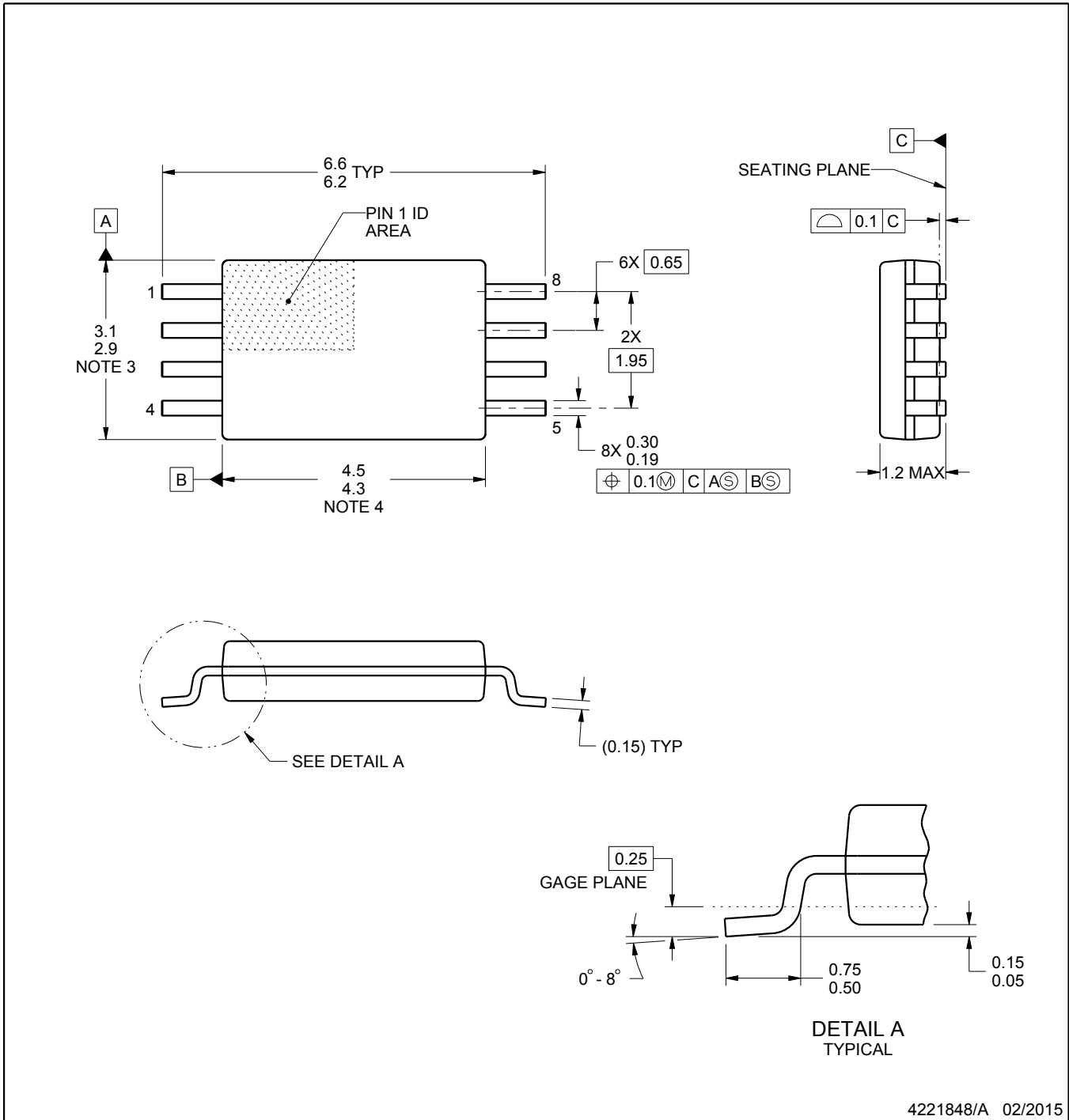
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

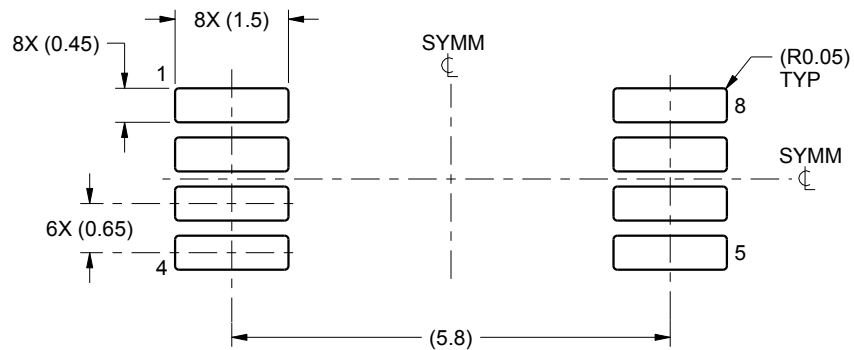
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

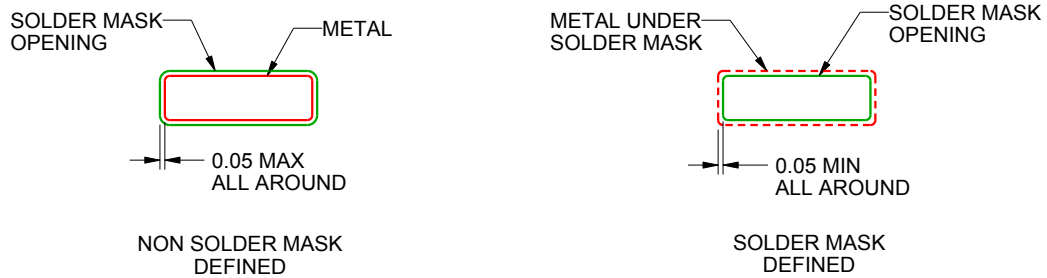
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

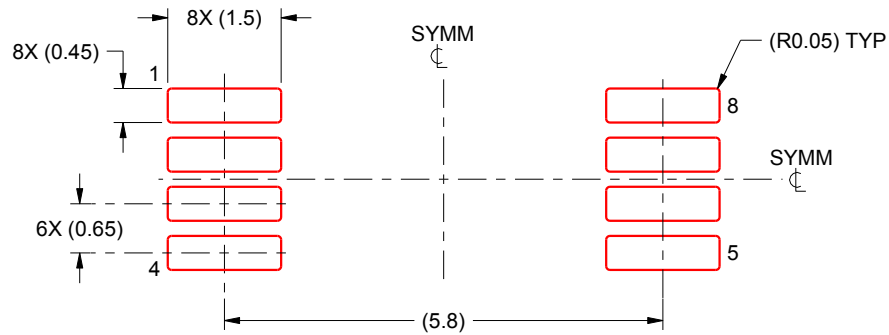
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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