TPS53126 Dual Synchronous Step-down Controller For Low Voltage Power Rails

1 Features

- D-CAP2™ Mode Control
  - Fast Transient Response
  - No External Parts Required For Loop Compensation
  - Compatible with Ceramic Output Capacitors
- High Initial Reference Accuracy (±1%)
- Low Output Ripple
- Wide Input Voltage Range: 4.5 V to 24 V
- Output Voltage Range: 0.76 V to 5.5 V
- Low-Side $R_{DS(on)}$ Loss-Less Current Sensing
- Adaptive Gate Drivers with Integrated Boost Diode
- Internal 1.2 ms Voltage-Servo Soft Start
- Pre-Biased Soft Start
- Selectable Switching Frequency: 350 kHz / 700 kHz
- Cycle-by-Cycle Over-Current Limiting Control
- 30 mV to 300 mV OCP Threshold Voltage
- Thermally Compensated OCP by 4000 ppm/C° at I_{TRIP}

2 Applications

- Point-of-Load Regulation in Low Power Systems for Wide Range of Applications
  - Digital TV Power Supply
  - Networking Home Terminal
  - Digital Set Top Box (STB)
  - DVD Player/Recorder
  - Gaming Consoles and Other

3 Description

The TPS53126 is a dual, adaptive on-time, D-CAP2™ mode synchronous Buck controller. The TPS53126 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low external component count, and low standby current solution. The main control loop for the TPS53126 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS53126 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 24 V and output voltages from 0.76 V to 5.5 V.

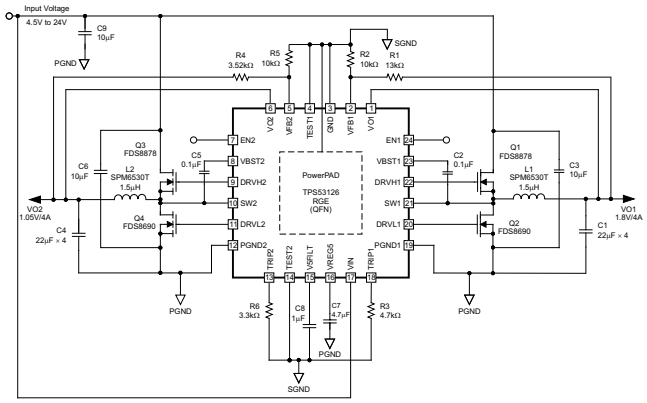
The TPS53126 is available in 4mm x 4mm 24 pin VQFN (RGE) or 24 pin TSSOP (PW) packages and is specified from –40°C to 85°C ambient temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53126	VQFN (24)	4.00 mm x 4.00 mm
TPS53126	TSSOP (24)	7.80 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematics



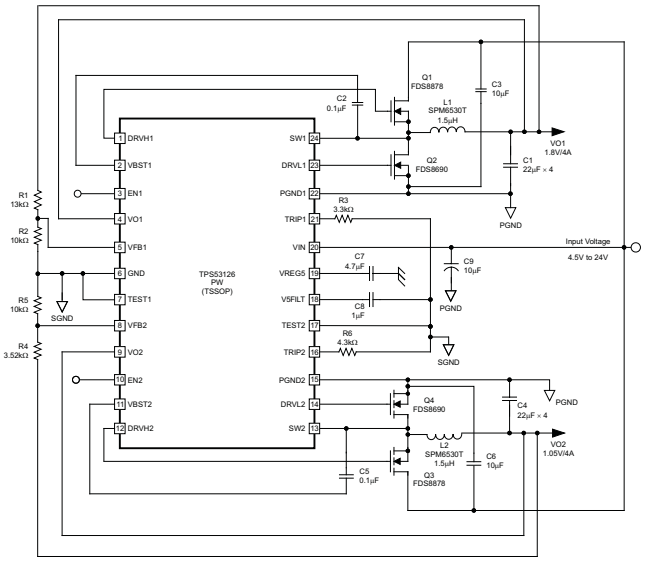


Table of Contents

5 Revision History

Changes from Revision A (July 2013) to Revision B — **Page**

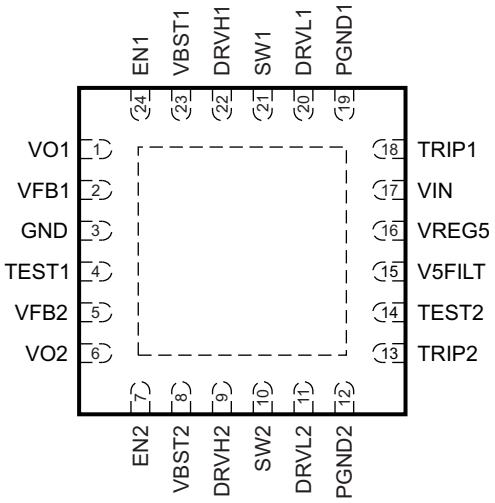
- Changed the datasheet to the new TI standard format ... 1
- Replaced QFN and TSSOP schematics ... 1
- Changed V_{VREG5} MIN from 4.8 V to 4.6 V ... 5
- Changed R_{DRVL} Source, I_{DRVLx} = –100 mA MAX from 8 Ω to 12 Ω ... 5
- Added Design Parameter and Detailed Design Procedure sections ... 19

Changes from Original (May 2009) to Revision A — **Page**

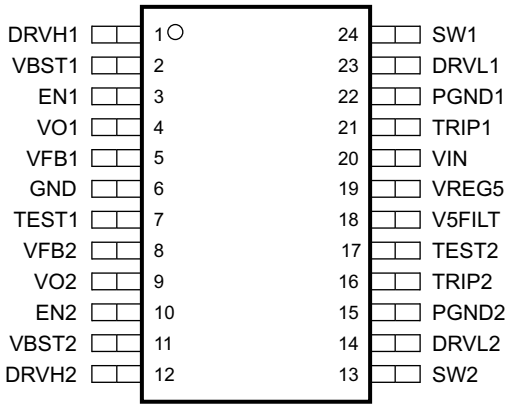
- Changed Equation 1 ... 12
- Changed Equation 13 ... 16

6 Pin Configurations and Functions

24 Pin VQFN
RGE Package
(Top View)



24 Pin TSSOP
PW Package
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VQFN 24 NUMBER	TSSOP 24 NUMBER		
VBST1, VBST2	23, 8	2, 11	I	Supply input for high-side NFET driver (Boost Terminal). Bypass to SWx with a high-quality 0.1µF ceramic capacitor. An external schottky diode can be added if forward drop is critical to drive the high-side FET.
EN1, EN2	24, 7	3, 10	I	Channel 1 and channel 2 high level enable pins.
VO1, VO2	1, 6	4, 9	I	Output voltage inputs for on-time adjustment and output discharge. Connect directly to the output voltage.
VFB1, VFB2	2, 5	5, 8	I	D-CAP2 feedback inputs. Connect to output voltage with resistor divider.
GND	3	6	I	Signal ground pin. Connect to PGND1, PGND2 and system ground at a single point.
DRVH1, DRVH2	22, 9	1, 12	O	High-side MOSFET gate driver outputs. SWx referenced drivers switch between SWx (OFF) and VBSTx (ON).
SW1, SW2	21, 10	24, 13	I/O	Switch node connections for both the high-side drivers and the current comparators.
DRVL1, DRVL2	20, 11	23, 14	O	Low-side MOSFET gate driver outputs. PGND referenced drivers switch between PGNDx (OFF) and VREG5 (ON).
PGND1, PGND2	19, 12	22, 15	I/O	Power ground connections for both the low-side drivers and the current comparators. Connect PGND1, PGND2 and GND strongly together near the IC.
TRIP1, TRIP2	18, 13	21, 16	I	Over current trip point programming pin. Connect to GND with a resistor to GND to set threshold for low-side $R_{DS(on)}$ current limit.
VIN	17	20	I	Supply Input for 5V linear regulator.
V5FILT	15	18	I	5V supply input for the entire control circuit except the MOSFET drivers. Bypass to GND with a minimum 1.0µF, high-quality ceramic capacitor. V5FILT is connected to VREG5 via an internal 10Ω resistor.
VREG5	16	19	O	Output of 5V linear regulator and supply for MOSFET drivers. Bypass to GND with a minimum 4.7µF high-quality ceramic capacitor. VREG5 is connected to V5FILT via an internal 10Ω resistor.
TEST1	4	7	O	Test interface pin, not used during application. Connect directly to GND.
TEST2	14	17	I	Frequency select pin. Connect to GND for 350kHz switching. Connect to V5FILT for 700kHz switching.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Input voltage	VIN, EN1, EN2	–0.3	26	V
		VBST1, VBST2	–0.3	32	
		VBST1, VBST2 (wrt SWx)	–0.3	6	
		V5FILT, VFB1, VFB2, TRIP1, TRIP2, VO1, VO2, TEST1, TEST2	–0.3	6	
		SW1, SW2	–2	26	
	Output voltage	DRVH1, DRVH2	–1	32	V
		DRVH1, DRVH2 (wrt SWx)	–0.3	6	
		DRVL1, DRVL2, VREG5	–0.3	6	
		PGND1, PGND2	–0.3	0.3	
T_A	Operating ambient temperature range		–40	85	°C
T_J	Junction temperature range		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
	Supply input voltage range	VIN	4.5	24	V
		V5FILT	4.5	5.5	
	Input voltage range	VBST1, VBST2	–0.1	30	V
		VBST1, VBST2 (wrt SWx)	–0.1	5.5	
		VFB1, VFB2, VO1, VO2, TEST1, TEST2	–0.1	5.5	
		TRIP1, TRIP2	–0.1	0.3	
		EN1, EN2	–0.1	24	
		SW1, SW2	–1.8	24	
	Output voltage range	DRVH1, DRVH2	–0.1	30	V
		VBST1, VBST2 (wrt SWx)	–0.1	5.5	
		DRVL1, DRVL2, VREG5	–0.1	5.5	
		PGND1, PGND2	–0.1	0.1	
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS53126		UNIT
		PW (24 PINS)	RGE(24 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.9	35.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	39.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	13.6	
ψ_{JT}	Junction-to-top characterization parameter	1.1	0.5	
ψ_{JB}	Junction-to-board characterization parameter	43.0	13.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended free-air temperature range, VIN = 12 V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN supply current	VIN current, T_A = 25°C, VREG5 tied to V5FLT, EN1 = EN2 = 5V, VFB1 = VFB2 = 0.8V, SW1 = SW2 = 0.5V		450	800	µA
I_{VINSDN}	VIN shutdown current	VIN current, T_A = 25°C, No load, EN1 = EN2 = 0 V, VREG5 = ON		30	60	µA
VFB VOLTAGE and DISCHARGE RESISTANCE						
V_{BG}	Bandgap initial regulation accuracy	T_A = 25°C	-1.0%		1.0%	
$V_{VFBTHLx}$	VFBx threshold voltage	T_A = 25°C, TEST2 = 0 V, SWinj = OFF	755	765	775	mV
		T_A = –40°C to 85°C, TEST2 = 0 V, SWinj = OFF(1)	752		778	
$V_{VFBTHHx}$	VFBx threshold voltage	T_A = 25°C, TEST2 = V5FILT, SWinj = OFF	748	758	768	mV
		T_A = –40°C to 85°C, TEST2 = V5FILT, SWinj = OFF(1)	745		771	
I_{VFB}	VFB input current	VFBx = 0.8 V, T_A = 25°C		–0.01	±0.1	µA
R_{Dischg}	VO discharge resistance	ENx = 0 V, VOx = 0.5 V, T_A = 25°C		40	80	Ω
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A = 25°C, 5.5 V < VIN < 24 V, 0 < I_{VREG5} < 10 mA	4.6	5.0	5.2	V
V_{LN5}	Line regulation	5.5 V < VIN < 24 V, I_{VREG5} = 10 mA			20	mV
V_{LD5}	Load regulation	1 mA < I_{VREG5} < 10 mA			40	mV
I_{VREG5}	Output current	VIN = 5.5 V, V_{VREG5} = 4 V, T_A = 25°C		170		mA
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVHx} = –100 mA		5.5	11	Ω
		Sink, I_{DRVHx} = 100 mA		2.5	5	
R_{DRVL}	DRVL resistance	Source, I_{DRVLx} = –100 mA		4	12	Ω
		Sink, I_{DRVLx} = 100 mA		2	4	
INTERNAL BOOST DIODE						
V_{FBST}	Forward voltage	$V_{VREG5-VBSTx}$, I_F = 10 mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	VBSTx = 29 V, SWx = 24 V, T_A = 25°C		0.1	1	µA
SOFT START						
T_{ss}	Internal SS time	Internal soft start VFBx = 0.735 V	0.85	1.2	1.4	ms
UVLO						
$V_{UV5VFILT}$	V5FILT UVLO threshold	Wake up	3.7	4.0	4.3	V
		Hysteresis	0.2	0.3	0.4	

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over recommended free-air temperature range, VIN = 12 V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD						
V_{ENH}	ENx H-level input voltage	EN ½	2.0			V
V_{ENL}	ENx L-level input voltage	EN ½			0.3	V
CURRENT SENSE						
I_{TRIP}	TRIP source current	V_{TRIPx} = 0.1 V, T_A = 25°C	8.5	10	11.5	µA
TC_{ITRIP}	I_{TRIP} temperature coefficient	On the basis of 25°C(2)		4000		ppm/°C
V_{OCLoff}	OCP compensation offset	($V_{TRIPx-GND}$-$V_{PGNDx-SWx}$) voltage, $V_{TRIPx-GND}$ = 60 mV, T_A = 25°C	–15	0	15	mV
		($V_{TRIPx-GND}$-$V_{PGNDx-SWx}$) voltage, $V_{TRIPx-GND}$ = 60 mV	–20		20	
V_{Rtrip}	Current limit threshold setting range	$V_{TRIPx-GND}$ voltage	30		300	mV
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	110%	115%	120%	
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis (recovery < 20 µs)		10%		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(2)		150		°C
		Hysteresis(2)		20		

(2) Ensured by design. Not production tested.

7.6 Timing Requirements

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
t_D	Dead time	DRVHx-low to DRVLx-on	20	50	80	ns
		DRVLx-low to DRVHx-on	20	40	80	
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
t_{OVPDEL}	Output OVP prop delay time			1.5		µs
t_{UVPDEL}	Output UVP delay time		17	30	40	µs
t_{UVPEN}	Output UVP enable delay time	UVP enable delay	1.2	2	2.5	ms

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON1L}	CH1 on time	SW1 = 12 V, VO1 = 1.8 V, TEST2 = 0 V		490		ns
t_{ON2L}	CH2 on time	SW2 = 12 V, VO2 = 1.8 V, TEST2 = 0 V		390		ns
t_{OFF1L}	CH1 min off time	SW1 = 0.7 V, T_A = 25°C, VFB1 = 0.7 V, TEST2 = 0 V		285		ns
t_{OFF2L}	CH2 min off time	SW2 = 0.7 V, T_A = 25°C, VFB2 = 0.7 V, TEST2 = 0 V		285		ns
t_{ON1H}	CH1 on time	SW1 = 12 V, VO1 = 1.8 V, TEST2 = V5FILT		165		ns
t_{ON2H}	CH2 on time	SW2 = 12 V, VO2 = 1.8 V, TEST2 = V5FILT		140		ns
t_{OFF1H}	CH1 min off time	SW1 = 0.7 V, T_A = 25°C, VFB1 = 0.7 V, TEST2 = V5FILT		216		ns
t_{OFF2H}	CH2 min off time	SW2 = 0.7 V, T_A = 25°C, VFB2 = 0.7 V, TEST2 = V5FILT		216		ns

7.8 Typical Characteristics

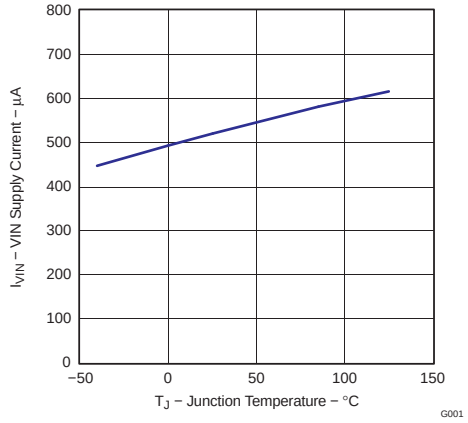


Figure 1. VIN Supply Current vs Junction Temperature

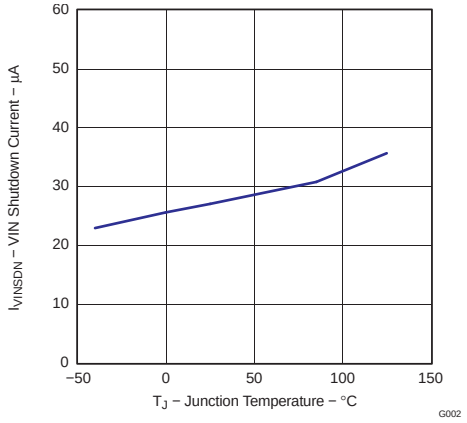


Figure 2. VIN Shutdown Current vs Junction Temperature

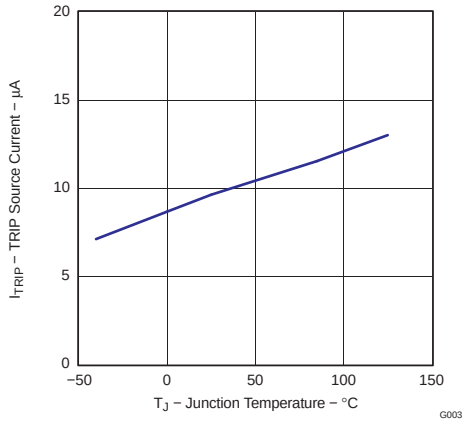


Figure 3. Trip Source Current vs Junction Temperature

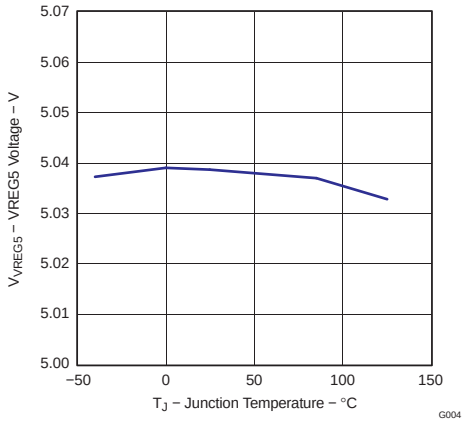


Figure 4. VREG5 Voltage vs Junction Temperature

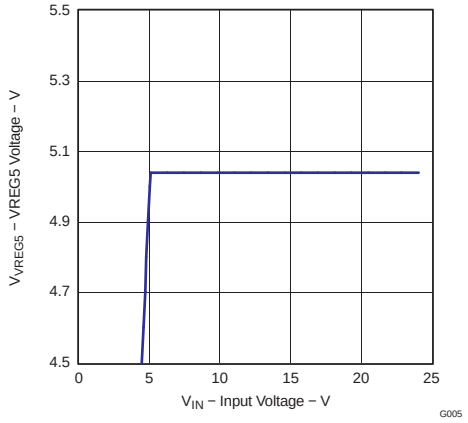
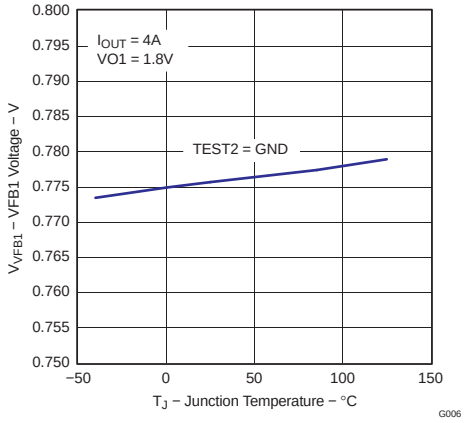


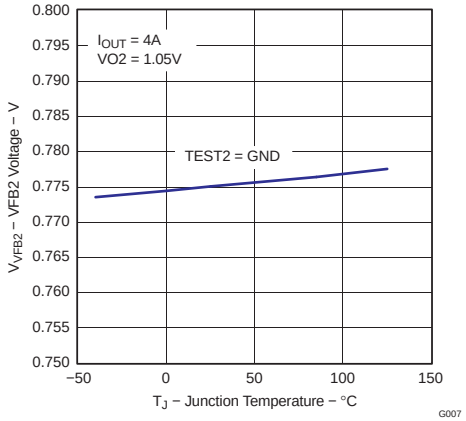
Figure 5. VREG5 Voltage vs Input Voltage



CH1 = 1.8 V, I_O = 4 A

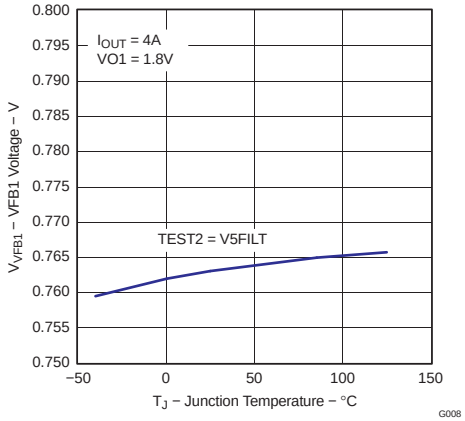
Figure 6. VFB1 Voltage vs Junction Temperature

Typical Characteristics (continued)



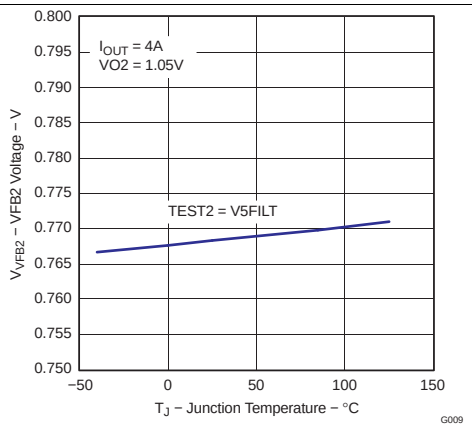
CH2 = 1.05 V, I_O = 4 A

Figure 7. VFB2 Voltage vs Junction Temperature



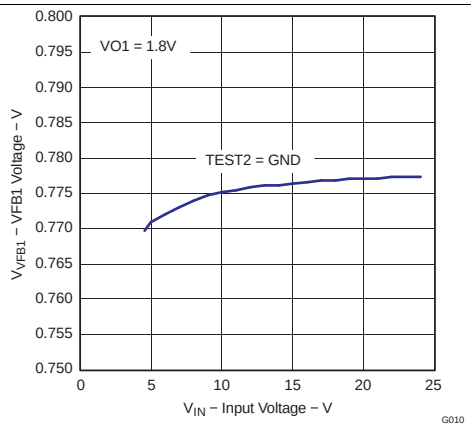
CH1 = 1.8 V, I_O = 4 A

Figure 8. VFB1 Voltage vs Junction Temperature



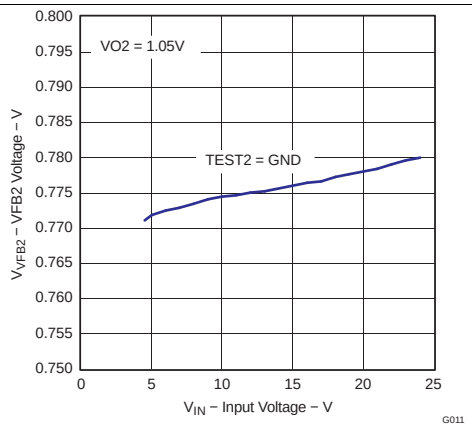
CH2 = 1.05 V, I_O = 4 A

Figure 9. VFB2 Voltage vs Junction Temperature



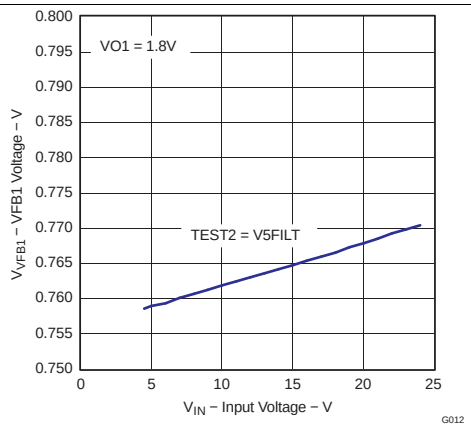
CH1 = 1.8 V

Figure 10. VFB1 Voltage vs Input Voltage



CH2 = 1.05 V

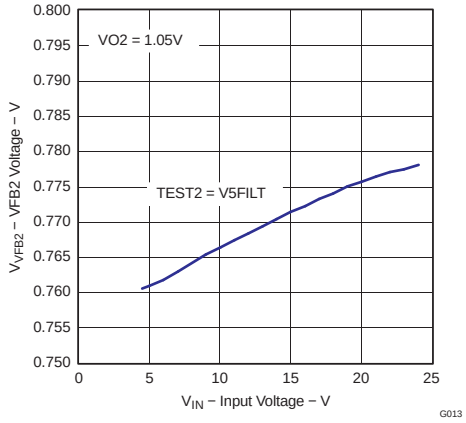
Figure 11. VFB2 Voltage vs Input Voltage



CH1 = 1.8 V

Figure 12. VFB1 Voltage vs Input Voltage

Typical Characteristics (continued)



CH2 = 1.05 V

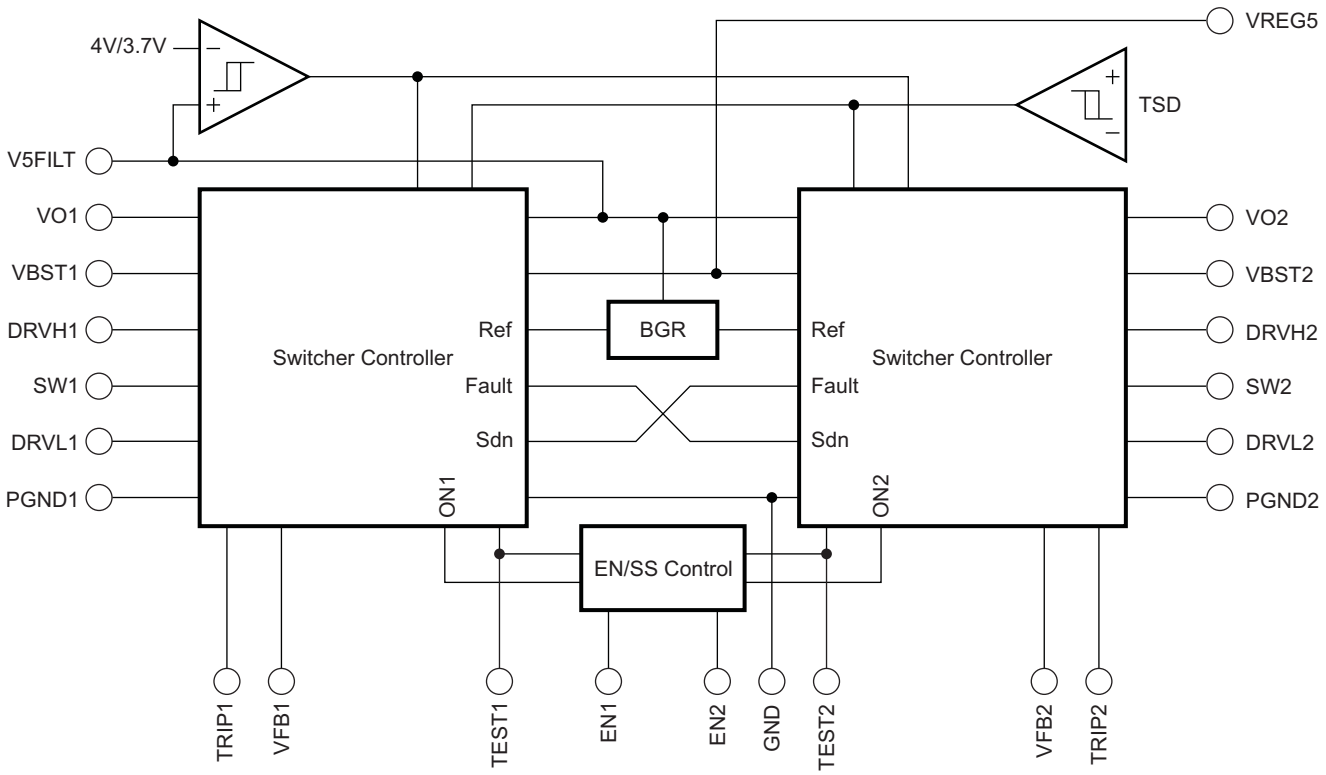
Figure 13. VFB2 Voltage vs Input Voltage

8 Detailed Description

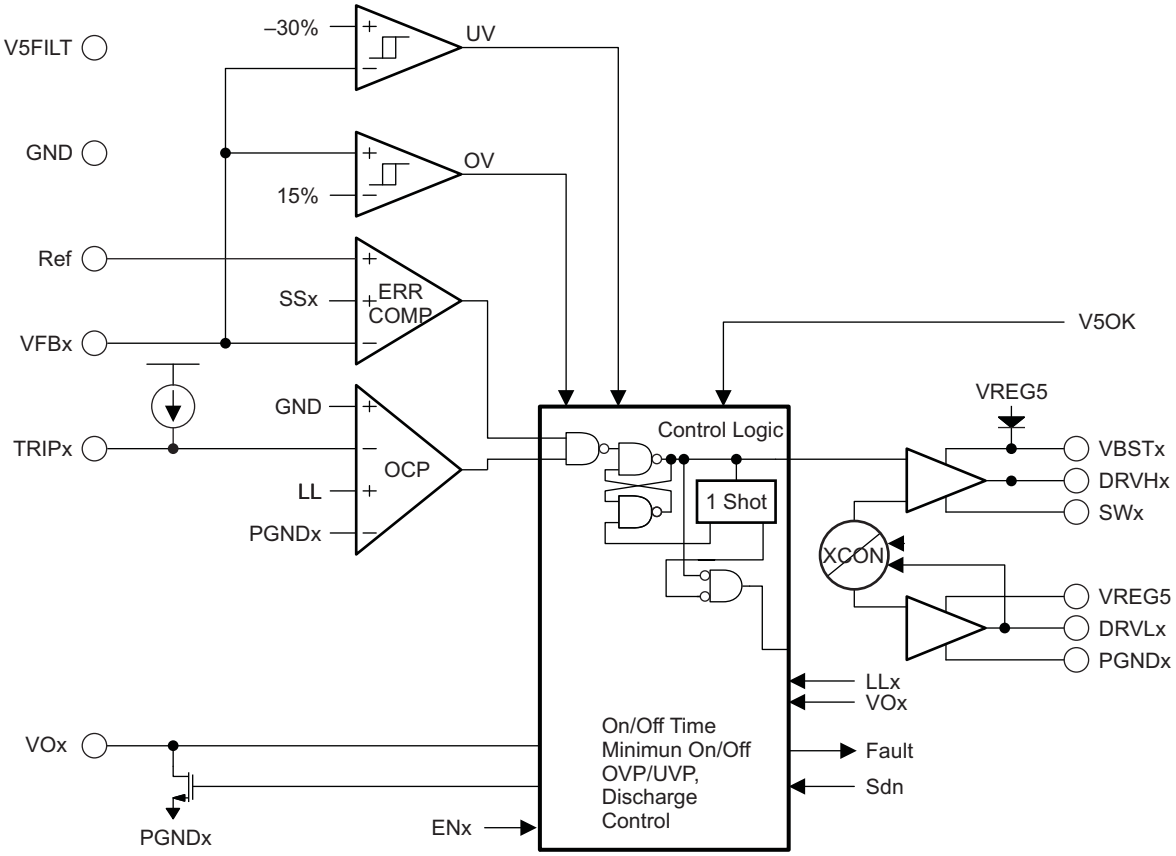
8.1 Overview

The TPS53126 is a dual, adaptive on-time, D-CAP2™ mode synchronous Buck controller. The TPS53126 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low external component count, and low standby current solution. The main control loop for the TPS53126 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS53126 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 24 V and output voltages from 0.76 V to 5.5 V.

8.2 Functional Block Diagram



Functional Block Diagram (continued)



8.3 Feature Description

8.3.1 PWM Operation

The main control loop of the TPS53126 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 Mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot timer is set by the converter input voltage ,VIN, and the output voltage ,VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP mode control.

8.3.2 Drivers

Each SMPS of the TPS53126 contains 2 high-current resistive MOSFET drivers. The Low-side driver is a ground referenced, VREG5 powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET whose source is connected to PGND. The High-side Driver is a floating SW referenced VBST powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET. To maintain the BST voltage during the high-side driver ON time, a capacitor is placed from SW to VBST. Each driver draws average current equal to Gate Charge (Qg AT Vgs = 5V) times Switching Frequency (fsw).

To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

Feature Description (continued)

8.3.3 PWM Frequency And Adaptive On-time Control

The TPS53126 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS53126 runs with pseudo-constant frequency by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

8.3.4 5 Volt Regulator

The TPS53126 has an internal 5V Low-Dropout (LDO) Regulator to provide a regulated voltage for all four drivers and the ICs internal logic. A capacitor from VREG5 to GND is required to stabilize the internal regular. An internal 10Ω resistor from VREG5 filters the regulator output to the IC's analog and logic input voltage, V5FILT. An additional capacitor is required from V5FILT to GND to filter switching noise from VREG5.

8.3.5 Soft Start

The TPS53126 has an internal, 1.2ms, voltage servo soft-start for each channel. When the ENx pin becomes high, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up. As the TPS53126 shares one DAC with both channels, if ENx pin is set to high while another channel is starting up, soft start is postponed until another channel soft start has completed. If both of EN1 and EN2 are set high at a same time, both channels start up at same time.

8.3.6 Pre-Bias Support

The TPS53126 supports pre-bias start-up without sinking current from the output capacitor. When enabled, the low-side driver is held off until the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage [VFB]), then the TPS53126 slowly activates synchronous rectification by limiting the first DRVL pulses with a narrow on-time. This limited on-time is then incremented on a cycle-by-cycle basis until it coincides with the full 1-D off-time. This scheme prevents the initial sinking of current from the pre-bias output, and ensure that the output voltage (VOUT) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

8.3.7 Switching Frequency Selection

The TPS53126 allows the user to select from 2 different switching frequencies by connecting the TEST2 pin to either GND or V5FILT. Connect TEST2 to GND for a switching frequency (fsw) of 350KHz. Connect TEST2 to V5FILT for a switching frequency of 700KHz.

8.3.8 Output Discharge Control

The TPS53126 discharges the outputs when ENx is low, or when the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges an output using an internal 40-Ω MOSFET which is connected to VOx and PGNDx. The external low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output. This discharge ensures that, on start, the regulated voltage always initializes from zero volts.

8.3.9 Overcurrent Limit

The TPS53126 has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(on)}$ during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53126 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(on)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, the TRIPx pin should be connected to GND through a trip voltage setting resistor, according to the following equations.

$$V_{trip} = \left(I_{OCL} - \frac{(V_{IN} - V_O)}{2 \times L1 \times f_{sw}} \times \frac{V_O}{V_{IN}} \right) \times R_{DS(on)} \quad (1)$$

$$R_{trip}(k\Omega) = \frac{V_{trip}(mV)}{I_{trip}(\mu A)} \quad (2)$$

Feature Description (continued)

The trip voltage should be between 30mV to 300mV over all operational temperature, including the 4000ppm/°C temperature slope compensation for the temperature dependency of the $R_{DS(on)}$. If the load current exceeds the over-current limit, the voltage will begin to drop. If the over-current conditions continues the output voltage will fall below the under voltage protection threshold and the TPS53126 will shut down.

8.3.10 Over/under Voltage Protection

The TPS53126 monitors the output voltage via the feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 115% of the reference voltage, the TPS53126 turns off the high-side MOSFET driver, turns on the low-side MOSFET driver and latches off.

When the feedback voltage becomes lower than 70% of the reference voltage, the TPS53126 begins an internal UVP delay counter. After 30µs, the TPS53126 turns off both top and bottom MOSFET drivers and latches off. The UVP function is enabled approximately 2.0ms after power-on to prevent detecting UVP during soft-start. Both OVP and UVP latch conditions are reset when V5FILT triggers UVLO or the ENx pin goes low.

8.3.11 UVLO Protection

The TPS53126 has under voltage lock out protection (UVLO) that monitors the voltage of V5FILT pin. When the V5FILT voltage is lower than UVLO threshold voltage, the device is shut off. During shut-off, VREG5 and all output drivers are OFF and output discharge is ON. The UVLO is non-latch protection.

8.3.12 Thermal Shutdown

The TPS53126 includes an over temperature protection shut-down feature. If the TPS53126 die temperature exceeds the OTP threshold (typically 150°C), both the high-side and low-side drivers are shut off, the output voltage discharge function is enabled and then the device is shut off until the die temperature drops. Thermal shutdown is a non-latch protection.

8.4 Device Functional Modes

The TPS53126 has two operating modes. The TPS53126 is in shut down mode when the EN1 and EN2 pins are low. When the EN1 and EN2 pins is pulled high, the TPS53126 enters the normal operating mode.

9 Application and Implementation

9.1 Application Information

9.2 350 kHz Operation Application

The schematic of Figure 14 shows a typical 350 kHz application schematic. The 350 kHz switching frequency is selected by connecting TEST2 to the GND pin. The input voltage is 4.5 V to 24 V and the output voltage is 1.8 V for VO1 and 1.05 V for VO2.

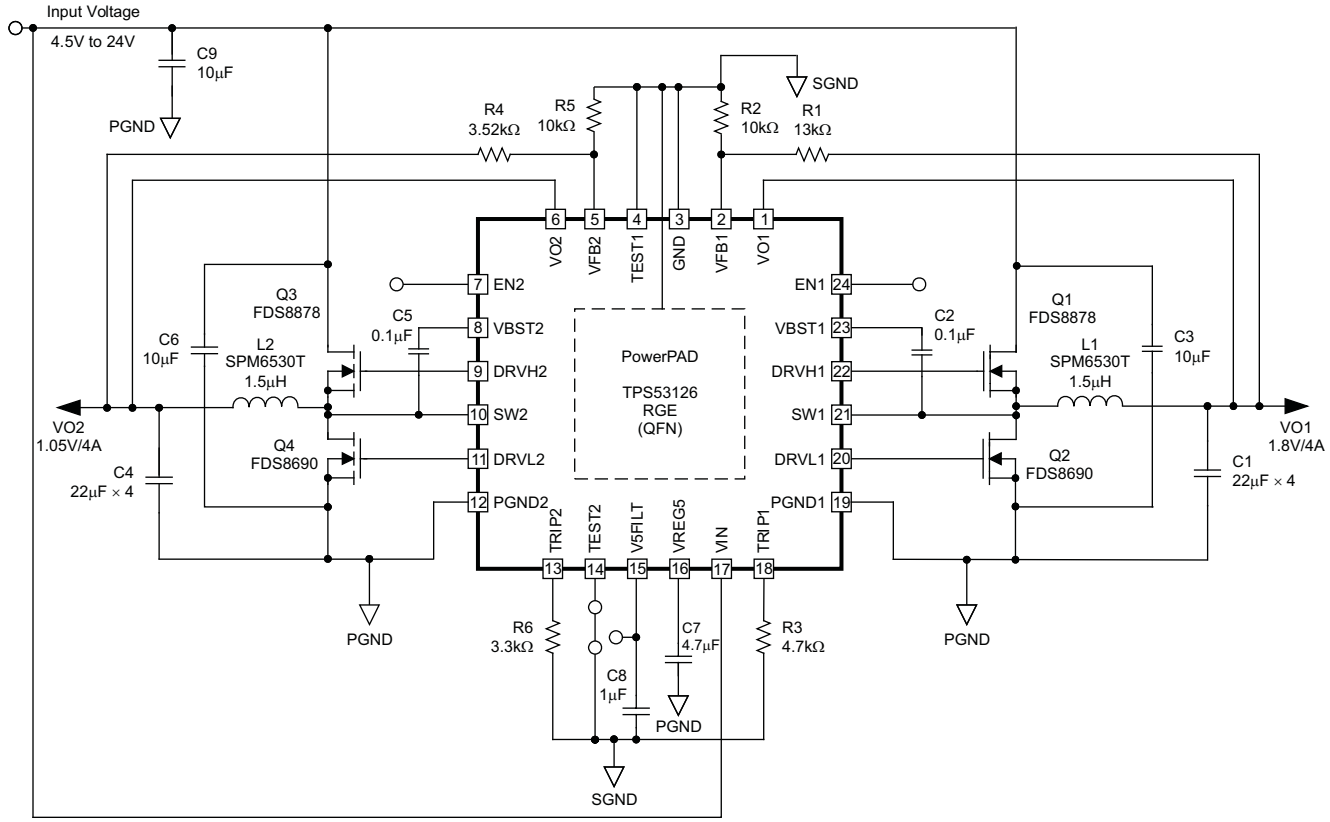


Figure 14. Typical Application Circuit at 350kHz Switching Frequency Selection (TEST2 Pin = GND)

9.2.1 Design Requirements

Table 1. Design Parameters

PARAMETERS	CHANNEL 1	CHANNEL 2
Input voltage	4.5 V to 24 V	4.5 V to 24 V
Output voltage	1.8 V	1.05 V
Output Current	4 A	4 A
Switching Frequency	350 kHz	350 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Choose Inductor

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation. Equation 3 can be used to calculate L1.

$$L1 = \frac{(V_{IN(max)} - Vo1)}{I_{L1(ripple)} \times fsw} \times \frac{Vo1}{V_{IN(max)}} = \frac{3 \times (V_{IN(max)} - Vo1)}{Io1 \times fsw} \times \frac{Vo1}{V_{IN(max)}} \quad (3)$$

The inductors current ratings needs to support both the RMS (thermal) current and the Peak (saturation) current. The RMS and peak inductor current can be estimated as follows:

$$I_{L1(ripple)} = \frac{V_{IN(max)} - Vo1}{L1 \times fsw} \times \frac{Vo1}{V_{IN(max)}} \quad (4)$$

$$I_{L1(peak)} = \frac{V_{trip}}{R_{DS(on)}} + I_{L1(ripple)} \quad (5)$$

$$I_{L1(RMS)} = \sqrt{Io1^2 + \frac{1}{12}\left(I_{L1(ripple)}\right)^2} \quad (6)$$

Note: The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

9.2.2.2 Choose Output Capacitor

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. Recommend to use ceramic output capacitor.

$$C1 = \frac{\Delta Iload^2 \times L1}{2 \times Vo1 \times \Delta Vos} \quad (7)$$

$$C1 = \frac{\Delta Iload^2 \times L1}{2 \times K \times \Delta Vus} \quad (8)$$

Where:

$$K = \left((V_{IN} - Vo1) - \frac{Tmin(off)}{Ton1} \times Vo1\right) \times \frac{Ton1}{Ton1 + Tmin(off)} \quad (9)$$

$$C1 = \frac{I_{L1(ripple)}}{8\ Vo1(ripple)} \times \frac{1}{fsw} \quad (10)$$

Select the capacitance value greater than the largest value calculated from Equation 7, Equation 8 and Equation 10. The capacitance for C1 should be greater than 66 µF.

Where:

ΔVos = the allowable amount of overshoot voltage in load transition

ΔVus = the allowable amount of undershoot voltage in load transition

Tmin(off) = Min-off time

9.2.2.3 Choose Input Capacitor

The TPS53126 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-µF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

9.2.2.4 Choose Bootstrap Capacitor

The TPS53126 requires a bootstrap capacitor from SWx to VBSTx to provide the floating supply for the high-side drivers. A minimum 0.1-µF high-quality ceramic capacitor is recommended. The voltage rating should be greater than 6 V.

9.2.2.5 Choose VREG5 and V5FILT Capacitors

The TPS53126 requires both the VREG5 regulator and V5FILT input are bypassed. A minimum 4.7-µF high-quality ceramic capacitor must be connected between the VREG5 and GND for proper operation. A minimum 1.0-µF high-quality ceramic capacitor must be connected between the V5FILT and GND for proper operation. Both of these capacitors' voltage ratings should be greater than 6 V.

9.2.2.6 Choose Output Voltage Set Point Resistors

The output voltage is set with a resistor divider from output voltage node to the VFBx pin. It is recommended to use 1% tolerance or better resisters. Select R2 between 10 kΩ and 100 kΩ and use Equation 11 and Equation 12 to calculate R1.

$$R1 = \left(\frac{Vo1}{0.765 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \times R2 \qquad (TEST2=GND) \tag{11}$$

$$R1 = \left(\frac{Vo1}{0.758 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \times R2 \qquad (TEST2 = V5FILT) \tag{12}$$

Where:

$VFB1_{(ripple)}$ = Ripple Voltage at VFB1

9.2.2.7 Choose Over Current Limit Set Point Resistors

$$V_{trip} = \left(I_{OCL} - \frac{(V_{IN} - V_O)}{2 \times L1 \times f_{sw}} \times \frac{V_O}{V_{IN}} \right) \times R_{DS(on)} \tag{13}$$

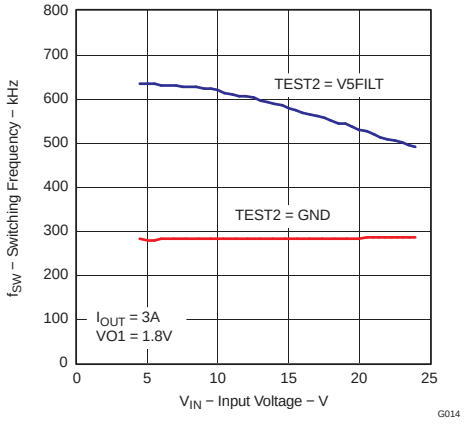
$$R_{trip}(k\Omega) = \frac{V_{trip}(mV)}{I_{trip}(\mu A)} \tag{14}$$

Where:

$R_{DS(on)}$ = Low Side FET on-resistance
I_{trip} = TRIP pin source current (= 10 µA)
I_{OCL} = Over current limit

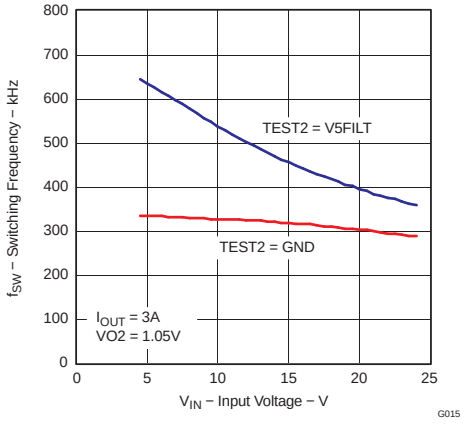
9.2.3 350 kHz Application Curves

Application curves Figure 15, Figure 16, Figure 17, Figure 18, Figure 23 and Figure 24 apply to both the circuits of 350 kHz Operation Application and 700 Khz Operation Application.



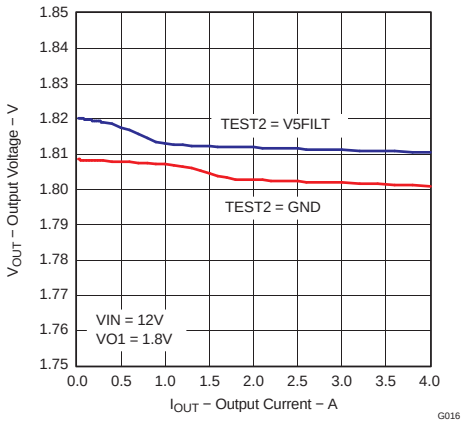
IO1 = 3 A

Figure 15. SWITCHING FREQUENCY vs INPUT VOLTAGE (CH1)



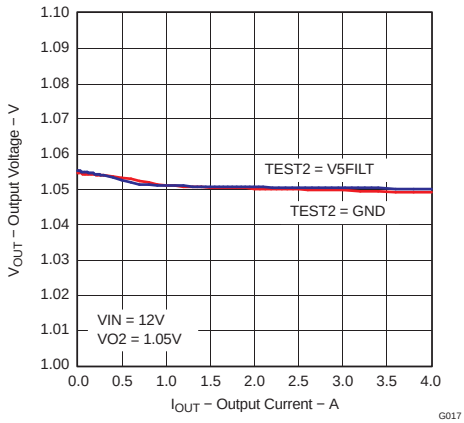
IO2 = 3 A

Figure 16. SWITCHING FREQUENCY vs INPUT VOLTAGE (CH2)



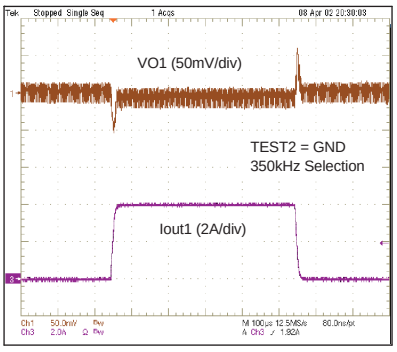
VIN = 12 V

Figure 17. OUTPUT VOLTAGE vs OUTPUT CURRENT (CH1)



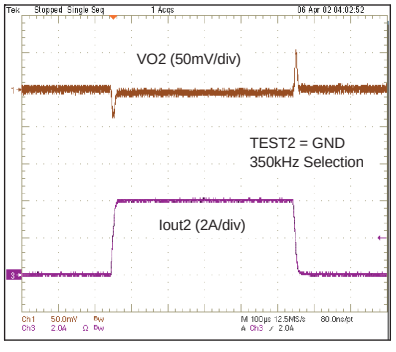
VIN = 12 V

Figure 18. OUTPUT VOLTAGE vs OUTPUT CURRENT (CH2)



CH1, TEST2 = GND

Figure 19. 1.8V LOAD TRANSIENT RESPONSE



CH2, TEST2 = GND

Figure 20. 1.05V LOAD TRANSIENT RESPONSE

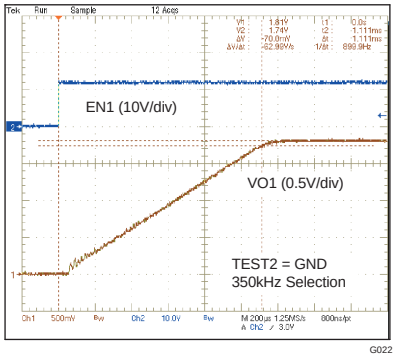
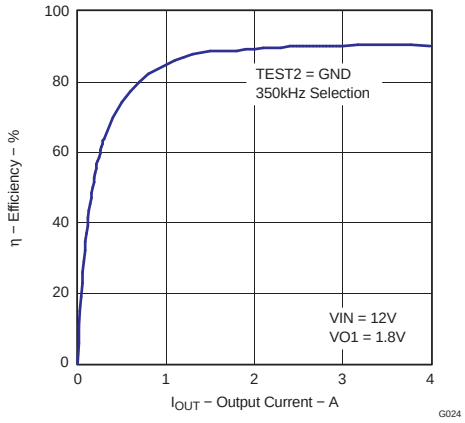
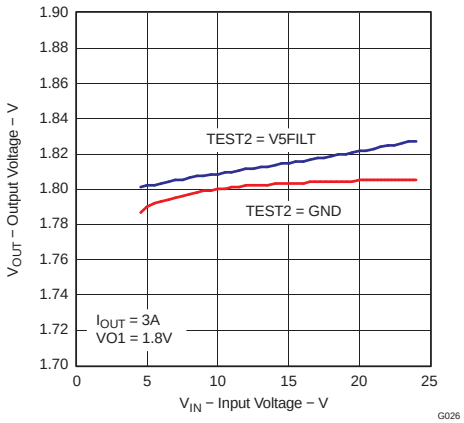


Figure 21. 1.8V START-UP WAVEFORMS



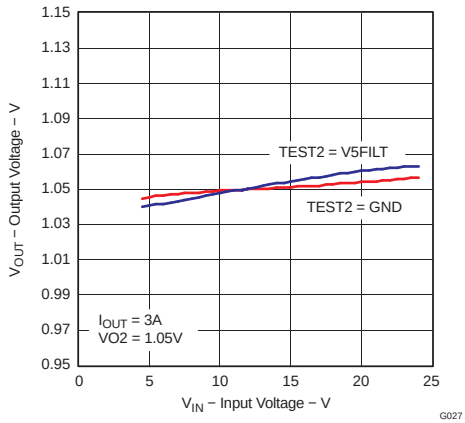
VIN = 12 V

Figure 22. 1.8V EFFICIENCY vs OUTPUT CURRENT (CH1)



I_O = 3 A

Figure 23. 1.8V OUTPUT VOLTAGE vs INPUT VOLTAGE



I_O = 3 A

Figure 24. 1.05V OUTPUT VOLTAGE vs INPUT VOLTAGE

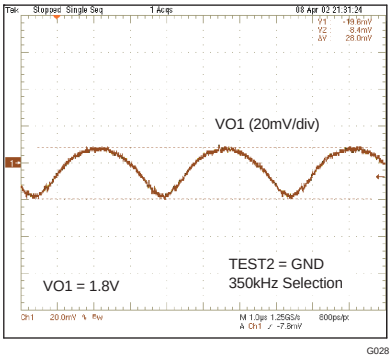


Figure 25. 1.8V OUTPUT RIPPLE VOLTAGE

9.3 700 Khz Operation Application

The schematic of Figure 26 shows a typical 700 kHz application schematic. The 700 kHz switching frequency is selected by connecting TEST2 to the V5FILT pin. The input voltage is 4.5 V to 24 V and the output voltage is 1.8 V for VO1 and 1.05 V for VO2.

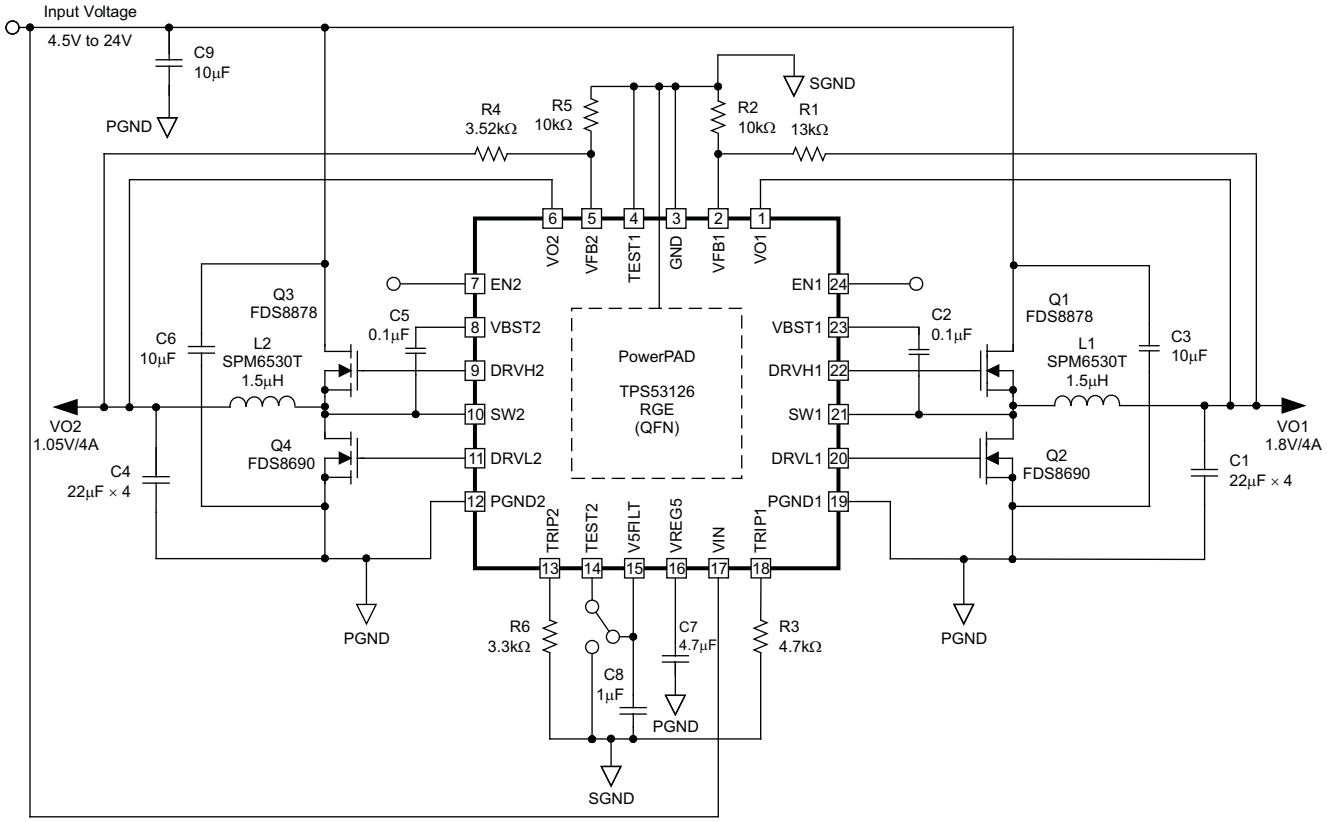


Figure 26. Typical Application Circuit at 700 kHz Switching frequency Selection (TEST2 Pin = V5FILT)

9.3.1 Design Parameters

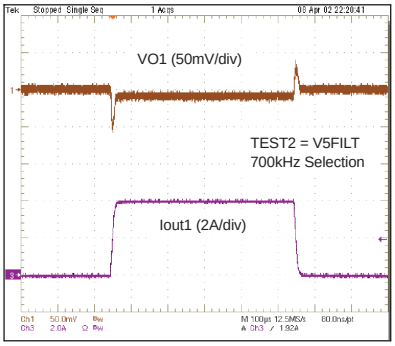
PARAMETERS	CHANNEL 1	CHANNEL 2
Input voltage	4.5 to 24 V	4.5 to 24 V
Output voltage	1.8 V	1.05 V
Output current	4 A	4 A
Switching Frequency	700 kHz	700 kHz

9.3.2 Detailed Design Procedure

For the Detailed Design Procedure, refer to Detailed Design Procedure.

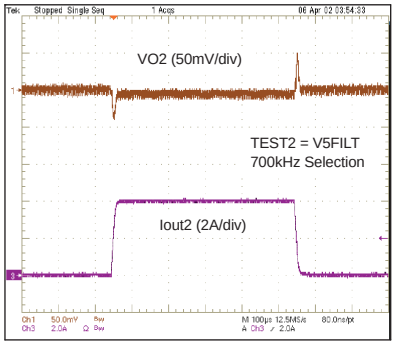
9.3.3 700 kHz Application Curves

Application curves Figure 15, Figure 16, Figure 17, Figure 18, Figure 23 and Figure 24 apply to both the circuits of 350 kHz Operation Application and 700 Khz Operation Application.



CH1, TEST2 = V5FILT

Figure 27. 1.8V LOAD TRANSIENT RESPONSE



CH2, TEST2 = V5FILT

Figure 28. 1.05V LOAD TRANSIENT RESPONSE

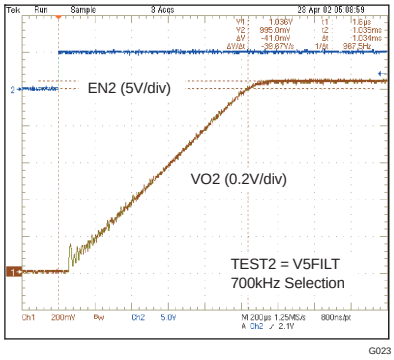
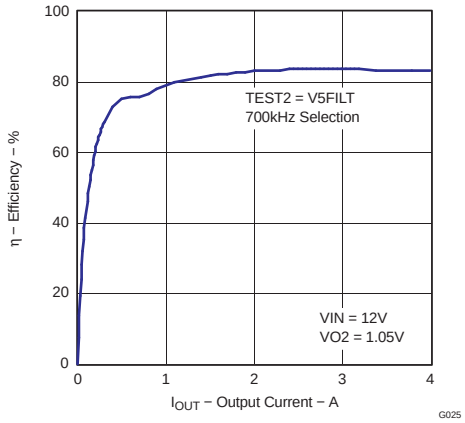


Figure 29. 1.05V START-UP WAVEFORMS



VIN = 12 V

Figure 30. 1.05V EFFICIENCY vs OUTPUT CURRENT (CH2)

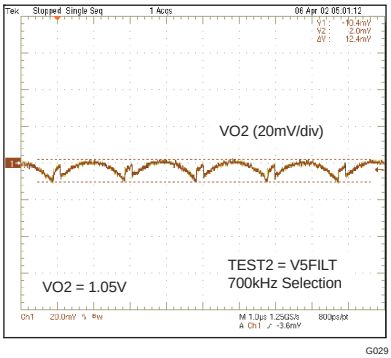


Figure 31. 1.05V OUTPUT RIPPLE VOLTAGE

10 Power Supply Recommendations

The TPS53126 is designed to operate from an input voltage supply range between 4.5 V and 24 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS53126 device additional 0.1 µF ceramic capacitance may be required in addition to the ceramic bypass capacitors, 10 µF.

11 Layout

11.1 Layout Guidelines

- Keep the input switching current loop as small as possible. (VIN ≥ C3 ≥ PNGD ≥ Sync FET ≥ SW ≥ Control FET)
- Place the input capacitor (C3) close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback terminal (FBx) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.(1)
- Do not allow switching current to flow under the device.
- DRVH and DRVL line should not run close to SW node or minimize it. (2)
- GND terminals for capacitors of SSx and V5FILT and resistors of feedback and TRIPx should be connected to SGND. (3)
- GND terminals for capacitors of VREG5 and VIN should be connected to PGND. (4)
- Signal lines should not run under/near Output Inductor or minimize it. (5)

11.2 Layout Example

The layout example of Figure 32 corresponds to the schematic of Figure 14.

Layout Example (continued)

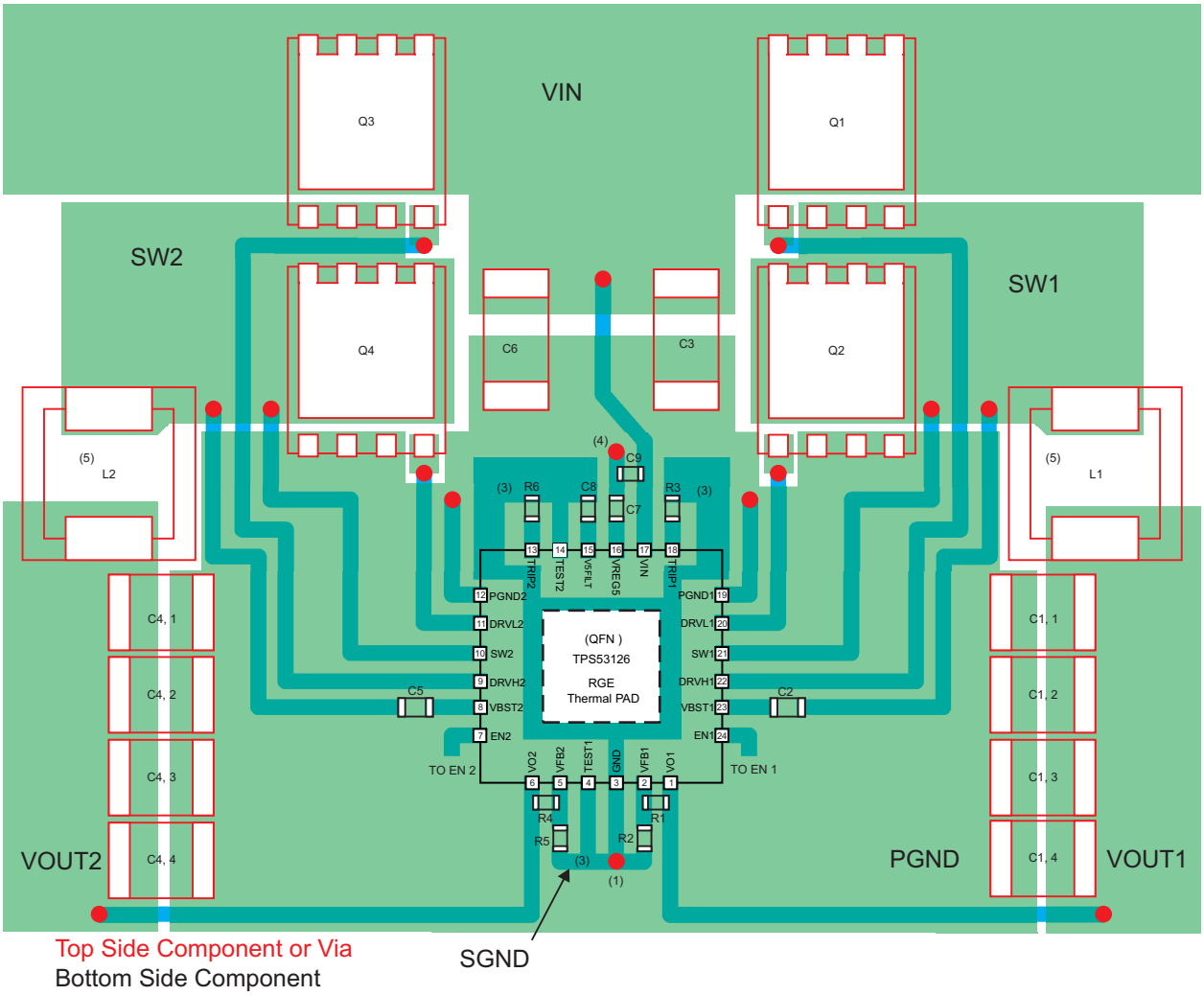


Figure 32. Board Layout

12 Device and Documentation Support

12.1 Trademarks

D-CAP2 is a trademark of Texas Instruments.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53126PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS53126	Samples
TPS53126PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS53126	Samples
TPS53126RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 53126	Samples
TPS53126RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 53126	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

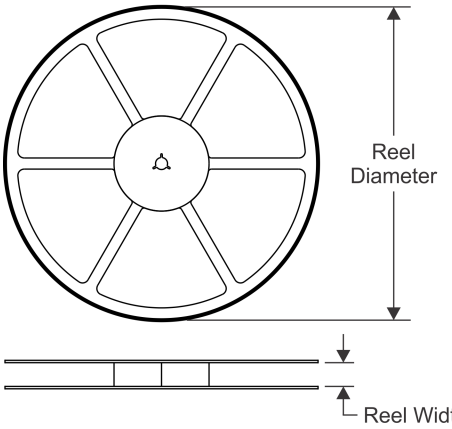
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

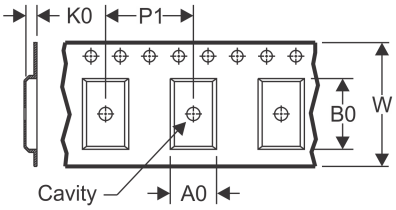
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

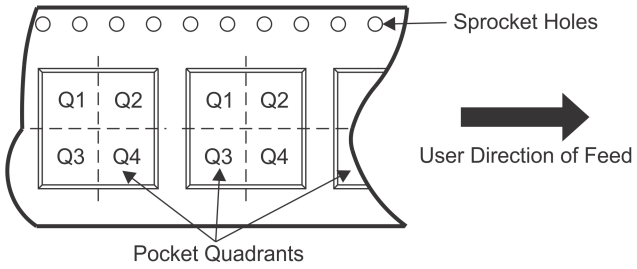


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

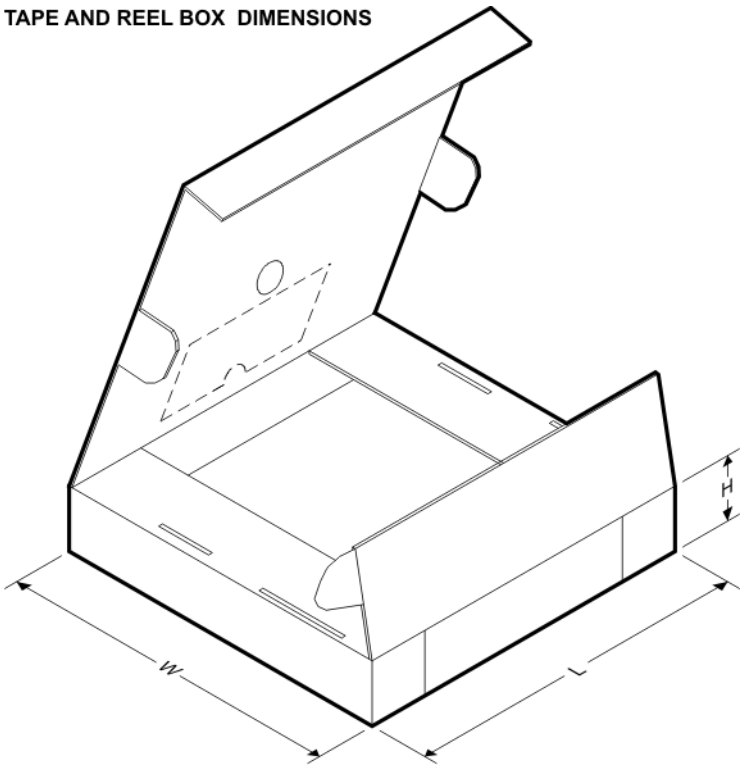
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53126PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS53126RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53126RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

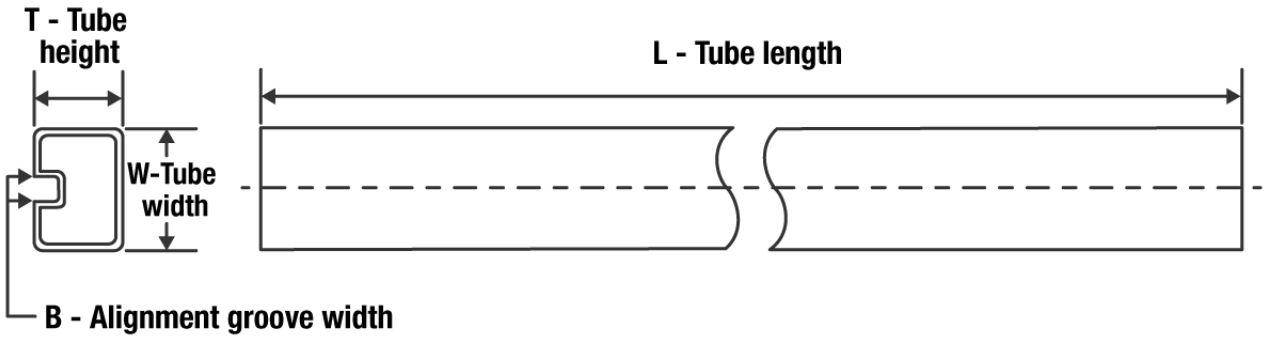
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53126PWR	TSSOP	PW	24	2000	853.0	449.0	35.0
TPS53126RGER	VQFN	RGE	24	3000	853.0	449.0	35.0
TPS53126RGET	VQFN	RGE	24	250	210.0	185.0	35.0

TUBE



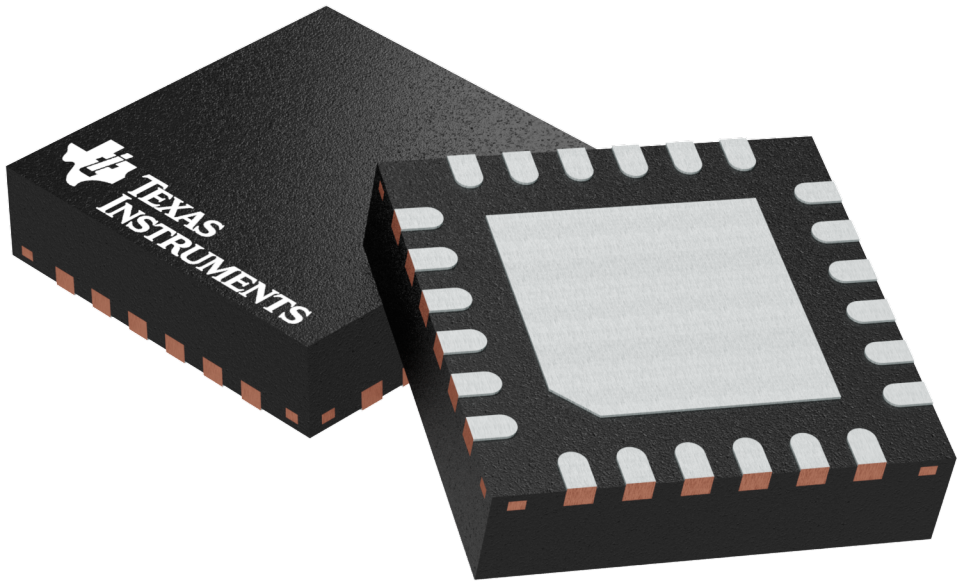
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS53126PW	PW	TSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

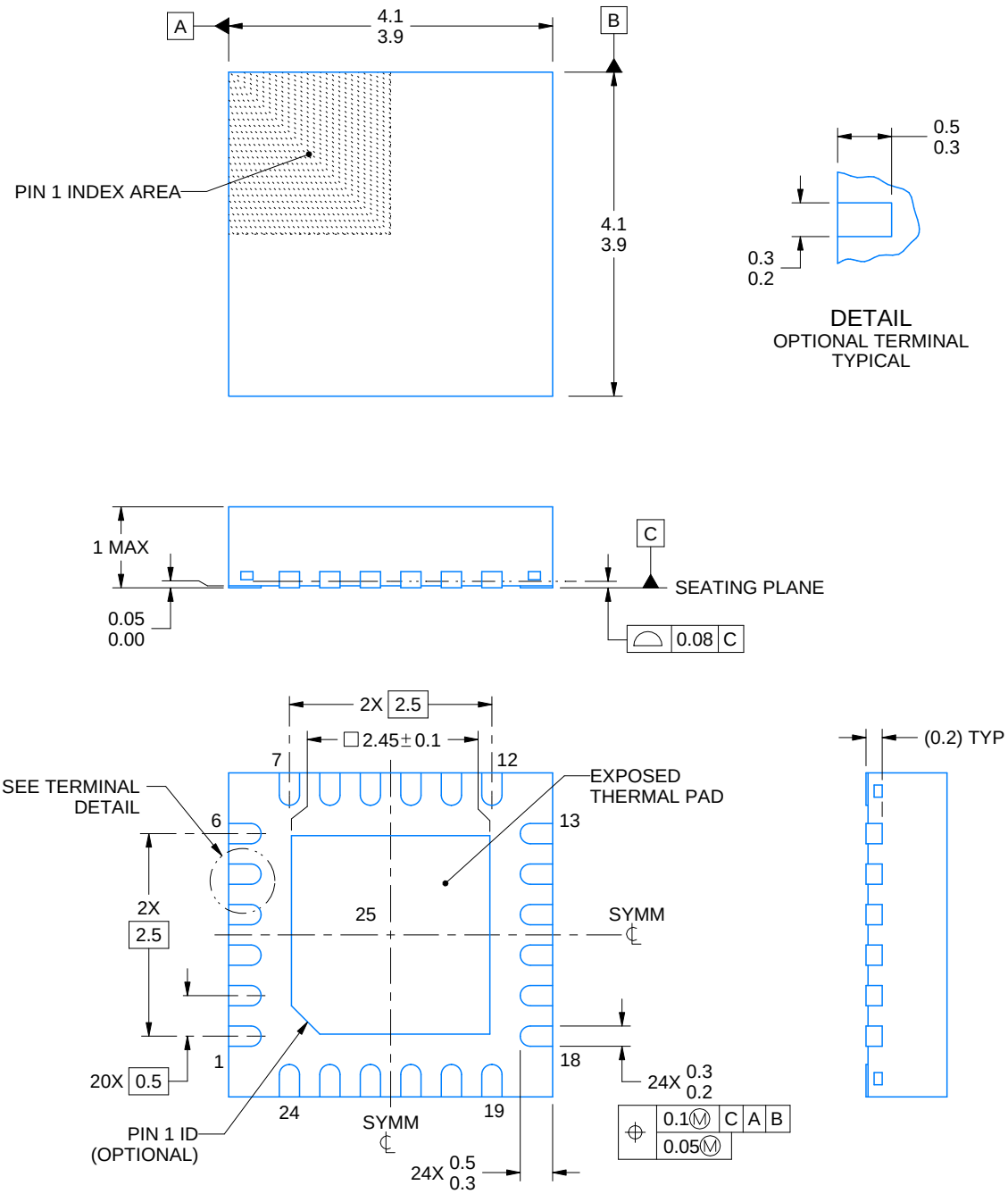
4204104/H

PACKAGE OUTLINE

RGE0024B

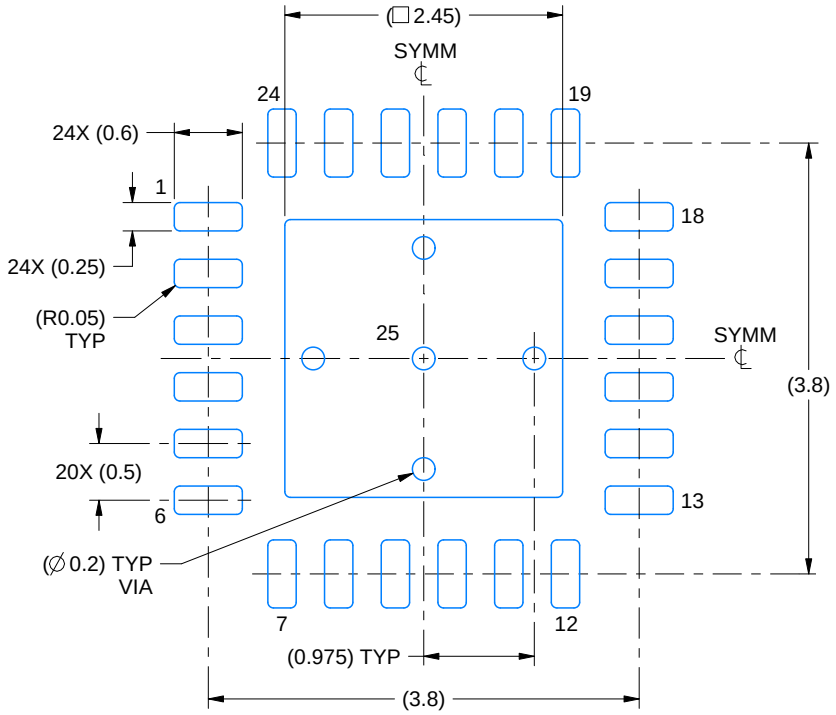
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

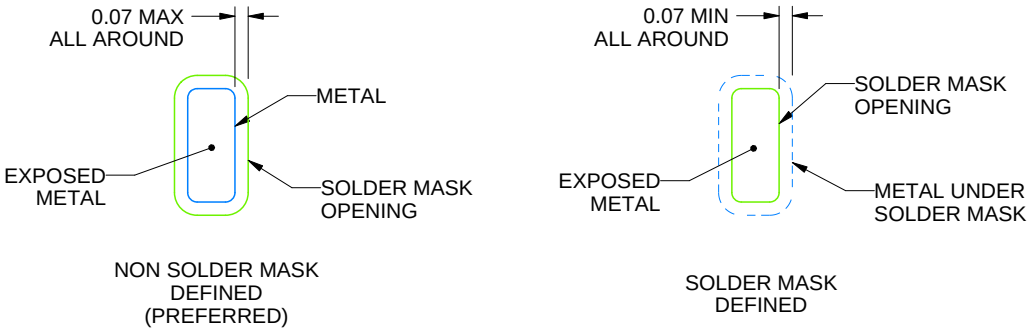


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

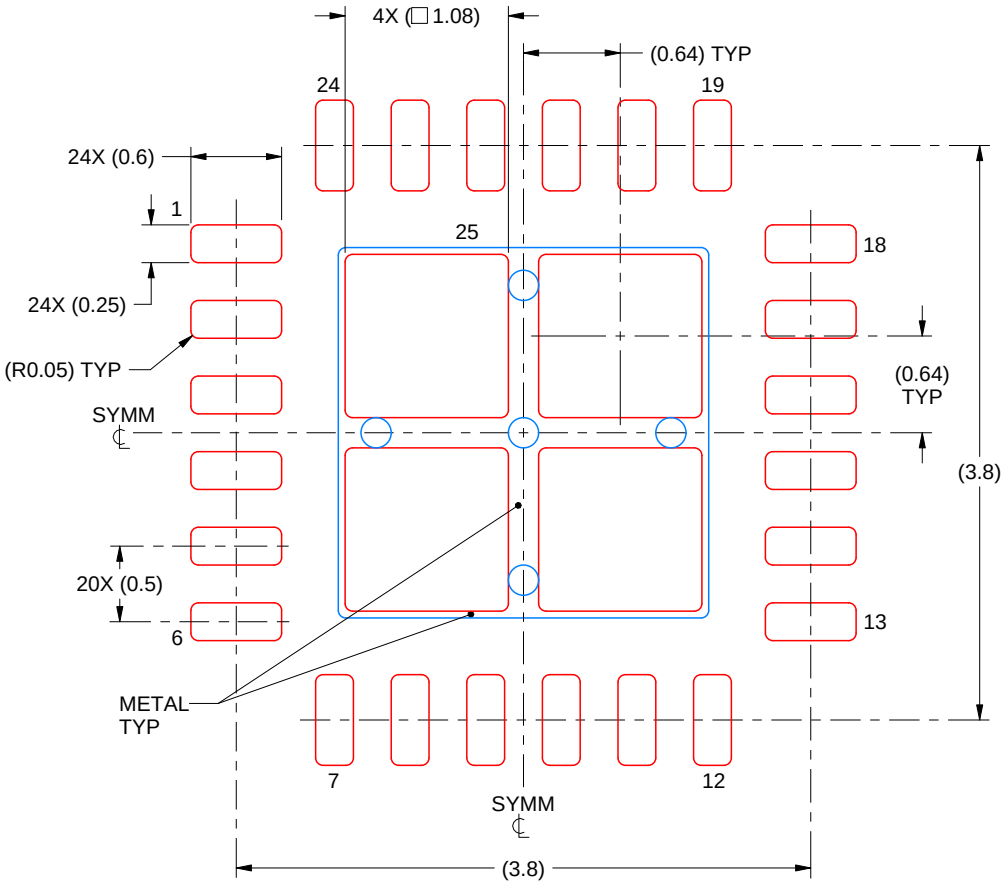


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

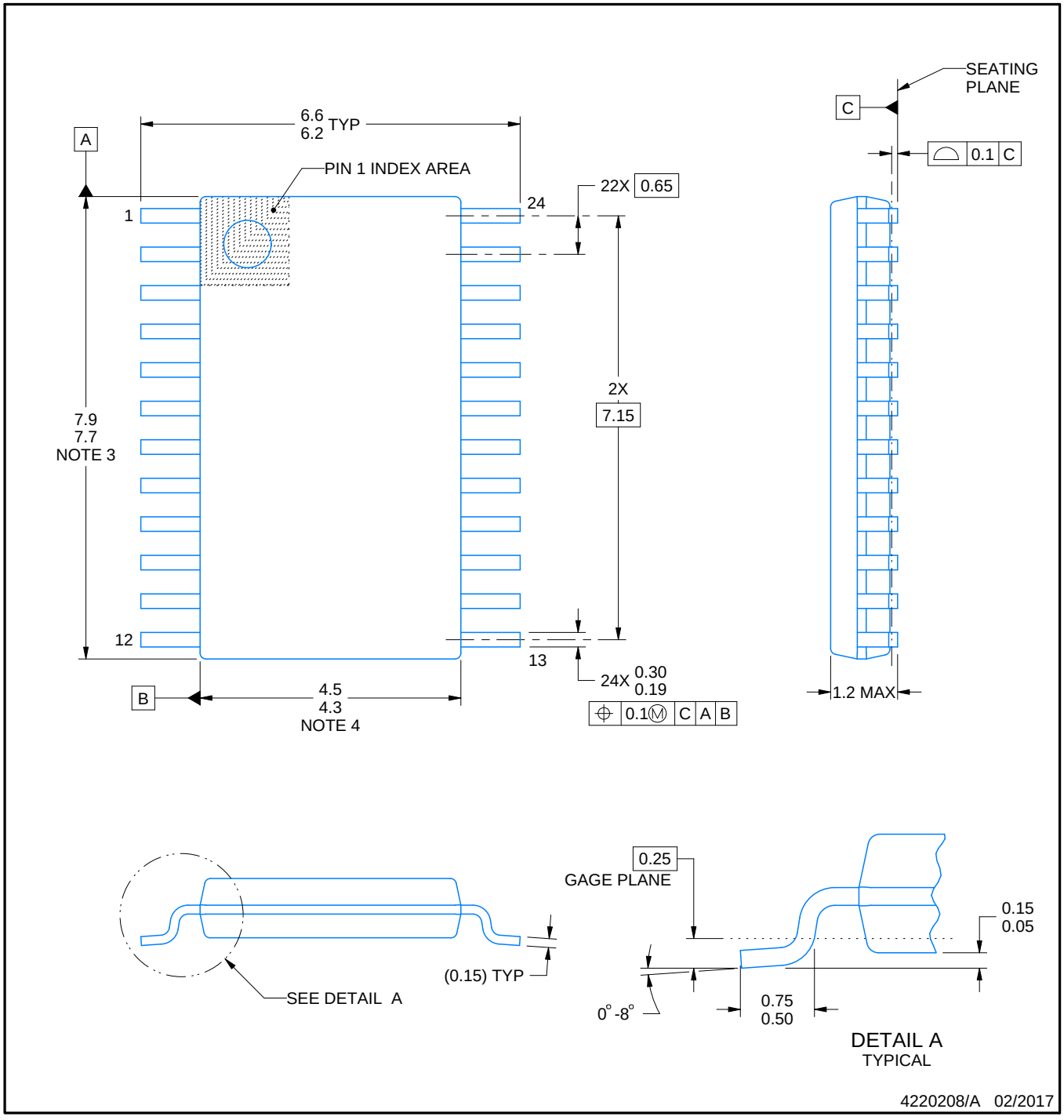
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0024A

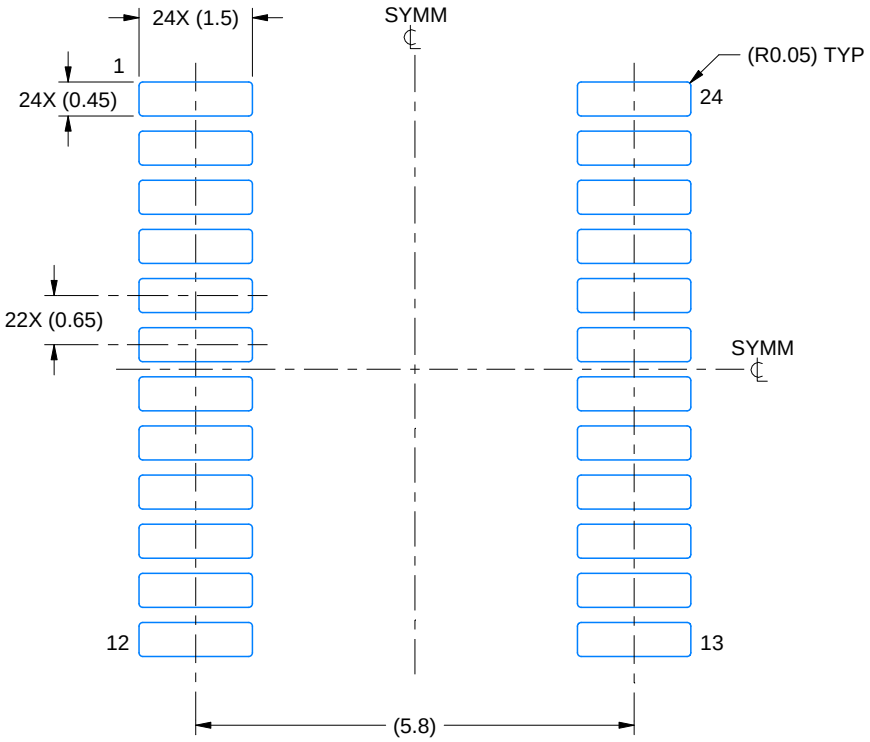
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

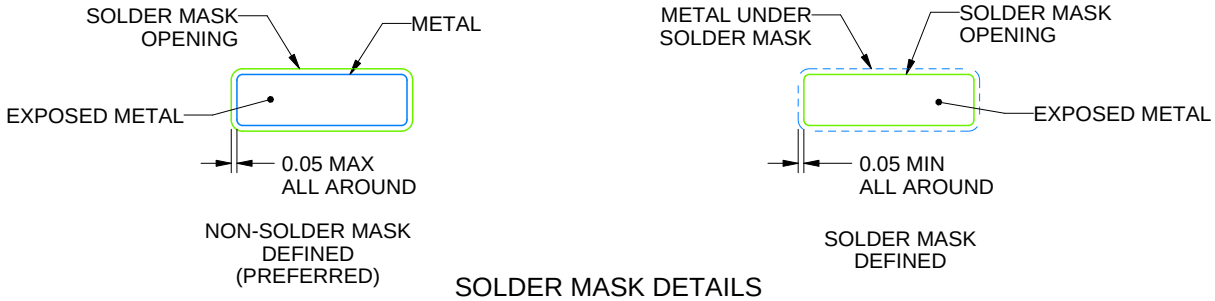


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

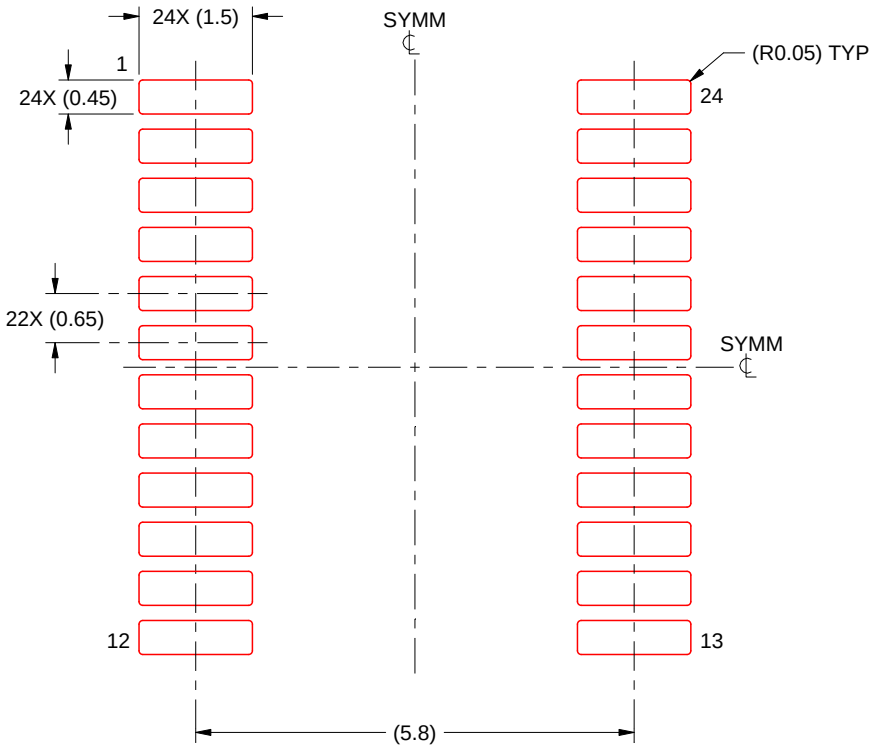


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265