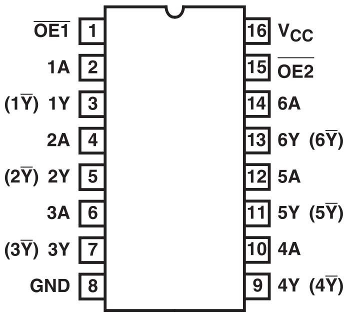
高速 CMOS 逻辑 6 路缓冲器/线路驱动器，三态同相和反相

查询样品: **CD74HC365-Q1**, **CD74HC366-Q1**, **CD74HCT365-Q1**

特性

- 适合于汽车应用
- 缓冲输入
- 大电流总线驱动器输出
- 典型传播延迟 t_{PLH}、t_{PHL} = **8ns** （在 V_{CC} = **5V**、C_L = **15pF**、T_A = **25**℃ 时）
- 扇出 （在整个温度范围内）
  - 标准输出 .... **10 LSTTL** 负载
  - 总线驱动器输出 .... **15 LSTTL** 负载
- 宽工作温度范围 .... **—40**℃ 至 **125**℃
- 平衡的传播延迟及转换时间
- 与 **LSTTL** 逻辑 **IC** 相比，功耗有了显著的降低
- **HC** 型号
  - **2V** 至 **6V** 工作电压
  - 高的噪声免疫力： 在 V_{CC} = **5V** 时，N_{IL} = **30%** V_{CC}，N_{IH} = **30% VCC**
- **HCT** 型号
  - **4.5V** 至 **5.5V** 工作电压
  - 可直接兼容 **LSTTL** 输入逻辑器件， V_{IL} = **0.8V** （最大值）， V_{IH} = **2V** （最小值）
  - 具有 **CMOS** 输入兼容性，**Il ≤ 1mA** （在 V_{OL}、V_{OH} 条件下）

D封装
(顶视图)



说明

CD74HC365-Q1、CD74HC366-Q1 和 CD74HCT365-Q1 硅栅 CMOS 三态缓冲器是通用型高速同相和反相缓冲器。 它们具有大驱动电流输出，因而即使在驱动大的总线电容时仍能实现高速运作。 这些电路具有很低的 CMOS 电路功耗，然而速度却与低功耗肖特基 TTL 电路不相上下。 这两种电路均能够驱动多达 15 个低功耗肖特基输入。

CD74HC365-Q1 和 CD74HCT365-Q1 是同相缓冲器，而 CD74HC366-Q1 则是一款反相缓冲器。 这些器件具有两个三态控制输入（$\overline{OE1}$ 和$\overline{OE2}$）， 对这两个输入进行“或非”逻辑运算以控制全部 6 个逻辑门。

HCT365-Q1 逻辑系列与标准的 LS 逻辑系列具有速度、功能和引脚兼容性。

订购信息[(1)]

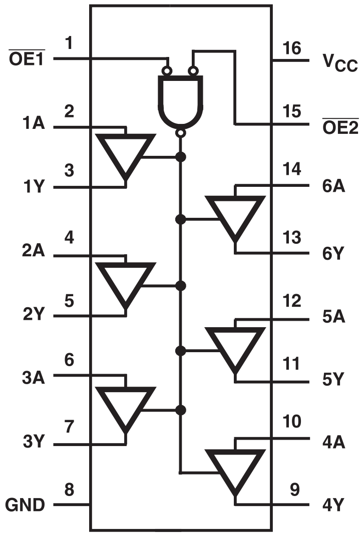
T_A	封装[(2)]		可订购的器件型号	顶端标记
－40℃至125℃	SOIC – D	卷盘 （ 2500 片 ）	CD74HC366QDRQ1	HC366Q
			CD74HC365QDRQ1	产品预览
			CD74HCT365QDRQ1	产品预览

(1) 有关最新的封装和订购信息，请参阅本文档结尾的“封装选项附录”，或访问 TI 网站：www.ti.com.cn。
(2) 封装图样、热数据和符号可登录 www.ti.com/package 获取。

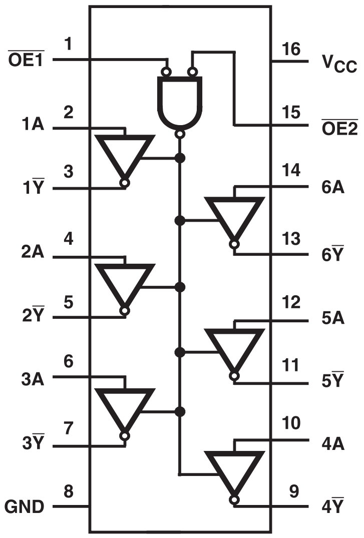
English Data Sheet: SCHS382

FUNCTIONAL DIAGRAMS

CD74HC365-Q1, CD74HCT365-Q1



CD74HC366-Q1

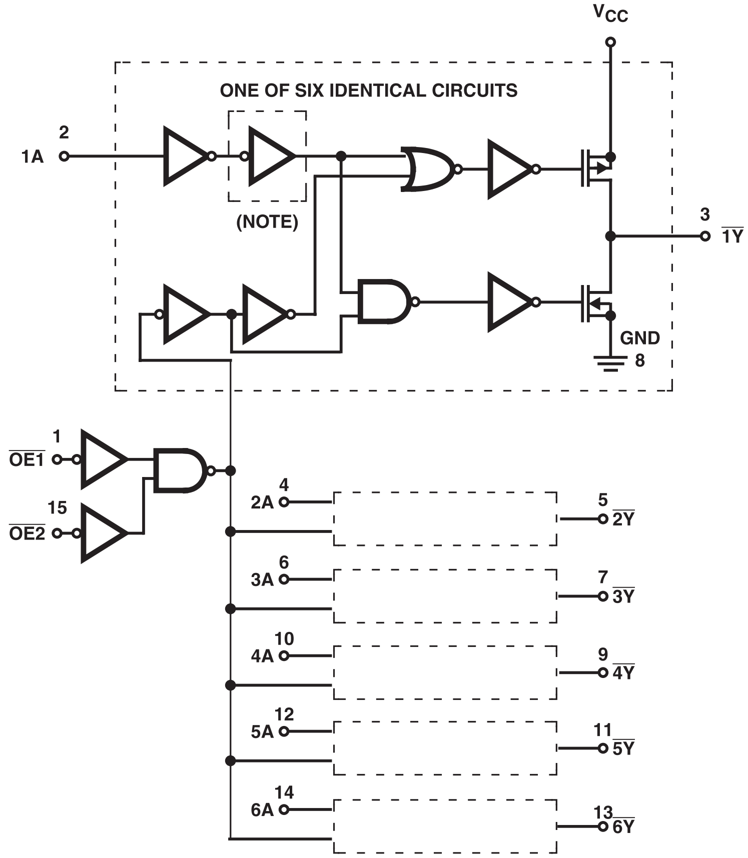


TRUTH TABLE(1)

INPUTS			OUTPUTS (Y)	
OE1	**OE2**	**A**	**HC/HCT365**	**HC366**
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

(1) H = High Voltage Level
L = Low Voltage Level
X = Don’t Care
Z = High Impedance (OFF) State

LOGIC DIAGRAM



NOTE: Inverter not included in CD74HC365-Q1, CD74HCT365-Q1

Figure 1. LOGIC DIAGRAM FOR THE HC/HCT365 AND HC366 (outputs for HC/HCT365 are complements of those shown, i.e., 1Y, 2Y, etc.)

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	CONDITIONS	VALUE
V_{CC}	DC supply voltage		-0.5V to +7V
I_{IK}	DC input diode current,	$V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	±20mA
I_{OK}	DC output diode current	$V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	±20mA
I_O	DC drain current per output	$V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	±35mA
	DC output source or sink current per output pin		±25mA
I_{CC}	DC V_{CC} or ground current		±50mA
ESD	Electrostatic discharge	Human-Body Model	1.5kV
		Machine Model	200V
		Field_Induced_Charged Device Model	250V
	Latch up		Class I

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER		MIN	MAX	UNIT
θ_{JA}	Thermal resistance (typical)[1]	D (SOIC) package		73	°C/W
J_T	Maximum junction temperature			150	°C
T_{stg}	Maximum storage temperature range		–65	150	°C
	Maximum lead temperature (soldering 10s)	(SOIC - lead tips only)		300	°C

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I	DC Input voltage		0	V_{CC}	V
V_O	DC Output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	125	°C
	Input Rise and Fall Time	2 V		1000	ns
		4.5 V		500	
		6 V		400	

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 125°C		UNITS
			V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	
HC Types											
V_{IH}	High-level input voltage		-	-	2	1.5	-	-	1.5	-	V
					4.5	3.15	-	-	3.15	-	
					6	4.2	-	-	4.2	-	
V_{IL}	Low-level input voltage		-	-	2	-	-	0.5	-	0.5	V
					4.5	-	-	1.35	-	1.35	
					6	-	-	1.8	-	1.8	
V_{OH}	High-level output voltage loads	CMOS	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	V
					4.5	4.4	-	-	4.4	-	
					6	5.9	-	-	5.9	-	
		TTL		-6	4.5	3.98	-	-	3.7	-	
				-7.8	6	5.48	-	-	5.2	-	
V_{OL}	Low-level output voltage loads	CMOS	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	V
					4.5	-	-	0.1	-	0.1	
					6	-	-	0.1	-	0.1	
		TTL		6	4.5	-	-	0.26	-	0.4	
				7.8	6	-	-	0.26	-	0.4	
I_I	Input leakage current		V_{CC} or GND	-	6	-	-	±0.1	-	±1	μA
I_{CC}	Quiescent device current		V_{CC} or GND	0	6	-	-	8	-	160	μA
I_{OZ}	Three-state leakage current		V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND	6	-	-	±0.5	-	±10	μA
HCT Types											
V_{IH}	High-level input voltage		-	-	4.5 to 5.5	2	-	-	2	-	V
V_{IL}	Low-level input voltage		-	-	4.5 to 5.5	-	-	0.8	-	0.8	V
V_{OH}	High-level output voltage loads	CMOS	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	V
		TTL		-4	4.5	3.98	-	-	3.7	-	
V_{OL}	Low-level output voltage loads	CMOS	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	V
		TTL		4	4.5	-	-	0.26	-	0.4	
I_I	Input leakage current		V_{CC} or GND	-	5.5	-	-	±0.1	-	±1	μA
I_{CC}	Quiescent device current		V_{CC} or GND	0	5.5	-	-	8	-	160	μA
ΔI_{CC}	Additional quiescent device current per input pin: 1 unit load (1)		V_{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	490	μA
I_{OZ}	Three-state leakage current		V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND	5.5	-	-	±0.5	-	±10	μA

(1) For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading

INPUT	UNIT LOADS
$\overline{\text{OE1}}$	0.6
All Others	0.55

SWITCHING CHARACTERISTICS

Input t_r, t_f = 6ns

PARAMETER			TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 125°C	UNITS
					TYP	MAX	MAX	
HC Types								
t_{PLH}, t_{PHL}	Propagation delay, data to outputs	HC365	C_L = 50pF	2	-	110	165	ns
				4.5	-	22	33	
				6	-	19	28	
			C_L = 15pF	5	9	-	-	
		HC366	C_L = 50pF	2	-	150	225	
				4.5	-	31	45	
				6	-	26	38	
			C_L = 15pF	5	12	-	-	
t_{TLH}, t_{THL}	Output transition time		C_L = 50pF	2	-	60	90	ns
				4.5	-	12	18	
				6	-	10	15	
C_I	Input capacitance		-	-	-	10	10	pF
C_O	Three-state output capacitance		-	-	-	20	20	pF
C_{PD}	Power dissipation capacitance (1) (2)		-	5	40	-	-	pF
HCT Types								
t_{PLH}, t_{PHL}	Propagation delay, data to outputs	HCT365	C_L = 50pF	4.5	-	25	38	ns
			CL = 15pF	5	9	-	-	
		HCT366	C_L = 50pF	4.5	-	27	41	
			CL = 15pF	5	11	-	-	
t_{PLH}, t_{PHL}	Propagation delay, output enable and disable to outputs		C_L = 50pF	4.5	-	35	53	ns
			C_L = 15pF	5	14	-	-	
t_{TLH}, t_{THL}	Output transition time		C_L = 50pF	4.5	-	12	18	ns
C_I	Input capacitance		-	-	-	10	10	pF
C_O	Three-state output capacitance		-	-	-	20	20	pF
C_{PD}	Power dissipation capacitance (1) (2)		-	5	42	-	-	pF

(1) C_{PD} is used to determine the dynamic power consumption, per inverter.

(2) $P_D = V_{CC2} \times f_i (C_{PD} + C_L)$, where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage

TEST CIRCUIT AND WAVEFORMS

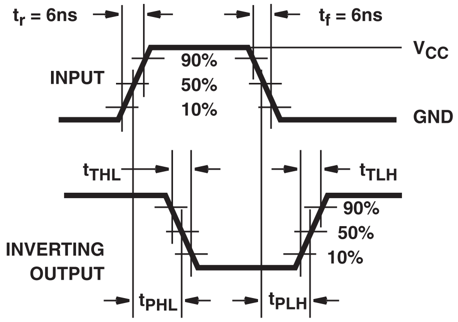


Figure 2. HC and HCU Transition Times and Propagation Delay Times, Combination Logic

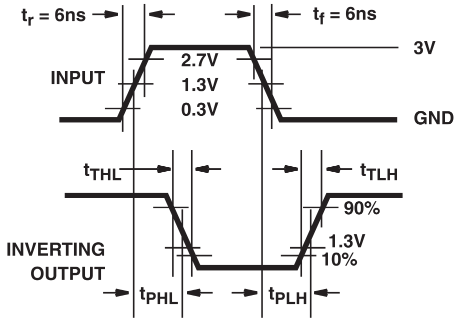


Figure 3. HCT Transition Times and Propagation Delay Times, Combination Logic

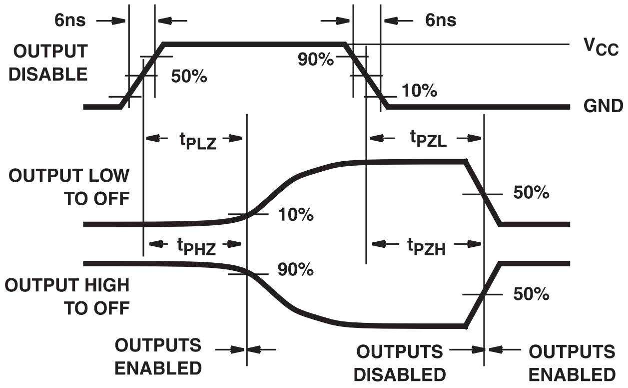


Figure 4. HC Three-State Propagation Delay Waveform

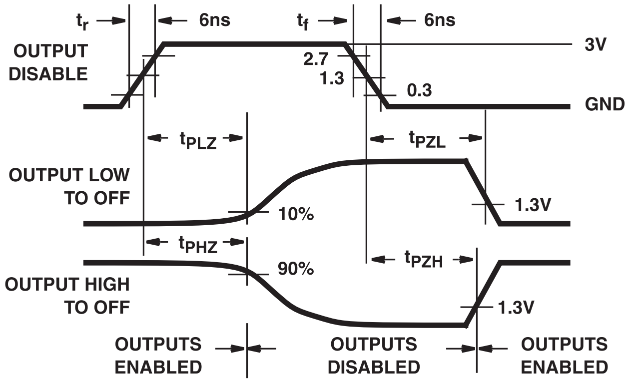
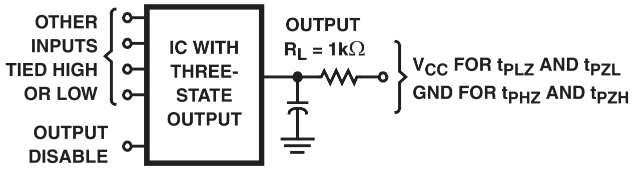


Figure 5. HCT Three-State Propagation Delay Waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

Figure 6. HC and HCT Three-State Propagation Delay Test Circuit

重要声明

可访问以下 URL 地址以获取有关其它 TI 产品和应用解决方案的信息：

产品	
放大器	http://www.ti.com.cn/amplifiers
数据转换器	http://www.ti.com.cn/dataconverters
DSP	http://www.ti.com.cn/dsp
接口	http://www.ti.com.cn/interface
逻辑	http://www.ti.com.cn/logic
电源管理	http://www.ti.com.cn/power
微控制器	http://www.ti.com.cn/microcontrollers
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宽带	http://www.ti.com.cn/broadband
数字控制	http://www.ti.com.cn/control
光纤网络	http://www.ti.com.cn/opticalnetwork
安全	http://www.ti.com.cn/security
电话	http://www.ti.com.cn/telecom
视频与成像	http://www.ti.com.cn/video
无线	http://www.ti.com.cn/wireless

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC366QDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC366Q	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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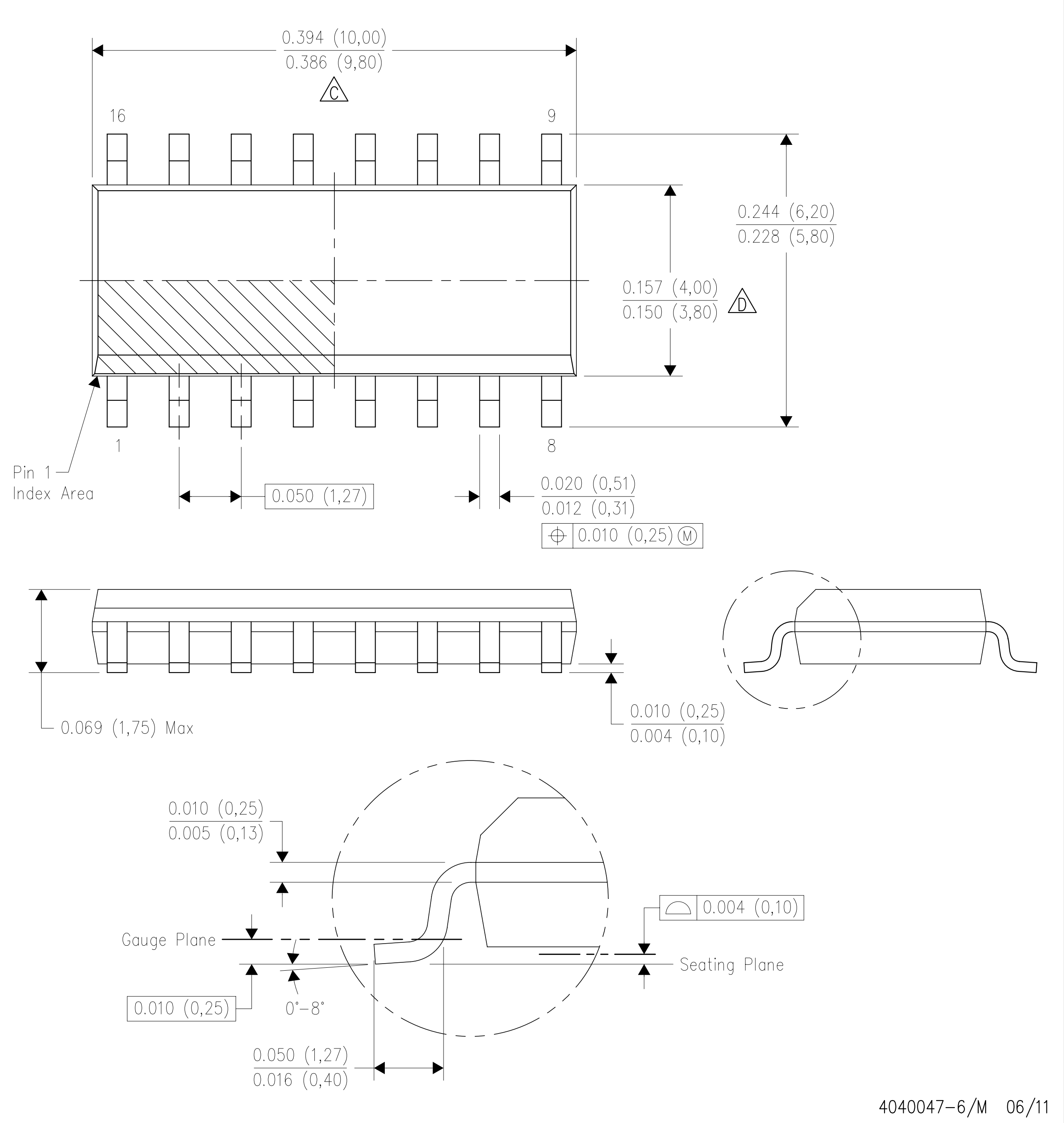
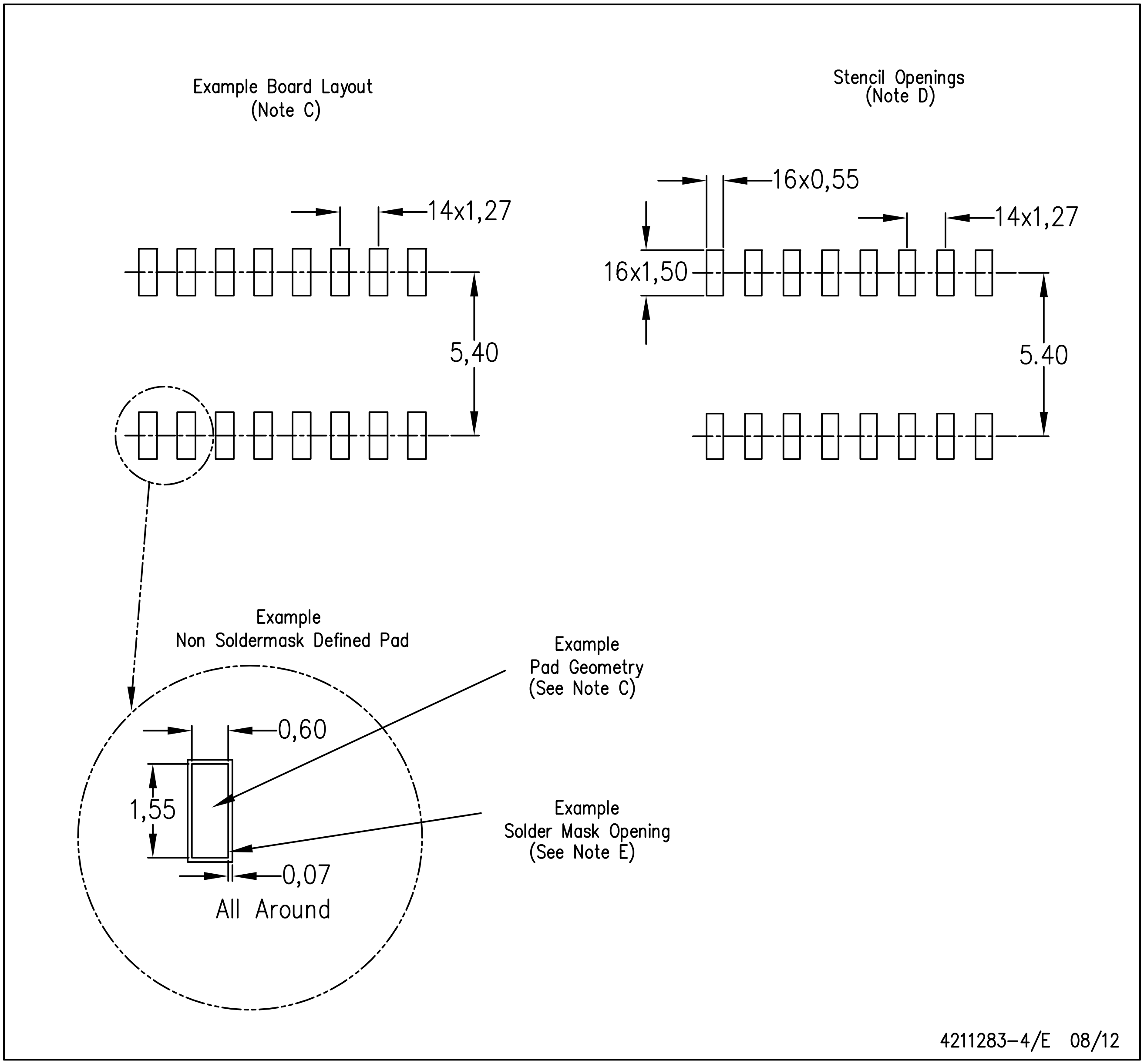
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122