# TLV170x 2.2V 至 36V 微功耗比较器

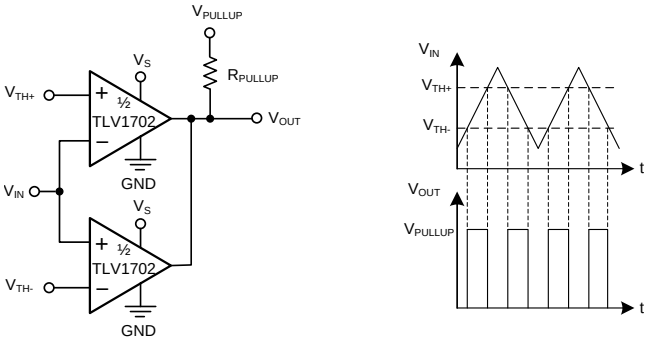
## 1 特性

- 电源范围：
  +2.2V 至 +36V 或 ±1.1V 至 ±18V
- 低静态电流：
  每个比较器 55µA
- 输入共模范围包括两个电源轨
- 低传播延迟：560ns
- 低输入偏移电压：300µV
- 集电极开路输出：
  - 最大可高出负电源 36V 且不受电源电压影响
- 工业温度范围：
  -40°C 至 +125°C
- 小型封装：
  - 单通道：SC70-5、SOT-23-5 和 SOT553-5
  - 双通道：VSSOP-8、X2QFN-8
  - 四通道：TSSOP-14

## 2 应用范围

- 过压和欠压检测器
- 窗口比较器
- 过流检测器
- 零交叉检测器
- 针对以下应用的系统监控：
  - 电源
  - 白色家电
  - 工业传感器
  - 汽车
  - 医疗

**TLV1702 作为窗口比较器**




## 3 说明

TLV170x 系列器件提供宽电源范围、轨到轨输入、低静态电流和低传播延迟。 所有这些特性均符合行业标准，采用极小封装，借此，这些器件得以成为目前市场上可提供的最佳通用比较器。

集电极开路输出具有能够将输出拉至任意电压轨（最大可高出负电源 +36V）的优势，且不受 TLV170x 电源电压影响。

这些器件均可提供单通道 (TLV1701)、双通道 (TLV1702) 和四通道 (TLV1704) 三种版本。 低输入偏移电压、低输入偏置电流、低电源电流和开集配置使得 TLV170x 系列能够灵活处理从简单电压检测到驱动单个继电器的大多数应用。

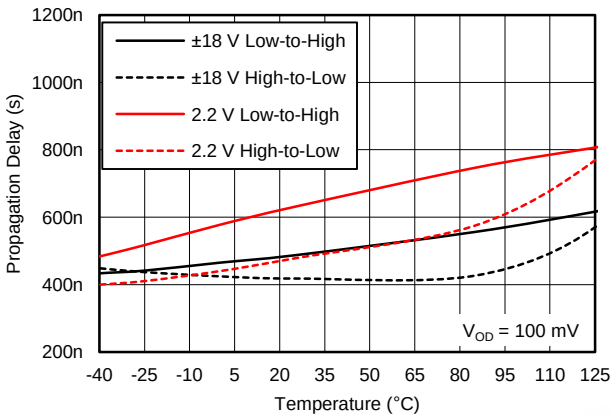
所有器件的额定工作温度均在扩展的工业温度范围 –40°C 到 +125°C 内。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TLV1701 | SOT553 (5) | 1.20mm × 1.60mm |
| | SC-70 (5) | 1.25mm × 2.00mm |
| | SOT-23 (5) | 1.60mm x 2.90mm |
| TLV1702 | X2QFN (8) | 1.50mm x 1.50mm |
| | VSSOP (8)(2) | 3.00mm × 3.00mm |
| TLV1704 | TSSOP (14) | 4.40mm × 5.00mm |

(1) 要了解所有可用封装，请见数据表末尾的封装选项附录。
(2) VSSOP 封装与 MSOP 封装相同。

稳定传播延迟与温度




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (December 2014) to Revision D** — **Page**

- 已将文档状态从“混合状态”更改为“量产数据” ... 1
- 已将 TLV1702 RUG 封装的状态更改为量产数据 ... 1

**Changes from Revision B (October 2014) to Revision C** — **Page**

- TLV1701 DCK 封装已从预览更改为量产数据 ... 1
- Changed Handling Ratings table to ESD Ratings table, and moved storage temperature to Absolute Maximum Ratings table ... 6

**Changes from Revision A (September 2014) to Revision B** — **Page**

- 更改了器件信息表中的脚注 2：已将 TLV1701 添加到可用器件列表中 ... 1
- Added TLV1701 to list of production data packages in footnote for the *Pin Configuration and Functions* section ... 5
- Added TLV1701 row to $V_{(ESD)}$ parameter in Handling Ratings table ... 6


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**Changes from Original (December 2013) to Revision A** **Page**

- 已将文档格式更改为符合最新的数据表标准；添加了新章节并移动了现有章节 ..... 1
- TLV1704 PW (TSSOP-14) 封装已从预览更改为量产数据 ..... 1
- 在集电极开路输出特性中添加了分项 ..... 1
- 在*说明*部分添加了第二段 ..... 1
- 已从*说明*部分中删除封装信息；冗余信息 ..... 1
- Changed Related Products table to Device Comparison table, moved from page 1, and added TLV370x family ..... 4
- Added TLV1701, TLV1702 RUG, and TLV704 package drawings ..... 5
- Added thermal information for TLV1702 RUG, TLV1704 PW, and all TLV1701 packages ..... 6
- Moved switching characteristics parameters from Electrical Characteristics table to new Switching Characteristics table .. 7
- Changed all typical values in Switching Characteristics table ..... 7
- Changed title for Figure 1 ..... 8
- Changed Figure 8 ..... 8
- Changed Figure 9 ..... 8
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- Changed Figure 11 ..... 8
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- Changed Figure 13 ..... 9
- Changed Figure 14 ..... 9
- Changed *Application Information* and moved section ..... 13
- Deleted *Application Examples* section ..... 13

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# 5 Device Comparison

| DEVICE | FEATURES |
|---|---|
| TLV3201 | 40-ns, 40-µA, push-pull comparator |
| TLV3202 | |
| TLV3501 | 4.5-ns, rail-to-rail, push-pull, high-speed comparator |
| TLV3502 | |
| TLV3401 | Nanopower open-drain output comparator |
| TLV3402 | |
| TLV3404 | |
| TLV3701 | Nanopower push-pull output comparator |
| TLV3702 | |
| TLV3704 | |
| REF3325 | 3.9-µA, SC70-3 voltage reference |
| REF3330 | |
| REF3333 | |


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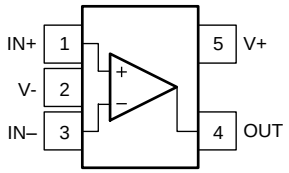
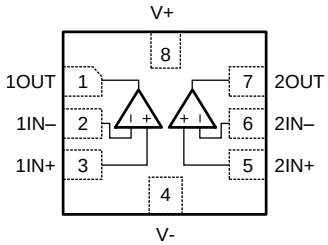
# 6 Pin Configuration and Functions

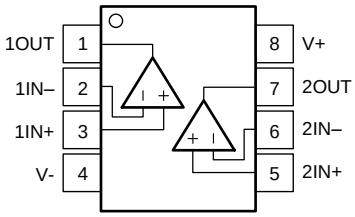
**TLV1701**
**DBV (SOT-23-5), DCK (SC70-5), DRL (SOT553-5) Packages**
**Top View**



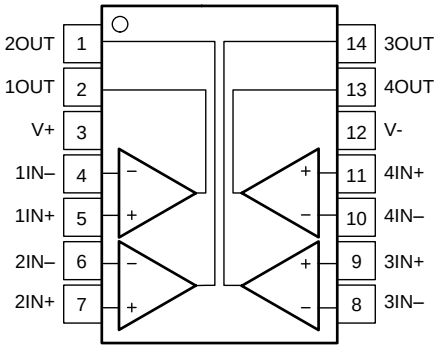

**TLV1702**
**RUG (X2QFN-8) Package**
**Top View**




**TLV1702**
**DGK (VSSOP-8) Package**
**Top View**




**TLV1704**
**PW (TSSOP-14) Package**
**Top View**




## Pin Functions

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| | NO. | | | | |
| NAME | TLV1701 DBV, DCK, DRL | TLV1702 DGK, RUG | TLV1704 PW | | |
| IN+ | 1 | — | — | I | Noninverting input |
| 1IN+ | — | 3 | 5 | I | Noninverting input, channel 1 |
| 2IN+ | — | 5 | 7 | I | Noninverting input, channel 2 |
| 3IN+ | — | — | 9 | I | Noninverting input, channel 3 |
| 4IN+ | — | — | 11 | I | Noninverting input, channel 4 |
| IN– | 3 | — | — | I | Inverting input |
| 1IN– | — | 2 | 4 | I | Inverting input, channel 1 |
| 2IN– | — | 6 | 6 | I | Inverting input, channel 2 |
| 3IN– | — | — | 8 | I | Inverting input, channel 3 |
| 4IN– | — | — | 10 | I | Inverting input, channel 4 |
| OUT | 4 | — | — | O | Output |
| 1OUT | — | 1 | 2 | O | Output, channel 1 |
| 2OUT | — | 7 | 1 | O | Output, channel 2 |
| 3OUT | — | — | 14 | O | Output, channel 3 |
| 4OUT | — | — | 13 | O | Output, channel 4 |
| V+ | 5 | 8 | 3 | — | Positive (highest) power supply |
| V– | 2 | 4 | 12 | — | Negative (lowest) power supply |

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# 7 Specifications

## 7.1 Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | | | +40 (±20) | V |
| Signal input pins | Voltage[(2)] | ($V_S$–) – 0.5 | ($V_S$+) + 0.5 | V |
| | Current[(2)] | | ±10 | mA |
| Output short-circuit[(3)] | | Continuous | | mA |
| Operating temperature range | | –55 | +150 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | +150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground; one comparator per package.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| TLV1701 and TLV1702 | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)] | ±1500 | |
| TLV1704 | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)] | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage $V_S$ = ($V_S$+) – ($V_S$–) | 2.2 (±1.1) | | 36 (±18) | V |
| Specified temperature | –40 | | 125 | °C |

## 7.4 Thermal Information: TLV1701

| THERMAL METRIC[(1)] | | TLV1701 | | | UNIT |
|---|---|---|---|---|---|
| | | DRL (SOT553) | DCK (SC70) | DBV (SOT23) | |
| | | 5 PINS | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 271.5 | 283.6 | 233.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 115.6 | 94.1 | 156.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 89.7 | 61.3 | 60.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 17.6 | 1.9 | 35.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 89.2 | 60.5 | 59.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


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## 7.5 Thermal Information: TLV1702 and TLV1704

| THERMAL METRIC[1] | | TLV1702 | | TLV1704 | UNIT |
|---|---|---|---|---|---|
| | | RUG (QFN) | DGK (VSSOP) | PW (TSSOP) | |
| | | 8 PINS | 8 PINS | 14 PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 205.6 | 199 | 128.1 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 77.1 | 89.5 | 56.5 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 107.0 | 120.4 | 69.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.0 | 22.0 | 9.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 107.0 | 118.7 | 69.3 | °C/W |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.6 Electrical Characteristics

at $T_A$ = +25°C, $V_S$ = +2.2 V to +36 V, $C_L$ = 15 pF, $R_{PULLUP}$ = 5.1 kΩ, $V_{CM}$ = $V_S$ / 2, and $V_S$ = $V_{PULLUP}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $T_A$ = 25°C, $V_S$ = 2.2 V | | ±0.5 | ±3.5 | mV |
| | | $T_A$ = 25°C, $V_S$ = 36 V | | ±0.3 | ±2.5 | mV |
| | | $T_A$ = –40°C to +125°C | | | ±5.5 | mV |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_A$ = –40°C to +125°C | | ±4 | ±20 | µV/°C |
| PSRR | Power-supply rejection ratio | | | 15 | 100 | µV/V |
| | | $T_A$ = –40°C to +125°C | | 20 | | µV/V |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage range | $T_A$ = –40°C to +125°C | (V–) | | (V+) | V |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | | | 5 | 15 | nA |
| | | $T_A$ = –40°C to +125°C | | | 20 | nA |
| $I_{OS}$ | Input offset current | | | 0.5 | | nA |
| $C_{LOAD}$ | Capacitive load drive | | See *Typical Characteristics* | | | |
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing from rail | $I_O$ ≤ 4 mA, input overdrive = 100 mV, $V_S$ = 36 V | | | 900 | mV |
| | | $I_O$ = 0 mA, input overdrive = 100 mV, $V_S$ = 36 V | | | 600 | mV |
| $I_{SC}$ | Short circuit sink current | | | 20 | | mA |
| | Output leakage current | $V_{IN+}$ > $V_{IN–}$ | | 70 | | nA |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage range | | 2.2 | | 36 | V |
| $I_Q$ | Quiescent current (per channel) | $I_O$ = 0 A | | 55 | 75 | µA |
| | | $I_O$ = 0 A, $T_A$ = –40°C to +125°C | | | 100 | µA |

## 7.7 Switching Characteristics

at $T_A$ = +25°C, $V_S$ = +2.2 V to +36 V, $C_L$ = 15 pF, $R_{PULLUP}$ = 5.1 kΩ, $V_{CM}$ = $V_S$ / 2, and $V_S$ = $V_{PULLUP}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pHL}$ | Propagation delay time, high-to-low | Input overdrive = 100 mV | | 460 | | ns |
| $t_{pLH}$ | Propagation delay time, low-to-high | Input overdrive = 100 mV | | 560 | | ns |
| $t_R$ | Rise time | Input overdrive = 100 mV | | 365 | | ns |
| $t_F$ | Fall time | Input overdrive = 100 mV | | 240 | | ns |

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## 7.8 Typical Characteristics

at $T_A$ = +25°C, $V_S$ = +5 V, $R_{PULLUP}$ = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)

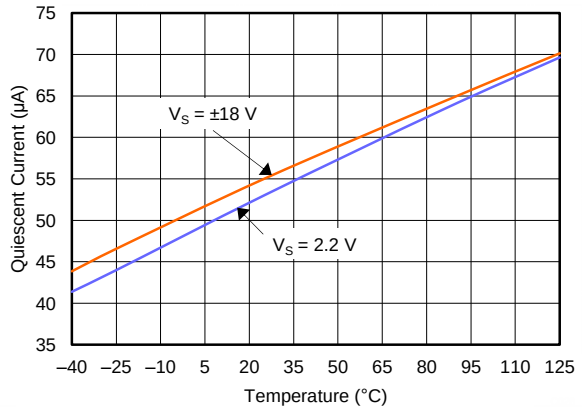


**Figure 1. Quiescent Current vs Temperature**

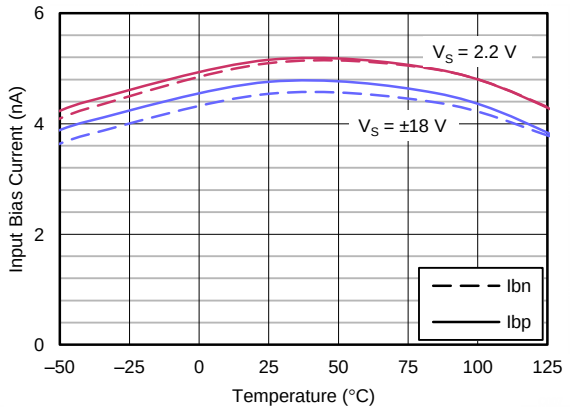


**Figure 2. Input Bias Current vs Temperature**

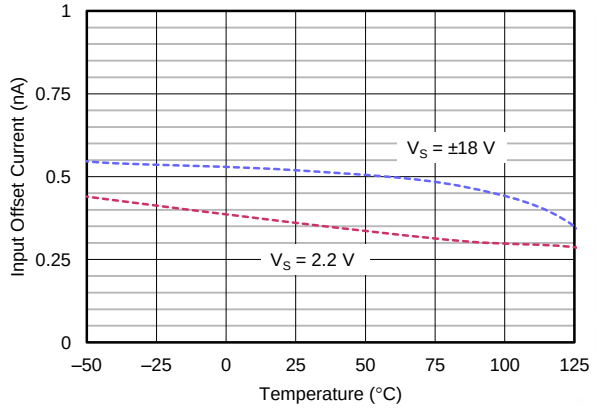


**Figure 3. Input Offset Current vs Temperature**

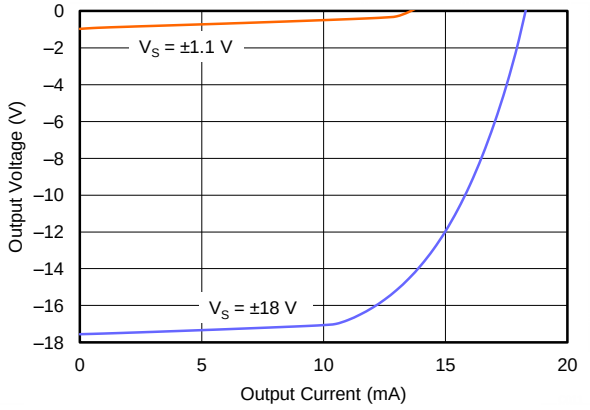


**Figure 4. Output Voltage vs Output Current**

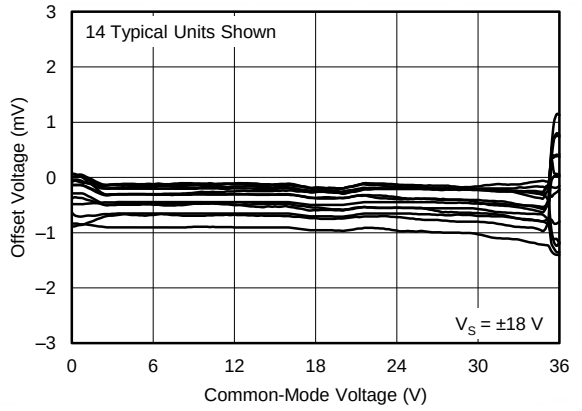


**Figure 5. Offset Voltage vs Common-Mode Voltage**

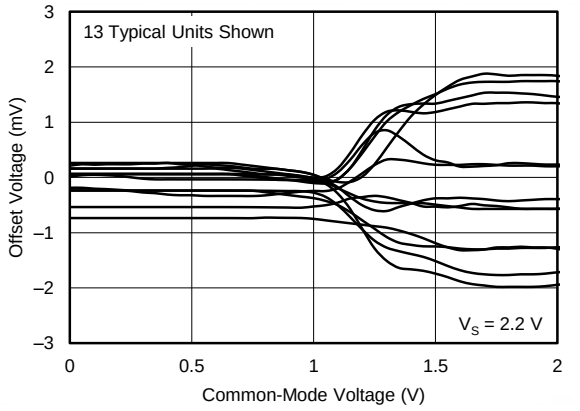


**Figure 6. Offset Voltage vs Common-Mode Voltage**


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## Typical Characteristics (continued)

at $T_A$ = +25°C, $V_S$ = +5 V, $R_{PULLUP}$ = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)

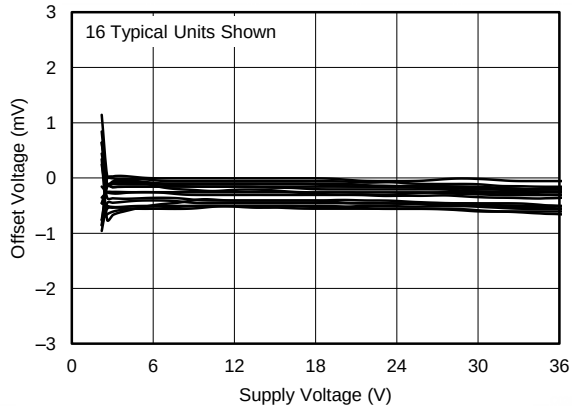


**Figure 7. Offset Voltage vs Supply Voltage**

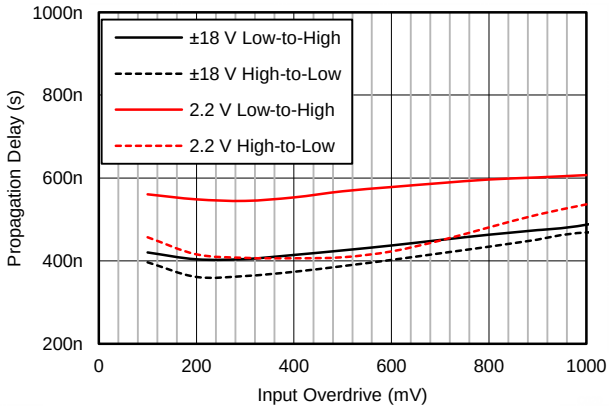


**Figure 8. Propagation Delay vs Input Overdrive**

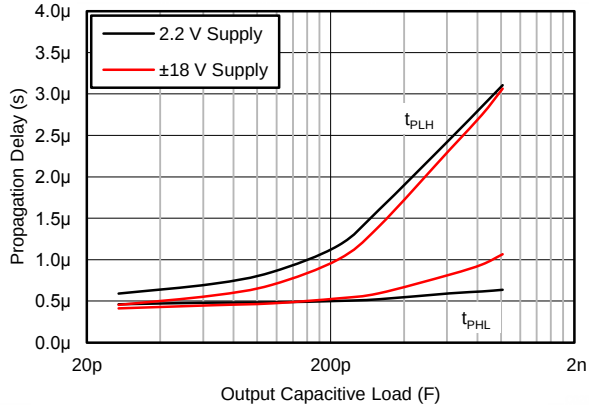


**Figure 9. Propagation Delay vs Capacitive Load**

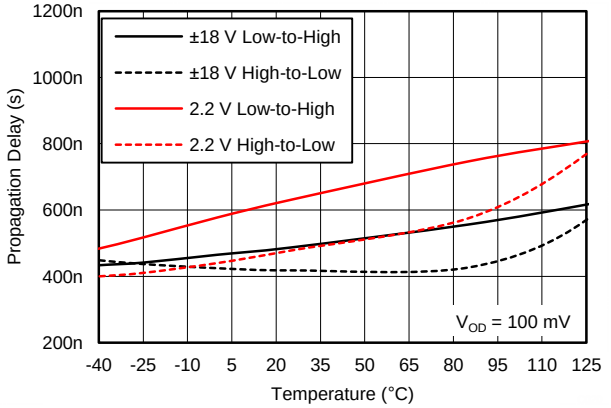


**Figure 10. Propagation Delay vs Temperature**

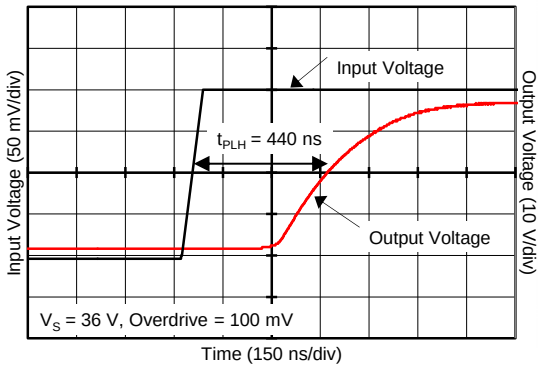


**Figure 11. Propagation Delay ($T_{pLH}$)**

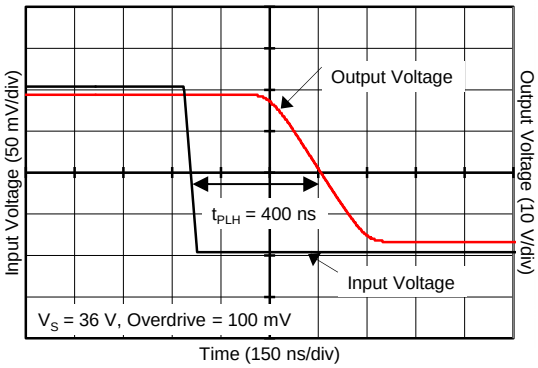


**Figure 12. Propagation Delay ($T_{pHL}$)**

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## Typical Characteristics (continued)

at $T_A$ = +25°C, $V_S$ = +5 V, $R_{PULLUP}$ = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)

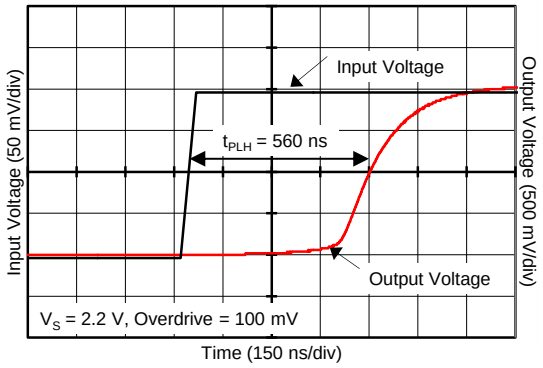


**Figure 13. Propagation Delay ($T_{pLH}$)**

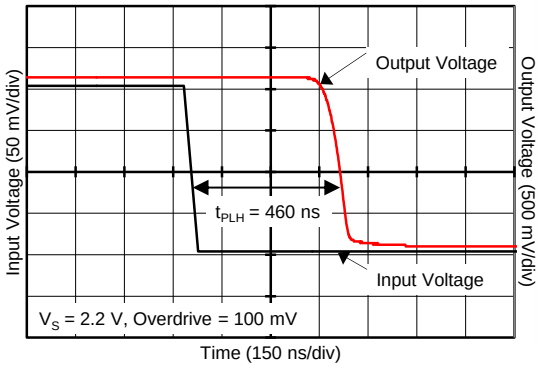


**Figure 14. Propagation Delay ($T_{pHL}$)**

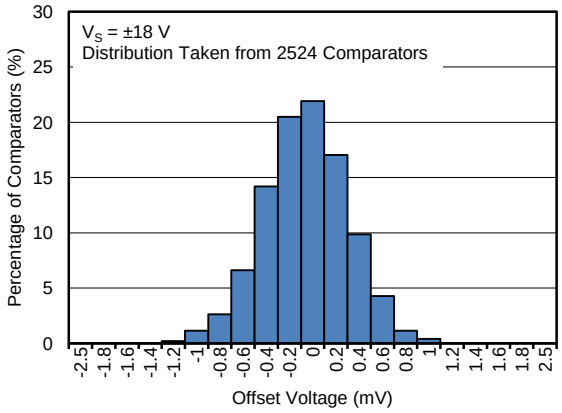


**Figure 15. Offset Voltage Production Distribution**

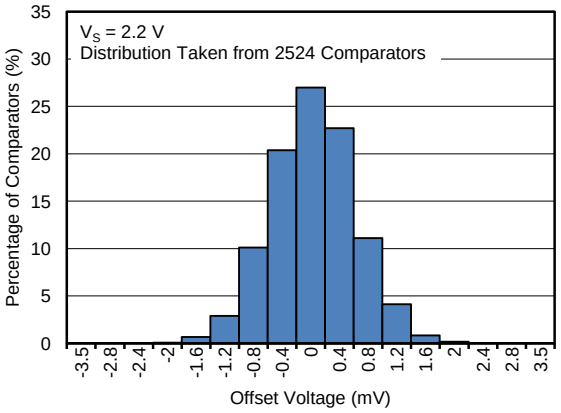


**Figure 16. Offset Voltage Production Distribution**

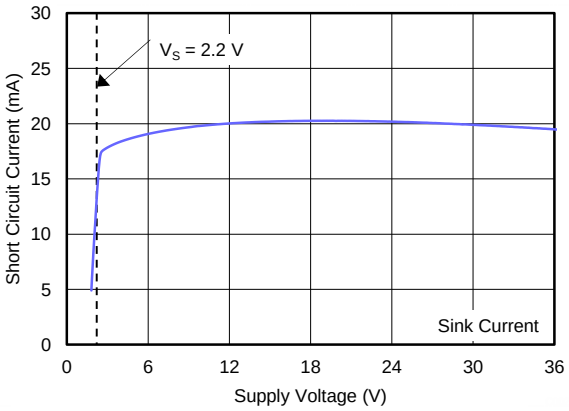


**Figure 17. Short-Circuit Current vs Supply Voltage**


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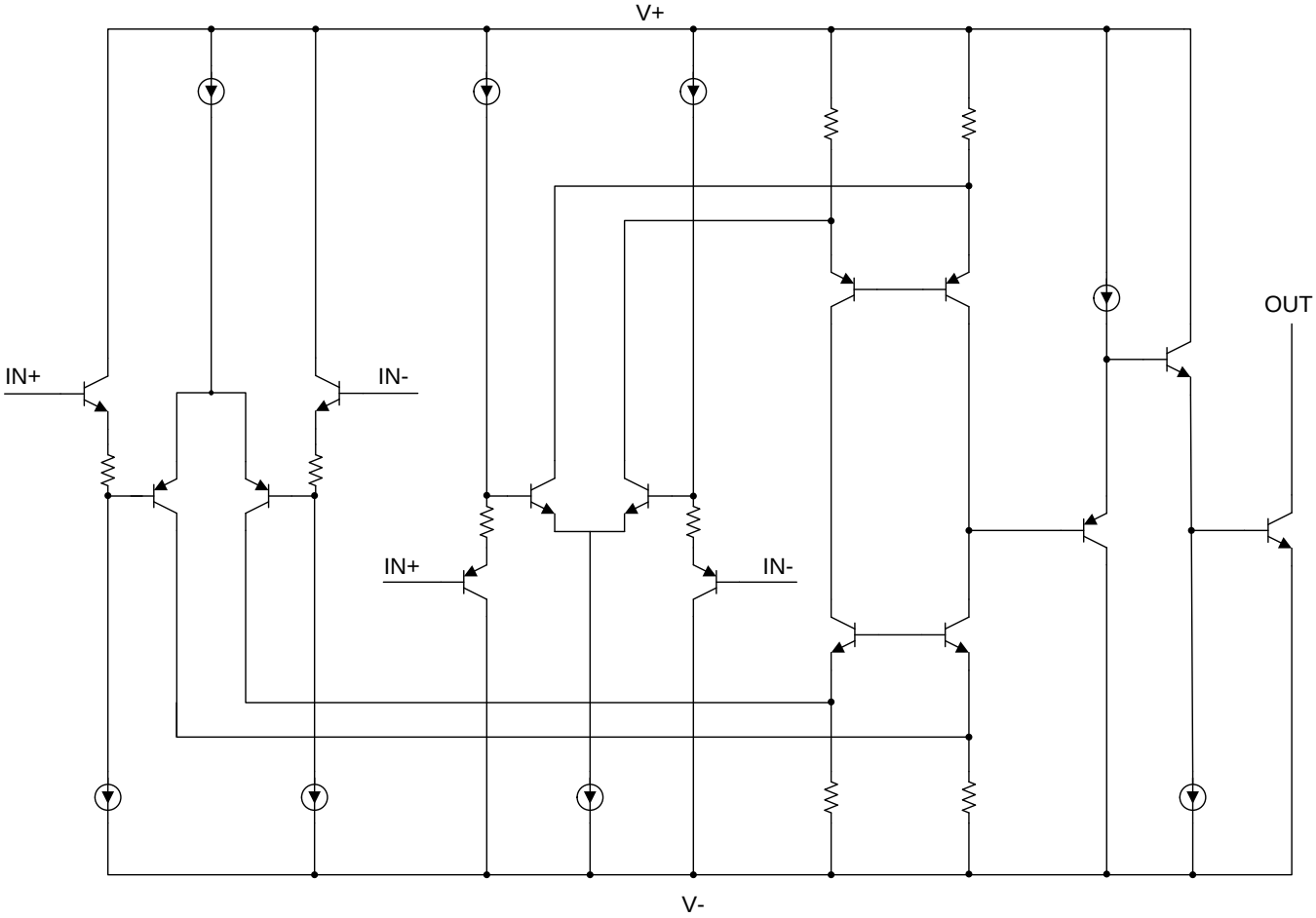
# 8 Detailed Description

## 8.1 Overview

The TLV170x comparators features rail-to-rail input and output on supply voltages as high as 36 V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55 µA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Comparator Inputs

The TLV170x are rail-to-rail input comparators, with an input common-mode range that includes the supply rails. The TLV170x is designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 18 shows the TLV170x response when input voltages exceed the supply, resulting in no phase inversion.

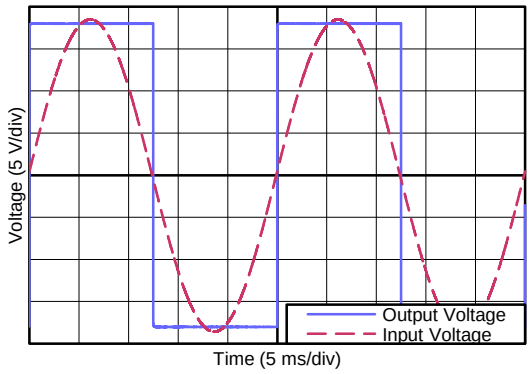



**Figure 18. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)**

## 8.4 Device Functional Modes

### 8.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV170x. The REF3333, as shown in Figure 19, provides a 3.3-V reference voltage with low drift and only 3.9 µA of quiescent current.

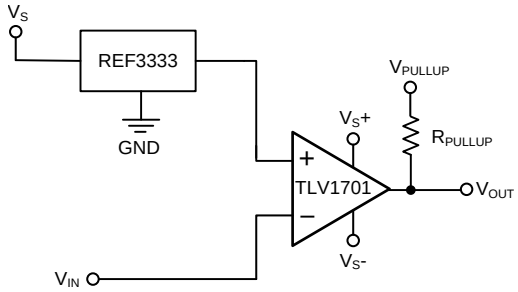



**Figure 19. Reference Voltage for the TLV170x**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# 9 Applications and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TLV170x can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

## 9.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

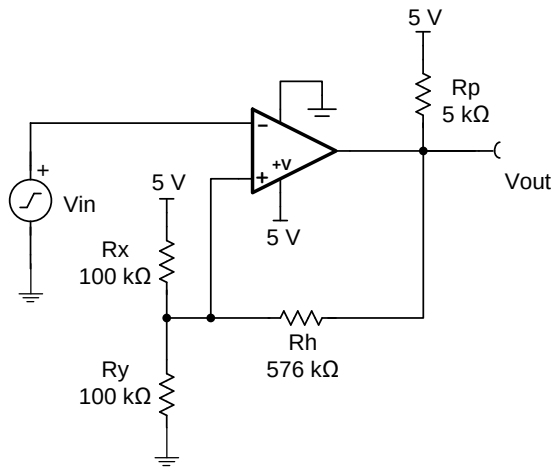


**Figure 20. Comparator Schematic with Hysteresis**

### 9.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V
- Input: 0 V to 5 V
- Lower threshold (VL) = 2.3 V ±0.1 V
- Upper threshold (VH) = 2.7 V ±0.1 V
- VH – VL = 2.4 V ±0.1 V
- Low power consumption

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

Figure 20 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if Rh > 100Rp.

When the output is at a logic high (5 V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7 V. The input signal must drive above VH = 2.7 V to cause the output to transition to logic low (0 V).

When the output is at logic low (0 V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3 V. The input signal must drive below VL = 2.3 V to cause the output to transition to logic high (5 V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design TIPD144, *Comparator with Hysteresis Reference Design*.

### 9.2.3 Application Curve

Figure 21 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76 V and the lower threshold is 2.34 V, both of which are close to the design target.

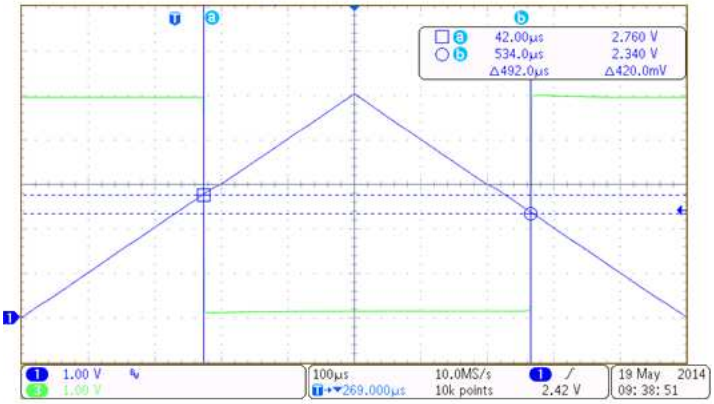


**Figure 21. TLV1701 Upper and Lower Threshold with Hysteresis**

## 10 Power Supply Recommendations

The TLV170x is specified for operation from 2.2 V to 36 V (±1.1 to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *Layout Guidelines* section.


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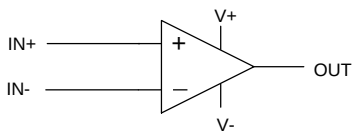
# 11 Layout

## 11.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV170x.
- To minimize supply noise, place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to $V_S$ as shown in Figure 22.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

## 11.2 Layout Example




(Schematic Representation)

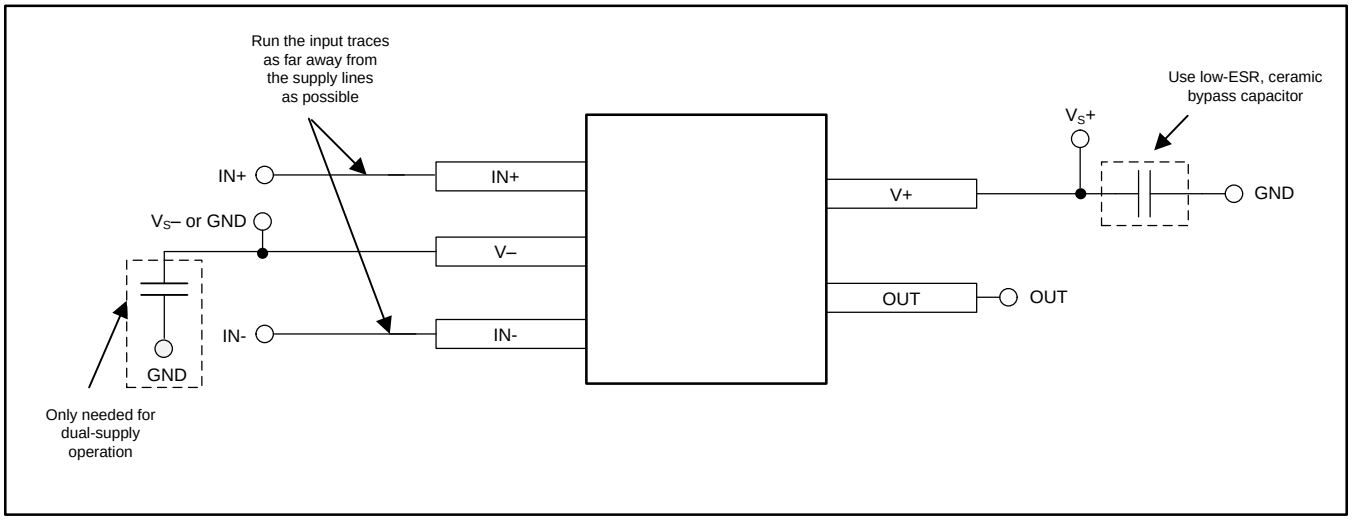



**Figure 22. Comparator Board Layout**

# 12 器件和文档支持

## 12.1 文档支持

### 12.1.1 相关文档

TIDU020 — *高精度设计，采用滞后参考设计的比较器。*

SBOS392 — REF3333 数据手册

## 12.2 相关链接

表 1 列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

**表 1. 相关链接**

| 器件 | 产品文件夹 | 样片与购买 | 技术文档 | 工具与软件 | 支持与社区 |
|---|---|---|---|---|---|
| TLV1701 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| TLV1702 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| TLV1704 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

## 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 术语表

SLYZ022 — *TI 术语表。*

这份术语表列出并解释术语、首字母缩略词和定义。

# 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV1701AIDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ZAYF | Samples |
| TLV1701AIDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ZAYF | Samples |
| TLV1701AIDCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SIR | Samples |
| TLV1701AIDCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SIR | Samples |
| TLV1701AIDRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | SIS | Samples |
| TLV1701AIDRLT | ACTIVE | SOT-5X3 | DRL | 5 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | SIS | Samples |
| TLV1702AIDGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1702 | Samples |
| TLV1702AIDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1702 | Samples |
| TLV1702AIRUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | Call TI \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FC | Samples |
| TLV1704AIPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TL1704 | Samples |
| TLV1704AIPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TL1704 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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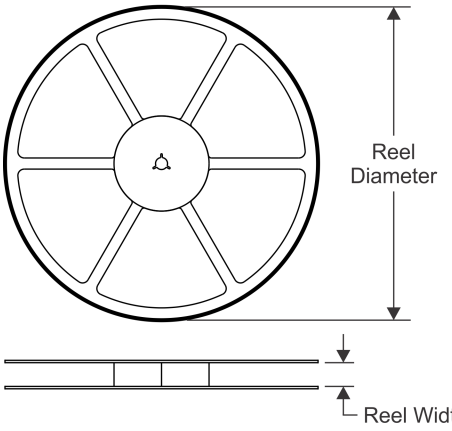
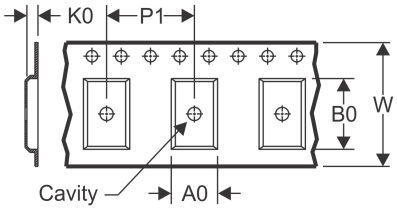
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

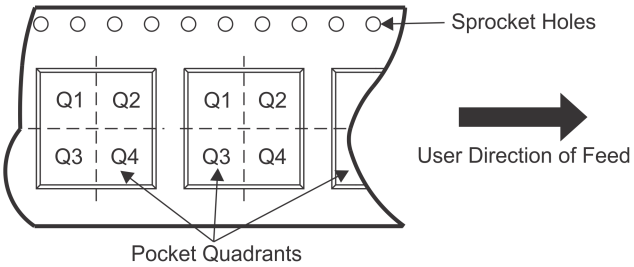



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

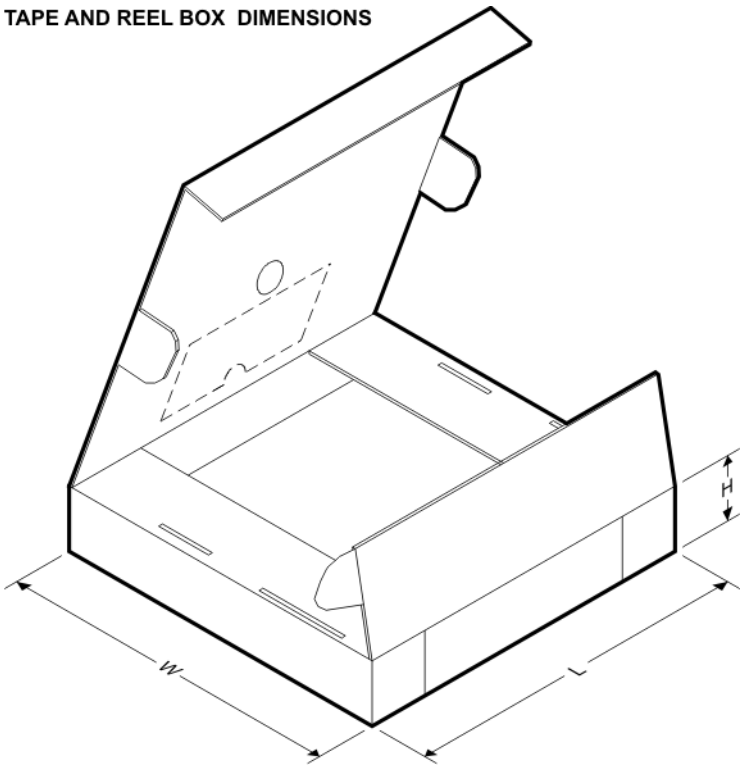
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV1701AIDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV1701AIDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV1701AIDCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV1701AIDCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV1701AIDRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| TLV1701AIDRLT | SOT-5X3 | DRL | 5 | 250 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| TLV1702AIDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV1702AIRUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 8.4 | 1.6 | 1.6 | 0.66 | 4.0 | 8.0 | Q2 |
| TLV1704AIPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

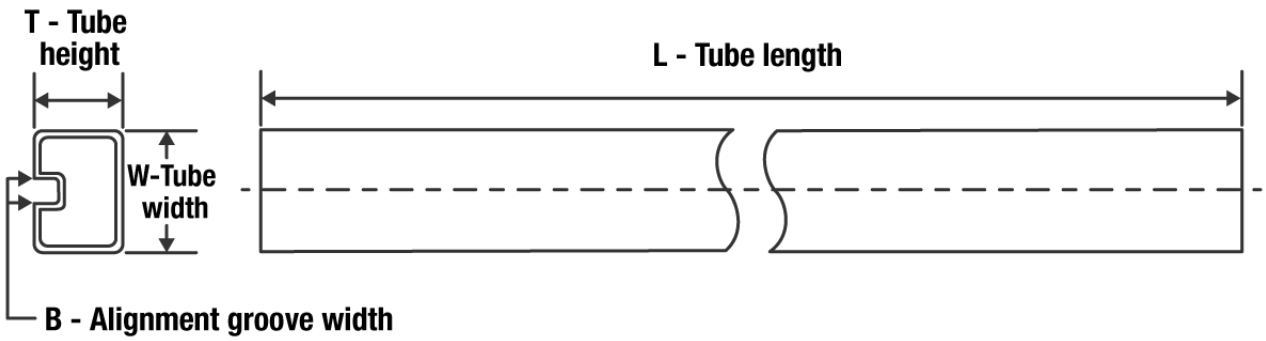
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV1701AIDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV1701AIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV1701AIDCKR | SC70 | DCK | 5 | 3000 | 190.0 | 190.0 | 30.0 |
| TLV1701AIDCKT | SC70 | DCK | 5 | 250 | 190.0 | 190.0 | 30.0 |
| TLV1701AIDRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| TLV1701AIDRLT | SOT-5X3 | DRL | 5 | 250 | 202.0 | 201.0 | 28.0 |
| TLV1702AIDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV1702AIRUGR | X2QFN | RUG | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV1704AIPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |

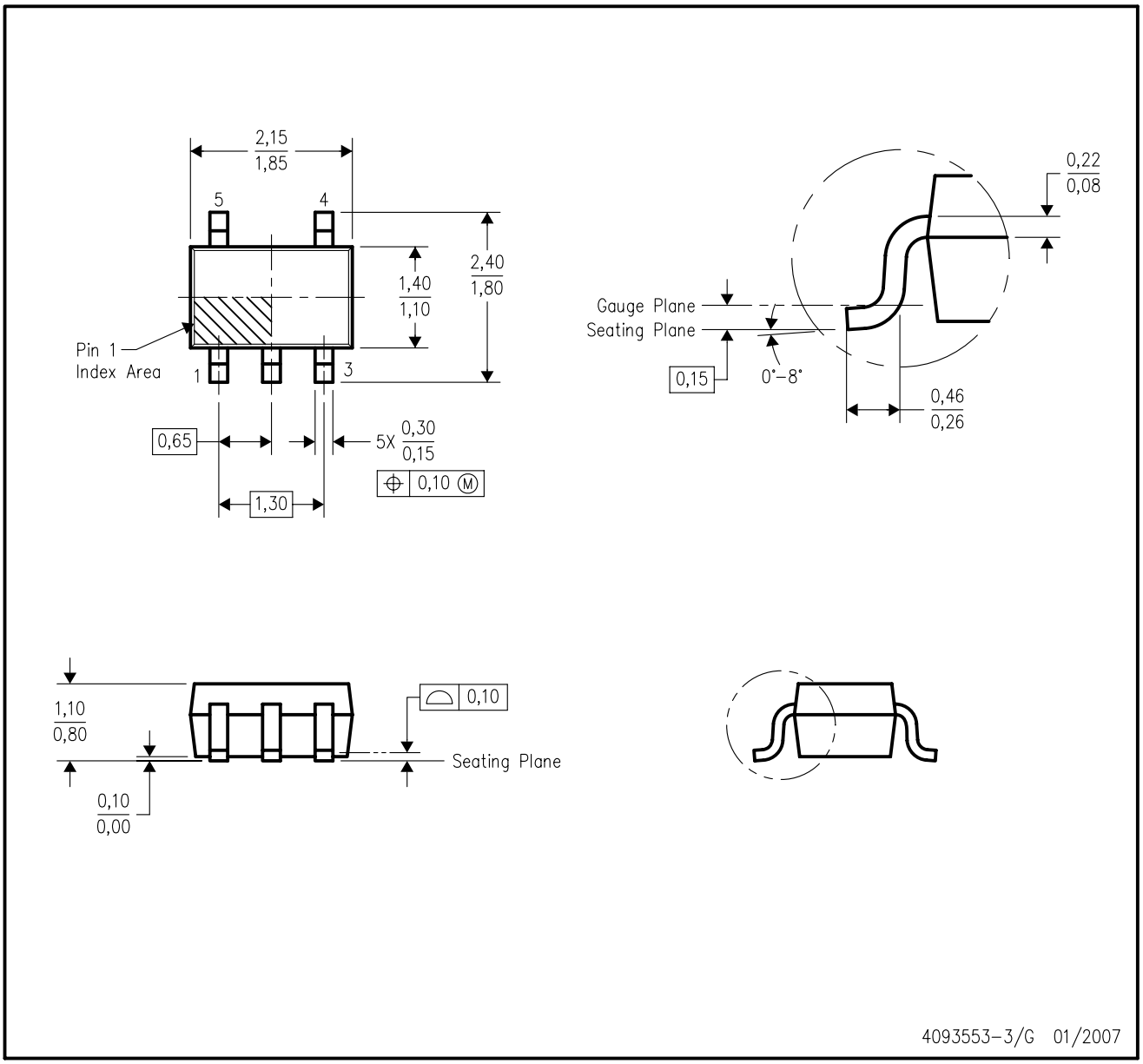
## TUBE




*All dimensions are nominal

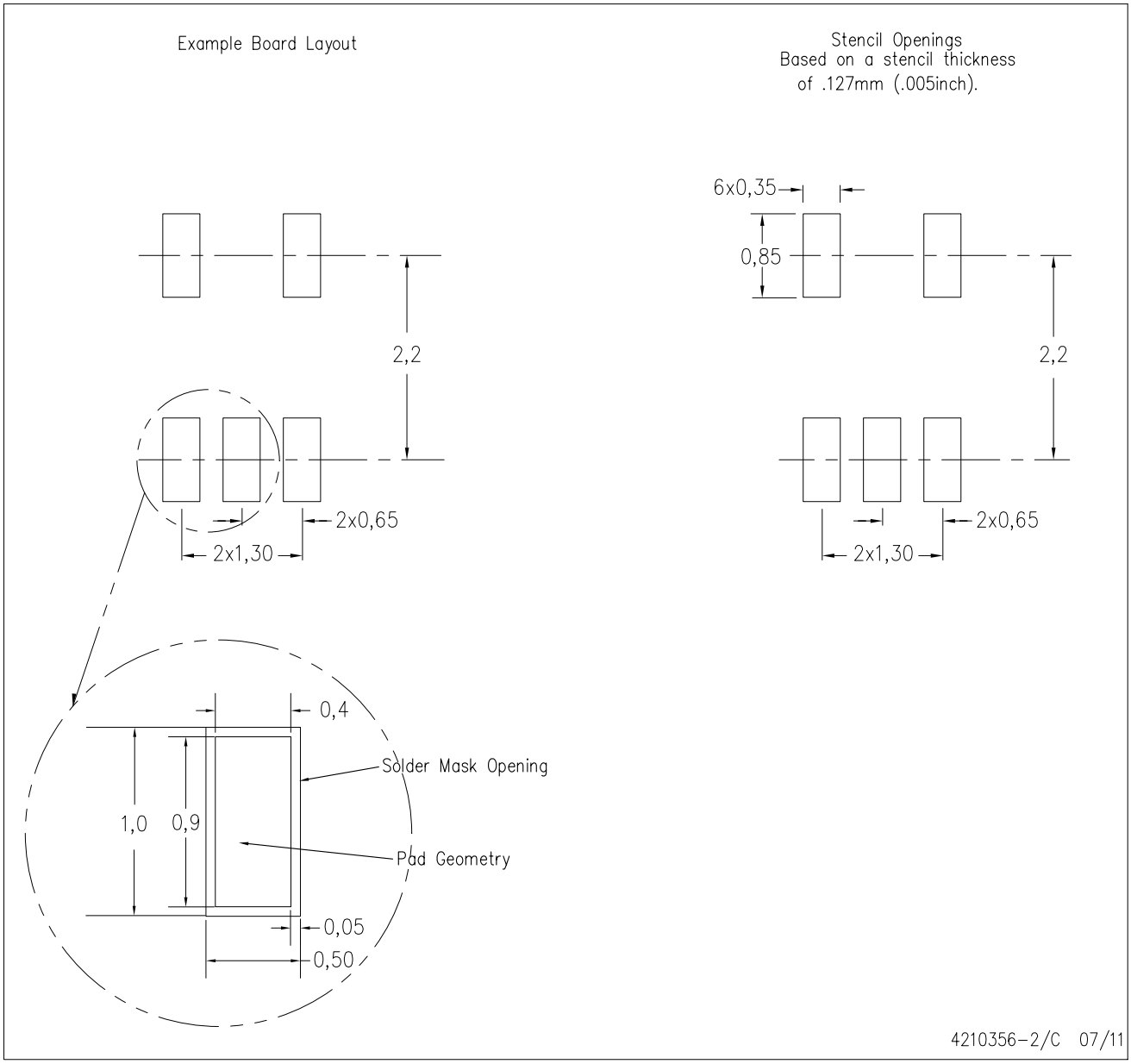
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TLV1702AIDGK | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TLV1704AIPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

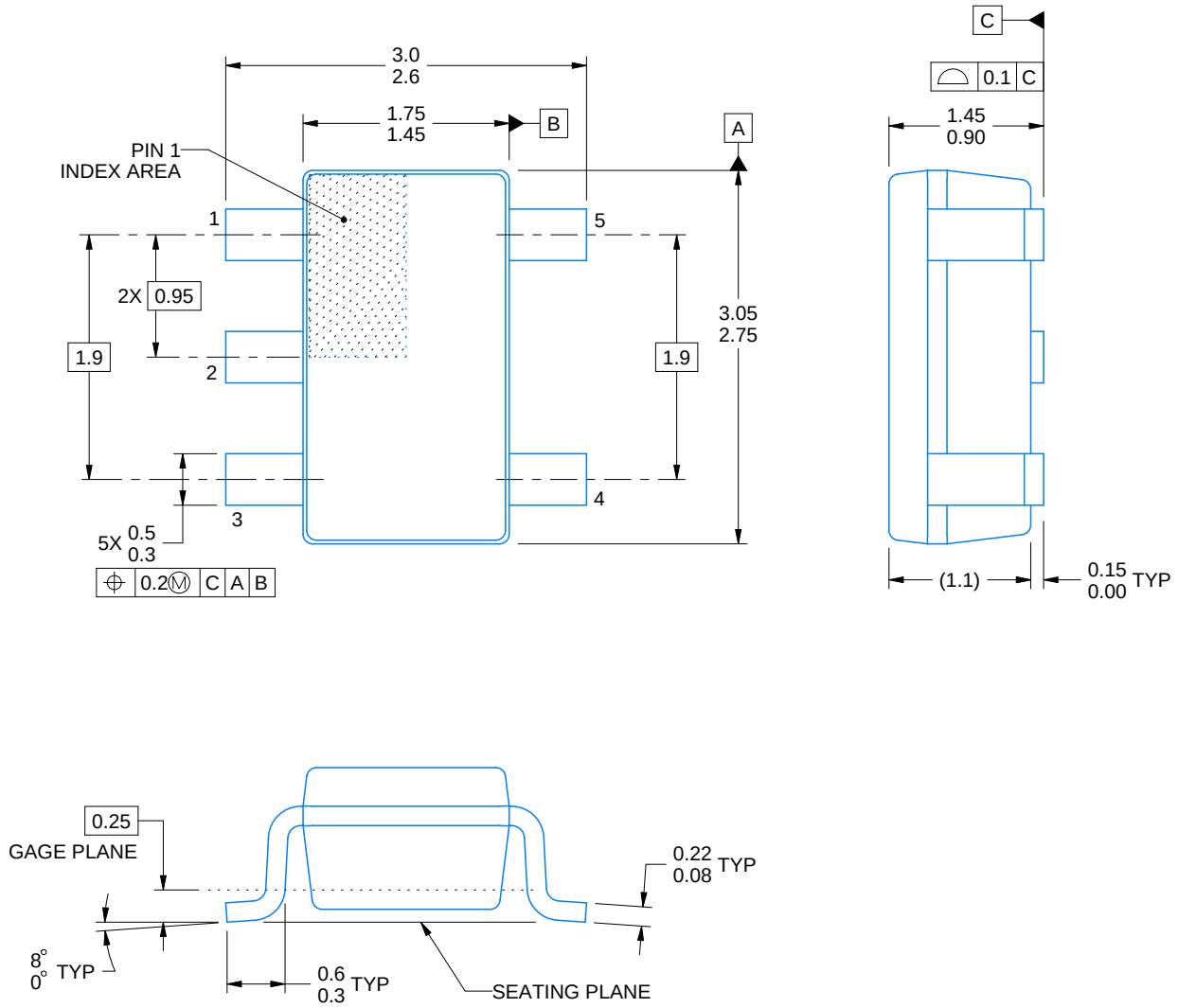



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE



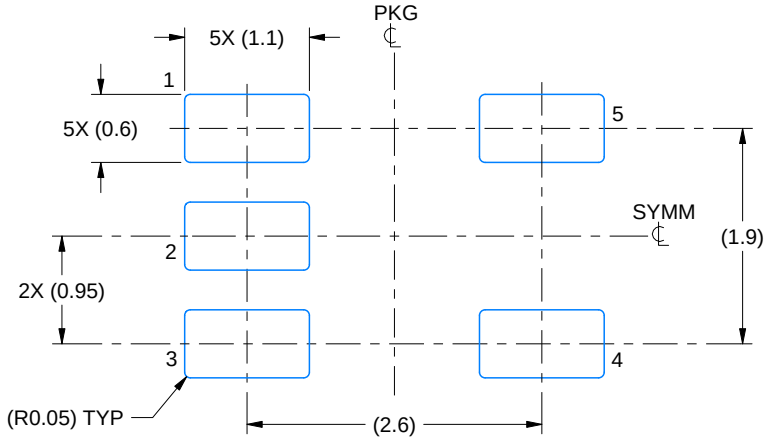

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



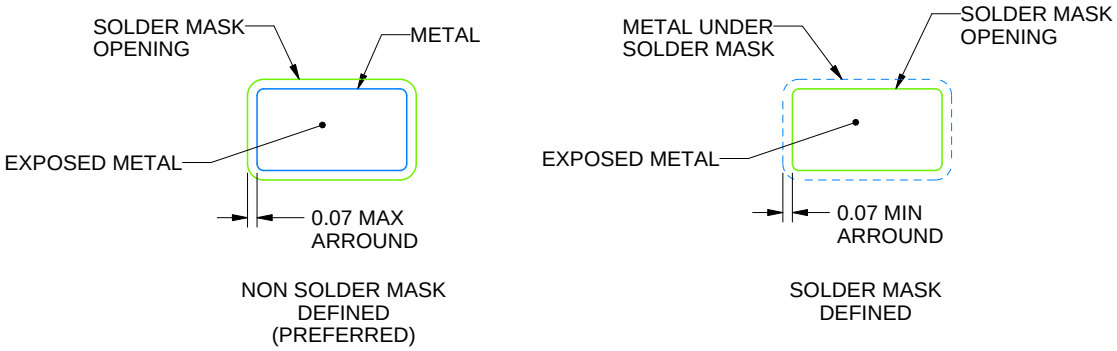

4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

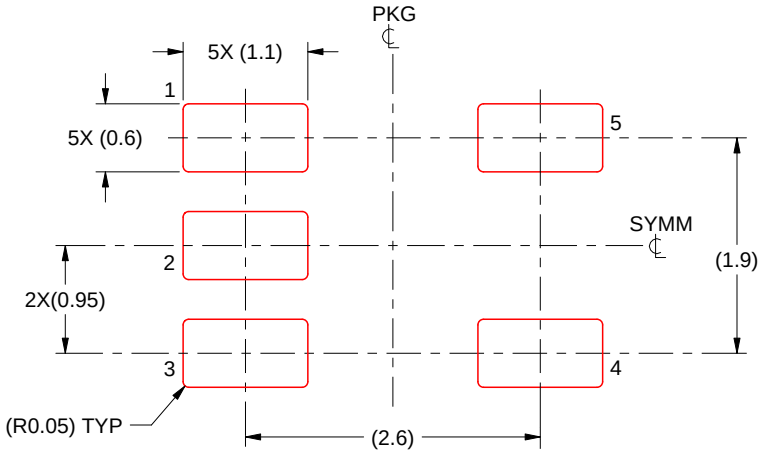



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



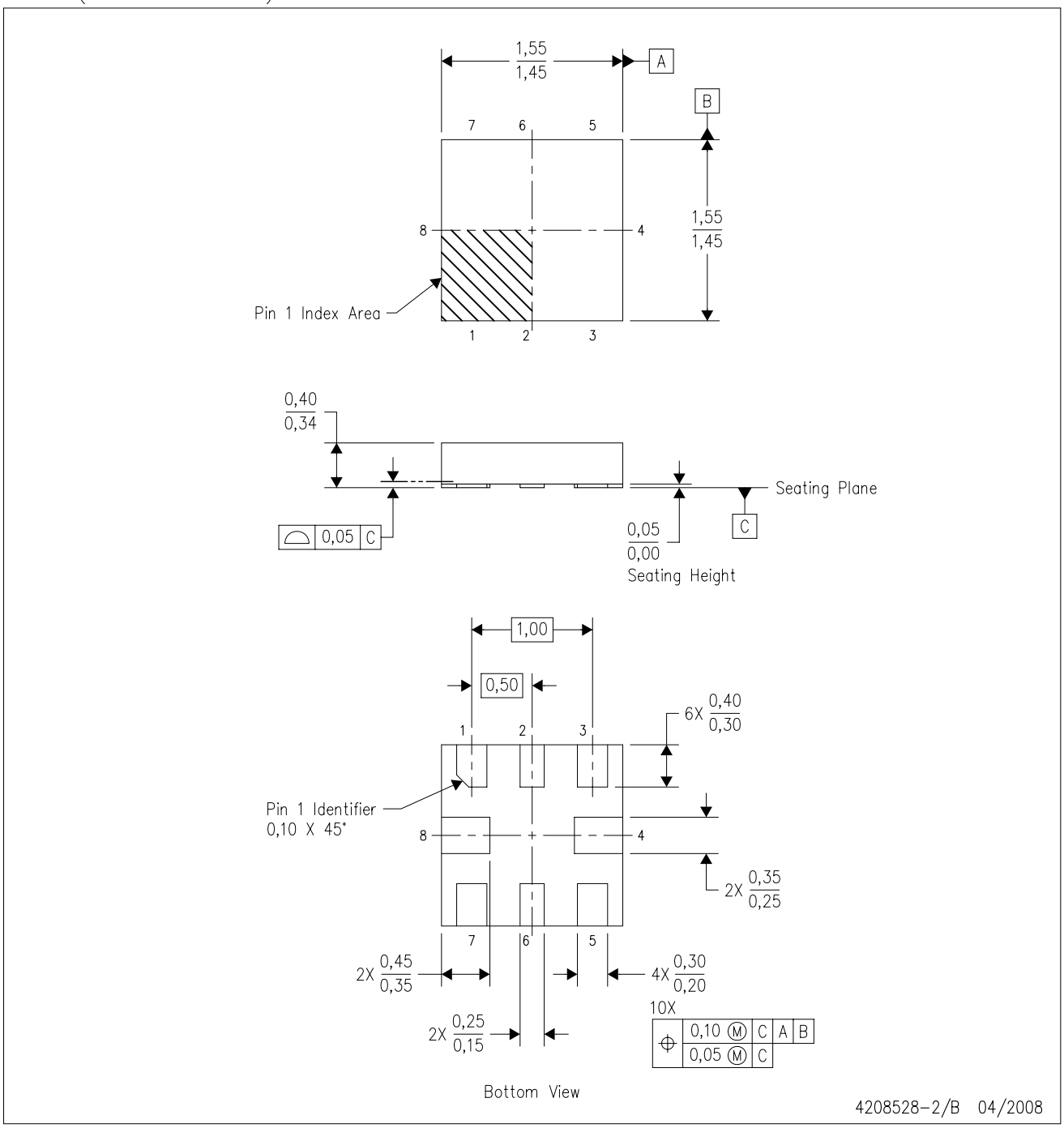

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

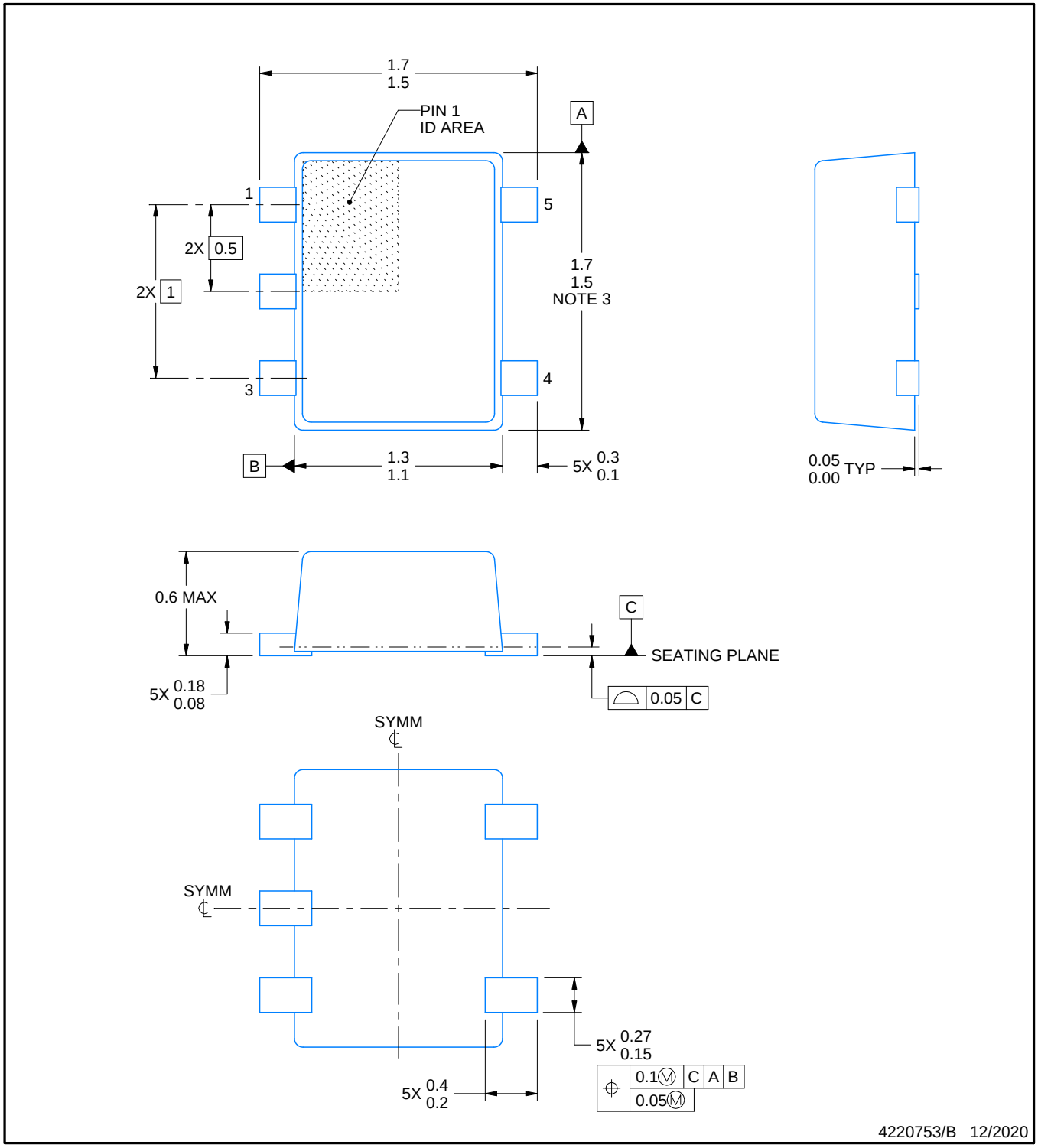
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

RUG (S–PQFP–N8) PLASTIC QUAD FLATPACK

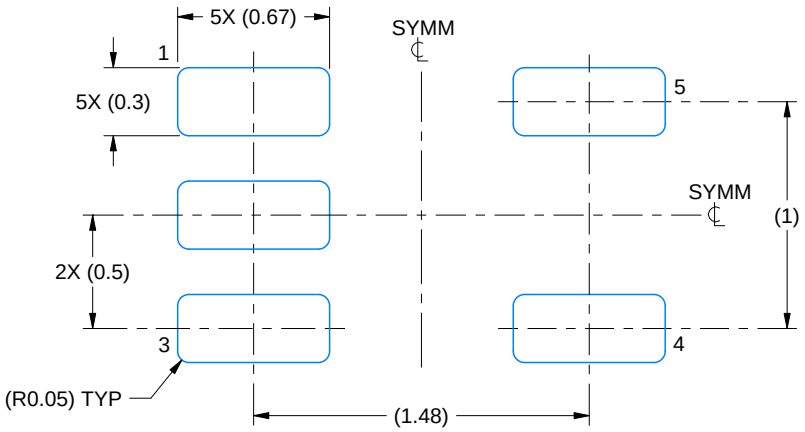



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2ECD.

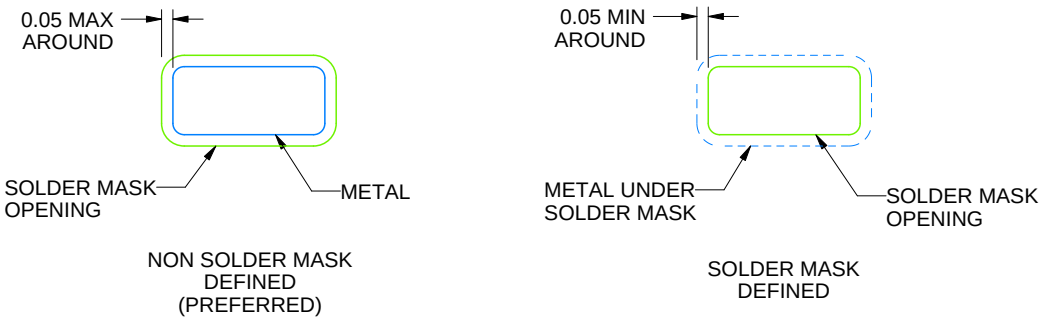



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1




LAND PATTERN EXAMPLE
SCALE:30X

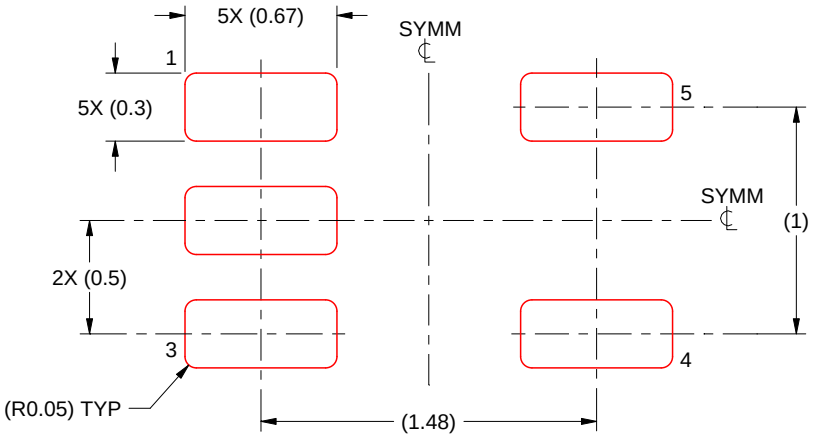



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



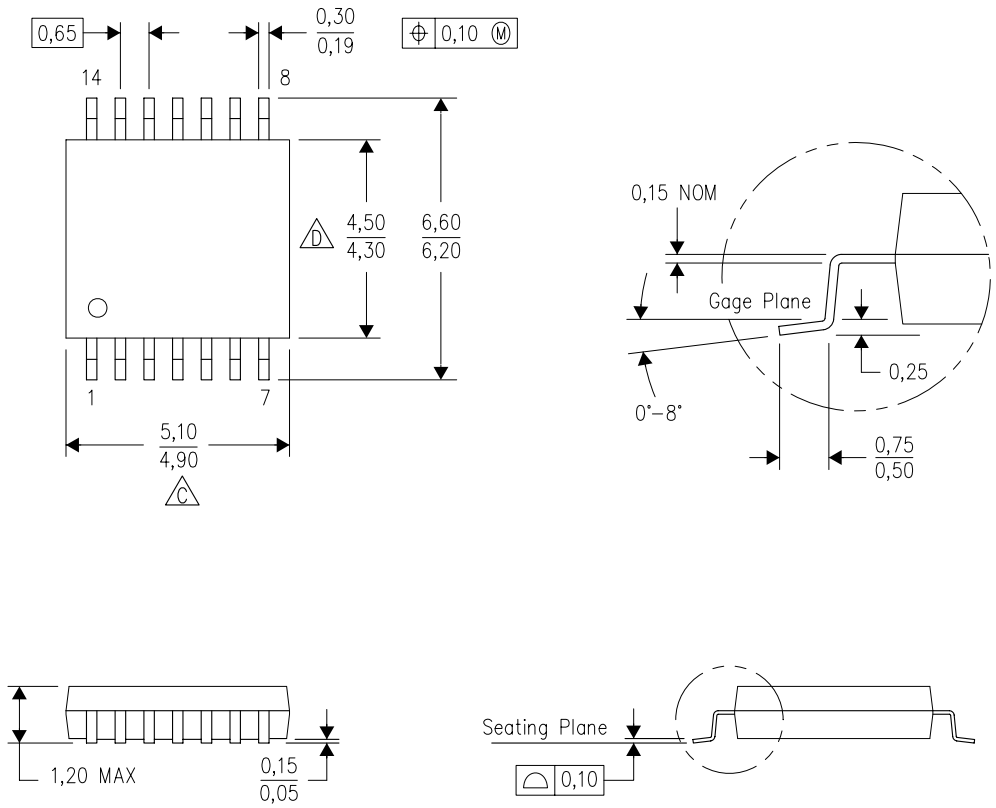

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

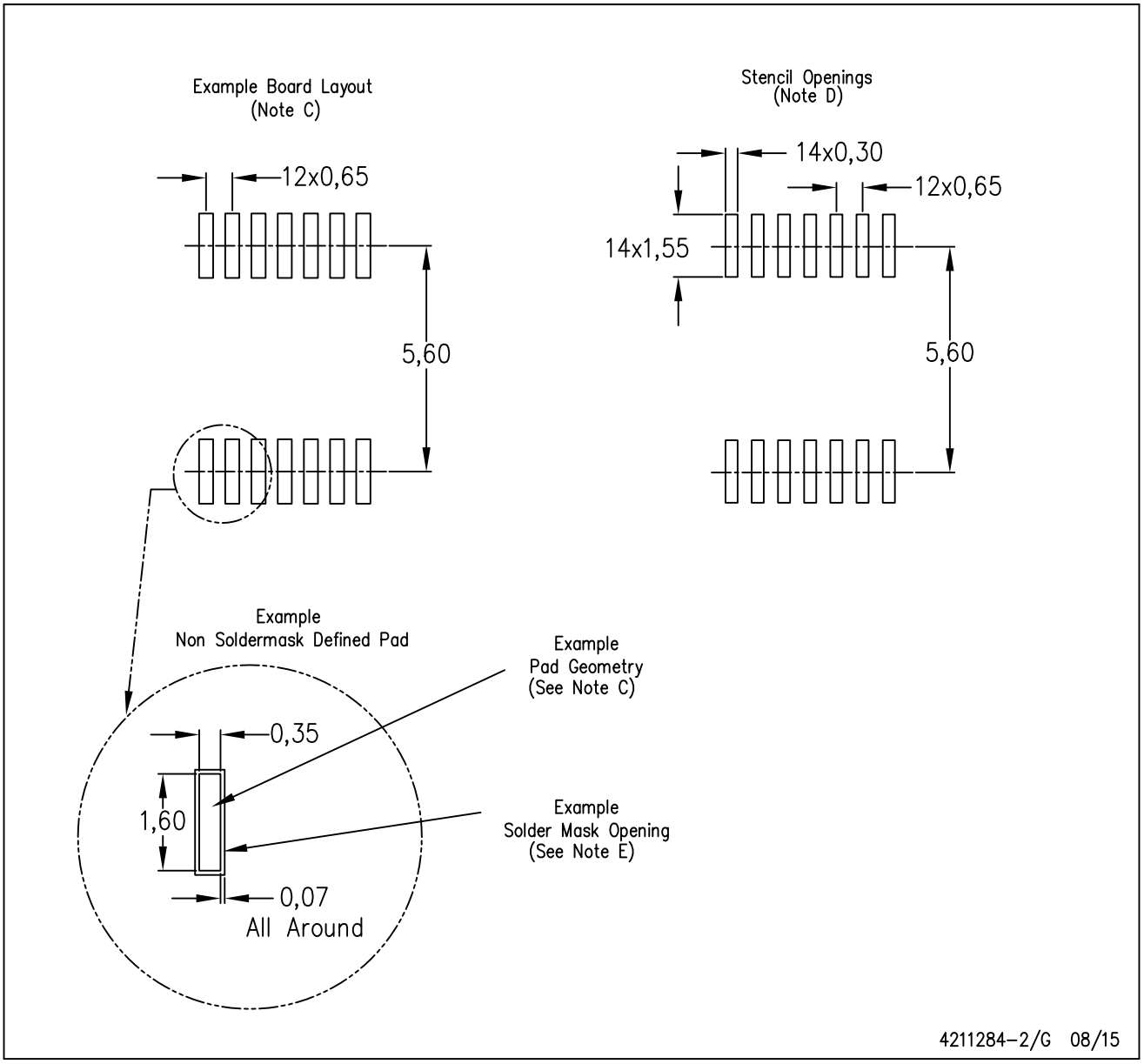
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



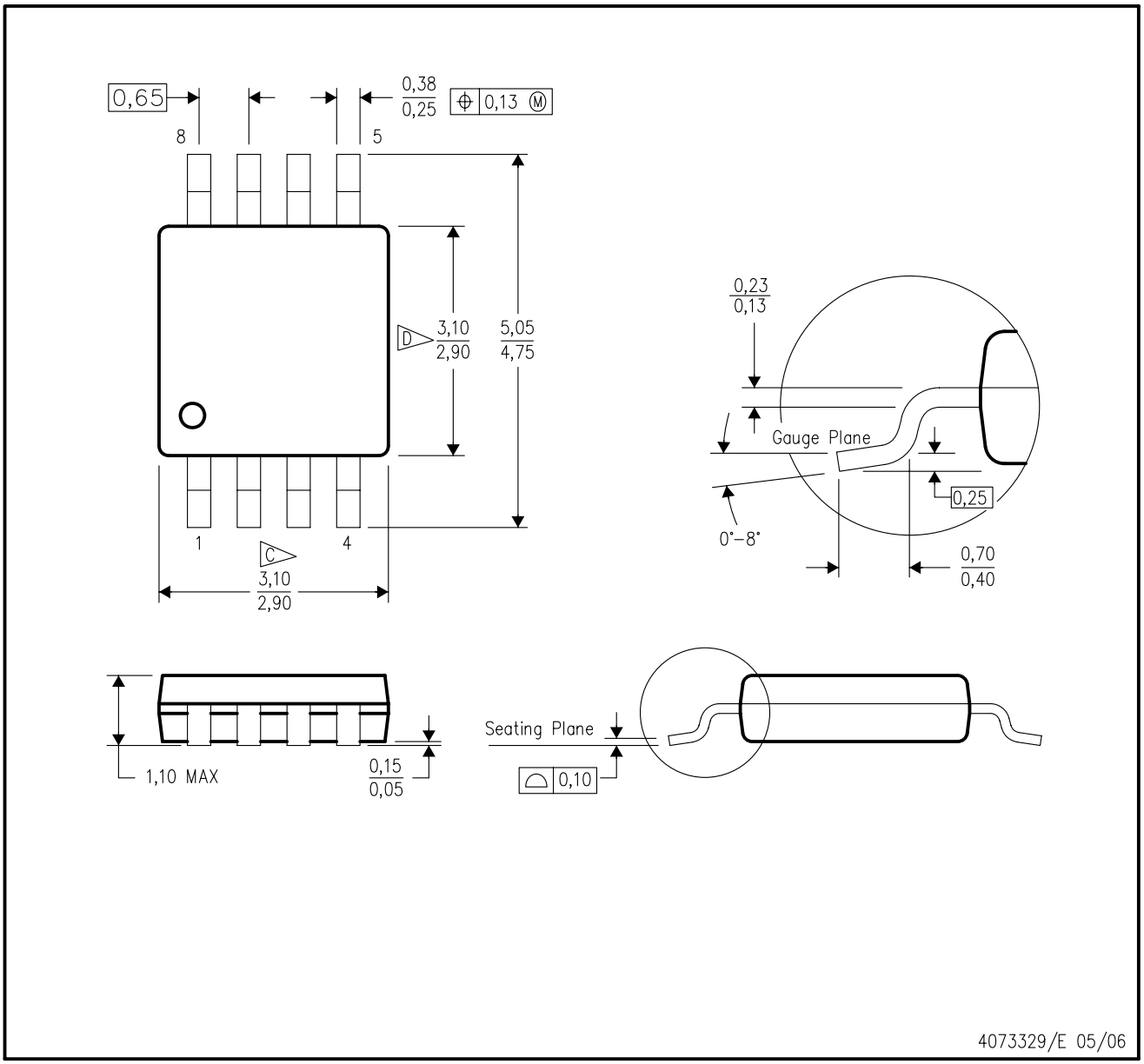

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



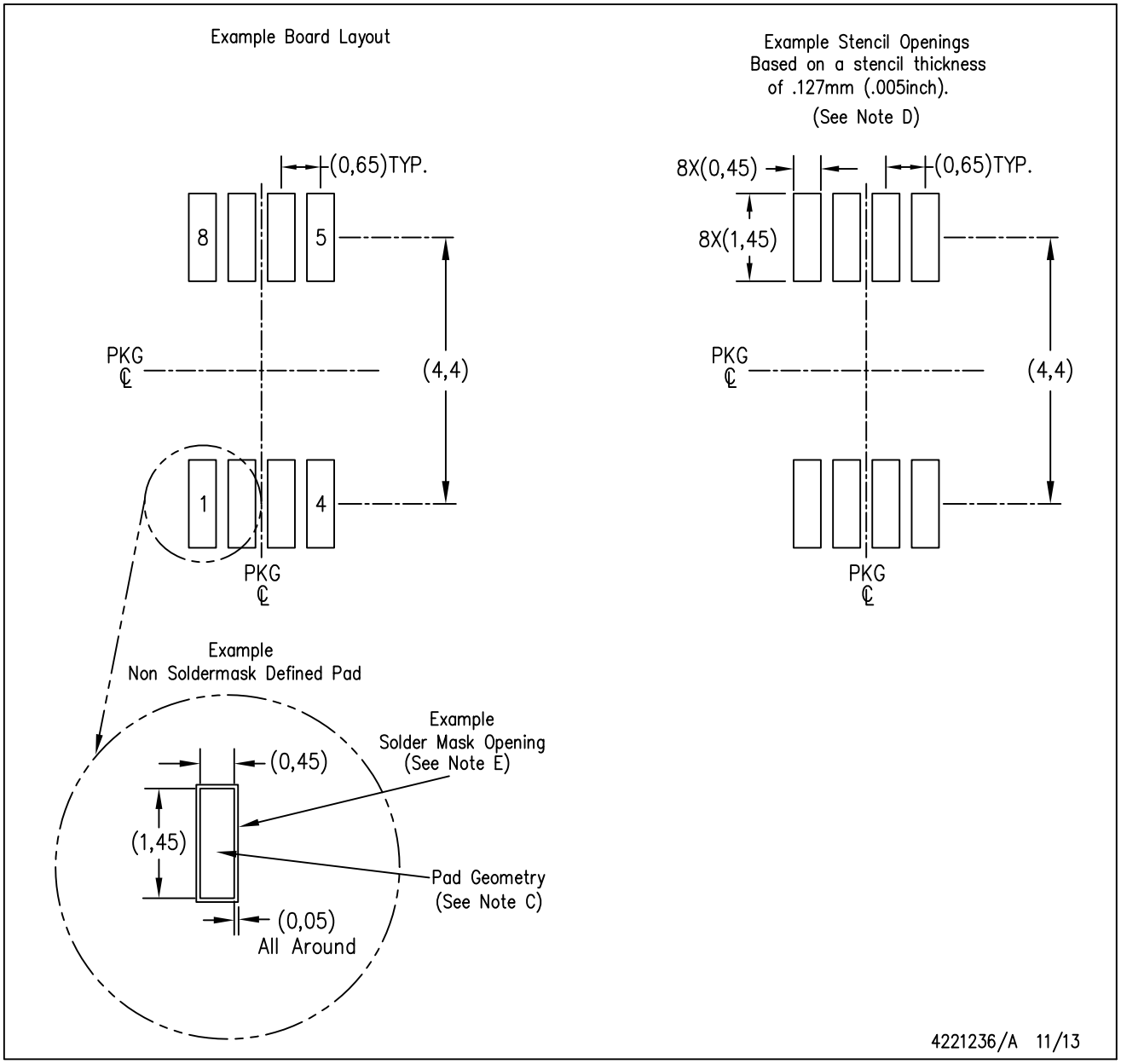

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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