



## DESCRIPTION (CONTINUED)

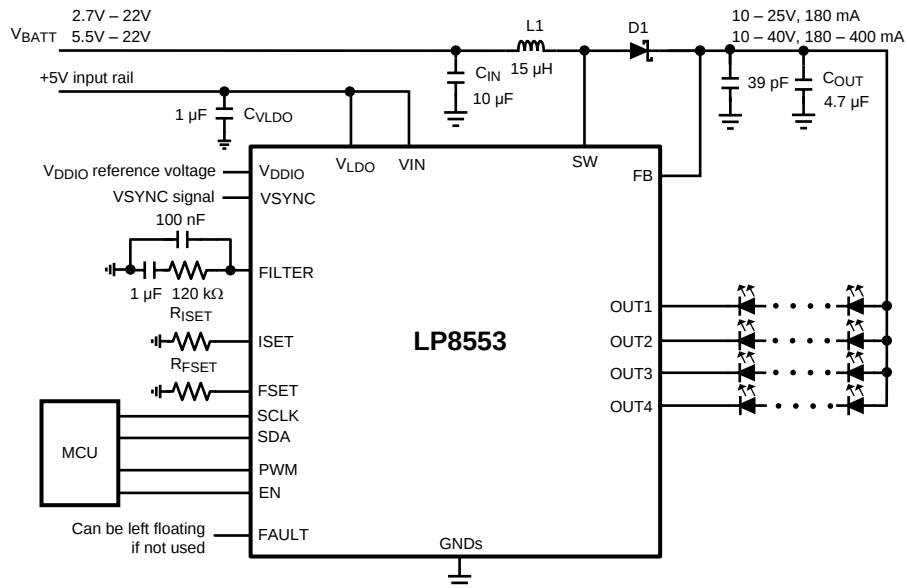
Automatic PWM dimming at lower brightness values and current dimming at higher brightness values can be used to improve the optical efficiency.

Internal EEPROM is used for storing the configuration data. This makes it possible to have minimum external component count and make the solution very small.

LP8553 has safety features which make it possible to detect LED outputs with open or short fault. Low input voltage and boost over-current conditions are also monitored, and the chip is turned off when these events occur. Thermal de-rating function prevents overheating of the device by reducing backlight brightness when set temperature has been reached.

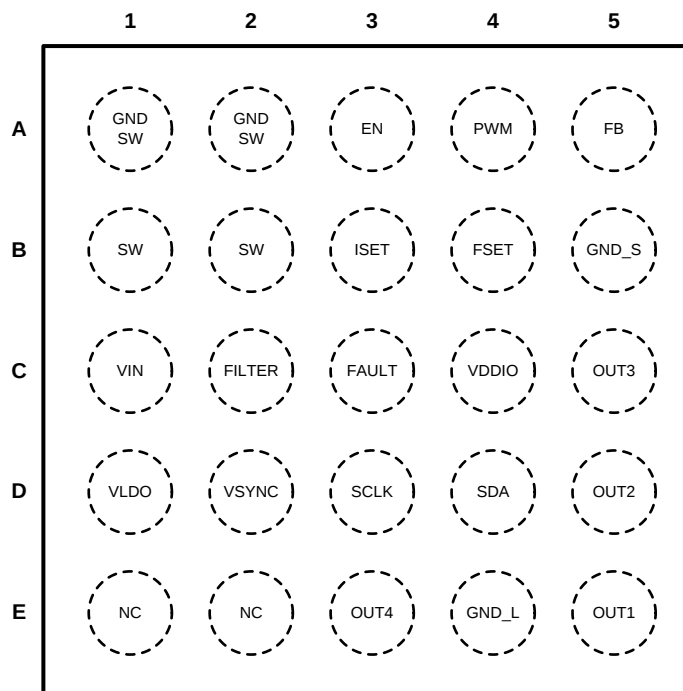
LP8553 is available in TI's DSBGA 25-bump package.

## Typical Application for Low Input Voltage (2)

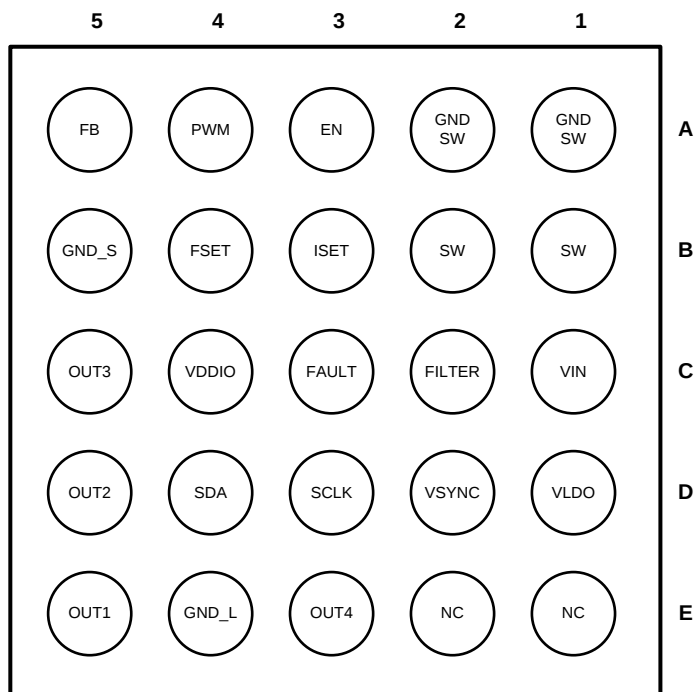


**Note:** Separate 5V rail to V<sub>LDO</sub> can be also used to improve efficiency for applications with higher battery voltage. No power sequencing requirements between V<sub>IN</sub>/V<sub>LDO</sub> and V<sub>BATT</sub>.

## Connection Diagrams



**Figure 1. Package Number YZR002511A  
Top View**



**Figure 2. Package Number YZR002511A  
Bottom View**

**PIN DESCRIPTIONS<sup>(1)</sup>**

| Pin # | Name   | Type | Description                                                                                                                                                                         |
|-------|--------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1    | GND_SW | G    | Boost switch ground                                                                                                                                                                 |
| A2    | GND_SW | G    | Boost switch ground                                                                                                                                                                 |
| A3    | EN     | I    | Enable input pin                                                                                                                                                                    |
| A4    | PWM    | A    | PWM dimming input. This pin must be connected to GND if not used.                                                                                                                   |
| A5    | FB     | A    | Boost feedback input                                                                                                                                                                |
| B1    | SW     | A    | Boost switch                                                                                                                                                                        |
| B2    | SW     | A    | Boost switch                                                                                                                                                                        |
| B3    | ISET   | A    | Set resistor for LED current. This pin can be left floating if not used.                                                                                                            |
| B4    | FSET   | A    | PWM frequency set resistor. This pin can be left floating if not used.                                                                                                              |
| B5    | GND_S  | G    | Signal ground                                                                                                                                                                       |
| C1    | VIN    | P    | Input power supply up to 22V. If $2.7V \leq V_{BATT} < 5.5V$ ( <a href="#">Typical Application for Low Input Voltage (2)</a> ) then external 5V rail must be used for VLDO and VIN. |
| C2    | FILTER | A    | Low pass filter for PLL. This pin can be left floating if not used.                                                                                                                 |
| C3    | FAULT  | OD   | Fault indication output. If not used, can be left floating.                                                                                                                         |
| C4    | VDDIO  | P    | Digital IO reference voltage (1.65V...5V) for I <sup>2</sup> C interface and PWM input.                                                                                             |
| C5    | OUT3   | A    | Current sink output                                                                                                                                                                 |
| D1    | VLDO   | P    | LDO output voltage. External 5V rail can be connected to this pin in low voltage application.                                                                                       |
| D2    | VSYNC  | I    | V <sub>SYNC</sub> input. This pin must be connected to GND if not used.                                                                                                             |
| D3    | SCLK   | I    | Serial clock. This pin must be connected to GND if not used.                                                                                                                        |
| D4    | SDA    | I/O  | Serial data. This pin must be connected to GND if not used.                                                                                                                         |
| D5    | OUT2   | A    | Current sink output                                                                                                                                                                 |
| E1    | NC     | -    | Not connected                                                                                                                                                                       |
| E2    | NC     | -    | Not connected                                                                                                                                                                       |
| E3    | OUT4   | A    | Current sink output                                                                                                                                                                 |
| E4    | GND_L  | G    | LED ground                                                                                                                                                                          |
| E5    | OUT1   | A    | Current sink output                                                                                                                                                                 |

(1) **A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O: Input/Output Pin, O: Output Pin, OD: Open Drain Pin**



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## Absolute Maximum Ratings <sup>(1)(2)(3)</sup>

|                                                    |                       |
|----------------------------------------------------|-----------------------|
| V <sub>IN</sub>                                    | –0.3V to +24.0V       |
| V <sub>LDO</sub>                                   | –0.3V to +6.0V        |
| Voltage on Logic Pins (VSYNC, PWM, EN, SCLK, SDA)  | –0.3V to +6.0V        |
| Voltage on Logic Pin (FAULT)                       | –0.3V to VDDIO + 0.3V |
| Voltage on Analog Pins (FILTER, VDDIO, ISET, FSET) | –0.3V to +6.0V        |
| V (OUT1...OUT4, SW, FB)                            | –0.3V to +44.0V       |
| Continuous Power Dissipation <sup>(4)</sup>        | Internally Limited    |
| Junction Temperature (T <sub>J-MAX</sub> )         | 125°C                 |
| Storage Temperature Range                          | –65°C to +150°C       |
| Maximum Lead Temperature (Soldering)               | <sup>(5)</sup>        |
| ESD Rating                                         | <sup>(6)</sup>        |
| Human Body Model:                                  | 2 kV                  |
| Machine Model:                                     | 200V                  |
| Charged Device Model:                              | 1 kV                  |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) All voltages are with respect to the potential at the GND pins.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T<sub>J</sub> = 150°C (typ.) and disengages at T<sub>J</sub> = 130°C (typ.).
- (5) For detailed soldering specifications and information, please refer to Texas Instrument AN1112: *DSBGA Wafer Level Chip Scale Package*.
- (6) Human Body Model, applicable standard JESD22-A114C. Machine Model, applicable standard JESD22- A115-A. Charged Device Model, applicable standard JESD22A-C101.

## Operating Ratings <sup>(1)(2)</sup>

|                                                                         |                 |
|-------------------------------------------------------------------------|-----------------|
| Input Voltage Range (V <sub>IN</sub> )<br>typ. app. (1)                 | 5.5V to 22V     |
| Input Voltage Range (V <sub>IN</sub> + V <sub>LDO</sub> ) typ. app. (2) | 4.5V to 5.5V    |
| V <sub>DDIO</sub>                                                       | 1.65V to 5V     |
| V(OUT1...OUT4, SW, FB)                                                  | 0V to 40V       |
| Junction Temperature (T <sub>J</sub> ) Range                            | –30°C to +125°C |
| Ambient Temperature (T <sub>A</sub> ) Range <sup>(3)</sup>              | –30°C to +85°C  |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pins.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T<sub>A-MAX</sub>) is dependent on the maximum operating junction temperature (T<sub>J-MAX-OP</sub> = 125°C), the maximum power dissipation of the device in the application (P<sub>D-MAX</sub>), and the junction-to ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A-MAX</sub> = T<sub>J-MAX-OP</sub> – (θ<sub>JA</sub> × P<sub>D-MAX</sub>).

## Thermal Properties

|                                                                                       |              |
|---------------------------------------------------------------------------------------|--------------|
| Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ), YZR Package <sup>(1)</sup> | 40 to 73°C/W |
|---------------------------------------------------------------------------------------|--------------|

- (1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

## Electrical Characteristics <sup>(1)(2)</sup>

Limits in standard typeface are for  $T_A = 25^\circ\text{C}$ . Limits in **boldface** type apply over the full operating junction temperature range ( $-30^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ ). Unless otherwise specified:  $V_{IN} = 12.0\text{V}$ ,  $V_{DDIO} = 2.8\text{V}$ ,  $C_{VLDO} = 1\text{ }\mu\text{F}$ ,  $L1 = 15\text{ }\mu\text{H}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $R_{ISET} = 16\text{ k}\Omega$  <sup>(3)</sup>

| Symbol    | Parameter                              | Condition                                                                           | Min                    | Typ | Max                    | Units         |
|-----------|----------------------------------------|-------------------------------------------------------------------------------------|------------------------|-----|------------------------|---------------|
| $I_{IN}$  | Standby Supply Current                 | Internal LDO disabled<br>EN=L and PWM=L                                             |                        |     | <b>1</b>               | $\mu\text{A}$ |
|           | Normal Mode Supply Current             | LDO enabled, boost enabled, no current going through LED outputs<br>5 MHz PLL Clock |                        | 3.0 |                        | mA            |
|           |                                        | 10 MHz PLL Clock                                                                    |                        | 3.7 |                        |               |
|           |                                        | 20 MHz PLL Clock                                                                    |                        | 4.7 |                        |               |
|           |                                        | 40 MHz PLL Clock                                                                    |                        | 6.7 |                        |               |
| $f_{OSC}$ | Internal Oscillator Frequency Accuracy |                                                                                     | <b>-4</b><br><b>-7</b> |     | <b>+4</b><br><b>+7</b> | %             |
| $V_{LDO}$ | Internal LDO Voltage                   |                                                                                     | <b>4.5</b>             | 5.0 | <b>5.5</b>             | V             |
| $I_{LDO}$ | Internal LDO External Loading          |                                                                                     |                        |     | 5.0                    | mA            |

(1) All voltages are with respect to the potential at the GND pins.

(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

## Boost Converter Electrical Characteristics

| Symbol           | Parameter                       | Condition                                                                | Min | Typ                       | Max | Units    |
|------------------|---------------------------------|--------------------------------------------------------------------------|-----|---------------------------|-----|----------|
| $R_{DS_{ON}}$    | Switch ON Resistance            | $I_{SW} = 0.5\text{A}$                                                   |     | 0.12                      |     | $\Omega$ |
| $V_{MAX}$        | Boost Maximum Output Voltage    |                                                                          |     | 40                        |     | V        |
| $I_{LOAD}$       | Maximum Continuous Load Current | $9.0\text{V} \leq V_{BATT}, V_{OUT} = 35\text{V}$                        |     | 450                       |     | mA       |
|                  |                                 | $6.0\text{V} \leq V_{BATT}, V_{OUT} = 35\text{V}$                        |     | 300                       |     |          |
|                  |                                 | $3.0\text{V} \leq V_{BATT}, V_{OUT} = 25\text{V}$                        |     | 180                       |     |          |
| $V_{OUT}/V_{IN}$ | Conversion Ratio                | $f_{SW} = 1.25\text{ MHz}$                                               |     |                           | 10  |          |
| $f_{SW}$         | Switching Frequency             | BOOST_FREQ = 00<br>BOOST_FREQ = 01<br>BOOST_FREQ = 10<br>BOOST_FREQ = 11 |     | 156<br>312<br>625<br>1250 |     | kHz      |
| $V_{OV}$         | Over-voltage Protection Voltage |                                                                          |     | $V_{BOOST} + 1.6\text{V}$ |     | V        |
| $t_{PULSE}$      | Switch Pulse Minimum Width      | no load                                                                  |     | 50                        |     | ns       |
| $t_{STARTUP}$    | Startup Time                    | <sup>(1)</sup>                                                           |     | 6                         |     | ms       |
| $I_{MAX}$        | SW Pin Current Limit            | BOOST_IMAX = 0<br>BOOST_IMAX = 1                                         |     | 1.4<br>2.5                |     | A        |

(1) Startup time is measured from the moment boost is activated until the  $V_{OUT}$  crosses 90% of its target value.

## LED Driver Electrical Characteristics

| Symbol        | Parameter                                 | Condition                                   | Min                    | Typ | Max                    | Units         |
|---------------|-------------------------------------------|---------------------------------------------|------------------------|-----|------------------------|---------------|
| $I_{LEAKAGE}$ | Leakage Current                           | Outputs OUT1...OUT4, $V_{OUT} = 40\text{V}$ |                        | 0.1 | 1                      | $\mu\text{A}$ |
| $I_{MAX}$     | Maximum Source Current<br>OUT1...OUT4     | EN_I_RES = 0, CURRENT[7:0] = FFh            |                        | 30  |                        | mA            |
|               |                                           | EN_I_RES = 1, CURRENT[7:0] = FFh            |                        | 50  |                        |               |
| $I_{OUT}$     | Output Current Accuracy<br><sup>(1)</sup> | Output current set to 23 mA, EN_I_RES = 1   | <b>-3</b><br><b>-4</b> |     | <b>+3</b><br><b>+4</b> | %             |
| $I_{MATCH}$   | Matching <sup>(1)</sup>                   | Output current set to 23 mA, EN_I_RES = 1   |                        | 0.5 |                        | %             |

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1 to OUT4), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated:  $(MAX - AVG)/AVG$  and  $(AVG - MIN)/AVG$ . The largest number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts. Note that some manufacturers have different definitions in use.

## LED Driver Electrical Characteristics (continued)

| Symbol             | Parameter                              | Condition                                            | Min | Typ   | Max        | Units |
|--------------------|----------------------------------------|------------------------------------------------------|-----|-------|------------|-------|
| PWM <sub>RES</sub> | PWM Output Resolution <sup>(2)</sup>   | f <sub>LED</sub> = 5 kHz, f <sub>PLL</sub> = 5 MHz   |     | 10    |            | bits  |
|                    |                                        | f <sub>LED</sub> = 10 kHz, f <sub>PLL</sub> = 5 MHz  |     | 9     |            |       |
|                    |                                        | f <sub>LED</sub> = 20 kHz, f <sub>PLL</sub> = 5 MHz  |     | 8     |            |       |
|                    |                                        | f <sub>LED</sub> = 5 kHz, f <sub>PLL</sub> = 40 MHz  |     | 13    |            |       |
|                    |                                        | f <sub>LED</sub> = 10 kHz, f <sub>PLL</sub> = 40 MHz |     | 12    |            |       |
|                    |                                        | f <sub>LED</sub> = 20 kHz, f <sub>PLL</sub> = 40 MHz |     | 11    |            |       |
| f <sub>LED</sub>   | LED Switching Frequency <sup>(2)</sup> | PWM_FREQ[4:0] = 00000b<br>PLL clock 5 MHz            |     | 600   |            | Hz    |
|                    |                                        | PWM_FREQ[4:0] = 11111b<br>PLL clock 5 MHz            |     | 19.2k |            |       |
| V <sub>SAT</sub>   | Saturation Voltage <sup>(3)</sup>      | Output current set to 20 mA                          |     | 105   | <b>220</b> | mV    |
|                    |                                        | Output current set to 30 mA                          |     | 160   | <b>290</b> |       |

(2) PWM output resolution and frequency depend on the PLL settings. Please see [PWM Frequency Setting](#) for full description

(3) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1V.

## PWM Interface Characteristics

| Symbol               | Parameter                                  | Condition                                       | Min | Typ | Max | Units |
|----------------------|--------------------------------------------|-------------------------------------------------|-----|-----|-----|-------|
| f <sub>PWM</sub>     | PWM Frequency Range                        |                                                 | 0.1 |     | 25  | kHz   |
| t <sub>MIN_ON</sub>  | Minimum Pulse ON time                      |                                                 |     | 1   |     | μs    |
| t <sub>MIN_OFF</sub> | Minimum Pulse OFF time                     |                                                 |     | 1   |     |       |
| t <sub>STARTUP</sub> | Turn on delay from standby to backlight on | PWM input active, EN pin rise from low to high  |     | 6   |     | ms    |
| T <sub>STBY</sub>    | Turn Off Delay                             | PWM input low time for turn off, slope disabled |     | 50  |     | ms    |
| PWM <sub>RES</sub>   | PWM Input Resolution                       | f <sub>IN</sub> < 9.0 kHz                       |     | 10  |     | bits  |
|                      |                                            | f <sub>IN</sub> < 4.5 kHz                       |     | 11  |     |       |
|                      |                                            | f <sub>IN</sub> < 2.2 kHz                       |     | 12  |     |       |
|                      |                                            | f <sub>IN</sub> < 1.1 kHz                       |     | 13  |     |       |

## Under-Voltage Protection

| Symbol            | Parameter                              | Condition               | Min  | Typ      | Max  | Units |
|-------------------|----------------------------------------|-------------------------|------|----------|------|-------|
| V <sub>UVLO</sub> | V <sub>IN</sub> UVLO Threshold Voltage | UVLO[1:0] = 00          |      | Disabled |      | V     |
|                   |                                        | UVLO[1:0] = 01, falling | 2.55 | 2.70     | 2.94 |       |
|                   |                                        | UVLO[1:0] = 01, rising  | 2.62 | 2.76     | 3.00 |       |
|                   |                                        | UVLO[1:0] = 10, falling | 5.11 | 5.40     | 5.68 |       |
|                   |                                        | UVLO[1:0] = 10, rising  | 5.38 | 5.70     | 5.98 |       |
|                   |                                        | UVLO[1:0] = 11, falling | 7.75 | 8.10     | 8.45 |       |
|                   |                                        | UVLO[1:0] = 11, rising  | 8.36 | 8.73     | 9.20 |       |

## Logic Interface Characteristics

| Symbol                   | Parameter        | Condition | Min         | Typ | Max        | Units |
|--------------------------|------------------|-----------|-------------|-----|------------|-------|
| <b>Logic Input EN</b>    |                  |           |             |     |            |       |
| V <sub>IL</sub>          | Input Low Level  |           |             |     | <b>0.4</b> | V     |
| V <sub>IH</sub>          | Input High Level |           | <b>1.2</b>  |     |            | V     |
| I <sub>I</sub>           | Input Current    |           | <b>-1.0</b> |     | <b>1.0</b> | μA    |
| <b>Logic Input VSYNC</b> |                  |           |             |     |            |       |
| V <sub>IL</sub>          | Input Low Level  |           |             |     | <b>0.4</b> | V     |
| V <sub>IH</sub>          | Input High Level |           | <b>2.2</b>  |     |            | V     |
| I <sub>I</sub>           | Input Current    |           | <b>-1.0</b> |     | <b>1.0</b> | μA    |
| f <sub>VSYNC</sub>       | Frequency Range  |           | 58          | 60  | 55000      | Hz    |

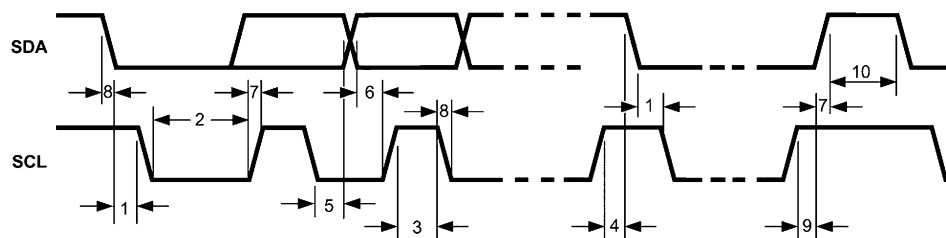
**Logic Interface Characteristics (continued)**

| Symbol                          | Parameter              | Condition                                  | Min                   | Typ | Max                   | Units   |
|---------------------------------|------------------------|--------------------------------------------|-----------------------|-----|-----------------------|---------|
| <b>Logic Input PWM</b>          |                        |                                            |                       |     |                       |         |
| $V_{IL}$                        | Input Low Level        |                                            |                       |     | $0.2 \times V_{DDIO}$ | V       |
| $V_{IH}$                        | Input High Level       |                                            | $0.8 \times V_{DDIO}$ |     |                       | V       |
| $I_I$                           | Input Current          |                                            | -1.0                  |     | 1.0                   | $\mu A$ |
| <b>Logic Inputs SCL, SDA</b>    |                        |                                            |                       |     |                       |         |
| $V_{IL}$                        | Input Low Level        |                                            |                       |     | $0.2 \times V_{DDIO}$ | V       |
| $V_{IH}$                        | Input High Level       |                                            | $0.8 \times V_{DDIO}$ |     |                       | V       |
| $I_I$                           | Input Current          |                                            | -1.0                  |     | 1.0                   | $\mu A$ |
| <b>Logic Outputs SDA, FAULT</b> |                        |                                            |                       |     |                       |         |
| $V_{OL}$                        | Output Low Level       | $I_{OUT} = 3 \text{ mA}$ (pull-up current) |                       | 0.3 | 0.5                   | V       |
| $I_L$                           | Output Leakage Current | $V_{OUT} = 2.8 \text{ V}$                  | -1.0                  |     | 1.0                   | $\mu A$ |

**I<sup>2</sup>C Serial Bus Timing Parameters (SDA, SCLK) <sup>(1)</sup>**

| Symbol     | Parameter                                                                        | Limit          |     | Units   |
|------------|----------------------------------------------------------------------------------|----------------|-----|---------|
|            |                                                                                  | Min            | Max |         |
| $f_{SCLK}$ | Clock Frequency                                                                  |                | 400 | kHz     |
| 1          | Hold Time (repeated) START Condition                                             | 0.6            |     | $\mu s$ |
| 2          | Clock Low Time                                                                   | 1.3            |     | $\mu s$ |
| 3          | Clock High Time                                                                  | 600            |     | ns      |
| 4          | Setup Time for a Repeated START Condition                                        | 600            |     | ns      |
| 5          | Data Hold Time                                                                   | 50             |     | ns      |
| 6          | Data Setup Time                                                                  | 100            |     | ns      |
| 7          | Rise Time of SDA and SCL                                                         | $20 + 0.1 C_b$ | 300 | ns      |
| 8          | Fall Time of SDA and SCL                                                         | $15 + 0.1 C_b$ | 300 | ns      |
| 9          | Set-up Time for STOP condition                                                   | 600            |     | ns      |
| 10         | Bus Free Time between a STOP and a START Condition                               | 1.3            |     | $\mu s$ |
| $C_b$      | Capacitive Load Parameter for Each Bus Line<br>Load of 1 pF corresponds to 1 ns. | 10             | 200 | ns      |

(1) Ensured by design.  $V_{DDIO} = 1.65 \text{ V}$  to  $5.5 \text{ V}$ .



## Typical Performance Characteristics

Unless otherwise specified:  $V_{BATT} = 12.0V$ ,  $C_{VLD0} = 1 \mu F$ ,  $L1 = 33 \mu H$ ,  $C_{IN} = 10 \mu F$ ,  $C_{OUT} = 10 \mu F$

LED Drive Efficiency,  $f_{LED} = 9.6 \text{ kHz}$

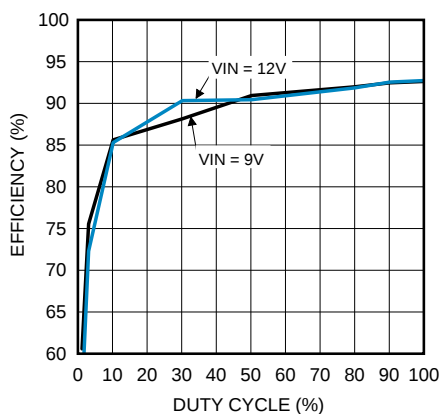


Figure 3.

LED Drive Efficiency,  $f_{LED} = 9.6 \text{ kHz}$ ,  $L1 = 15 \mu H$

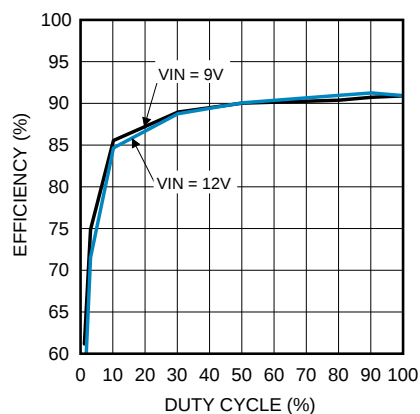


Figure 4.

Boost Converter Efficiency

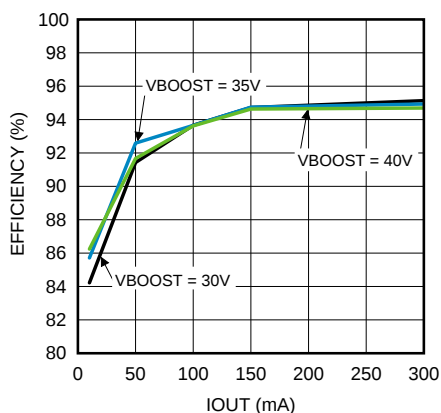


Figure 5.

Battery Current

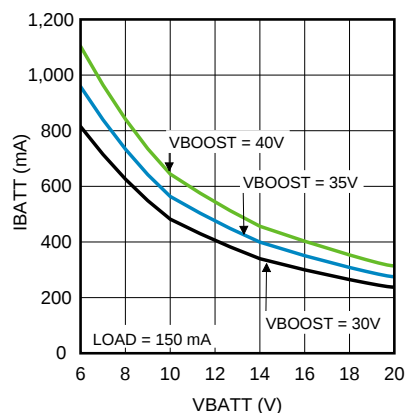


Figure 6.

$I_{LED}$   
VS.  
 $R_{ISET}$

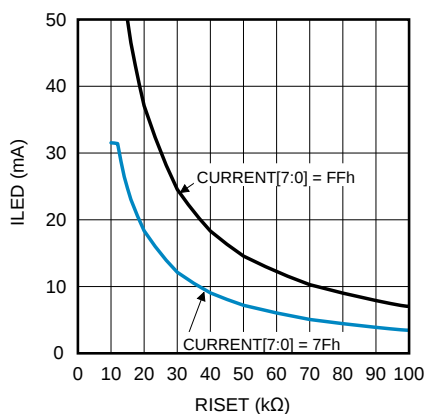


Figure 7.

Typical Waveforms,  $f_{LED} = 9.6 \text{ kHz}$

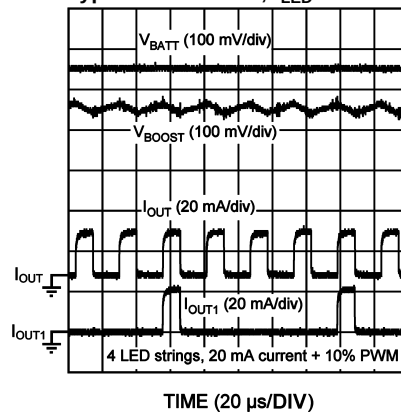


Figure 8.

## Typical Performance Characteristics (continued)

Unless otherwise specified:  $V_{BATT} = 12.0V$ ,  $C_{VLDO} = 1 \mu F$ ,  $L1 = 33 \mu H$ ,  $C_{IN} = 10 \mu F$ ,  $C_{OUT} = 10 \mu F$

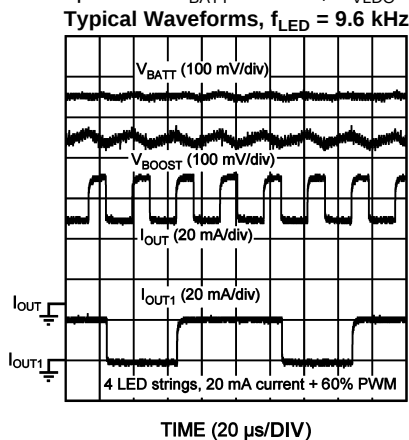


Figure 9.

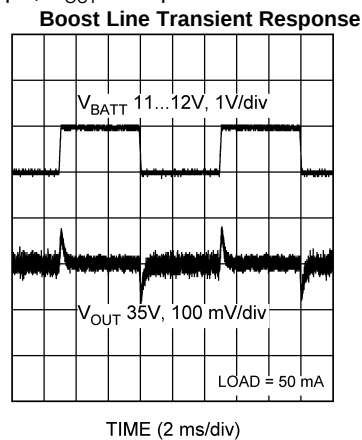


Figure 10.

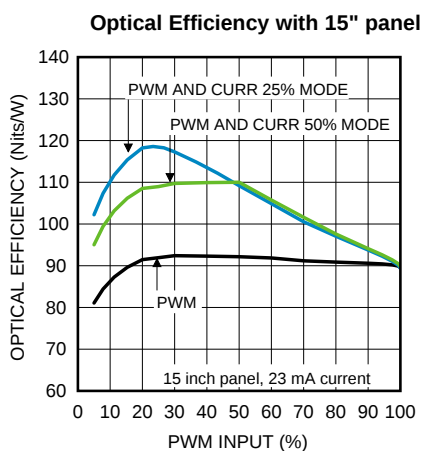


Figure 11.

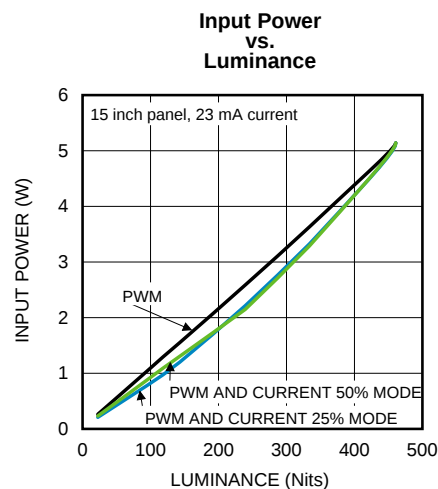


Figure 12.

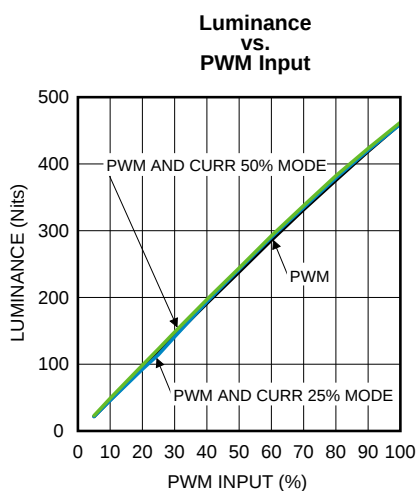


Figure 13.

### Power saved with PWM & current mode compared to PWM mode

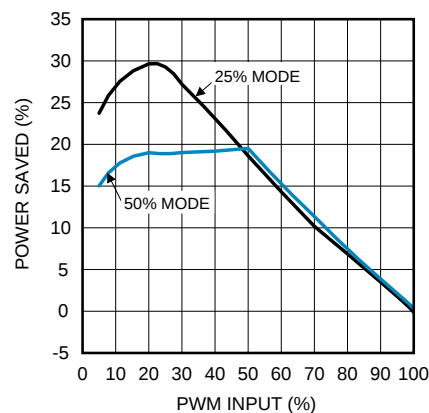
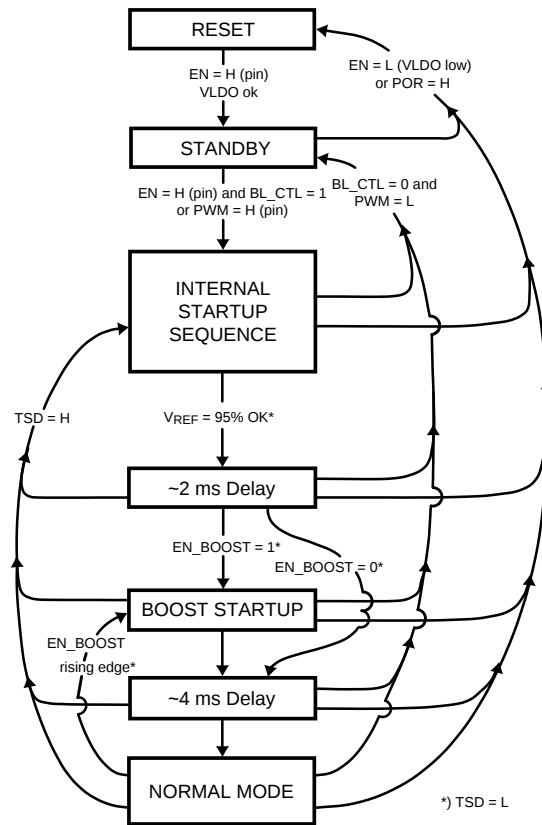


Figure 14.

## MODES OF OPERATION



**RESET:** In the RESET mode all the internal registers are reset to the default values. Reset is entered always when VLDO voltage is low. EN pin is enable for the internal LDO. Power On Reset (POR) will activate during the chip startup or when the supply voltage VLDO fall below POR level. Once VLDO rises above POR level, POR will inactivate and the chip will continue to the STANDBY mode.

**STANDBY:** The STANDBY mode is entered if the register bit BL\_CTL is LOW and external PWM input is not active and POR is not active. This is the low power consumption mode, when only internal 5V LDO is enabled. Registers can be written in this mode and the control bits are effective immediately after start up.

**STARTUP:** When BL\_CTL bit is written high or PWM signal is high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (VREF, Bias, Oscillator etc.). Internal EPROM and EEPROM are read in this mode. To ensure the correct oscillator initialization etc, a 2 ms delay is generated by the internal state-machine. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation and STARTUP mode is entered until no thermal shutdown event is present.

**BOOST STARTUP:** Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is raised in low current PWM mode during the 4 ms delay generated by the state-machine. All LED outputs are off during the 4 ms delay to ensure smooth startup. The Boost startup is entered from Internal Startup Sequence if EN\_BOOST is HIGH.

**NORMAL:** During NORMAL mode the user controls the chip using the external PWM input or with Control Registers through I<sup>2</sup>C. The registers can be written in any sequence and any number of bits can be altered in a register in one write.

## Functional Overview

LP8553 is a high-voltage LED driver for medium sized LCD backlight applications. It includes high-voltage boost converter. Boost voltage automatically sets to the correct level needed to drive the LED strings. This is done by monitoring LED output voltage drop in real time.

Four LED outputs are driven either with constant current sinks with PWM control or by controlling both PWM and current. Constant current value is set with EEPROM bits and with  $R_{ISET}$  resistor. Brightness (PWM) is controlled either with I<sup>2</sup>C register or with PWM input. PWM frequencies are set with EEPROM bits and with  $R_{FSET}$  resistor. Special Phase-Shift PWM mode can be used to reduce boost output current peak, thus reducing output ripple, capacitor size and audible noise.

With LP8553 it is possible to synchronize the PWM output frequency to  $V_{SYNC}$  signal received from video processor. Internal PLL ensures that the PWM output clock is always synchronized to the  $V_{SYNC}$  signal.

Special dithering mode makes it possible to increase output resolution during fading between two brightness values and by this making the transition look very smooth with virtually no stepping. Transition slope time can be adjusted with EEPROM bits.

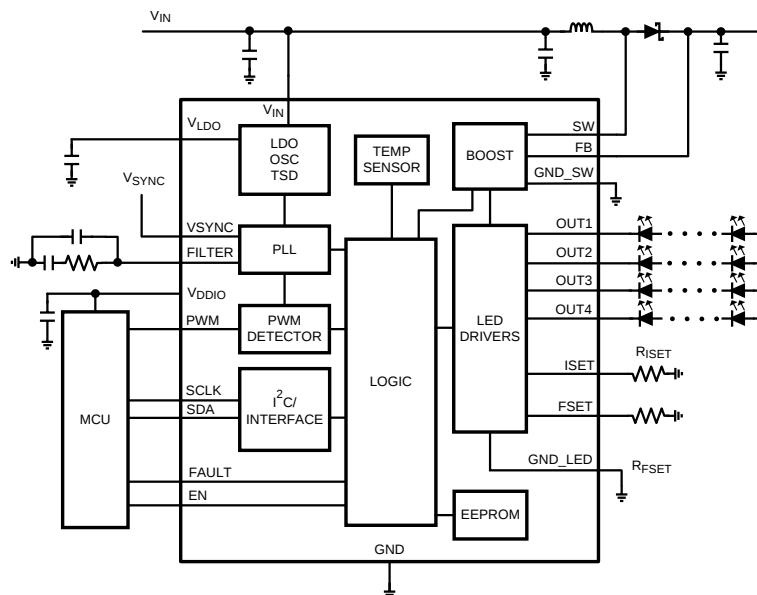
Safety features include LED fault detection with open and short detection. LED fault detection will prevent system overheating in case of open in some of the LED strings. Chip internal temperature is constantly monitored and based on this LP8553 can reduce the brightness of the backlight to reduce thermal loading once certain trip point is reached. Threshold is programmable in EEPROM. If chip internal temperature reaches too high, the boost converter and LED outputs are completely turned off until the internal temperature has reached acceptable level. Boost converter is protected against too high load current and over-voltage. LP8553 notifies the system about the fault through I<sup>2</sup>C register and with FAULT pin.

EEPROM programmable functions include:

- PWM frequencies
- Phase shift PWM mode
- LED constant current
- Boost output frequency
- Temperature thresholds
- Slope for brightness changes
- Dithering options
- PWM output resolution
- Boost control bits

External components  $R_{ISET}$  and  $R_{FSET}$  can also be used for selecting the output current and PWM frequencies.

## Block Diagram



## Clock Generation

LP8553 has an internal 5 MHz oscillator which is used for clocking the boost converter, state machine, PWM input duty cycle measurement, internal timings such as slope time for output brightness changes.

An internal clock can be used for generating the PWM output frequency. In this case the 5 MHz clock can be multiplied with the internal PLL to achieve higher resolution. The higher the clock frequency for PWM generation block, the higher the resolution but the tradeoff is higher  $I_Q$  of the part. Clock multiplication is set with <PWM\_RESOLUTION[1:0]> EEPROM Bits.

The PLL can also be used for generating the required PWM generation clock from the  $V_{SYNC}$  signal. This makes sure that the LED output PWM is always synchronized to the  $V_{SYNC}$  signal and there is no clock variation between LCD display video update and the LED backlight output frequency. Also  $H_{SYNC}$  signal up to 55 kHz can be used.

PLL has internal counter which has 13-bit control <PLL[12:0]> to achieve correct output clock frequency based on the  $V_{SYNC}$  frequency.

For the PLL it can take couple of seconds to synchronize to 60 Hz  $V_{SYNC}$  signal in startup and before this correct PWM clock frequency is generated from internal oscillator. FILTER pin component selection affects the time it takes from the PLL to lock to  $V_{SYNC}$  signal.

Special logic is implemented for allowing steady clock frequency even if there are missing  $V_{SYNC}$  pulses. In case pulses are randomly left out, the LP8553 can generate the pulses internally while keeping the same PWM output frequency. When  $V_{SYNC}$  pulses are available again, the internal logic will automatically switch to the external  $V_{SYNC}$  clock without glitch.

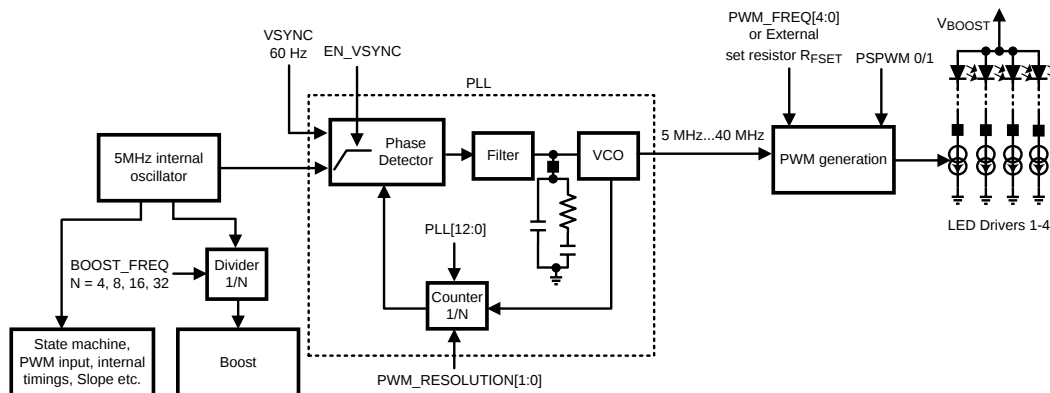


Figure 15. Principle of the Clock Generation

## Brightness Control Methods

LP8553 controls the brightness of the backlight with PWM. PWM control is received either from PWM input pin or from I<sup>2</sup>C register bits. The PWM source selection is done with <BRT\_MODE[1:0]> bits as follows:

| BRT_MODE[1] | BRT_MODE[0] | PWM source                                 |
|-------------|-------------|--------------------------------------------|
| 0           | 0           | PWM input pin duty cycle control. Default. |
| 0           | 1           | PWM input pin duty cycle control.          |
| 1           | 0           | Brightness register                        |
| 1           | 1           | PWM direct control (PWM in = PWM out)      |

## PWM Input Duty Cycle

With PWM input pin duty-cycle control the output PWM is controlled by PWM input duty cycle. PWM detector block measures the duty cycle in the PWM pin and uses this 13-bit value to generate the output PWM. Output PWM can have different frequency than input in this mode and also phase shift PWM mode can be used. Slope and dither are effective in this mode. PWM input resolution is defined by the input PWM clock frequency.

## Brightness Register Control

With brightness register control the output PWM is controlled with 8-bit resolution <BRT7:0> register bits. Phase shift scheme can be used with this and the output PWM frequency can be freely selected. Slope and dither are effective in this mode.

## PWM Direct Control

With PWM direct control the output PWM will directly follow the input PWM. Due to the internal logic structure the input is anyway clocked with the 5 MHz clock or the PLL clock. PSPWM mode is not possible in this mode. Slope and dither are not effective in this mode.

## PWM Calculation Data Flow

Below is flow chart of the PWM calculation data flow. In PWM direct control mode most of the blocks are bypassed and this flow chart does not apply.

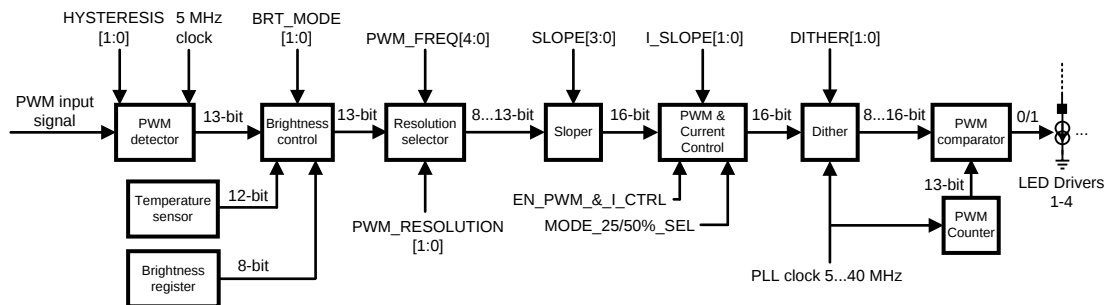


Figure 16. PWM Calculation Data Flow

## PWM Detector

The PWM detector block measures the duty cycle of the input PWM signal. Resolution depends on the input signal frequency. Hysteresis selection sets the minimum allowable change to the input. If smaller change is detected, it is ignored. With hysteresis the constant changing between two brightness values is avoided if there is small jitter in the input signal.

## Brightness Control

Brightness control block gets 13-bit value from the PWM detector, 12-bit value from the temperature sensor and also 8-bit value from the brightness register. <BRT\_MODE[1:0]> selects whether to use PWM input duty cycle value or the brightness register value as described earlier. Based on the temperature sensor value the duty cycle is reduced if the temperature has reached the temperature limit set to the <TEMP\_LIM[1:0]> EEPROM bits.

## Resolution Selector

Resolution selector takes the necessary MSB bits from the input data to match the output resolution. For example if 11-bit resolution is used for output, then 11 MSB bits are selected from the input. Dither bits are not taken into account for the output resolution. This is to make sure that in steady state condition, there is no dithering used for the output.

## Sloper

Sloper makes the smooth transition from one brightness value to another. Slope time can be adjusted from 0 to 500 ms with <SLOPE[3:0]> EEPROM bits. The sloper output is 16-bit value.

## PWM & Current Control

Automatic PWM & current control improves the optical efficiency of the LEDs by using PWM control with small brightness values and current control with bigger values. <EN\_PWM\_&\_I\_CTRL> EEPROM bit selects whether the PWM & current control is used instead of PWM control or not. PWM to current dimming switch point can be set to 25% or 50% of the brightness range with <MODE\_25/50\_SEL> EEPROM bit. Current slope can be adjusted by using the <I\_SLOPE[1:0]> EEPROM bits.

## Dither

With dithering the output resolution can be “artificially” increased during sloping from one brightness value to another. This way the brightness change steps are not visible to eye. Dithering can be from 0 to 3 bits, and is selected with <DITHER[1:0]> EEPROM bits.

## PWM Comparator

The PWM counter clocks the PWM comparator based on the duty cycle value received from Dither block. Output of the PWM comparator controls directly the LED drivers. If PSPWM mode is used, then the signal to each LED output is delayed certain amount.

## Current Setting

Maximum current of the LED outputs is controlled with CURRENT[7:0] EEPROM register bits linearly from 0 to 30 mA. If <EN\_I\_RES> = 1 the maximum LED output current can be scaled also with external resistor, R<sub>SET</sub>. R<sub>SET</sub> controls the LED current as follows:

$$I_{LED} = \frac{600 * 1.23V}{R_{SET}} * \frac{CURRENT [7:0]}{255}$$

- Default value for CURRENT[7:0] = 7Fh (127d). (1)

Therefore the output current can be calculated as follows:

$$R_{SET} = \frac{600 * 1.23}{I_{LED}} * \frac{1}{2} = \frac{369}{I_{LED}}$$

Note: formula is only approximation for the actual current.

- E.g. If 16 kΩ R<sub>SET</sub> resistor is used, then the LED maximum current is 23 mA. (2)

## PWM Frequency Setting

PWM frequency is selected with PWM\_FREQ[4:0] EEPROM register. If PLL clock frequency multiplication is used, it will affect the output PWM frequency as well. <PWM\_RESOLUTION[1:0]> EEPROM bits will select the PLL output frequency and hence the PWM frequency and resolution. Below are listed PWM frequencies with <EN\_VSYNC> = 0. PWM resolution setting affects the PLL clock frequency (5 MHz...40 MHz). Highlighted frequencies with boldface can be selected also with external resistor R<sub>FSET</sub>. To activate R<sub>FSET</sub> frequency selection the <EN\_F\_RES> EEPROM bit must be 1.

| PWM_RES[1:0]  | 00           | 01           | 10           | 11     |                   |
|---------------|--------------|--------------|--------------|--------|-------------------|
| PWM_FREQ[4:0] | 5 MHz        | 10 MHz       | 20 MHz       | 40 MHz | Resolution (bits) |
| 11111         | <b>19232</b> | -            | -            | -      | 8                 |
| 11110         | <b>16828</b> | -            | -            | -      | 8                 |
| 11101         | <b>14424</b> | -            | -            | -      | 8                 |
| 11100         | <b>12020</b> | -            | -            | -      | 8                 |
| 11011         | <b>9616</b>  | <b>19232</b> | -            | -      | 9                 |
| 11010         | <b>7963</b>  | <b>15927</b> | -            | -      | 9                 |
| 11001         | <b>6386</b>  | <b>12771</b> | -            | -      | 9                 |
| 11000         | <b>4808</b>  | <b>9616</b>  | <b>19232</b> | -      | 10                |
| 10111         | 4658         | 9316         | 18631        | -      | 10                |
| 10110         | 4508         | 9015         | 18030        | -      | 10                |
| 10101         | 4357         | <b>8715</b>  | 17429        | -      | 10                |
| 10100         | 4207         | 8414         | 16828        | -      | 10                |
| 10011         | 4057         | 8114         | <b>16227</b> | -      | 10                |
| 10010         | 3907         | <b>7813</b>  | 15626        | -      | 10                |
| 10001         | 3756         | 7513         | 15025        | -      | 10                |
| 10000         | 3606         | 7212         | <b>14424</b> | -      | 10                |
| 01111         | 3456         | 6912         | 13823        | -      | 10                |
| 01110         | 3306         | 6611         | 13222        | -      | 10                |

| PWM_RES[1:0]  | 00    | 01          | 10           | 11           |                   |
|---------------|-------|-------------|--------------|--------------|-------------------|
| PWM_FREQ[4:0] | 5 MHz | 10 MHz      | 20 MHz       | 40 MHz       | Resolution (bits) |
| 01101         | 3155  | <b>6311</b> | 12621        | -            | 10                |
| 01100         | 3005  | 6010        | <b>12020</b> | -            | 10                |
| 01011         | 2855  | 5710        | 11419        | -            | 10                |
| 01010         | 2705  | 5409        | 10818        | -            | 10                |
| 01001         | 2554  | 5109        | 10217        | -            | 10                |
| 01000         | 2404  | <b>4808</b> | <b>9616</b>  | <b>19232</b> | 11                |
| 00111         | 2179  | 4357        | 8715         | <b>17429</b> | 11                |
| 00110         | 1953  | 3907        | <b>7813</b>  | <b>15626</b> | 11                |
| 00101         | 1728  | 3456        | 6912         | 13823        | 11                |
| 00100         | 1503  | 3005        | <b>6010</b>  | <b>12020</b> | 11                |
| 00011         | 1202  | 2404        | <b>4808</b>  | <b>9616</b>  | 12                |
| 00010         | 1052  | 2104        | 4207         | <b>8414</b>  | 12                |
| 00001         | 826   | 1653        | 3306         | <b>6611</b>  | 12                |
| 00000         | 601   | 1202        | 2404         | <b>4808</b>  | 13                |

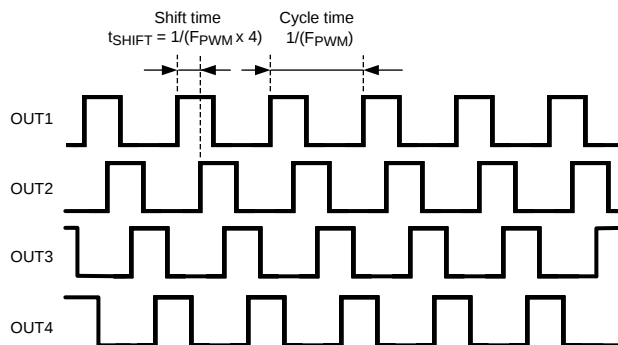
R<sub>FSET</sub> resistance values with corresponding PWM frequencies:

| PWM_RES[1:0] | 00          |            | 01           |            | 10           |            | 11           |            |
|--------------|-------------|------------|--------------|------------|--------------|------------|--------------|------------|
| RFSET (kΩ)   | 5 MHz Clock | Resolution | 10 MHz Clock | Resolution | 20 MHz Clock | Resolution | 40 MHz Clock | Resolution |
| 10...15      | 19232       | 8          | 19232        | 9          | 19232        | 10         | 19232        | 11         |
| 26...29      | 16828       | 8          | 15927        | 9          | 16227        | 10         | 17429        | 11         |
| 36...41      | 14424       | 8          | 12771        | 9          | 14424        | 10         | 15626        | 11         |
| 50...60      | 12020       | 8          | 9616         | 10         | 12020        | 10         | 12020        | 11         |
| 85...100     | 9616        | 9          | 8715         | 10         | 9616         | 11         | 9616         | 12         |
| 135...150    | 7963        | 9          | 7813         | 10         | 7813         | 11         | 8414         | 12         |
| 200...300    | 6386        | 9          | 6311         | 10         | 6010         | 11         | 6811         | 12         |
| 450...       | 4808        | 10         | 4808         | 11         | 4808         | 12         | 4808         | 13         |

### Phase Shift PWM Scheme

Phase shift PWM scheme allows delaying the time when each LED output is active. When the LED output are not activated simultaneously, the peak load current from the boost output is greatly decreased. This reduces the ripple seen on the boost output and allows smaller output capacitors. Reduced ripple also reduces the output ceramic capacitor audible ringing. PSPWM scheme also increases the load frequency seen on boost output by x4 and therefore transfers the possible audible noise to so high frequency that human ear cannot hear it.

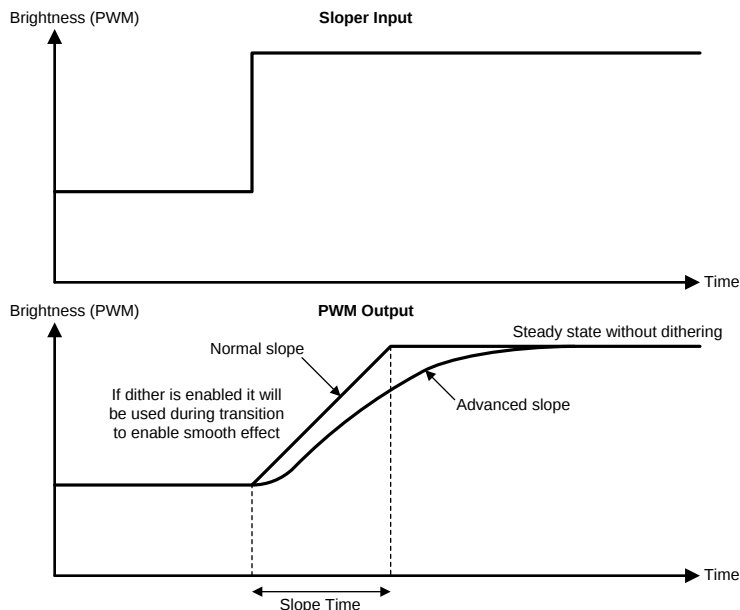
Description of the PSPWM mode is seen on the following diagram. PSPWM mode is enabled by setting <EN\_PSPWM> EEPROM bit to 1. Shift time is the delay between outputs and it is defined as  $1 / (f_{PWM} \times 4)$ . If the <EN\_PSPWM> bit is 0, then the delay is 0 and all outputs are active simultaneously.



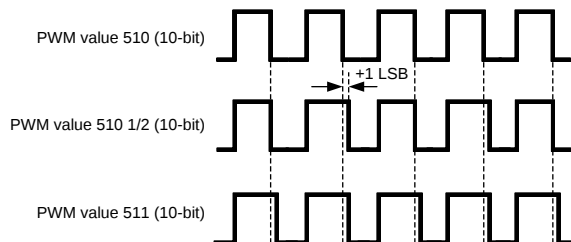
**Figure 17. Phase Shift PWM Mode**

### Slope and Dithering

During transition between two brightness (PWM) values special dithering scheme is used if the slope is enabled. It allows increased resolution and smaller average steps size. Dithering is not used in steady state condition. Slope time can be programmed with EEPROM bits <SLOPE[3:0]> from 0 to 500 ms. Same slope time is used for sloping up and down. Advanced slope makes brightness changes smooth for the eye. Dithering can be programmed with EEPROM bits <DITHER[1:0]> from 0 to 3 bits. Example below is for 1-bit dithering, e.g., for 3-bit dithering, every 8th pulse is made 1 LSB longer to increase the average value by 1/8 of LSB.



**Figure 18. Sloper Operation**



**Figure 19. Example of the Dithering,  
1-bit dither, 10-bit resolution**

## Driver Headroom Control

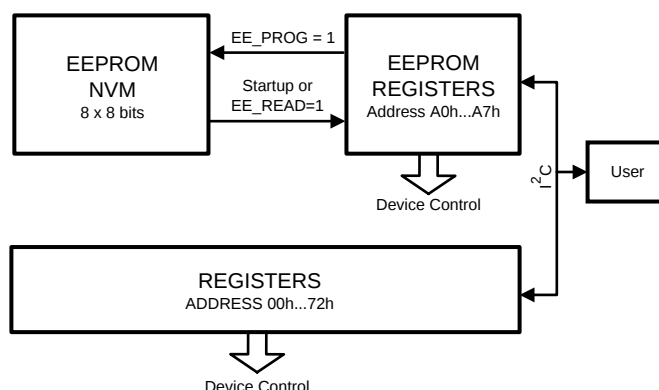
Driver headroom can be controlled with <DRV\_HEADR[2:0]> EEPROM bits. Driver headroom control sets the minimum threshold for the voltage over the LED output which has the smallest driver headroom and controls the boost output voltage accordingly. Boost output voltage step size is 125 mV. The LED output which has the smallest forward voltage is the one which has highest  $V_F$  across the LEDs. The strings with highest forward voltage is detected automatically. To achieve best possible efficiency smallest possible headroom voltage should be selected. If there is high variation between LED strings, the headroom can be raised slightly to prevent any visual artifacts.

## EEPROM

EEPROM memory stores various parameters for chip control. The 64-bit EEPROM memory is organized as 8 x 8 bits. The EEPROM structure consists of a register front-end and the non-volatile memory (NVM). Register data can be read and written through the serial interface, and data will be effective immediately. To read and program NVM, separate commands need to be sent. Erase and program voltages are generated on-chip charge pump, no other voltages than normal input voltage are required. A complete EEPROM memory map is shown in the chapter LP8553 [Table 3](#).

### NOTE

EEPROM NVM can be programmed or read by customer for bench validation. Programming for production devices should be done in TI production test, where appropriate checks will be performed to confirm EEPROM validity. Writing to EEPROM Control register of production devices (for burning or reading EEPROM) is not recommended. If special EEPROM configuration is required, please contact the TI Sales Office for availability.

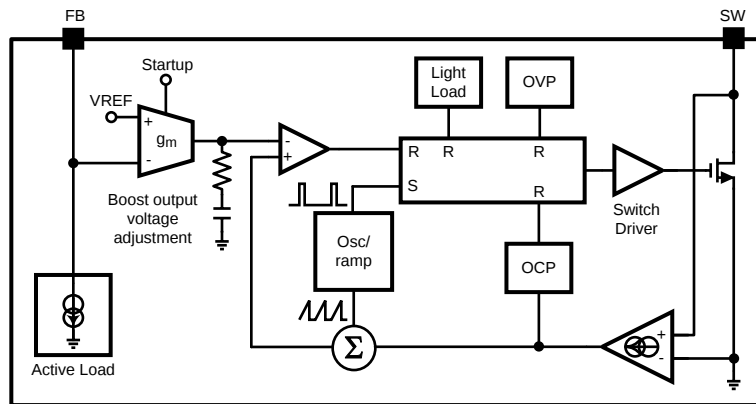


## Boost Converter

### Operation

The LP8553 boost DC/DC converter generates a 10...40V supply voltage for the LEDs from 2.7...22V input voltage. The output voltage can be controlled either with EEPROM register bits <VBOOST[4:0]> or automatic adaptive voltage control can be used. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The topology of the magnetic boost converter is called CPM (current programmed mode) control, where the inductor current is measured and controlled with the feedback. Switching frequency is selectable between 156 kHz and 1.25 MHz with EEPROM bit <BOOST\_FREQ[1:0]>. When <EN\_BOOST> EEPROM register bit is set to 1, then boost will activate automatically when backlight is enabled.

In adaptive mode the boost output voltage is adjusted automatically based on LED driver headroom voltage. Boost output voltage control step size is in this case 125 mV to ensure as small as possible driver headroom and high efficiency. Enabling the adaptive mode is done with <EN\_ADAPT> EEPROM bit. If boost is started with adaptive mode enabled, then the initial boost output voltage value is defined with the <VBOOST[4:0]> EEPROM register bits in order to eliminate long output voltage iteration time when boost is started for the first time. The following figure shows the boost topology with the protection circuitry:



## Protection

Three different protection schemes are implemented:

1. Over-voltage protection, limits the maximum output voltage.
  - Over-voltage protection limit changes dynamically based on output voltage setting.
  - Keeps the output below breakdown voltage.
  - Prevents boost operation if battery voltage is much higher than desired output.
2. Over-current protection, limits the maximum inductor current.
3. Duty cycle limiting.

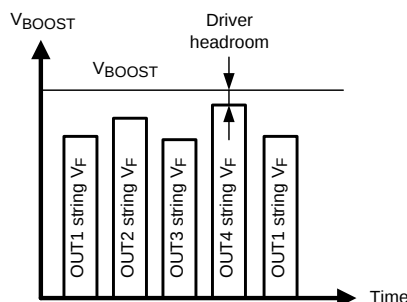
## Manual Output Voltage Control

User can control the boost output voltage with <VBOOST[4:0]> EEPROM register bits when adaptive mode is disabled.

| VBOOST[4:0] |     | Voltage (typical) |
|-------------|-----|-------------------|
| Bin         | Dec | Volts             |
| 00000       | 0   | 10                |
| 00001       | 1   | 11                |
| 00010       | 2   | 12                |
| 00011       | 3   | 13                |
| 00100       | 4   | 14                |
| ...         | ... | ...               |
| 11101       | 29  | 39                |
| 11110       | 30  | 40                |
| 11111       | 31  | 40                |

## Adaptive Boost Control

Adaptive boost control function adjusts the boost output voltage to the minimum sufficient voltage for proper LED driver operation. The output with highest  $V_F$  LED string is detected and boost output voltage adjusted accordingly. Driver headroom can be adjusted with <DRIVER\_HEADR[2:0]> EEPROM bits from ~300 mV to 1200 mV. Boost adaptive control voltage step size is 125 mV. Boost adaptive control operates similarly with and without PSPWM.



**Figure 20. Boost Adaptive Control Principle with PSPWM**

## Fault Detection

LP8553 has fault detection for LED fault, low-battery voltage, over-current and thermal shutdown. The open drain output pin (FAULT) can be used to indicate occurred fault. The cause for the fault can be read from status register. Reading the fault register will also reset the fault. Setting the EN pin low will also reset the faults, even if an external 5V line is used to power VLDO pin.

### LED Fault Detection

With LED fault detection, the voltages across the LED drivers are constantly monitored. Shorted or open LED string is detected.

If LED fault is detected:

- The corresponding LED string is taken out of boost adaptive control loop;
- Fault bits are set in the fault register to identify whether the fault has been open/short and how many strings are faulty; and
- Fault open-drain pin is pulled down.

LED fault sensitivity can be adjusted with <LED\_FAULT\_THR> EEPROM bit which sets the allowable variation between LED output voltage to 3.3V or 5.3V. Depending on application and how much variation there can be in normal operation between LED string forward voltages this setting can be adjusted.

Fault is cleared by setting EN pin low or by reading the fault register.

By default the LED fault detection is active only in automatic PWM & current dimming mode. If LED fault detection is needed in PWM dimming mode, please contact TI representative for guidance.

### Under-Voltage Detection

LP8553 has detection for too-low VIN voltage. Threshold level for the voltage is set with EEPROM register bits as seen in the following table:

| UVLO[1:0] | Threshold (V) |
|-----------|---------------|
| 00        | OFF           |
| 01        | 2.7V          |
| 10        | 5.4V          |
| 11        | 8.1V          |

When under voltage is detected the LED outputs and boost will shutdown, FAULT pin is pulled down and corresponding fault bit is set in fault register. LEDs and boost will start again when the voltage has increased above the threshold level. Hysteresis is implemented to threshold level to avoid continuous triggering of fault when threshold is reached.

Fault is cleared by setting EN pin low or by reading the fault register.

## Over-Current Protection

LP8553 has detection for too-high loading on the boost converter. When over-current fault is detected, the LP8553 will shut down.

Fault is cleared by setting EN pin low or by reading the fault register.

## Device Thermal Regulation

LP8553 has an internal temperature sensor which can be used to measure the junction temperature of the device and protect the device from overheating. During thermal regulation, LED PWM is reduced by 2% of full scale per °C whenever the temperature threshold is reached. Temperature regulation is enabled automatically when chip is enabled. 11-bit temperature value can be read from Temp MSB and Temp LSB registers, MSB should be read first. Temperature limit can be programmed in EEPROM as shown in the following table.

Thermal regulation function does not generate fault signal.

| TEMP_LIM[1:0] | Over-Temp Limit (°C) |
|---------------|----------------------|
| 00            | OFF                  |
| 01            | 110                  |
| 10            | 120                  |
| 11            | 130                  |

## Thermal Shutdown

If the LP8553 reaches thermal shutdown temperature (150°C ) the LED outputs and boost will shut down to protect it from damage. Also the fault pin will be pulled down to indicate the fault state. Device will activate again when temperature drops below 130°C degrees.

Fault is cleared by setting EN pin low or by reading the fault register.

## I<sup>2</sup>C-Compatible Serial Bus Interface

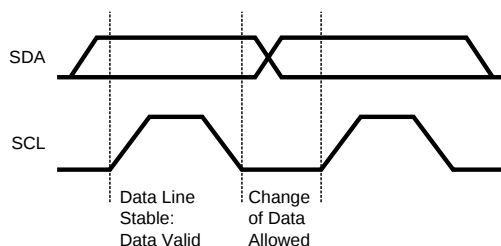
### Interface Bus Overview

The I<sup>2</sup>C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCLK). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

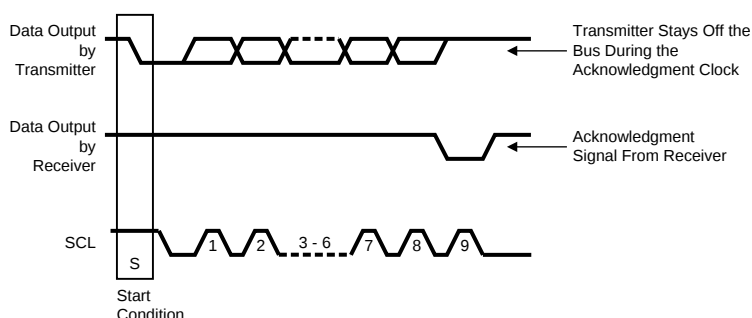
Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the SCLK. The LP8553 is always a slave device.

### Data Transactions

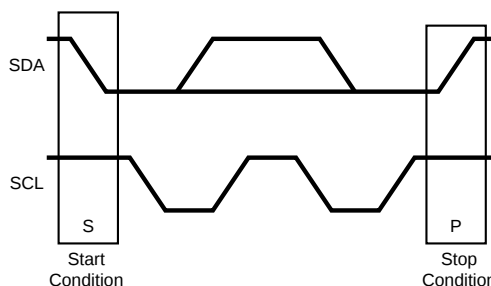
One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock SCLK. Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCLK and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCLK state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

**Figure 21. Bit Transfer**

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

**Figure 22. Start and Stop**

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCLK) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCLK is high indicates a Stop Condition.

**Figure 23. Start and Stop Conditions**

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

### Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

### “Acknowledge After Every Byte” Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

### Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP8553 operates as a slave device with 7-bit address combined with data direction bit. Slave address is 2Ch as 7-bit or 58h for write and 59h for read in 8-bit format.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.



**Figure 24. I<sup>2</sup>C Chip Address**

### Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

### Control Register Read Cycle

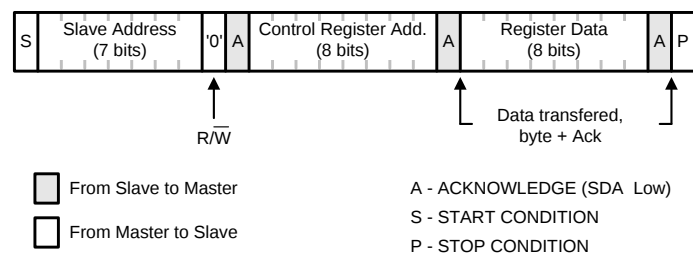
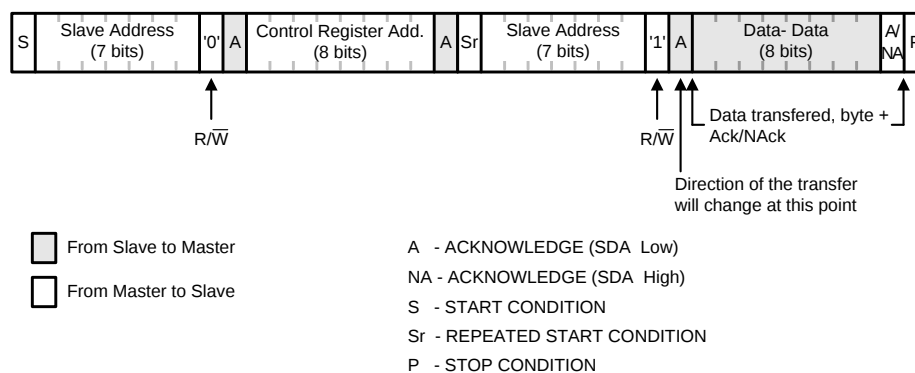
- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.

- Master sends the slave address (7 bits) and the data direction bit ( $r/w = 1$ ).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

**Table 1. Data Read and Write Cycles**

|            | Address Mode                                                                                                                                                                                                                                                             |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data Read  | <Start Condition><br><Slave Address>< $r/w = 0$ >[Ack]<br><Register Addr.>[Ack]<br><Repeated Start Condition><br><Slave Address>< $r/w = 1$ >[Ack]<br>[Register Data]<Ack or NAck><br>... additional reads from subsequent register address possible<br><Stop Condition> |
| Data Write | <Start Condition><br><Slave Address>< $r/w = 0$ >[Ack]<br><Register Addr.>[Ack]<br><Register Data>[Ack]<br>... additional writes to subsequent register address possible<br><Stop Condition>                                                                             |

&lt;&gt;Data from master [ ] Data from slave

**Register Read and Write Detail****Register Write Format****Register Read Format**

## Recommended External Components

### Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and should be preferred.

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current.

The equation below shows the worst case conditions.

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE}$$

Where  $I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$

Where  $D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})}$  and  $D' = (1 - D)$

- $I_{RIPPLE}$ : Average to peak inductor current
- $I_{OUTMAX}$ : Maximum load current
- $V_{IN}$ : Maximum input voltage in application
- $L$ : Min inductor value including worst case tolerances
- $f$ : Minimum switching frequency
- $D$ : Duty cycle for CCM Operation
- $V_{OUT}$ : Output voltage

(3)

Example using above equations:

- $V_{IN} = 12V$
- $V_{OUT} = 38V$
- $I_{OUT} = 400\text{ mA}$
- $L = 15\text{ }\mu\text{H} - 20\% = 12\text{ }\mu\text{H}$
- $f = 1.25\text{ MHz}$
- $I_{SAT} = 1.6A$

As a result the inductor should be selected according to the  $I_{SAT}$ . A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 2.5A. A 15  $\mu\text{H}$  inductor with a saturation current rating of 2.5A is recommended for most applications. The inductor's resistance should be less than 300 m $\Omega$  for good efficiency. For high efficiency choose an inductor with high frequency core material such as ferrite to reduce core losses. To minimize radiated noise, use shielded core inductor. Inductor should be placed as close to the SW pin and the IC as possible. Special care should be used when designing the PCB layout to minimize radiated noise and to get good performance from the boost converter. For more information on the PCB layout recommendations, please refer to LP8553 PCB layout guide.

### Output Capacitor

A ceramic capacitor with 50V voltage rating or higher is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. For light loads a 4.7  $\mu\text{F}$  capacitor is sufficient. Effectively the capacitance should be 4  $\mu\text{F}$  for < 150 mA loads. For maximum output voltage/current 10  $\mu\text{F}$  capacitor (or two 4.7  $\mu\text{F}$  capacitors) is recommended to minimize the output ripple.

### LDO Capacitor

A 1 $\mu\text{F}$  ceramic capacitor with 10V voltage rating is recommended for the LDO capacitor.

## Output Diode

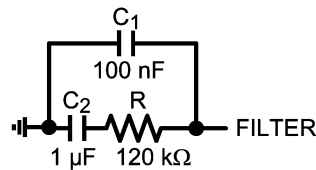
A Schottky diode should be used for the output diode. Peak repetitive current should be greater than inductor peak current (2.5A) to ensure reliable operation. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown voltage of the Schottky diode significantly larger (~60V) than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

## Resistors for Setting the LED Current and PWM Frequency

See [Table 3](#) on how to select values for these resistors

## Filter Component Values

Optimal components for 60 Hz  $V_{\text{SYNC}}$  frequency and 4 Hz cut-off frequency of the low-pass filter are shown in the [Typical Application](#) diagrams and in the figure below. If 2 Hz cut-off frequency i.e. slower response time is desired, filter components are:  $C_1 = 1 \mu\text{F}$ ,  $C_2 = 10 \mu\text{F}$  and  $R = 47 \text{ k}\Omega$ . If different  $V_{\text{SYNC}}$  frequency or response time is desired, please contact TI representative for guidance.



**Table 2. Register Map**

| ADDR | REGISTER           | D7           | D6       | D5             | D4            | D3       | D2            | D1      | D0      | DEFAULT   |
|------|--------------------|--------------|----------|----------------|---------------|----------|---------------|---------|---------|-----------|
| 00H  | Brightness Control | BRT[7:0]     |          |                |               |          |               |         |         | 0000 0000 |
| 01H  | Device Control     |              |          |                |               |          | BRT_MODE[1:0] |         | BL_CTL  | 0000 0000 |
| 02H  | Fault              | OPEN         | SHORT    | 2_CHANN<br>ELS | 1_CHANN<br>EL | BL_FAULT | OCF           | TSD     | UVLO    | 0000 0000 |
| 03H  | ID                 | PANEL        | MFG[3:0] |                |               |          | REV[2:0]      |         |         | 1111 1100 |
| 04H  | Direct Control     |              |          |                |               | OUT[4:1] |               |         |         | 0000 0000 |
| 05H  | Temp MSB           | TEMP[10:3]   |          |                |               |          |               |         |         | 0000 0000 |
| 06H  | Temp LSB           | TEMP[2:0]    |          |                |               |          |               |         |         | 0000 0000 |
| 72H  | EEPROM_con<br>trol | EE_READ<br>Y |          |                |               |          | EE_INIT       | EE_PROG | EE_READ | 0000 0000 |

**Table 3. EEPROM Memory Map**

| ADDR | REGISTER       | D7                      | D6          | D5                     | D4                  | D3         | D2             | D1              | D0             |
|------|----------------|-------------------------|-------------|------------------------|---------------------|------------|----------------|-----------------|----------------|
| A0H  | eeeprom addr 0 | CURRENT[7:0]            |             |                        |                     |            |                |                 |                |
| A1H  | eeeprom addr 1 | BOOST_FREQ[1:0]         |             | EN_PWM<br>& I_CTR<br>L | TEMP_LIM[1:0]       |            | SLOPE[2:0]     |                 |                |
| A2H  | eeeprom addr 2 | ADAPTIVE_SPEED[1:0]     |             | ADV_SLO<br>PE          | MODE_25/<br>50%_SEL | EN_ADAPT   | EN_BOOS<br>T   | BOOST_IM<br>AX  | I_SLOPE[<br>1] |
| A3H  | eeeprom addr 3 | UVLO[1:0]               |             | EN_PSP<br>WM           | PWM_FREQ[4:0]       |            |                |                 |                |
| A4H  | eeeprom addr 4 | PWM_RESOLUTION[1:<br>0] |             | EN_I_RE<br>S           | LED_FAUL<br>T_THR   | I_SLOPE[0] | DRV_HEADR[2:0] |                 |                |
| A5H  | eeeprom addr 5 | EN_VSY<br>NC            | DITHER[1:0] |                        | VBOOST[4:0]         |            |                |                 |                |
| A6H  | eeeprom addr 6 | PLL[12:5]               |             |                        |                     |            |                |                 |                |
| A7H  | eeeprom addr 7 | PLL[4:0]                |             |                        |                     |            | EN_F_RES       | HYSTERESIS[1:0] |                |

## Register Bit Explanations

### Brightness Control

Address 00h

Reset value 0000 0000b

| Brightness Control register |     |        |                                     |   |   |   |   |
|-----------------------------|-----|--------|-------------------------------------|---|---|---|---|
| 7                           | 6   | 5      | 4                                   | 3 | 2 | 1 | 0 |
| BRT[7:0]                    |     |        |                                     |   |   |   |   |
| Name                        | Bit | Access | Description                         |   |   |   |   |
| BRT                         | 7:0 | R/W    | Backlight PWM 8-bit linear control. |   |   |   |   |

### Device Control

Address 01h

Reset value 0000 0000b

| Device Control register |     |        |                                                                                                                                                                             |   |               |   |        |
|-------------------------|-----|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---------------|---|--------|
| 7                       | 6   | 5      | 4                                                                                                                                                                           | 3 | 2             | 1 | 0      |
|                         |     |        |                                                                                                                                                                             |   | BRT_MODE[1:0] |   | BL_CTL |
| Name                    | Bit | Access | Description                                                                                                                                                                 |   |               |   |        |
| BRT_MODE                | 2:1 | R/W    | PWM source mode                                                                                                                                                             |   |               |   |        |
|                         |     |        | 00b = PWM input pin duty cycle control (default)                                                                                                                            |   |               |   |        |
|                         |     |        | 01b = PWM input pin duty cycle control                                                                                                                                      |   |               |   |        |
|                         |     |        | 10b = Brightness register                                                                                                                                                   |   |               |   |        |
|                         |     |        | 11b = Direct PWM control from PWM input pin                                                                                                                                 |   |               |   |        |
| BL_CTL                  | 0   | R/W    | Enable backlight                                                                                                                                                            |   |               |   |        |
|                         |     |        | 0 = Backlight disabled and chip turned off if BRT_MODE[1:0] = 10. In external PWM pin control the state of the chip is defined with the PWM pin and this bit has no effect. |   |               |   |        |
|                         |     |        | 1 = Backlight enabled and chip turned on if BRT_MODE[1:0] = 10. In external PWM pin control the state of the chip is defined with the PWM pin and this bit has no effect.   |   |               |   |        |

### Fault

Address 02h

Reset value 0000 0000b

| Fault register |       |            |                                                                                                                               |          |     |     |      |
|----------------|-------|------------|-------------------------------------------------------------------------------------------------------------------------------|----------|-----|-----|------|
| 7              | 6     | 5          | 4                                                                                                                             | 3        | 2   | 1   | 0    |
| OPEN           | SHORT | 2_CHANNELS | 1_CHANNEL                                                                                                                     | BL_FAULT | OCP | TSD | UVLO |
| Name           | Bit   | Access     | Description                                                                                                                   |          |     |     |      |
| OPEN           | 7     | R          | LED open fault detection                                                                                                      |          |     |     |      |
|                |       |            | 0 = No fault                                                                                                                  |          |     |     |      |
|                |       |            | 1 = LED open fault detected. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.  |          |     |     |      |
| SHORT          | 6     | R          | LED short fault detection                                                                                                     |          |     |     |      |
|                |       |            | 0 = No fault                                                                                                                  |          |     |     |      |
|                |       |            | 1 = LED short fault detected. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low. |          |     |     |      |

| Fault register |   |   |                                                                                                                                                                                                                                                                                                                                                            |
|----------------|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2_CHANNELS     | 5 | R | LED fault detection                                                                                                                                                                                                                                                                                                                                        |
|                |   |   | 0 = No fault                                                                                                                                                                                                                                                                                                                                               |
|                |   |   | 1 = 2 or more channels have generated either short or open fault. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.                                                                                                                                                                                          |
| 1_CHANNEL      | 4 | R | LED fault detection                                                                                                                                                                                                                                                                                                                                        |
|                |   |   | 0 = No fault                                                                                                                                                                                                                                                                                                                                               |
|                |   |   | 1 = 1 channel has generated either short or open fault. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.                                                                                                                                                                                                    |
| BL_FAULT       | 3 | R | LED fault detection                                                                                                                                                                                                                                                                                                                                        |
|                |   |   | 0 = No fault                                                                                                                                                                                                                                                                                                                                               |
|                |   |   | 1 = LED fault detected. Generated with OR function of all LED faults. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.                                                                                                                                                                                      |
| OCP            | 2 | R | Over current protection                                                                                                                                                                                                                                                                                                                                    |
|                |   |   | 0 = No fault                                                                                                                                                                                                                                                                                                                                               |
|                |   |   | 1 = Over current detected in boost output. OCP detection block monitors the boost output and if the boost output has been too low for more than 50 ms it will generate OCP fault and disable the boost. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low. After clearing the fault boost will startup again. |
| TSD            | 1 | R | Thermal shutdown                                                                                                                                                                                                                                                                                                                                           |
|                |   |   | 0 = No fault                                                                                                                                                                                                                                                                                                                                               |
|                |   |   | 1 = Thermal fault generated, 150°C reached. Boost converted and LED outputs will be disabled until the temperature has dropped down to 130°C. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.                                                                                                              |
| UVLO           | 0 | R | Under voltage detection                                                                                                                                                                                                                                                                                                                                    |
|                |   |   | 0 = No fault                                                                                                                                                                                                                                                                                                                                               |
|                |   |   | 1 = Under voltage detected in VIN pin. Boost converted and LED outputs will be disabled until V <sub>IN</sub> voltage is above the threshold voltage. Threshold voltage is set with EEPROM bits from 3V...9V. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.                                              |

## Identification

Address 03h

Reset value 1111 1100b

| Identification register |          |        |                      |   |          |   |   |
|-------------------------|----------|--------|----------------------|---|----------|---|---|
| 7                       | 6        | 5      | 4                    | 3 | 2        | 1 | 0 |
| PANEL                   | MFG[3:0] |        |                      |   | REV[2:0] |   |   |
| Name                    | Bit      | Access | Description          |   |          |   |   |
| PANEL                   | 7        | R      | Panel ID code        |   |          |   |   |
| MFG                     | 6:3      | R      | Manufacturer ID code |   |          |   |   |
| REV                     | 2:0      | R      | Revision ID code     |   |          |   |   |

## Direct Control

Address 04h

Reset value 0000 0000b

| Direct Control register |     |        |             |          |   |   |   |
|-------------------------|-----|--------|-------------|----------|---|---|---|
| 7                       | 6   | 5      | 4           | 3        | 2 | 1 | 0 |
|                         |     |        |             | OUT[4:1] |   |   |   |
| Name                    | Bit | Access | Description |          |   |   |   |

| Direct Control register |     |     |                                                           |
|-------------------------|-----|-----|-----------------------------------------------------------|
| OUT                     | 5:0 | R/W | Direct control of the LED outputs                         |
|                         |     |     | 0 = Normal operation. LED output are controlled with PWM. |
|                         |     |     | 1 = LED output is forced to 100% PWM.                     |

### Temp MSB

Address 05h

Reset value 0000 0000b

| Temp MSB register |     |        |                                                                                                                                        |   |   |   |   |
|-------------------|-----|--------|----------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|
| 7                 | 6   | 5      | 4                                                                                                                                      | 3 | 2 | 1 | 0 |
| TEMP[10:3]        |     |        |                                                                                                                                        |   |   |   |   |
| Name              | Bit | Access | Description                                                                                                                            |   |   |   |   |
| TEMP              | 7:0 | R      | Device internal temperature sensor reading first 8 MSB. MSB must be read before LSB, because reading of MSB register latches the data. |   |   |   |   |

### Temp LSB

Address 06h

Reset value 0000 0000b

| Temp LSB register |     |        |                                                                                                                                       |   |   |   |   |
|-------------------|-----|--------|---------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|
| 7                 | 6   | 5      | 4                                                                                                                                     | 3 | 2 | 1 | 0 |
| TEMP[2:0]         |     |        |                                                                                                                                       |   |   |   |   |
| Name              | Bit | Access | Description                                                                                                                           |   |   |   |   |
| TEMP              | 7:5 | R      | Device internal temperature sensor reading last 3 LSB. MSB must be read before LSB, because reading of MSB register latches the data. |   |   |   |   |

### EEPROM Control

Address 72h

Reset value 0000 0000b

| EEPROM Control register |     |        |                                                                                                                                                                                                                                                                                         |   |         |         |         |
|-------------------------|-----|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---------|---------|---------|
| 7                       | 6   | 5      | 4                                                                                                                                                                                                                                                                                       | 3 | 2       | 1       | 0       |
| EE_READY                |     |        |                                                                                                                                                                                                                                                                                         |   | EE_INIT | EE_PROG | EE_READ |
| Name                    | Bit | Access | Description                                                                                                                                                                                                                                                                             |   |         |         |         |
| EE_READY                | 7   | R      | EEPROM ready                                                                                                                                                                                                                                                                            |   |         |         |         |
|                         |     |        | 0 = EEPROM programming or read in progress                                                                                                                                                                                                                                              |   |         |         |         |
|                         |     |        | 1 = EEPROM ready, not busy                                                                                                                                                                                                                                                              |   |         |         |         |
| EE_INIT                 | 2   | R/W    | EEPROM initialization bit. This bit must be written 1 before EEPROM read or programming.                                                                                                                                                                                                |   |         |         |         |
| EE_PROG                 | 1   | R/W    | EEPROM programming.                                                                                                                                                                                                                                                                     |   |         |         |         |
|                         |     |        | 0 = Normal operation                                                                                                                                                                                                                                                                    |   |         |         |         |
|                         |     |        | 1 = Start the EEPROM programming sequence. EE_INIT must be written 1 before EEPROM programming can be started. Programs data currently in the EEPROM registers to non volatile memory (NVM). Programming sequence takes about 200 ms. Programming voltage is generated inside the chip. |   |         |         |         |
| EE_READ                 | 0   | R/W    | EEPROM read                                                                                                                                                                                                                                                                             |   |         |         |         |
|                         |     |        | 0 = Normal operation                                                                                                                                                                                                                                                                    |   |         |         |         |
|                         |     |        | 1 = Reads the data from NVM to the EEPROM registers. Can be used to restore default values if EEPROM registers are changed during testing.                                                                                                                                              |   |         |         |         |

Programming sequence (program data permanently from registers to NVM):

1. Turn on the chip by writing BL\_CTL bit to 1 and BRT\_MODE[1:0] to 10b (05h to address 01h)
2. Write data to EEPROM registers (address A0h...A7h).
3. Write EE\_INIT to 1 in address 72h. (04h to address 72h).
4. Write EE\_PROG to 1 and EE\_INIT to 0 in address 72h. (02h to address 72h).
5. Wait 200 ms.
6. Write EE\_PROG to 0 in address 72h. (00h to address 72h).

Read sequence (load data from NVM to registers):

1. Turn on the chip by writing BL\_CTL bit to 1 and BRT\_MODE[1:0] to 10b (05h to address 01h).
2. Write EE\_INIT to 1 in address 72h. (04h to address 72h).
3. Write EE\_READ to 1 and EE\_INIT to 0 in address 72h. (01h to address 72h).
4. Wait 200 ms.
5. Write EE\_READ to 0 in address 72h. (00h to address 72h).

Note: Data written to EEPROM registers is effective immediately even if the EEPROM programming sequence has not been done. When power is turned off, the device will however lose the data if it is not programmed to the NVM. During startup device automatically loads the data from NVM to registers.

#### NOTE

EEPROM NVM can be programmed or read by customer for bench validation. Programming for production devices should be done in TI production test, where appropriate checks will be performed to confirm EEPROM validity. Writing to EEPROM Control register of production devices (for burning or reading EEPROM) is not recommended. If special EEPROM configuration is required, please contact the TI Sales Office for availability.

## EEPROM Bit Explanations

### EEPROM Default Values

| ADDR | Default value |
|------|---------------|
| A0h  | 0111 1111     |
| A1h  | 1111 0101     |
| A2h  | 1011 1111     |
| A3h  | 0111 1011     |
| A4h  | 0010 1000     |
| A5h  | 0100 1111     |
| A6h  | 0110 0100     |
| A7h  | 0010 1101     |

## EEPROM Address 0

Address A0h

| EEPROM ADDRESS 0 register |     |        |                                                                                                                                                                                                                                                                                                             |   |                 |                                                                |   |
|---------------------------|-----|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|-----------------|----------------------------------------------------------------|---|
| 7                         | 6   | 5      | 4                                                                                                                                                                                                                                                                                                           | 3 | 2               | 1                                                              | 0 |
| CURRENT[7:0]              |     |        |                                                                                                                                                                                                                                                                                                             |   |                 |                                                                |   |
| Name                      | Bit | Access | Description                                                                                                                                                                                                                                                                                                 |   |                 |                                                                |   |
| CURRENT                   | 7:0 | R/W    | Backlight current adjustment. If EN_I_RES = 0 the maximum backlight current is defined only with these bits as described below. If EN_I_RES = 1, then the external resistor connected to ISET pin also scales the LED current. With 16 kΩ resistor and CURRENT set to 7Fh the output current is then 23 mA. |   |                 |                                                                |   |
|                           |     |        |                                                                                                                                                                                                                                                                                                             |   | EN_I_RES = 0    | EN_I_RES = 1                                                   |   |
|                           |     |        | 0000 0000                                                                                                                                                                                                                                                                                                   |   | 0 mA            | 0 mA                                                           |   |
|                           |     |        | 0000 0001                                                                                                                                                                                                                                                                                                   |   | 0.12 mA         | $(1/255) \times 600 \times 1.23V/R_{ISET}$                     |   |
|                           |     |        | 0000 0010                                                                                                                                                                                                                                                                                                   |   | 0.24 mA         | $(2/255) \times 600 \times 1.23V/R_{ISET}$                     |   |
|                           |     |        | ...                                                                                                                                                                                                                                                                                                         |   | ...             | ...                                                            |   |
|                           |     |        | <b>0111 1111 (default)</b>                                                                                                                                                                                                                                                                                  |   | <b>15.00 mA</b> | <b><math>(127/255) \times 600 \times 1.23V/R_{ISET}</math></b> |   |
|                           |     |        | ...                                                                                                                                                                                                                                                                                                         |   | ...             | ...                                                            |   |
|                           |     |        | 1111 1101                                                                                                                                                                                                                                                                                                   |   | 29.76 mA        | $(253/255) \times 600 \times 1.23V/R_{ISET}$                   |   |
|                           |     |        | 1111 1110                                                                                                                                                                                                                                                                                                   |   | 29.88 mA        | $(254/255) \times 600 \times 1.23V/R_{ISET}$                   |   |
|                           |     |        | 1111 1111                                                                                                                                                                                                                                                                                                   |   | 30.00 mA        | $(255/255) \times 600 \times 1.23V/R_{ISET}$                   |   |

## EEPROM Address 1

Address A1h

| EEPROM ADDRESS 1 register |     |                 |                                                            |   |            |   |   |
|---------------------------|-----|-----------------|------------------------------------------------------------|---|------------|---|---|
| 7                         | 6   | 5               | 4                                                          | 3 | 2          | 1 | 0 |
| BOOST_FREQ[1:0]           |     | EN_PWM_&_I_CTRL | TEMP_LIM[1:0]                                              |   | SLOPE[2:0] |   |   |
| Name                      | Bit | Access          | Description                                                |   |            |   |   |
| BOOST_FREQ                | 7:6 | R/W             | Boost Converter Switch Frequency                           |   |            |   |   |
|                           |     |                 | 00 = 156 kHz                                               |   |            |   |   |
|                           |     |                 | 01 = 312 kHz                                               |   |            |   |   |
|                           |     |                 | 10 = 625 kHz                                               |   |            |   |   |
|                           |     |                 | 11 = 1250 kHz                                              |   |            |   |   |
| EN_PWM_&_I_CTRL           | 5   | R/W             | Enable PWM & current control                               |   |            |   |   |
|                           |     |                 | 0 = PWM control used with constant current                 |   |            |   |   |
|                           |     |                 | 1 = Automatic PWM & current control enabled                |   |            |   |   |
| TEMP_LIM                  | 4:3 | R/W             | Thermal deration function temperature threshold            |   |            |   |   |
|                           |     |                 | 00 = thermal deration function disabled                    |   |            |   |   |
|                           |     |                 | 01 = 110°C                                                 |   |            |   |   |
|                           |     |                 | 10 = 120°C                                                 |   |            |   |   |
|                           |     |                 | 11 = 130°C                                                 |   |            |   |   |
| SLOPE                     | 2:0 | R/W             | Slope time for brightness change                           |   |            |   |   |
|                           |     |                 | 000 = Slope function disabled, immediate brightness change |   |            |   |   |
|                           |     |                 | 001 = 50 ms                                                |   |            |   |   |
|                           |     |                 | 010 = 75 ms                                                |   |            |   |   |
|                           |     |                 | 011 = 100 ms                                               |   |            |   |   |
|                           |     |                 | 100 = 150 ms                                               |   |            |   |   |
|                           |     |                 | 101 = 200 ms                                               |   |            |   |   |
|                           |     |                 | 110 = 300 ms                                               |   |            |   |   |
|                           |     |                 | 111 = 500 ms                                               |   |            |   |   |

**EEPROM Address 2**

Address A2h

| EEPROM ADDRESS 2 register |     |           |                                                                                                                                                                                                                                                                                 |          |          |            |            |
|---------------------------|-----|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|------------|------------|
| 7                         | 6   | 5         | 4                                                                                                                                                                                                                                                                               | 3        | 2        | 1          | 0          |
| ADAPTIVE_SPEED[1:0]       |     | ADV_SLOPE | MODE_25/50_SEL                                                                                                                                                                                                                                                                  | EN_ADAPT | EN_BOOST | BOOST_IMAX | I_SLOPE[1] |
| Name                      | Bit | Access    | Description                                                                                                                                                                                                                                                                     |          |          |            |            |
| ADAPTIVE_SPEED[1]         | 7   | R/W       | Boost converter adaptive control speed adjustment                                                                                                                                                                                                                               |          |          |            |            |
|                           |     |           | 0 = Normal mode                                                                                                                                                                                                                                                                 |          |          |            |            |
|                           |     |           | 1 = Adaptive mode optimized for light loads. Activating this helps the voltage droop with light loads during boost / backlight startup.                                                                                                                                         |          |          |            |            |
| ADAPTIVE_SPEED[0]         | 6   | R/W       | Boost converter adaptive control speed adjustment                                                                                                                                                                                                                               |          |          |            |            |
|                           |     |           | 0 = Adjust boost once for each phase shift cycle or normal PWM cycle                                                                                                                                                                                                            |          |          |            |            |
|                           |     |           | 1 = Adjust boost every 16th phase shift cycle or normal PWM cycle                                                                                                                                                                                                               |          |          |            |            |
| ADV_SLOPE                 | 5   | R/W       | Advanced slope                                                                                                                                                                                                                                                                  |          |          |            |            |
|                           |     |           | 0 = Advanced slope is disabled                                                                                                                                                                                                                                                  |          |          |            |            |
|                           |     |           | 1 = Use advanced slope for brightness change to make brightness changes smooth for eye                                                                                                                                                                                          |          |          |            |            |
| MODE_25/50_SEL            | 4   | R/W       | 25% or 50% mode selection for PWM & current control                                                                                                                                                                                                                             |          |          |            |            |
|                           |     |           | 0 = 50% mode selected                                                                                                                                                                                                                                                           |          |          |            |            |
|                           |     |           | 1 = 25% mode selected                                                                                                                                                                                                                                                           |          |          |            |            |
| EN_ADAPT                  | 3   | R/W       | Enable boost converter adaptive mode                                                                                                                                                                                                                                            |          |          |            |            |
|                           |     |           | 0 = adaptive mode disabled, boost converter output voltage is set with VBOOST EEPROM register bits                                                                                                                                                                              |          |          |            |            |
|                           |     |           | 1 = adaptive mode enabled. Boost converter startup voltage is set with VBOOST EEPROM register bits, and after startup voltage is reached the boost converter will adapt to the highest LED string $V_F$ . LED driver output headroom is set with DRV_HEADR EEPROM control bits. |          |          |            |            |
| EN_BOOST                  | 2   | R/W       | Enable boost converter                                                                                                                                                                                                                                                          |          |          |            |            |
|                           |     |           | 0 = boost is disabled                                                                                                                                                                                                                                                           |          |          |            |            |
|                           |     |           | 1 = boost is enabled and will turn on automatically when backlight is enabled                                                                                                                                                                                                   |          |          |            |            |
| BOOST_IMAX                | 1   | R/W       | Boost converter inductor maximum current                                                                                                                                                                                                                                        |          |          |            |            |
|                           |     |           | 0 = 1.4A                                                                                                                                                                                                                                                                        |          |          |            |            |
|                           |     |           | 1 = 2.5A (recommended)                                                                                                                                                                                                                                                          |          |          |            |            |
| I_SLOPE[1]                | 0   | R/W       | Current slope I_SLOPE[1:0] trim bits adjust the constant current level of the PWM control range in the PWM & current control mode                                                                                                                                               |          |          |            |            |
|                           |     |           | I_SLOPE[1:0]                                                                                                                                                                                                                                                                    | 25% MODE | 50% MODE |            |            |
|                           |     |           | 00                                                                                                                                                                                                                                                                              | –2.5%    | –1.25%   |            |            |
|                           |     |           | 01                                                                                                                                                                                                                                                                              | –5.0%    | –2.50%   |            |            |
|                           |     |           | 10                                                                                                                                                                                                                                                                              | –7.5%    | –3.75%   |            |            |
|                           |     |           | 11                                                                                                                                                                                                                                                                              | –10.0%   | –5.00%   |            |            |

**EEPROM Address 3**

Address A3h

| EEPROM ADDRESS 3 register |     |          |               |   |   |   |   |
|---------------------------|-----|----------|---------------|---|---|---|---|
| 7                         | 6   | 5        | 4             | 3 | 2 | 1 | 0 |
| UVLO[1:0]                 |     | EN_PSPWM | PWM_FREQ[4:0] |   |   |   |   |
| Name                      | Bit | Access   | Description   |   |   |   |   |

| EEPROM ADDRESS 3 register |     |     |                                                                                                                                      |
|---------------------------|-----|-----|--------------------------------------------------------------------------------------------------------------------------------------|
| UVLO                      | 7:6 | R/W | 00 = Disabled                                                                                                                        |
|                           |     |     | 01 = 2.7V                                                                                                                            |
|                           |     |     | 10 = 5.4V                                                                                                                            |
|                           |     |     | 11 = 8.1V                                                                                                                            |
| EN_PSPWM                  | 5   | R/W | Enable phase shift PWM scheme                                                                                                        |
|                           |     |     | 0 = phase shift PWM disabled, normal PWM mode used                                                                                   |
|                           |     |     | 1 = phase shift PWM enabled                                                                                                          |
| PWM_FREQ                  | 4:0 | R/W | PWM output frequency setting. See table in <a href="#">PWM Frequency Setting</a> for full description of selectable PWM frequencies. |

## EEPROM Address 4

Address A4h

| EEPROM ADDRESS 4 register |     |          |                                                                                                                                                                                                          |            |                |   |   |
|---------------------------|-----|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|----------------|---|---|
| 7                         | 6   | 5        | 4                                                                                                                                                                                                        | 3          | 2              | 1 | 0 |
| PWM_RESOLUTION[1:0]       |     | EN_I_RES | LED_FAULT_THR                                                                                                                                                                                            | I_SLOPE[0] | DRV_HEADR[2:0] |   |   |
| Name                      | Bit | Access   | Description                                                                                                                                                                                              |            |                |   |   |
| PWM RESOLUTION            | 7:6 | R/W      | PWM output resolution selection. Actual resolution depends also on the output frequency. See <a href="#">PWM Frequency Setting</a> for full description.                                                 |            |                |   |   |
|                           |     |          | 00 = 8...10 bits (19.2 kHz...4.8 kHz)                                                                                                                                                                    |            |                |   |   |
|                           |     |          | 01 = 9...11 bits (19.2 kHz... 4.8 kHz)                                                                                                                                                                   |            |                |   |   |
|                           |     |          | 10 = 10...12 bits (19.2 kHz...4.8 kHz)                                                                                                                                                                   |            |                |   |   |
|                           |     |          | 11 = 11...13 bits (19.2 kHz...4.8 kHz)                                                                                                                                                                   |            |                |   |   |
| EN_I_RES                  | 5   | R/W      | Enable LED current set resistor                                                                                                                                                                          |            |                |   |   |
|                           |     |          | 0 = Resistor is disabled and current is set only with CURRENT EEPROM register bits                                                                                                                       |            |                |   |   |
|                           |     |          | 1 = Enable LED current set resistor. LED current is defined by the R <sub>IS</sub> <sub>ET</sub> resistor and the CURRENT EEPROM register bits.                                                          |            |                |   |   |
| LED_FAULT_T<br>HR         | 4   | R/W      | LED fault detector thresholds. V <sub>SAT</sub> is the saturation voltage of the driver, typically 200 mV.                                                                                               |            |                |   |   |
|                           |     |          | 0 = 3.3V                                                                                                                                                                                                 |            |                |   |   |
|                           |     |          | 1 = 5.3V                                                                                                                                                                                                 |            |                |   |   |
| I_SLOPE[0]                | 3   | R/W      | Current slope I_SLOPE[1:0] trim bits adjust the constant current level of PWM control range in the PWM & current control mode. See I_SLOPE[1] bit description in <a href="#">EEPROM Address 2</a> table. |            |                |   |   |
| DRV_HEADR                 | 2:0 | R/W      | LED output driver headroom control. V <sub>SAT</sub> is the saturation voltage of the driver, typically 200 mV.                                                                                          |            |                |   |   |
|                           |     |          | 000 = V <sub>SAT</sub> + 125 mV                                                                                                                                                                          |            |                |   |   |
|                           |     |          | 001 = V <sub>SAT</sub> + 250 mV                                                                                                                                                                          |            |                |   |   |
|                           |     |          | 010 = V <sub>SAT</sub> + 375 mV                                                                                                                                                                          |            |                |   |   |
|                           |     |          | 011 = V <sub>SAT</sub> + 500 mV                                                                                                                                                                          |            |                |   |   |
|                           |     |          | 100 = V <sub>SAT</sub> + 625 mV                                                                                                                                                                          |            |                |   |   |
|                           |     |          | 101 = V <sub>SAT</sub> + 750 mV                                                                                                                                                                          |            |                |   |   |
|                           |     |          | 110 = V <sub>SAT</sub> + 875 mV                                                                                                                                                                          |            |                |   |   |
|                           |     |          | 111 = V <sub>SAT</sub> + 1000 mV                                                                                                                                                                         |            |                |   |   |

## EEPROM Address 5

Address A5h

| EEPROM ADDRESS 5 register |             |   |             |   |   |   |   |
|---------------------------|-------------|---|-------------|---|---|---|---|
| 7                         | 6           | 5 | 4           | 3 | 2 | 1 | 0 |
| EN_VSYNC                  | DITHER[1:0] |   | VBOOST[4:0] |   |   |   |   |

| EEPROM ADDRESS 5 register |     |        |                                                                                                                                                                                                                                                        |
|---------------------------|-----|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name                      | Bit | Access | Description                                                                                                                                                                                                                                            |
| EN_VSYNC                  | 7   | R/W    | Enable V <sub>SYNC</sub> function                                                                                                                                                                                                                      |
|                           |     |        | 0 = V <sub>SYNC</sub> input disabled                                                                                                                                                                                                                   |
|                           |     |        | 1 = V <sub>SYNC</sub> input enabled. V <sub>SYNC</sub> signal is used by the internal PLL to generate PWM output and boost frequency.                                                                                                                  |
| DITHER                    | 6:5 | R/W    | Dither function controls                                                                                                                                                                                                                               |
|                           |     |        | 00 = Dither function disabled                                                                                                                                                                                                                          |
|                           |     |        | 01 = 1-bit dither used for output PWM transitions                                                                                                                                                                                                      |
|                           |     |        | 10 = 2-bit dither used for output PWM transitions                                                                                                                                                                                                      |
|                           |     |        | 11 = 3-bit dither used for output PWM transitions                                                                                                                                                                                                      |
| VBOOST                    | 4:0 | R/W    | Boost voltage control from 10V to 40V with 1V step. If adaptive boost control is enabled, this sets the initial start voltage for the boost converter. If adaptive mode is disabled, this will directly set the output voltage of the boost converter. |
|                           |     |        | 0 0000 = 10V                                                                                                                                                                                                                                           |
|                           |     |        | 0 0001 = 11V                                                                                                                                                                                                                                           |
|                           |     |        | 0 0010 = 12V                                                                                                                                                                                                                                           |
|                           |     |        | ...                                                                                                                                                                                                                                                    |
|                           |     |        | 1 1101 = 39V                                                                                                                                                                                                                                           |
|                           |     |        | 1 1110 = 40V                                                                                                                                                                                                                                           |
|                           |     |        | 1 1111 = 40V                                                                                                                                                                                                                                           |

## EEPROM Address 6

Address A6h

| EEPROM ADDRESS 6 register |     |        |                                                                                                                                 |   |   |   |   |
|---------------------------|-----|--------|---------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|
| 7                         | 6   | 5      | 4                                                                                                                               | 3 | 2 | 1 | 0 |
| PLL[12:5]                 |     |        |                                                                                                                                 |   |   |   |   |
| Name                      | Bit | Access | Description                                                                                                                     |   |   |   |   |
| PLL                       | 7:0 | R/W    | 13-bit counter value for PLL, 8 MSB bits. PLL[12:0] bits are used when en_vsync = 1. See table below for PLL value calculation. |   |   |   |   |

## EEPROM Address 7

Address A7h

| EEPROM ADDRESS 7 register |     |        |                                                                                                                                                                                                |   |          |                 |   |
|---------------------------|-----|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|----------|-----------------|---|
| 7                         | 6   | 5      | 4                                                                                                                                                                                              | 3 | 2        | 1               | 0 |
| PLL[4:0]                  |     |        |                                                                                                                                                                                                |   | EN_F_RES | HYSTERESIS[1:0] |   |
| Name                      | Bit | Access | Description                                                                                                                                                                                    |   |          |                 |   |
| PLL                       | 7:3 | R/W    | 13-bit counter value for PLL, 5 LSB bits. PLL[12:0] bits are used when en_vsync = 1. See table below for PLL value calculation.                                                                |   |          |                 |   |
| EN_F_RES                  | 2   | R/W    | Enable PWM output frequency set resistor                                                                                                                                                       |   |          |                 |   |
|                           |     |        | 0 = Resistor is disabled and PWM output frequency is set with PWM_FREQ EEPROM register bits                                                                                                    |   |          |                 |   |
|                           |     |        | 1 = PWM frequency set resistor is enabled. R <sub>FSET</sub> defines the output PWM frequency. See table in <a href="#">PWM Frequency Setting</a> for full description of the PWM frequencies. |   |          |                 |   |
| HYSTERESIS                | 1:0 | R/W    | PWM input hysteresis function. Will define how small changes in the PWM input are ignored to remove constant switching between two values.                                                     |   |          |                 |   |
|                           |     |        | 00 = OFF                                                                                                                                                                                       |   |          |                 |   |
|                           |     |        | 01 = 1-bit hysteresis with 11-bit resolution                                                                                                                                                   |   |          |                 |   |
|                           |     |        | 10 = 1-bit hysteresis with 10-bit resolution                                                                                                                                                   |   |          |                 |   |
|                           |     |        | 11 = 1-bit hysteresis with 8-bit resolution                                                                                                                                                    |   |          |                 |   |

**Table 4. PLL Value Calculation**

| en_vsync | PLL frequency [MHz] | PLL[12:0]                            |
|----------|---------------------|--------------------------------------|
| 0        | 5, 10, 20, 40       | not used                             |
| 1        | 5                   | 5 MHz / (26 x f <sub>VSYNC</sub> )   |
|          | 10                  | 10 MHz / (50 x f <sub>VSYNC</sub> )  |
|          | 20                  | 20 MHz / (98 x f <sub>VSYNC</sub> )  |
|          | 40                  | 40 MHz / (196 x f <sub>VSYNC</sub> ) |

PLL frequency is set by PWM\_RESOLUTION[1:0] bits.

For Example:

If f<sub>PLL</sub> = 5 MHz and f<sub>VSYNC</sub> = 60 Hz, then PLL[12:0] = 5000000 Hz / (26 \* 60 Hz) = 3205d = C85h.

If f<sub>PLL</sub> = 10 MHz and f<sub>VSYNC</sub> = 75 Hz, then PLL[12:0] = 10000000 Hz / (50 \* 75 Hz) = 2667d = A6Bh.

## REVISION HISTORY

| Changes from Original (May 2013) to Revision B | Page               |
|------------------------------------------------|--------------------|
| • Added note re: EEPROM configuration .....    | <a href="#">18</a> |
| • Added note re: EEPROM configuration .....    | <a href="#">30</a> |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP8553TLE/NOPB   | ACTIVE        | DSBGA        | YZR                | 25   | 250            | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -30 to 85    | 8553                    | <a href="#">Samples</a> |
| LP8553TLX/NOPB   | ACTIVE        | DSBGA        | YZR                | 25   | 3000           | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -30 to 85    | 8553                    | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

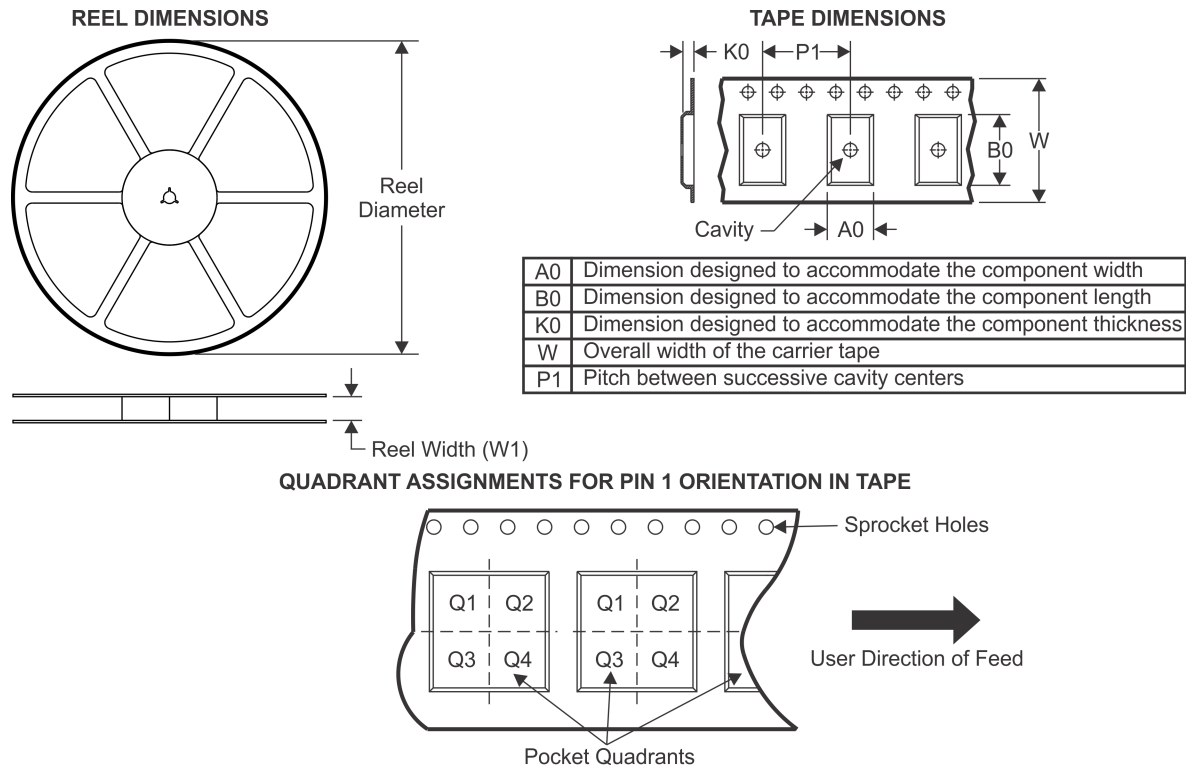
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

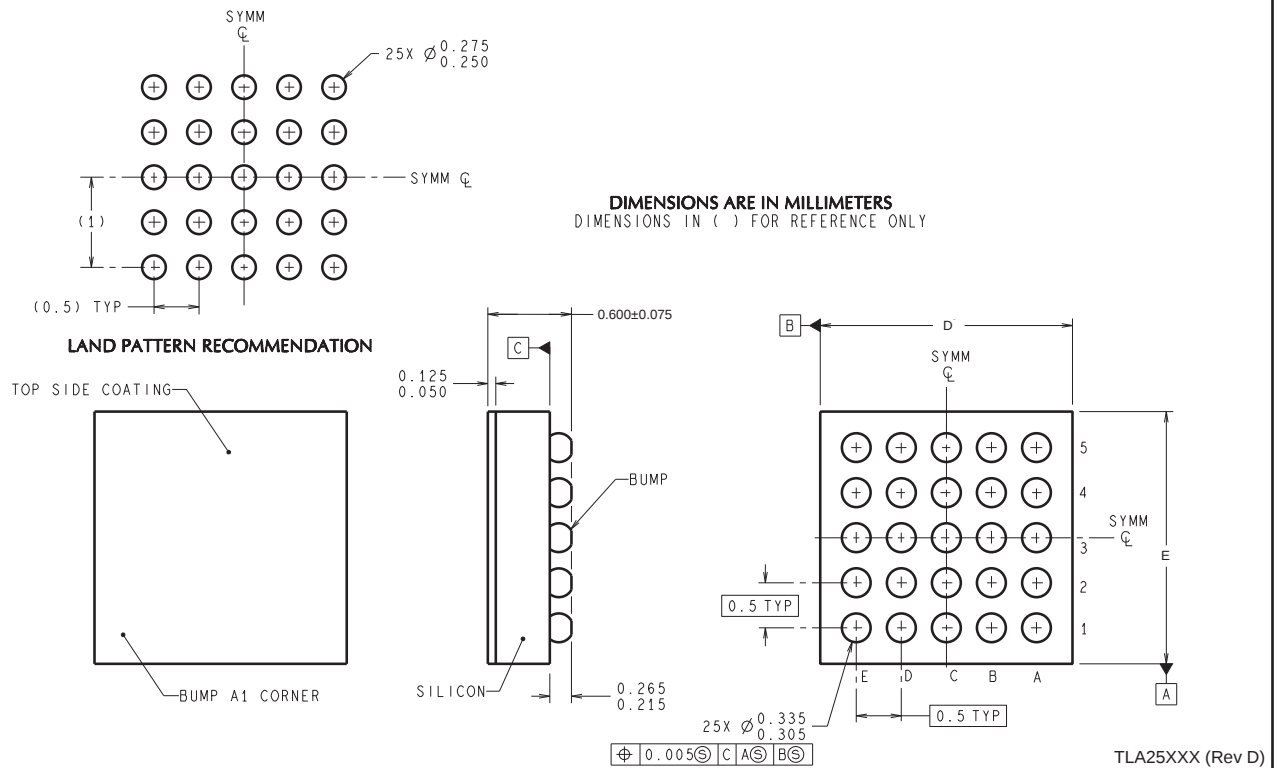
| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP8553TLE/NOPB | DSBGA        | YZR             | 25   | 250  | 178.0              | 8.4                | 2.69    | 2.69    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8553TLX/NOPB | DSBGA        | YZR             | 25   | 3000 | 178.0              | 8.4                | 2.69    | 2.69    | 0.76    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP8553TLE/NOPB | DSBGA        | YZR             | 25   | 250  | 208.0       | 191.0      | 35.0        |
| LP8553TLX/NOPB | DSBGA        | YZR             | 25   | 3000 | 208.0       | 191.0      | 35.0        |



D: Max = 2.49 mm, Min = 2.43 mm

E: Max = 2.49 mm, Min = 2.43 mm

4215055/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

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