

TCA39306 双向 I²C 总线和 SMBus 电压电平转换器

1 特性

- 适用于混合模式 I²C 应用中 SDA 和 SCL 线路的 2 位双向转换器
- 标准模式、快速模式和快速模式增强版 I²C 与 SMBus 兼容
- 与 I³C 兼容 (支持 12.5MHz)
- 可实现以下电压之间的电压电平转换
 - 0.9V V_{REF1} 和 1.8V、2.5V、3.3V 或 5V V_{REF2}
 - 1.2V V_{REF1} 和 1.8V、2.5V、3.3V 或 5V V_{REF2}
 - 1.8V V_{REF1} 和 2.5V、3.3V 或 5V V_{REF2}
 - 2.5V V_{REF1} 和 3.3V 或 5V V_{REF2}
 - 3.3V V_{REF1} 和 5V V_{REF2}
- 在无方向引脚的情况下提供双向电压转换
- 输入和输出端口之间的低导通电阻提供更少的信号失真
- 漏极开路 I²C I/O 端口 (SCL1、SDA1、SCL2 和 SDA2)
- 5V 耐压 I²C 和 I/O 端口可支持混合模式信号操作
- 针对 EN 为低电平的高阻抗 SCL1、SDA1、SCL2 和 SDA2 引脚
- 无闭锁操作可在 EN 为低电平时实现隔离
- 采用直通引脚排列以简化印刷电路板布线
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体模型 (A114-A)
 - 1000V 充电器件模型 (C101)

2 应用

- I²C、SMBus、PMBus、MDIO、UART、低速 SDIO、GPIO 和其他双信号接口
- 服务器
- 路由器 (电信交换设备)
- 个人计算机
- 工业自动化

3 说明

TCA39306 是一款采用使能 (EN) 输入的双路双向电压电平转换器, 与 I²C、SMBus 和 I³C 兼容, 可在 0.9V 至 3.3V V_{REF1} 和 1.8V 至 5.5V V_{REF2} 的范围内工作。

该器件可以在 0.85V 到 5V 之间实现双向电压转换而无须使用方向引脚。此开关具有低导通状态电阻 (R_{ON}), 可以在最短传播延迟情况下建立连接。当 EN 为高电平时, 转换器开关打开, 并且 SCL1 和 SDA1 I/O 被分别连接至 SCL2 和 SDA2 I/O, 从而实现端口间的双向数据流。当 EN 为低电平时, 转换器开关关闭, 在端口之间存在一个高阻态。

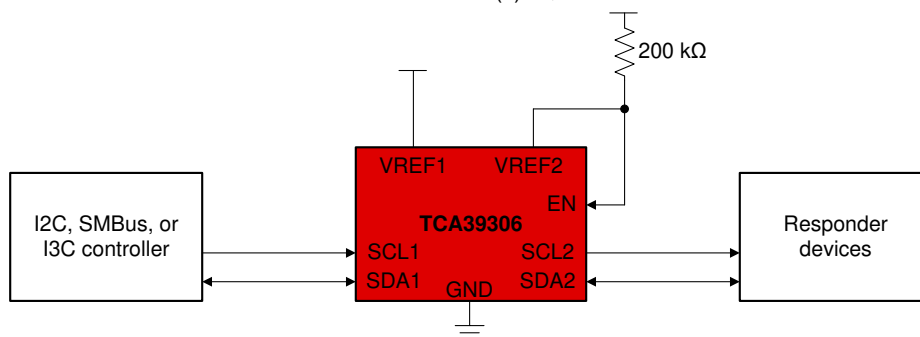
除了电压转换, TCA39306 还可用于将更高速度的总线与更低速度的总线隔离, 方法是在快速模式通信过程中控制 EN 引脚以断开较慢总线的连接。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TCA39306	VSSOP (8)	2.30mm x 2.00mm
	SOT-23 (8) ⁽²⁾	2.90mm x 1.60mm
	X2SON (8)	1.35mm x 0.80mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

(2) 产品预览



简化版应用示意图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2021) to Revision A (August 2021)	Page
• 将文件从 <i>預告信息</i> 更改为 <i>量产数据</i>	1

5 Pin Configuration and Functions

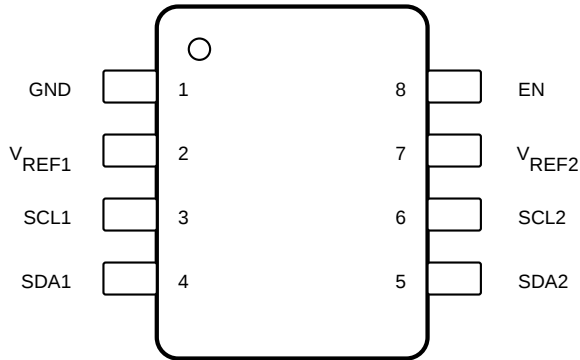


图 5-1. DDF Package, 8-Pin SOT, Top View

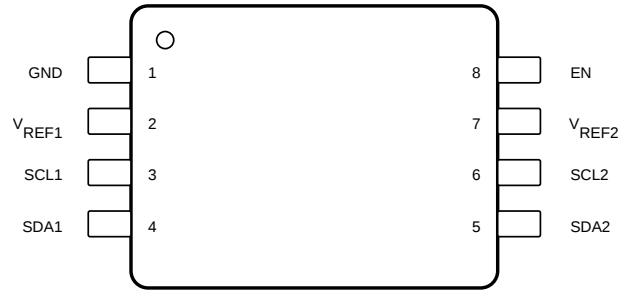
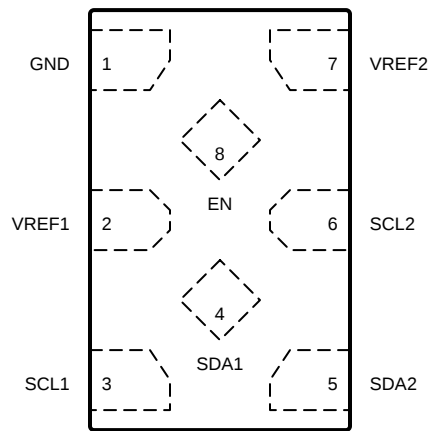


图 5-2. DCU Package, 8-Pin VSSOP, Top View



Not to scale

图 5-3. DTM Package, 8-Pin X2SON, Top View

表 5-1. Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	DCU, DDF	DTM		
EN	8	8	I	Switch enable input
GND	1	1	—	Ground, 0 V
SCL1	3	3	I/O	Serial clock, low-voltage side
SCL2	6	6	I/O	Serial clock, high-voltage side
SDA1	4	4	I/O	Serial data, low-voltage side
SDA2	5	5	I/O	Serial data, high-voltage side
VREF1	2	2	I	Low-voltage-side reference supply voltage for SCL1 and SDA1
VREF2	7	7	I	High-voltage-side reference supply voltage for SCL2 and SDA2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{REF1}	DC reference voltage range	- 0.5	7	V
V _{REF2}	DC reference bias voltage range	- 0.5	7	V
V _I	Input voltage range ⁽²⁾	- 0.5	7	V
V _{I/O}	Input-output voltage range ⁽²⁾	- 0.5	7	V
	Continuous channel current		128	mA
I _{IK}	Input Clamp Current (V _I < 0)		- 50	mA
T _{J(Max)}	Junction temperature		150	°C
T _{stg}	Storage temperature	- 65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and input-output negative voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{I/O}	Input-output voltage	SCL1, SDA1, SCL2, SDA2	0	5.5	V
V _{REF1} ⁽¹⁾	Reference Voltage		0	5.5	V
V _{REF2} ⁽¹⁾	Reference Voltage		0	5.5	V
EN-Switch ⁽²⁾	Switch mode enable voltage (Switch mode enable voltage)		1.5	5.5	V
EN	Enable input voltage		0	5.5	V
I _{PASS}	Pass switch current			64	mA
T _A	Ambient temperature		- 40	125	°C

- (1) To support translation, V_{REF1} supports 0.85 V to V_{REF2} - 0.6 V. V_{REF2} must be between V_{REF1} + 0.6 V to 5.5 V. See Typical Application for more information.
- (2) To support switching, V_{REF1} and V_{REF2} Do not need to be connected. EN pin should use a voltage not less than 1.5V when the switch mode is to be enabled. Enabled voltage on this pin should be equal to 1.5V or I/O supply voltage, whichever is higher.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TCA39306		UNIT
		DCU	DTM	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	275.5	289.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.1	185.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	186.9	193.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	65.7	27.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	185.9	193.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$	$EN = 0 \text{ V}$		-1.2	0		V	
I_{IH}	Input leakage current	$V_I = 5 \text{ V}, V_O = 0 \text{ V}$	$EN = 0 \text{ V}$			5		μA	
V_T	Threshold voltage	$I_O = 500 \mu\text{A}$	$V_I = 0.1 \text{ V}, V_O = 0 \text{ V}$, Find V_{EN} where $I_O = 500 \mu\text{A}$			0.7	1.0	V	
$C_{I(EN)}$	Input capacitance	$V_I = 3 \text{ V}$ or 0 V				11		pF	
$C_{IO(off)}$	Off capacitance	SCLn, SDAn $V_O = 3 \text{ V}$ or 0 V	$EN = 0 \text{ V}$			4	6	pF	
$C_{IO(on)}$	On capacitance	SCLn, SDAn $V_O = 3 \text{ V}$ or 0 V	$EN = 3 \text{ V}$			10.5	12.5	pF	
$R_{ON}^{(2)}$	On-state resistance	SCLn, SDAn (-40 to 125C)	$V_I = 0 \text{ V}^{(3)}$	$I_O = 64 \text{ mA}$	$EN = 4.5 \text{ V}$	3.5	5.5	Ω	
			$V_I = 0 \text{ V}^{(3)}$	$I_O = 64 \text{ mA}$	$EN = 3 \text{ V}$	4.7	7	Ω	
			$V_I = 0 \text{ V}^{(3)}$	$I_O = 64 \text{ mA}$	$EN = 2.3 \text{ V}$	6.3	9.5	Ω	
			$V_I = 0 \text{ V}^{(3)}$	$I_O = 15 \text{ mA}$	$EN = 1.5 \text{ V}$	25.5	32	Ω	
			$V_I = 2.4 \text{ V}^{(4)}$	$I_O = 15 \text{ mA}$	$EN = 4.5 \text{ V}$	1	6	15	Ω
			$V_I = 2.4 \text{ V}^{(4)}$	$I_O = 15 \text{ mA}$	$EN = 3 \text{ V}$	20	50	75	Ω
			$V_I = 1.7 \text{ V}^{(4)}$	$I_O = 15 \text{ mA}$	$EN = 2.3 \text{ V}$	20	55	75	Ω

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP (1)	MAX	UNIT
R _{ON}	On-state resistance	SCLn, SDAn	V _I = 0 V, V _{CC2} = 5 V ⁽⁵⁾	I _O = 64 mA	V _{CC1} = 1 V		5	25	Ω
					V _{CC1} = 1.8 V		4	10	
					V _{CC1} = 2.5 V		3	8	
					V _{CC1} = 3.3 V		3	7	
				I _O = 32 mA	V _{CC1} = 1 V		5	10	Ω
					V _{CC1} = 1.8 V		4	9	
					V _{CC1} = 2.5 V		3	8	
					V _{CC1} = 3.3 V		3	7	
			V _I = 1.8 V, V _{CC2} = 5 V ⁽⁵⁾	I _O = 15 mA	V _{CC1} = 3.3 V		4	13	Ω
			V _I = 1 V, V _{CC2} = 3.3 V ⁽⁵⁾	I _O = 10 mA	V _{CC1} = 1.8 V		7	24	Ω
V _I = 0 V, V _{CC2} = 3.3 V ⁽⁵⁾	I _O = 10 mA	V _{CC1} = 1 V		5	18	Ω			
V _I = 0 V, V _{CC2} = 1.8 V ⁽⁵⁾	I _O = 10 mA	V _{CC1} = 1 V		6	19	Ω			

(1) All typical values are at T_A = 25°C.

(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two terminals.

(3) Measured in current source configuration only. See [图 7-1](#)

(4) Measured in current sink configuration only. See [图 7-1](#)

(5) Measured in application connected current source configuration only. See [图 7-2](#)

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T _{PLH}	Low-to-high propagation delay ⁽¹⁾	V _{CC1} = 0.85 V, V _{CC2} = 1.98 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			13	ns
			C _L = 50 pF			32	
		V _{CC1} = 0.85 V, V _{CC2} = 3.6 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			15	ns
			C _L = 50 pF			45	
		V _{CC1} = 0.85 V, V _{CC2} = 5.5 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			20	ns
			C _L = 50 pF			46	
		V _{CC1} = 1.65 V, V _{CC2} = 3.6 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			8	ns
			C _L = 50 pF			20	
		V _{CC1} = 1.65 V, V _{CC2} = 5.5 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			15	ns
			C _L = 50 pF			35	
		V _{CC1} = 3 V, V _{CC2} = 5.5 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			2	ns
			C _L = 50 pF			5	

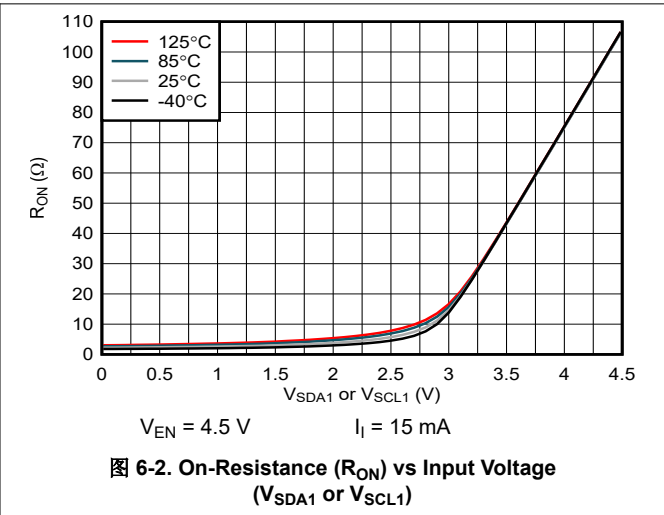
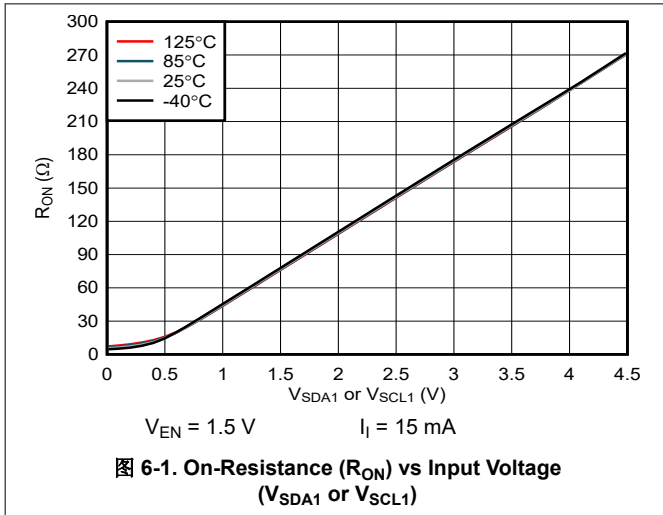
6.6 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
T _{PHL}	High-to-low propagation delay ⁽¹⁾	V _{CC1} = 0.85 V, V _{CC2} = 1.98 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			3	ns	
			C _L = 50 pF			4		
		V _{CC1} = 0.85 V, V _{CC2} = 3.6 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			3	ns	
			C _L = 50 pF			5		
		V _{CC1} = 0.85 V, V _{CC2} = 5.5 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			3	ns	
			C _L = 50 pF			5		
		V _{CC1} = 1.65 V, V _{CC2} = 3.6 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			2	ns	
			C _L = 50 pF			3		
		V _{CC1} = 1.65 V, V _{CC2} = 5.5 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF			3	ns	
			C _L = 50 pF			3		
		V _{CC1} = 3 V, V _{CC2} = 5.5 V, R _{L_Input} = 1.35 kΩ	C _L = 15 pF				1.5	ns
			C _L = 50 pF				2	

(1) Measured with an application propagation delay setup. See [图 7-3](#)

6.7 Typical Characteristics



7 Parameter Measurement Information

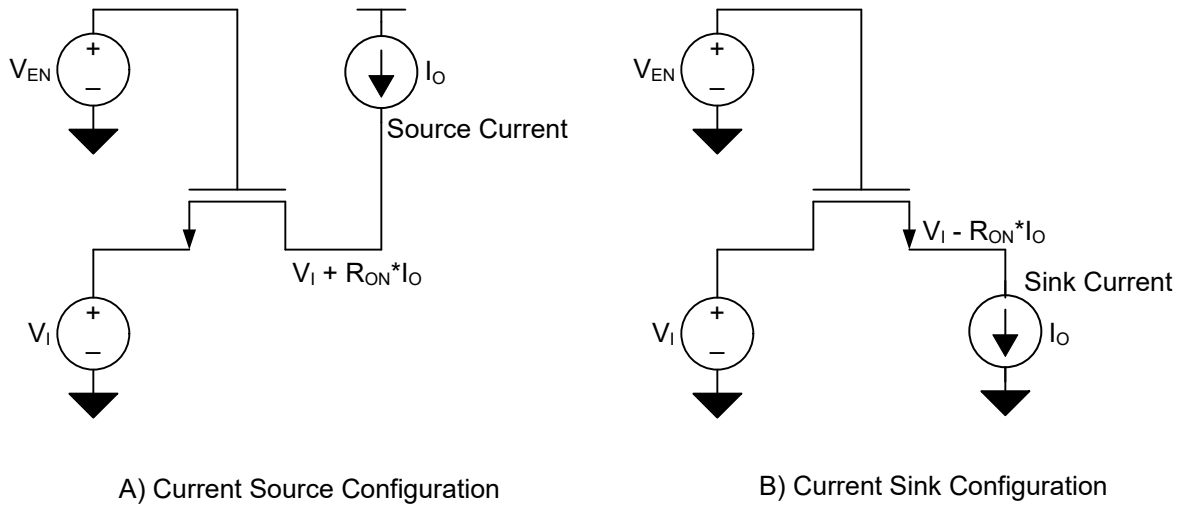


图 7-1. Current Source and Current Sink Configurations for Direct R_{ON} Measurements

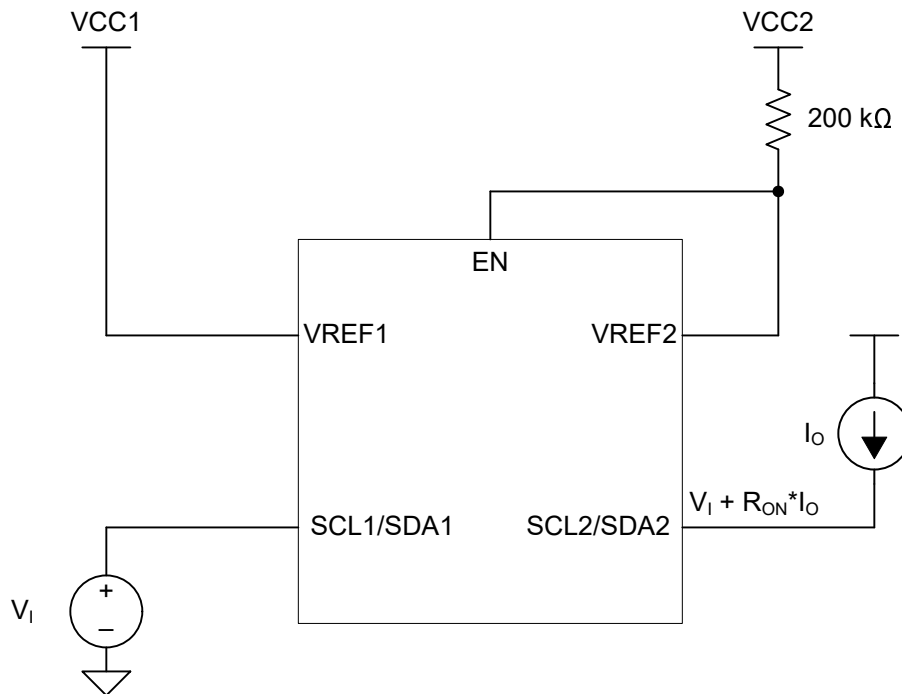


图 7-2. Application Setup for R_{ON} Delay

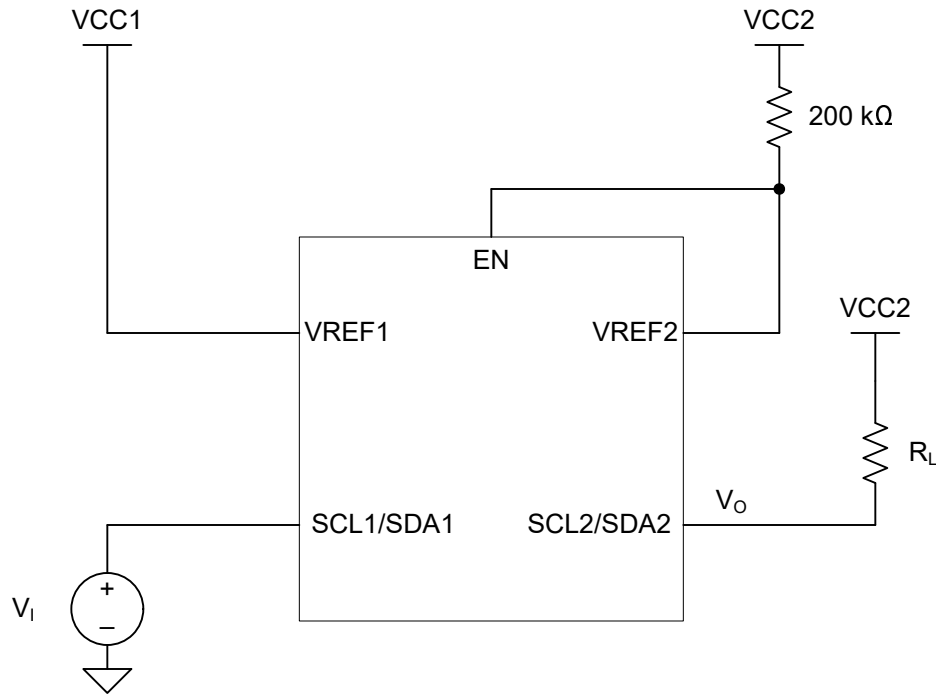
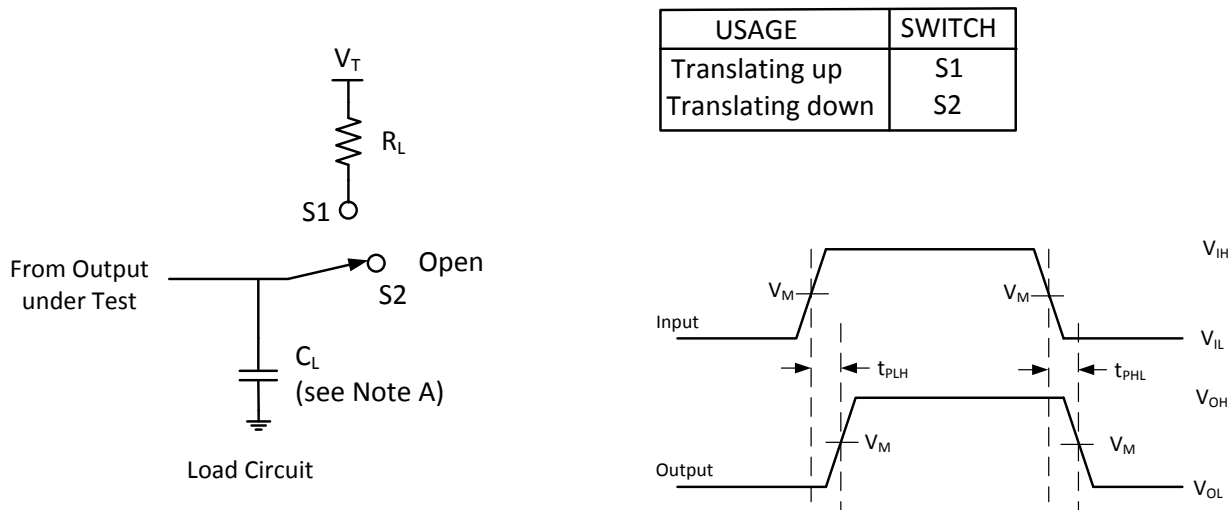


图 7-3. Application Setup for Propagation Delays Delay



USAGE	SWITCH
Translating up	S1
Translating down	S2

- NOTES: A. C_L includes probe and jig capacitance
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.

图 7-4. Load Circuit for Outputs

8 Detailed Description

8.1 Overview

The TCA39306 is a dual bidirectional voltage-level translator compatible with I²C, SMBus, and I³C with an enable (EN) input, and is operational from 0.9-V to 3.3-V V_{REF1} and 1.8-V to 5.5-V V_{REF2} .

The device allows bidirectional voltage translations between 0.85 V and 5 V, without the use of a direction pin. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In addition to voltage translation, the TCA39306 can be used to isolate a higher speed bus from a lower speed bus by controlling the EN pin to disconnect the slower bus during fast-mode communication.

In I²C applications, the bus capacitance limit of 400 pF for Standard and Fast Modes, 550 pF for Fast Mode Plus restricts the number of devices and bus length. The capacitive load on both sides of the device must be taken into account when approximating the total load of the system, specifying the sum of both sides is under 400/550 pF.

Both the SDA and SCL channels of the device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete-transistor voltage-translation solutions, because the fabrication of the switch is symmetrical.

8.1.1 Definition of threshold voltage

This document references a threshold voltage denoted as V_{th} , which appears multiple times throughout this document when discussing the NFET between V_{REF1} and V_{REF2} . The value of V_{th} is approximately 0.6 V at room temperature.

8.1.2 Correct Device Set Up

In a normal set up shown in 图 8-1, the enable pin and V_{REF2} are shorted together and tied to a 200-k Ω resistor, and a reference voltage equal to V_{REF1} plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.

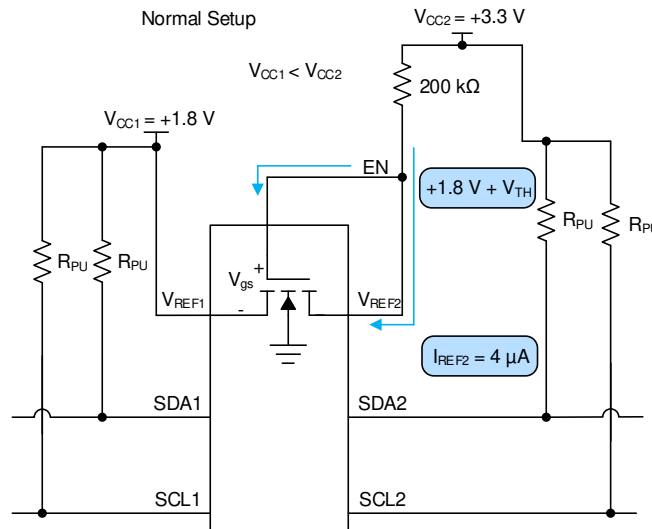


图 8-1. Normal Setup

Care should be taken to make sure V_{REF2} has an external resistor tied between it and V_{CC2} . If V_{REF2} is tied directly to the V_{CC2} rail without a resistor, then there is no external resistance from the V_{CC2} to V_{CC1} to limit the current such as in 图 8-2. This effectively looks like a low impedance path for current to travel through and

potentially break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in section 6.1. The continuous channel current is larger with a higher voltage difference between V_{CC1} and V_{CC2} .

图 8-2 shows an improper set up. If V_{CC2} is larger than V_{CC1} but less than V_{th} , the impedance between V_{CC1} and V_{CC2} is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when V_{CC2} becomes larger than V_{CC1} by V_{th} . During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.

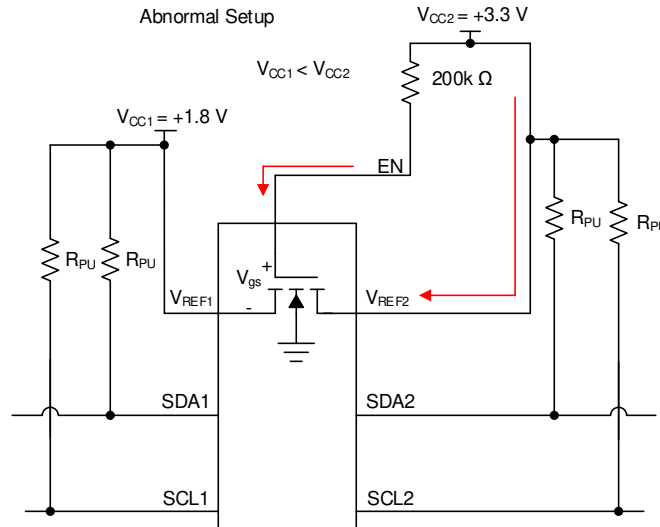


图 8-2. Abnormal Setup

8.1.3 Disconnecting a Responder from the Main Bus Using the EN Pin

TCA39306 can be used as a switch to disconnect one side of the device from the main bus, whether isolating I3C and I2C devices or different speed groups. This can be advantageous in multiple situations. One instance of this situation is if there are devices on the I2C bus which only supports fast mode (400 kHz) while other devices on the bus support fast mode plus (1 MHz). An example of this is displayed in 图 8-3.

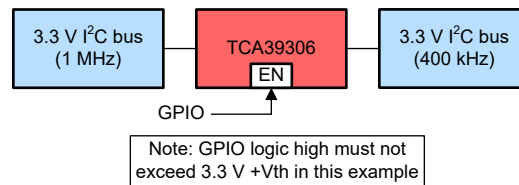


图 8-3. Example of an I2C bus with multiple supported frequencies

In this situation, if the controller is on the 1 MHz side then communicating at 1 MHz should not be attempted if TCA39306 were enabled. It needs to be disabled for the device to avoid possibly glitching state machines in devices which were designed to operate correctly at 400 kHz or slower. When the device is disabled, the controller can communicate with the 1 MHz devices without disturbing the 400 kHz bus. When the device is enabled, communication across both sides at 400 kHz is acceptable.

8.1.4 Supporting Remote Board Insertion to Backplane with TCA39306

Another situation where TCA39306 is advantageous when using its enable feature is when a remote board with I2C lines needs to be attached to a main board (backplane) with an I2C bus such as in 图 8-4. If connecting a remote board to a backplane is not done properly, the connection could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line. Which could glitch an I2C device state machine causing the I2C bus to get stuck.

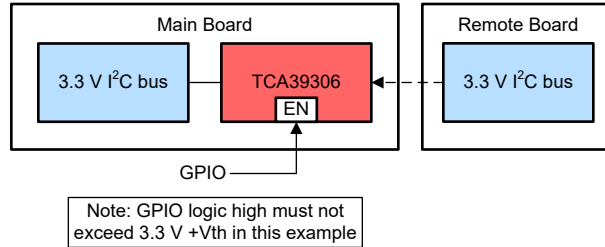


图 8-4. An example of connecting a remote board to a main board (backplane)

TCA39306 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

8.1.5 Switch Configuration

TCA39306 has the capability of being used with its V_{REF1} voltage equal to V_{REF2} . This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in 图 8-5 and translation mode is shown in 图 8-6.

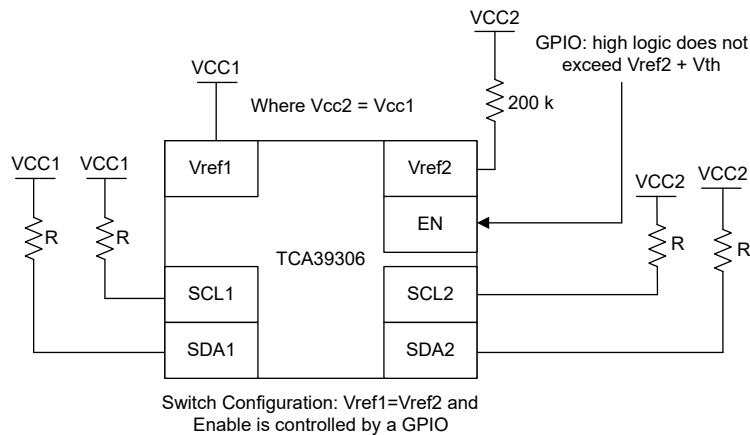


图 8-5. Switch Configuration

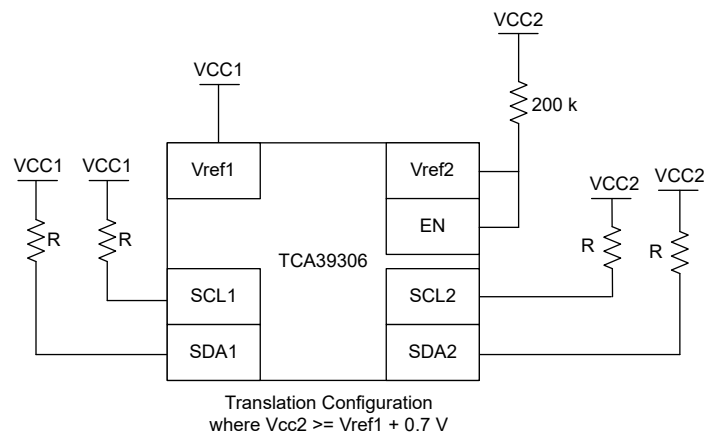


图 8-6. Translation Configuration

When TCA39306 is in the switch configuration ($V_{REF1} = V_{REF2}$), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the device has the same propagation delay from side one to two and side two to one. The propagation delays become lower when V_{CC1}/V_{CC2} is larger. For example, the propagation delay at 1.8 V is longer than at 5 V in the switching configuration. When the device is in translation

mode, side one propagate lows to side two faster than side two can propagate lows to side 1. This time difference becomes larger the larger the difference between V_{CC2} and V_{CC1} becomes.

8.1.6 Controller on Side 1 or Side 2 of Device

I2C and SMBus are bidirectional protocol meaning devices on the bus can both transmit and receive data. TCA39306 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the controller to be able to placed on either side of the device. 图 8-7 shows the controller on side two as opposed to the diagram on page 1 of this data sheet.

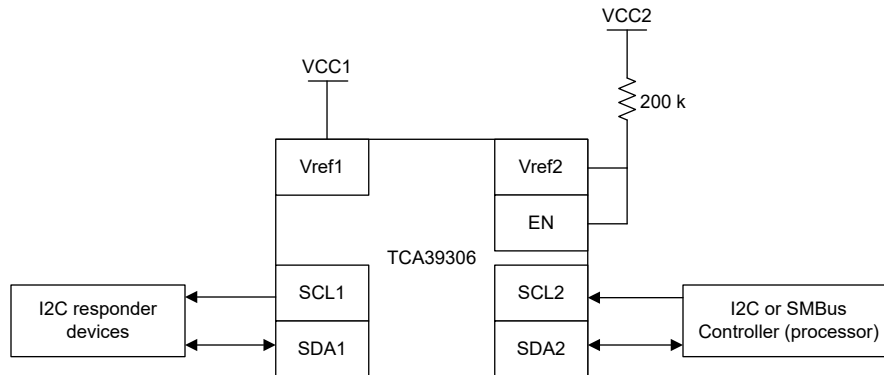


图 8-7. Controller on side 2

8.1.7 LDO and TCA39306 Concerns

The V_{REF1} pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO may lose its regulation because of the bias current from V_{REF2} to V_{REF1} . If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the V_{REF1} node (both external and parasitic). This results in an increase in voltage on the V_{REF1} node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the V_{REF1} node), then the V_{REF1} voltage ends up stabilizing when V_{gs} of the pass FET is equal to V_{th} . This means V_{REF1} node voltage is $V_{CC2} - V_{th}$. Note that any secondary or primaries running off of the LDO now see the $V_{CC2} - V_{th}$ voltage which may cause damage to those secondary or primaries if they are not rated to handle the increased voltage.

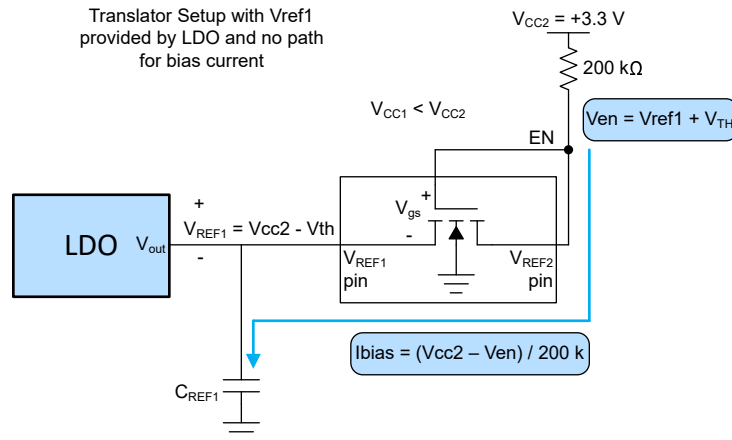
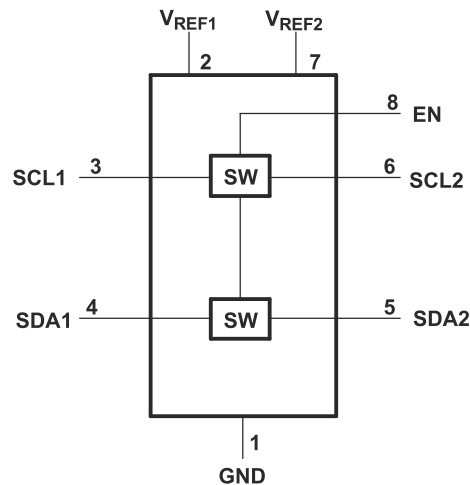


图 8-8. Example of no leakage current path when using LDO

To make sure the LDO does not lose regulation due to the bias current of TCA39306, a weak pull down resistor can be placed on V_{REF1} to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by 方程式 4 where 0.75 gives about 25% margin for error incase bias current increases during operation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable (EN) Pin

The device is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In [Figure 9-1](#), the device is always enabled when power is applied to V_{REF2} . In [Figure 9-2](#), the device is enabled when a control signal from a processor is in a logic-high state.

8.3.2 Voltage Translation

The primary feature of the device is translating voltage from an I²C bus referenced to V_{REF1} up to an I²C bus referenced to V_{DPU} , to which V_{REF2} is connected through a 200-k Ω pullup resistor. Translation on a standard, open-drain I²C bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to V_{REF1} and connecting pullup resistors from SCL2 and SDA2 to V_{DPU} . Information on sizing the pullup resistors can be found in the [Sizing Pullup Resistors](#) section.

8.4 Device Functional Modes

INPUT EN ⁽¹⁾	TRANSLATOR FUNCTION
H	Logic Lows are propagated from one side to the other, Logic Highs blocked (independent pull up resistors passively drive the line high)
L	Disconnect

(1) The SCL switch conducts if EN is ≥ 0.6 V higher than SCL1 or SCL2. The same is true of SDA.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 General Applications of I²C

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I²C devices in addition to SMBus devices. Standard-mode I²C devices only specify 3 mA in a generic I²C system where standard-mode devices and multiple controllers are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain (V_{DPU}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

9.2 Typical Application

图 9-1 和 图 9-2 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

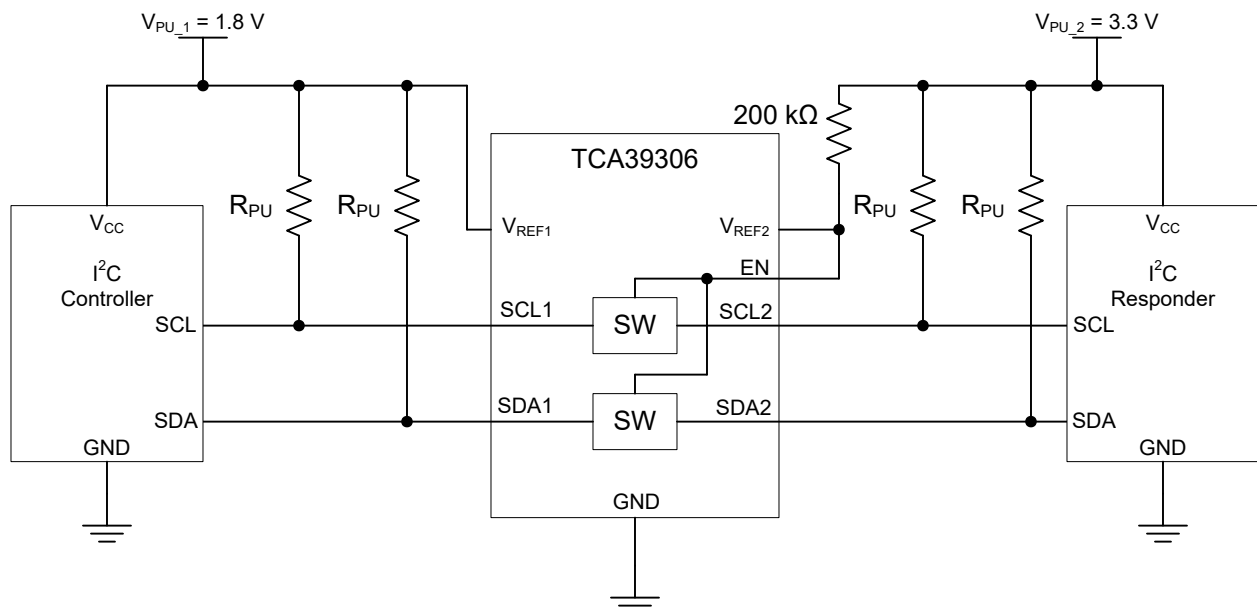


图 9-1. Typical Application Circuit (Switch Always Enabled)

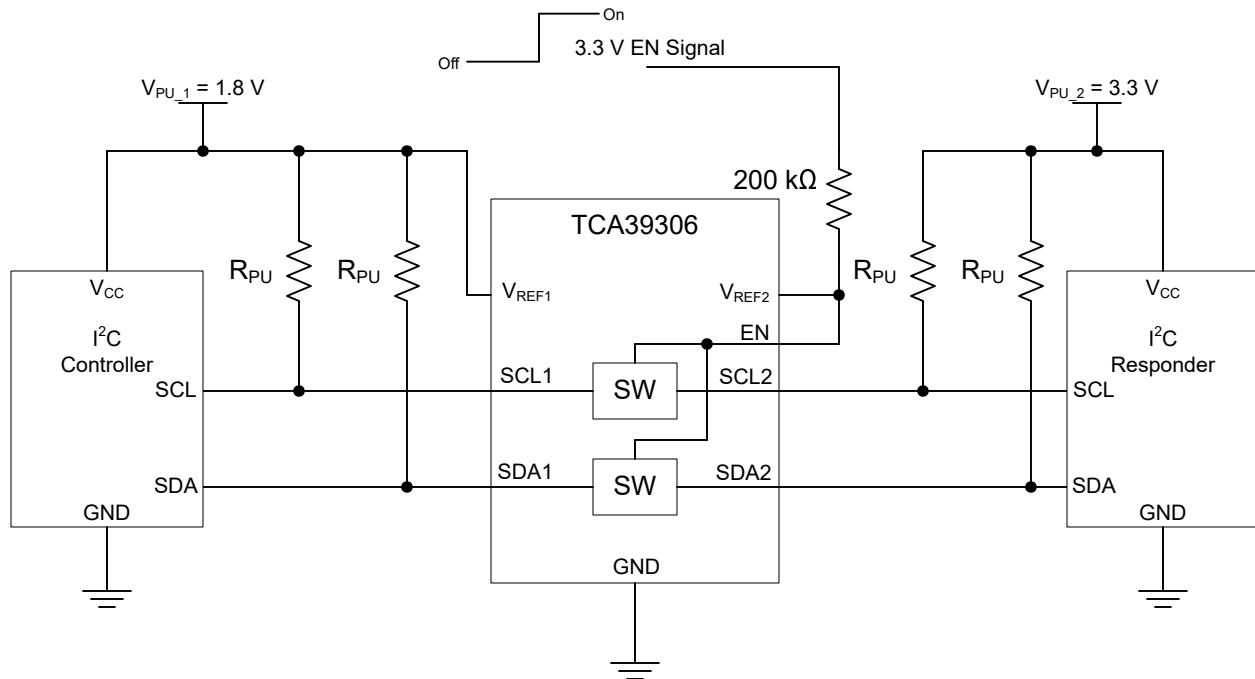


图 9-2. Typical Application Circuit (Switch Enable Control)

9.2.1 Design Requirements

		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{REF2}	Reference voltage	$V_{REF1} + 0.6$	2.1	5	V
EN	Enable input voltage	$V_{REF1} + 0.6$	2.1	5	V
V_{REF1}	Reference voltage	0.9	1.5	4.4	V
I_{PASS}	Pass switch current		6		mA
I_{REF}	Reference-transistor current		5		μ A

(1) All typical values are at $T_A = 25^\circ\text{C}$.

9.2.2 Detailed Design Procedure

9.2.2.1 Bidirectional Voltage Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200 k Ω). This allows V_{REF2} to regulate the EN input. A 100-pF filter capacitor connected to V_{REF2} is recommended. The I²C bus controller output can be push-pull or open-drain (pullup resistors may be required) and the I²C bus device output can be open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

9.2.2.2 Sizing Pullup Resistors

To get an estimate for the range of values that can be used for the pullup resistor, please refer to the application note [SLVA689](#). 图 9-3 and 图 9-4 respectively show the maximum and minimum pullup resistance allowable by the I²C specification for standard-mode (100 kHz) and fast-mode (400 kHz) operation.

9.2.2.3 Bandwidth

The maximum frequency of the device depends on the application. The device can operate at speeds of > 100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application.

However, this is an analog type of measurement. For digital applications, the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is important in determining the overall shape of the digital signal. In the case of the device, digital clock frequency of >100 MHz can be achieved.

The device does not provide any drive capability like the TCA9517 or other buffered translators. Therefore, higher-frequency applications require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the device is being driven by standard CMOS push-pull output driver. Ideally, it is best to minimize the trace length from device on the sink side (1.8 V) to minimize signal degradation.

You can then use a simple formula to compute the maximum *practical* frequency component or the *knee* frequency (f_{knee}). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate f_{knee} :

$$f_{knee} = 0.5 / RT \text{ (10\% - 90\%)} \quad (7)$$

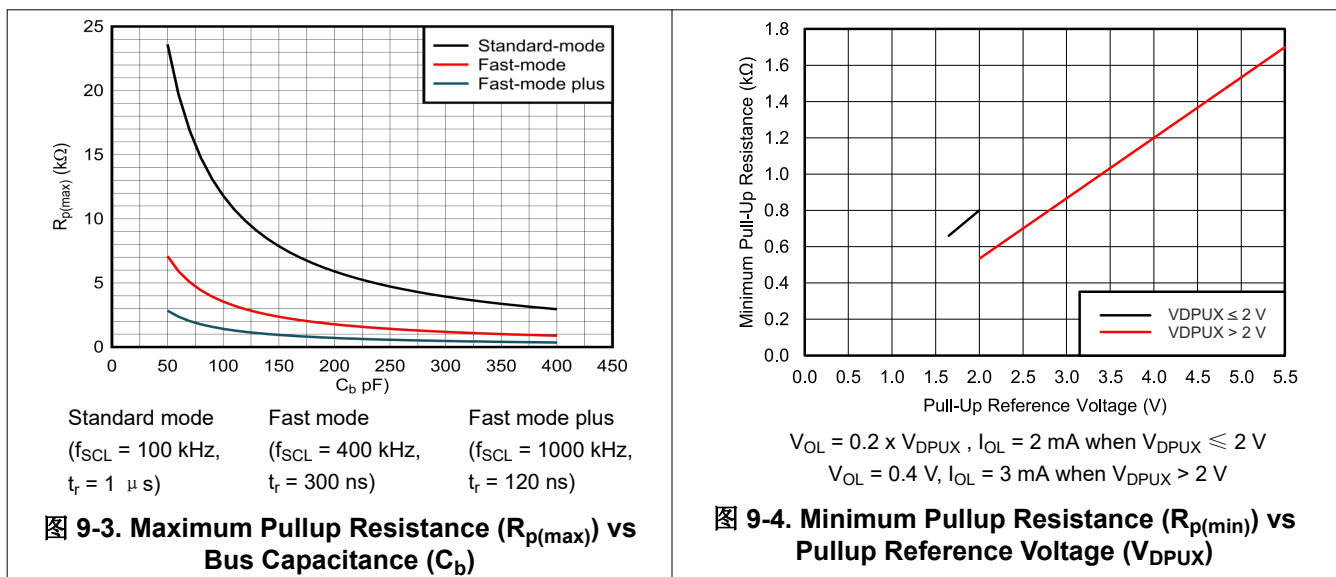
$$f_{knee} = 0.4 / RT \text{ (20\% - 80\%)} \quad (8)$$

For signals with rise-time characteristics based on 10- to 90-percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise-time characteristics based on 20- to 80-percent thresholds, which is very common in many current device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that help maximize the performance of the device:

- Keep trace length to a minimum by placing the device close to the I²C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

9.2.3 Application Curve



9.3 Systems Examples: I3C Usage Considerations

The TCA39306 has bandwidth to support the high speeds needed for I3C, but there are special considerations which are required. Since I3C uses both push-pull and open-drain, it may not be possible to support all I3C applications with a FET-based translator.

9.3.1 I3C Bus Switching

Bus switching is when the bus path is enabled or disabled, but does not translate the bus voltage. External pull-up resistors are not needed for I3C, because the controller enables or disables the pull-up resistor on the SDA line. This presents a unique challenge for FET-based translators, like the TCA39306, because they rely on a pull-up resistor to pull the output side of the switch all the way to supply. For the switching use case, there is no translation, but the enable voltage must be high enough for the switch to stay on for the entire voltage range of the bus (0 V to bus voltage).

R_{ON} must be low enough for the full push-pull voltage range. The EN voltage must be at least $1 V_t$ (~ 0.6 V) above the maximum desired pass-voltage. This comes out to $V_{EN} \geq V_{BUS} + 0.6$ V. Since the switch enable voltage is being directly controlled, the V_{REF1} and V_{REF2} pins are not needed, and can be shorted to ground to improve power consumption.

It is possible to control the EN pin with a voltage equal to V_{BUS} , but external pull-up resistors on the downstream side are a requirement to ensure the bus is pulled entirely to V_{BUS} .

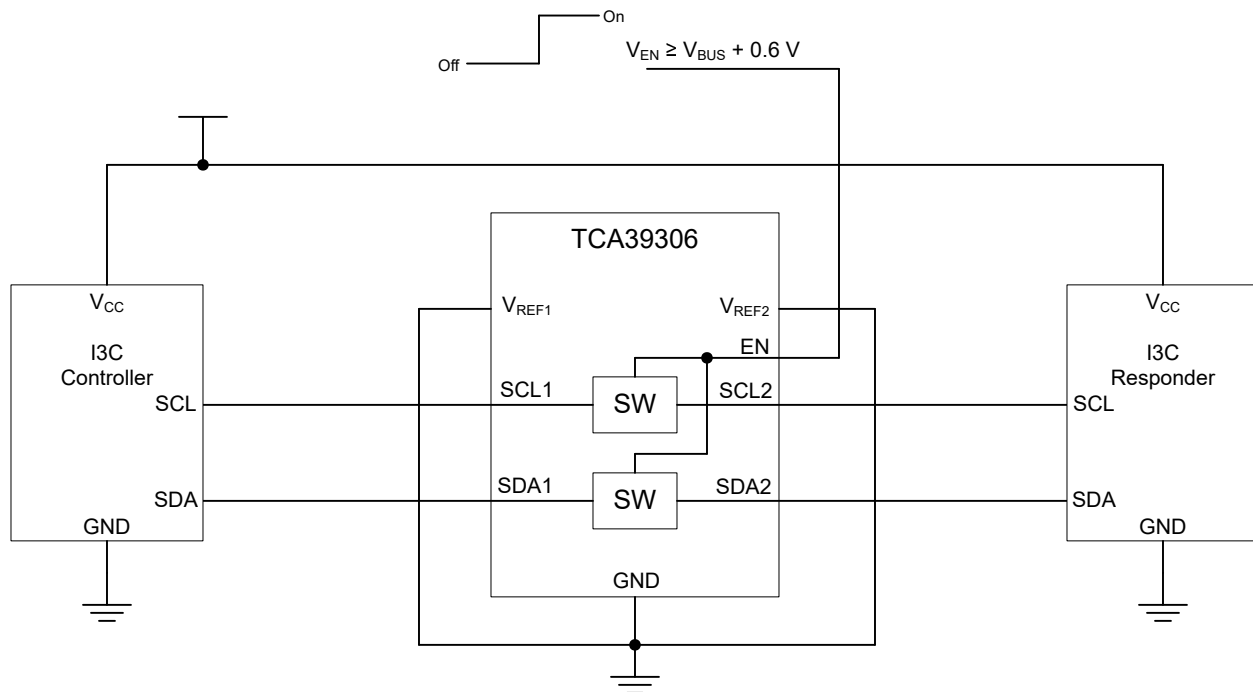


图 9-5. I3C Bus Switching Application (Without Pull-up Resistors)

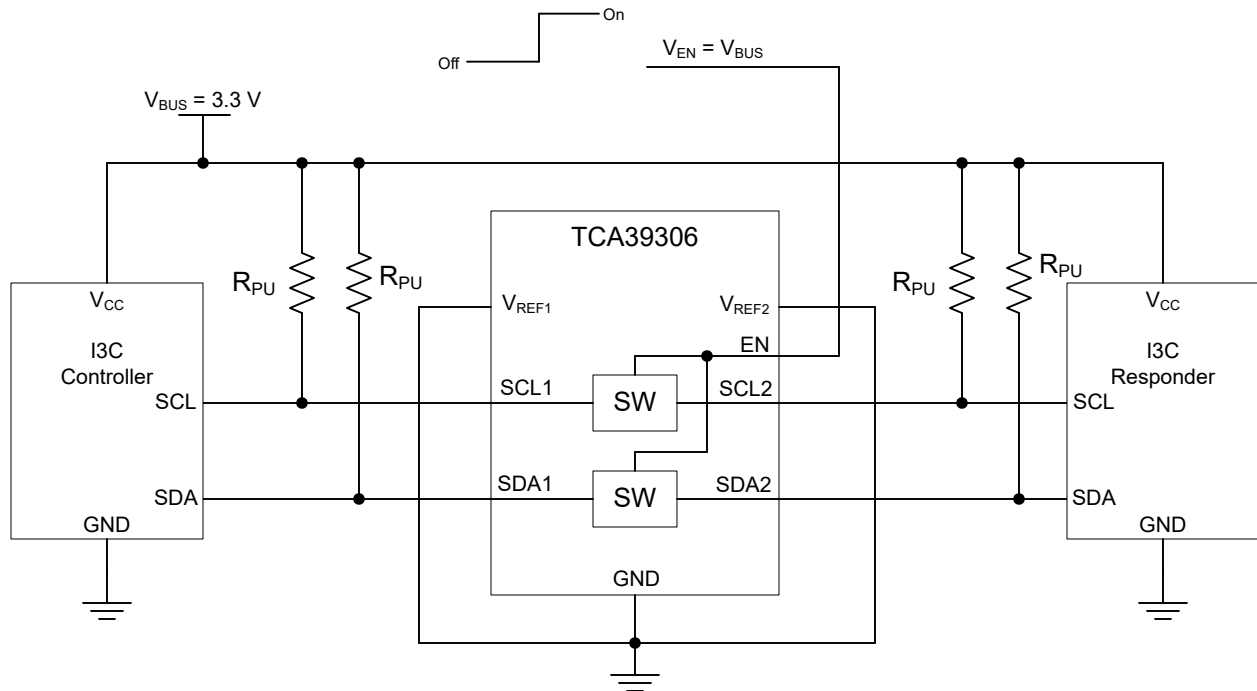


图 9-6. I3C Bus Switching Application (With Pull-up Resistors)

9.3.2 I3C Bus Voltage Translation

Bus voltage translation is when the bus voltage is translated up or down. This presents a unique challenge with I3C for FET-based translators, like the TCA39306, because they rely on a pull-up resistor to translate the voltage up from the low-voltage side. The pull-up resistor selected must be strong enough to meet the timing requirements (based on bus capacitance and translation voltages), but not so strong to violate the V_{IL} requirements of the I3C devices.

The pull-up resistors are needed on both sides. The reason for this is that with the normal translation setup, the switch is "on" when either side's bus voltage drops to roughly V_{PU_1} . This means that the pull-up resistors are required to pull the bus voltage on the high-voltage side from V_{PU_1} to V_{PU_2} . When the device on the high-voltage side is controlling the bus, the switch will turn off at V_{PU_1} . The pull-up resistors on the low-voltage side are used to bleed off any additional current that might "leak" through the switch.

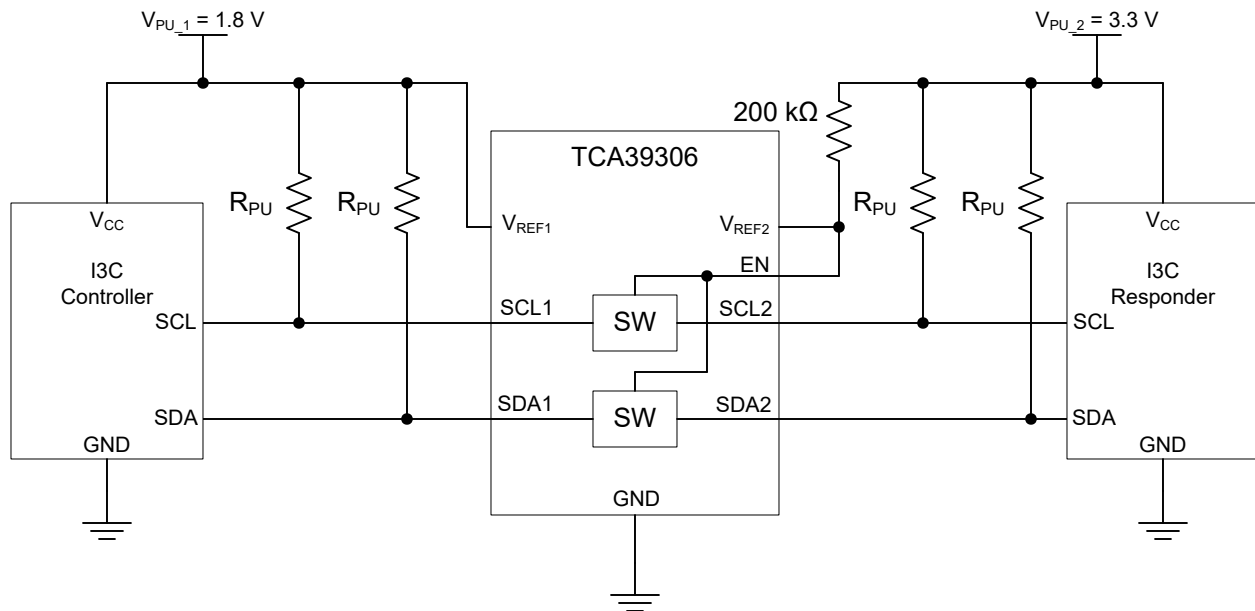


图 9-7. I3C Bus Translation

10 Power Supply Recommendations

For supplying power to the device, the V_{REF1} pin can be connected directly to a power supply. The V_{REF2} pin must be connected to the V_{DPU} power supply through a 200-k Ω resistor. Failure to have a high-impedance resistor between V_{REF2} and V_{DPU} results in excessive current draw and unreliable device operation. It is also worth noting, that in order to support voltage translation, the device must have the EN and VREF2 pins shorted and then pulled up to V_{DPU} through a high-impedance resistor.

11 Layout

11.1 Layout Guidelines

For printed-circuit board (PCB) layout of the device, common PCB layout practices should be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other on leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor should be placed as close to V_{REF2} as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-kΩ resistor results in longer turnon and turnoff times for the TCA39306 device. These best practices are shown in 图 11-1.

For the layout example provided in 图 11-1, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to V_{CC} or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in 图 11-1.

11.2 Layout Example

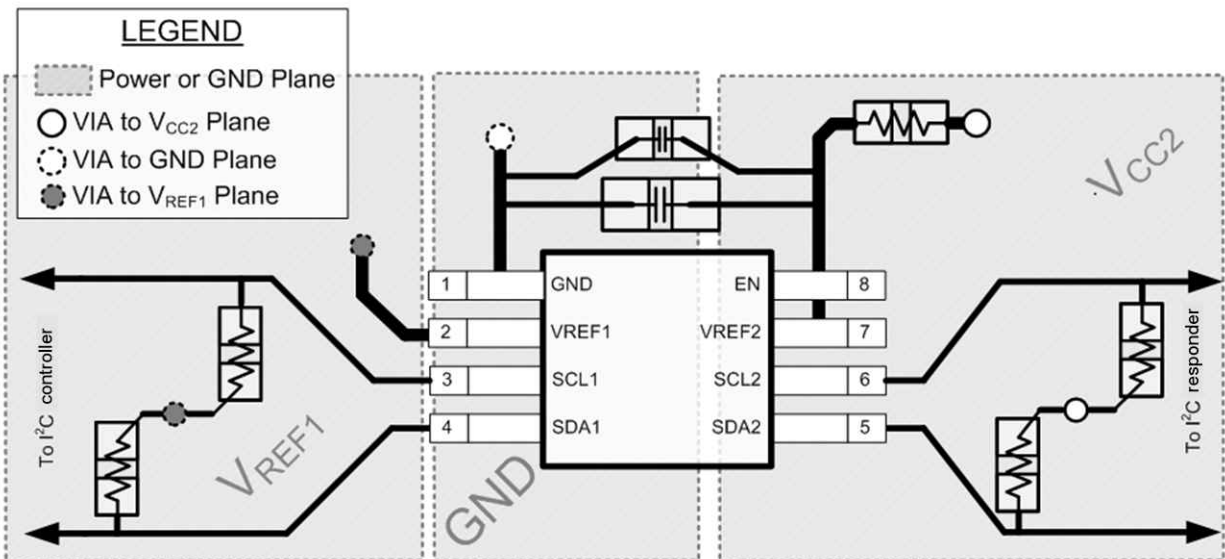


图 11-1. Layout Example

12 Device and Documentation Support

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12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA39306DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAUAG SN	Level-1-260C-UNLIM	-40 to 125	(2GPT, 2GVI)	Samples
TCA39306DTMR	ACTIVE	X2SON	DTM	8	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IH	Samples

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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- Automotive : [TCA39306-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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