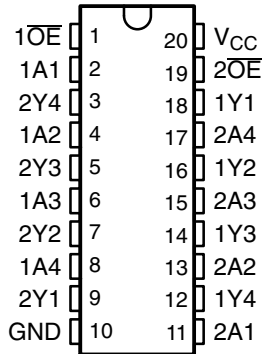


# SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

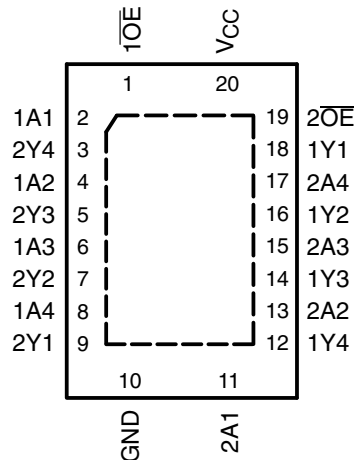
SCAS586J – DECEMBER 1996 – REVISED OCTOBER 2003

- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down to 2.7 V
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

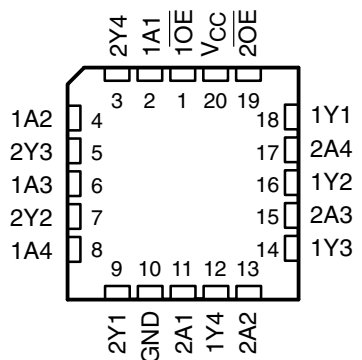
SN54LVTH244A . . . J OR W PACKAGE  
SN74LVTH244A . . . DB, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVTH244A . . . RGY PACKAGE  
(TOP VIEW)



SN54LVTH244A . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

## ORDERING INFORMATION

| $T_A$          | PACKAGE†              |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------------------|---------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RGY             | Tape and reel | SN74LVTH244ARGYR      | LXH244A          |
|                | SOIC – DW             | Tube          | SN74LVTH244ADW        | LVTH244A         |
|                |                       | Tape and reel | SN74LVTH244ADWR       |                  |
|                | SOP – NS              | Tape and reel | SN74LVTH244ANSR       | LVTH244A         |
|                | SSOP – DB             | Tape and reel | SN74LVTH244ADBR       | LXH244A          |
|                | TSSOP – PW            | Tape and reel | SN74LVTH244APWR       | LXH244A          |
|                | VFBGA – GQN           | Tape and reel | SN74LVTH244AGQNR      | LXH244A          |
| –55°C to 125°C | VFBGA – ZQN (Pb-free) |               | SN74LVTH244AZQNR      |                  |
|                | CDIP – J              | Tube          | SNJ54LVTH244AJ        | SNJ54LVTH244AJ   |
|                | CFP – W               | Tube          | SNJ54LVTH244AW        | SNJ54LVTH244AW   |
|                | LCCC – FK             | Tube          | SNJ54LVTH244AFK       | SNJ54LVTH244AFK  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH244A, SN74LVTH244A  
3.3-V ABT OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS

SCAS586J – DECEMBER 1996 – REVISED OCTOBER 2003

description/ordering information (continued)

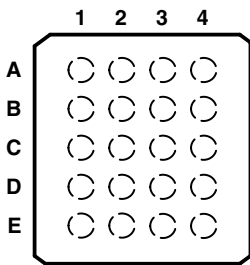
The 'LVTH244A devices are organized as two 4-bit line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the devices pass data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

SN74LVTH244A . . . GQN OR ZQN PACKAGE  
(TOP VIEW)



terminal assignments

|   | 1   | 2                 | 3        | 4                 |
|---|-----|-------------------|----------|-------------------|
| A | 1A1 | 1 $\overline{OE}$ | $V_{CC}$ | 2 $\overline{OE}$ |
| B | 1A2 | 2A4               | 2Y4      | 1Y1               |
| C | 1A3 | 2Y3               | 2A3      | 1Y2               |
| D | 1A4 | 2A2               | 2Y2      | 1Y3               |
| E | GND | 2Y1               | 2A1      | 1Y4               |

FUNCTION TABLE  
(each buffer)

| INPUTS          |   | OUTPUT<br>Y |
|-----------------|---|-------------|
| $\overline{OE}$ | A |             |
| L               | H | H           |
| L               | L | L           |
| H               | X | Z           |

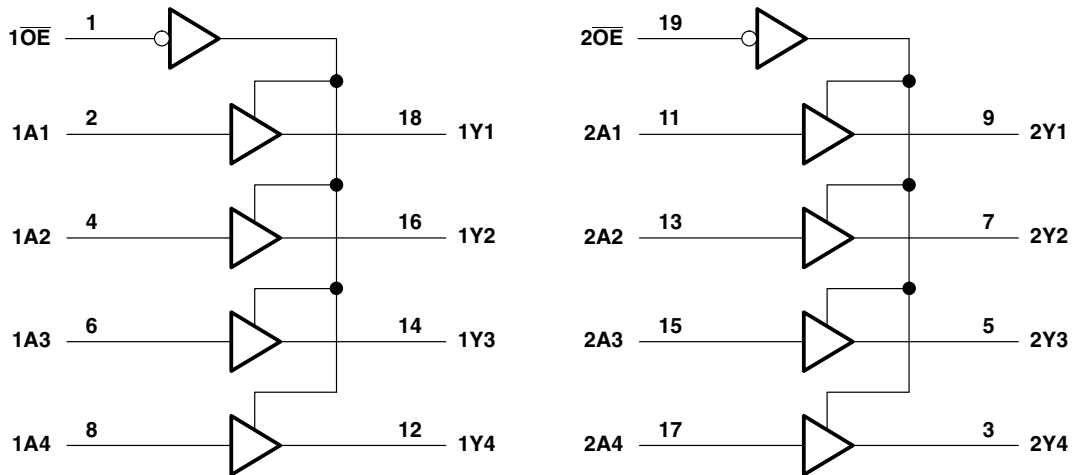
# SN54LVTH244A, SN74LVTH244A

## 3.3-V ABT OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCAS586J – DECEMBER 1996 – REVISED OCTOBER 2003

#### logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, NS, PW, RGY, and W packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                                  |                            |
|--------------------------------------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                                                   | –0.5 V to 4.6 V            |
| Input voltage range, $V_I$ (see Note 1)                                                          | –0.5 V to 7 V              |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | –0.5 V to 7 V              |
| Voltage range applied to any output in the high state, $V_O$ (see Note 1)                        | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, $I_O$ : SN54LVTH244A                                   | 96 mA                      |
| SN74LVTH244A                                                                                     | 128 mA                     |
| Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH244A                      | 48 mA                      |
| SN74LVTH244A                                                                                     | 64 mA                      |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                                      | –50 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                                     | –50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package                                | 70°C/W                     |
| (see Note 3): DW package                                                                         | 58°C/W                     |
| (see Note 3): GQN/ZQN package                                                                    | 78°C/W                     |
| (see Note 3): NS package                                                                         | 60°C/W                     |
| (see Note 3): PW package                                                                         | 83°C/W                     |
| (see Note 4): RGY package                                                                        | 37°C/W                     |
| Storage temperature range, $T_{stg}$                                                             | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. The package thermal impedance is calculated in accordance with JESD 51-5.

# SN54LVTH244A, SN74LVTH244A

## 3.3-V ABT OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCAS586J – DECEMBER 1996 – REVISED OCTOBER 2003

#### recommended operating conditions (see Note 5)

|                          |                                    | SN54LVTH244A    |     | SN74LVTH244A |     | UNIT      |
|--------------------------|------------------------------------|-----------------|-----|--------------|-----|-----------|
|                          |                                    | MIN             | MAX | MIN          | MAX |           |
| $V_{CC}$                 | Supply voltage                     | 2.7             | 3.6 | 2.7          | 3.6 | V         |
| $V_{IH}$                 | High-level input voltage           | 2               |     | 2            |     | V         |
| $V_{IL}$                 | Low-level input voltage            |                 | 0.8 |              | 0.8 | V         |
| $V_I$                    | Input voltage                      |                 | 5.5 |              | 5.5 | V         |
| $I_{OH}$                 | High-level output current          |                 | –24 |              | –32 | mA        |
| $I_{OL}$                 | Low-level output current           |                 | 48  |              | 64  | mA        |
| $\Delta t/\Delta v$      | Input transition rise or fall rate | Outputs enabled |     |              | 10  | ns/V      |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate                 | 200             |     | 200          |     | $\mu$ s/V |
| $T_A$                    | Operating free-air temperature     | –55             | 125 | –40          | 85  | °C        |

NOTE 5: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVTH244A, SN74LVTH244A

## 3.3-V ABT OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCAS586J – DECEMBER 1996 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                | TEST CONDITIONS                                                                                              |                                  | SN54LVTH244A         |      | SN74LVTH244A         |      | UNIT |
|----------------------|----------------|--------------------------------------------------------------------------------------------------------------|----------------------------------|----------------------|------|----------------------|------|------|
|                      |                |                                                                                                              |                                  | MIN                  | TYP† | MAX                  | MIN  |      |
| V <sub>IK</sub>      |                | V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = −18 mA                                                             |                                  | −1.2                 |      | −1.2                 |      | V    |
| V <sub>OH</sub>      |                | V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = −100 μA                                                  |                                  | V <sub>CC</sub> −0.2 |      | V <sub>CC</sub> −0.2 |      | V    |
|                      |                | V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = −8 mA                                                             |                                  | 2.4                  |      | 2.4                  |      |      |
|                      |                | V <sub>CC</sub> = 3 V                                                                                        | I <sub>OH</sub> = −24 mA         | 2                    |      |                      |      |      |
|                      |                |                                                                                                              | I <sub>OH</sub> = −32 mA         |                      |      | 2                    |      |      |
| V <sub>OL</sub>      |                | V <sub>CC</sub> = 2.7 V                                                                                      | I <sub>OL</sub> = 100 μA         | 0.2                  |      | 0.2                  |      | V    |
|                      |                |                                                                                                              | I <sub>OL</sub> = 24 mA          | 0.5                  |      | 0.5                  |      |      |
|                      |                | V <sub>CC</sub> = 3 V                                                                                        | I <sub>OL</sub> = 16 mA          | 0.4                  |      | 0.4                  |      |      |
|                      |                |                                                                                                              | I <sub>OL</sub> = 32 mA          | 0.5                  |      | 0.5                  |      |      |
|                      |                |                                                                                                              | I <sub>OL</sub> = 48 mA          | 0.55                 |      |                      |      |      |
|                      |                |                                                                                                              | I <sub>OL</sub> = 64 mA          |                      |      | 0.55                 |      |      |
| I <sub>I</sub>       | Control inputs | V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V                                                         | 50                               |                      | 10   |                      | μA   |      |
|                      |                | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND                                             | ±1                               |                      | ±1   |                      |      |      |
|                      | Data inputs    | V <sub>CC</sub> = 3.6 V                                                                                      | V <sub>I</sub> = V <sub>CC</sub> | 1                    |      | 1                    |      |      |
|                      |                |                                                                                                              | V <sub>I</sub> = 0               | −5                   |      | −5                   |      |      |
| I <sub>off</sub>     |                | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V                                           |                                  |                      | ±100 |                      | μA   |      |
| I <sub>I(hold)</sub> | Data inputs    | V <sub>CC</sub> = 3 V                                                                                        | V <sub>I</sub> = 0.8 V           | 75                   |      | 75                   |      | μA   |
|                      |                |                                                                                                              | V <sub>I</sub> = 2 V             | −75                  |      | −75                  |      |      |
|                      |                | V <sub>CC</sub> = 3.6 V‡, V <sub>I</sub> = 0 to 3.6 V                                                        |                                  |                      |      | 500<br>−750          |      |      |
| I <sub>OZH</sub>     |                | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V                                                                | 5                                |                      | 5    |                      | μA   |      |
| I <sub>OZL</sub>     |                | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V                                                              | −5                               |                      | −5   |                      | μA   |      |
| I <sub>OZPU</sub>    |                | V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care                                 |                                  | ±100*                |      | ±100                 |      | μA   |
| I <sub>OZPD</sub>    |                | V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care                                 |                                  | ±100*                |      | ±100                 |      | μA   |
| I <sub>CC</sub>      |                | V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND                         | Outputs high                     |                      | 0.39 |                      | 0.19 |      |
|                      |                |                                                                                                              | Outputs low                      |                      | 14   |                      | 5    |      |
|                      |                |                                                                                                              | Outputs disabled                 |                      | 0.39 |                      | 0.19 |      |
| ΔI <sub>CC</sub> §   |                | V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND |                                  | 0.2                  |      | 0.2                  |      | mA   |
| C <sub>i</sub>       |                | V <sub>I</sub> = 3 V or 0                                                                                    |                                  | 3                    |      | 3                    |      | pF   |
| C <sub>o</sub>       |                | V <sub>O</sub> = 3 V or 0                                                                                    |                                  | 7                    |      | 7                    |      | pF   |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.



# SN54LVTH244A, SN74LVTH244A

## 3.3-V ABT OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

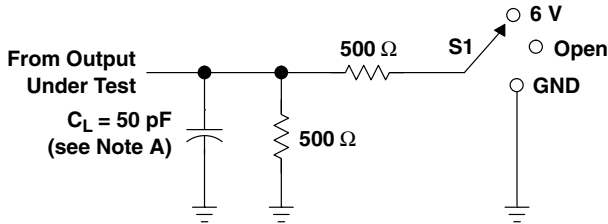
SCAS586J – DECEMBER 1996 – REVISED OCTOBER 2003

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

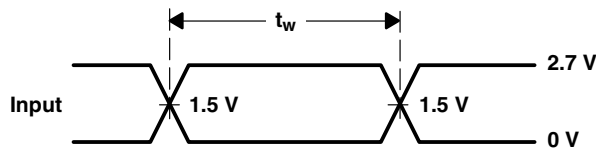
| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN54LVTH244A                       |     |                         |     | SN74LVTH244A                       |      |     |                         | UNIT |     |
|------------------|-----------------|----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|------|-----|-------------------------|------|-----|
|                  |                 |                | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |      |     | V <sub>CC</sub> = 2.7 V |      |     |
|                  |                 |                | MIN                                | MAX | MIN                     | MAX | MIN                                | TYP† | MAX | MIN                     |      | MAX |
| t <sub>PLH</sub> | A               | Y              | 0.5                                | 3.8 | 4.1                     |     | 1.1                                | 2.3  | 3.5 | 3.8                     |      | ns  |
| t <sub>PHL</sub> |                 |                | 0.5                                | 3.8 | 3.9                     |     | 1.3                                | 2.1  | 3.3 | 3.6                     |      |     |
| t <sub>PZH</sub> | OE              | Y              | 0.8                                | 5   | 6                       |     | 1.1                                | 2.5  | 4.5 | 5.3                     |      | ns  |
| t <sub>PZL</sub> |                 |                | 0.8                                | 5   | 5.4                     |     | 1.4                                | 2.7  | 4.4 | 4.9                     |      |     |
| t <sub>PHZ</sub> | OE              | Y              | 1.3                                | 5.5 | 5.8                     |     | 1.9                                | 2.8  | 4.4 | 4.5                     |      | ns  |
| t <sub>PLZ</sub> |                 |                | 1.2                                | 4.7 | 4.8                     |     | 1.8                                | 2.9  | 4.4 | 4.4                     |      |     |

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

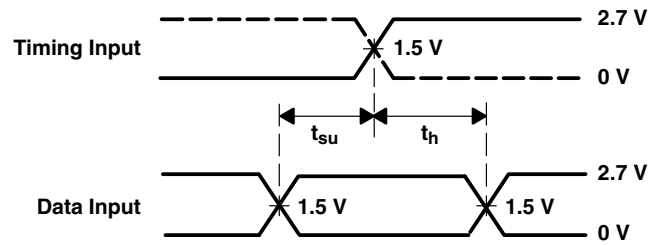
## PARAMETER MEASUREMENT INFORMATION



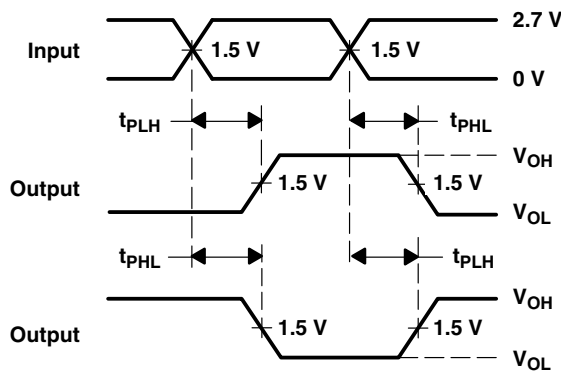
LOAD CIRCUIT



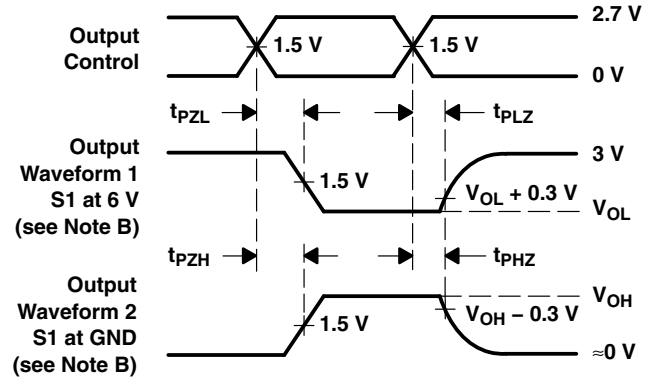
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                    | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|--------------------------------------------|-------------------------|
| 5962-9584401Q2A   | ACTIVE        | LCCC         | FK                 | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9584401Q2A<br>SNJ54LVTH<br>244AFK | <a href="#">Samples</a> |
| 5962-9584401QRA   | ACTIVE        | CDIP         | J                  | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9584401QR<br>A<br>SNJ54LVTH244AJ      | <a href="#">Samples</a> |
| 5962-9584401QSA   | ACTIVE        | CFP          | W                  | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9584401QS<br>A<br>SNJ54LVTH244AW      | <a href="#">Samples</a> |
| 5962-9584401V2A   | ACTIVE        | LCCC         | FK                 | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9584401V2A<br>SNV54LVTH<br>244AFK | <a href="#">Samples</a> |
| 5962-9584401VRA   | ACTIVE        | CDIP         | J                  | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9584401VR<br>A<br>SNV54LVTH244AJ      | <a href="#">Samples</a> |
| 5962-9584401VSA   | ACTIVE        | CFP          | W                  | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9584401VS<br>A<br>SNV54LVTH244AW      | <a href="#">Samples</a> |
| SN74LVTH244ADB    | ACTIVE        | SSOP         | DB                 | 20   | 70             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   |              | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244ADBR   | ACTIVE        | SSOP         | DB                 | 20   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244ADBRE4 | ACTIVE        | SSOP         | DB                 | 20   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244ADBRG4 | ACTIVE        | SSOP         | DB                 | 20   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244ADW    | ACTIVE        | SOIC         | DW                 | 20   | 25             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH244A                                   | <a href="#">Samples</a> |
| SN74LVTH244ADWE4  | ACTIVE        | SOIC         | DW                 | 20   | 25             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH244A                                   | <a href="#">Samples</a> |
| SN74LVTH244ADWG4  | ACTIVE        | SOIC         | DW                 | 20   | 25             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH244A                                   | <a href="#">Samples</a> |
| SN74LVTH244ADWR   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH244A                                   | <a href="#">Samples</a> |
| SN74LVTH244ADWRG4 | ACTIVE        | SOIC         | DW                 | 20   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH244A                                   | <a href="#">Samples</a> |

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                    | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|--------------------------------------------|-------------------------|
| SN74LVTH244ANSR   | ACTIVE        | SO           | NS                 | 20   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH244A                                   | <a href="#">Samples</a> |
| SN74LVTH244APW    | ACTIVE        | TSSOP        | PW                 | 20   | 70             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244APWG4  | ACTIVE        | TSSOP        | PW                 | 20   | 70             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244APWR   | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | RoHS & Green        | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244APWRE4 | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244APWRG4 | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SN74LVTH244ARGYR  | ACTIVE        | VQFN         | RGY                | 20   | 3000           | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | LXH244A                                    | <a href="#">Samples</a> |
| SNJ54LVTH244AFK   | ACTIVE        | LCCC         | FK                 | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9584401Q2A<br>SNJ54LVTH<br>244AFK | <a href="#">Samples</a> |
| SNJ54LVTH244AJ    | ACTIVE        | CDIP         | J                  | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9584401QR<br>A<br>SNJ54LVTH244AJ      | <a href="#">Samples</a> |
| SNJ54LVTH244AW    | ACTIVE        | CFP          | W                  | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9584401QS<br>A<br>SNJ54LVTH244AW      | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVTH244A, SN54LVTH244A-SP, SN74LVTH244A :**

- Catalog: [SN74LVTH244A](#), [SN54LVTH244A](#)
- Enhanced Product: [SN74LVTH244A-EP](#), [SN74LVTH244A-EP](#)
- Military: [SN54LVTH244A](#)
- Space: [SN54LVTH244A-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH244ADBR   | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVTH244ADWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LVTH244ANSR   | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LVTH244APWR   | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVTH244APWR   | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74LVTH244APWRG4 | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVTH244ARGYR  | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH244ADBR   | SSOP         | DB              | 20   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVTH244ADWR   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVTH244ANSR   | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVTH244APWR   | TSSOP        | PW              | 20   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVTH244APWR   | TSSOP        | PW              | 20   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVTH244APWRG4 | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LVTH244ARGYR  | VQFN         | RGY             | 20   | 3000 | 853.0       | 449.0      | 35.0        |

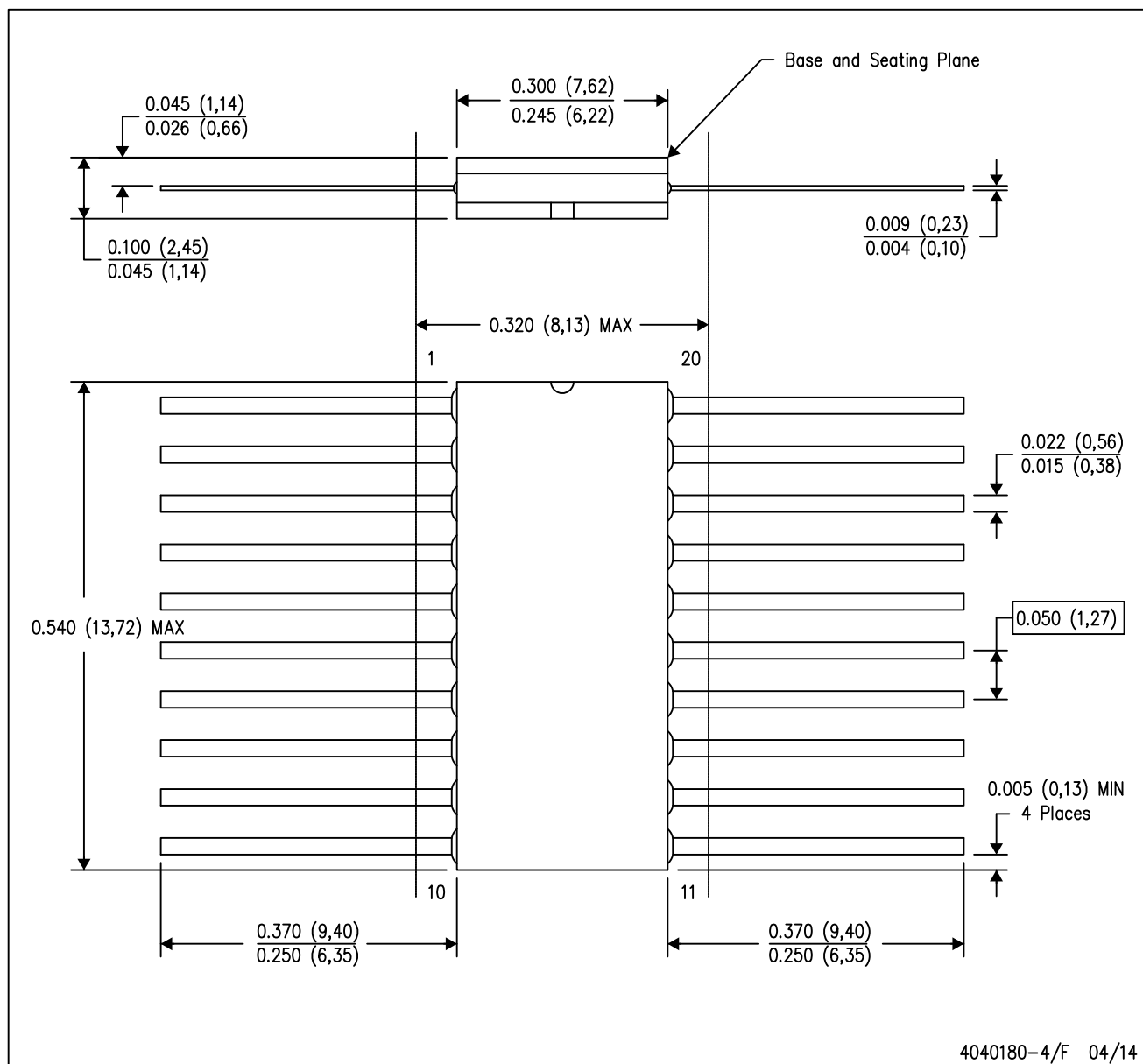
**TUBE**


\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9584401Q2A  | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| 5962-9584401V2A  | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| 5962-9584401VSA  | W            | CFP          | 20   | 1   | 506.98 | 26.16  | 6220   | NA     |
| SN74LVTH244ADB   | DB           | SSOP         | 20   | 70  | 530    | 10.5   | 4000   | 4.1    |
| SN74LVTH244ADW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LVTH244ADWE4 | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LVTH244ADWG4 | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LVTH244APW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVTH244APWG4 | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| SNJ54LVTH244AFK  | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



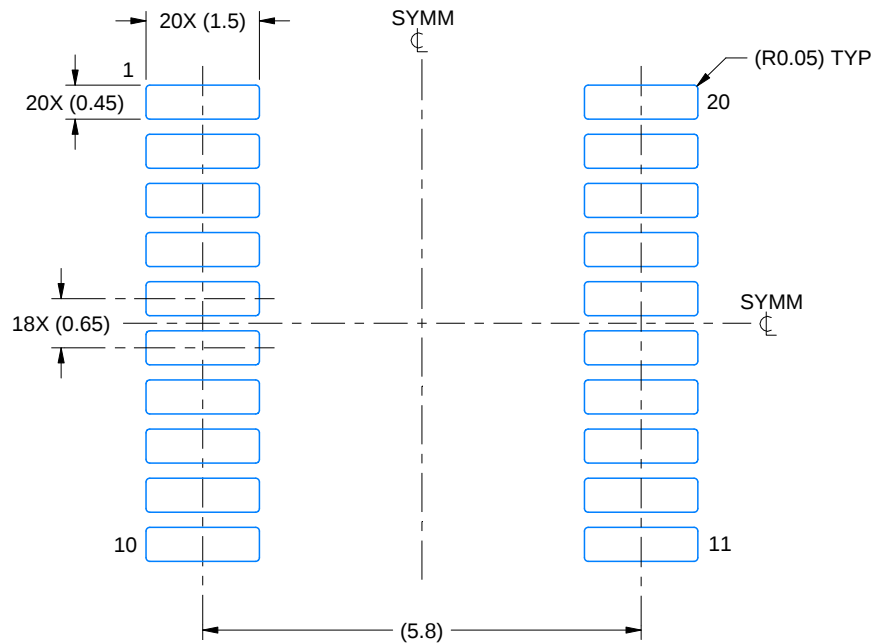
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

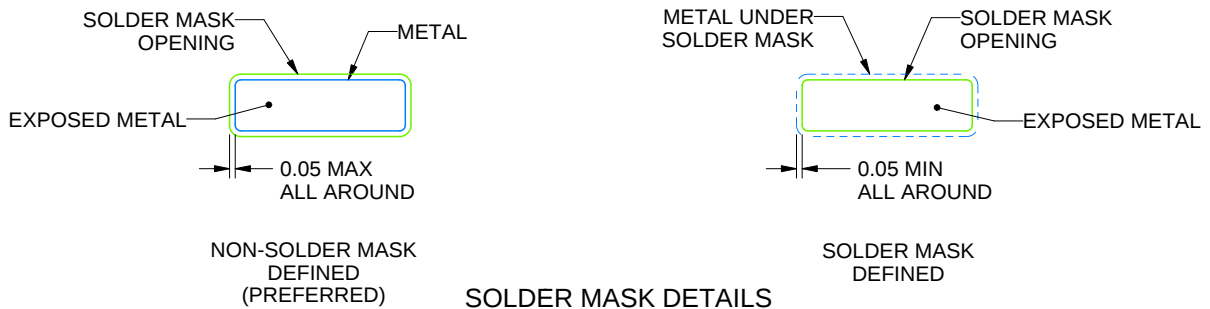
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

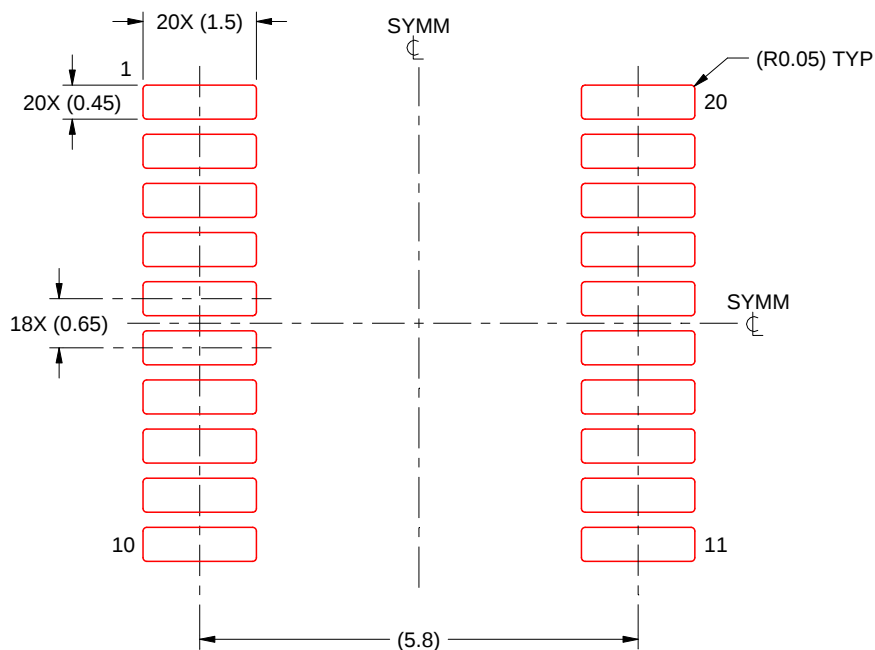
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



4214851/B 08/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

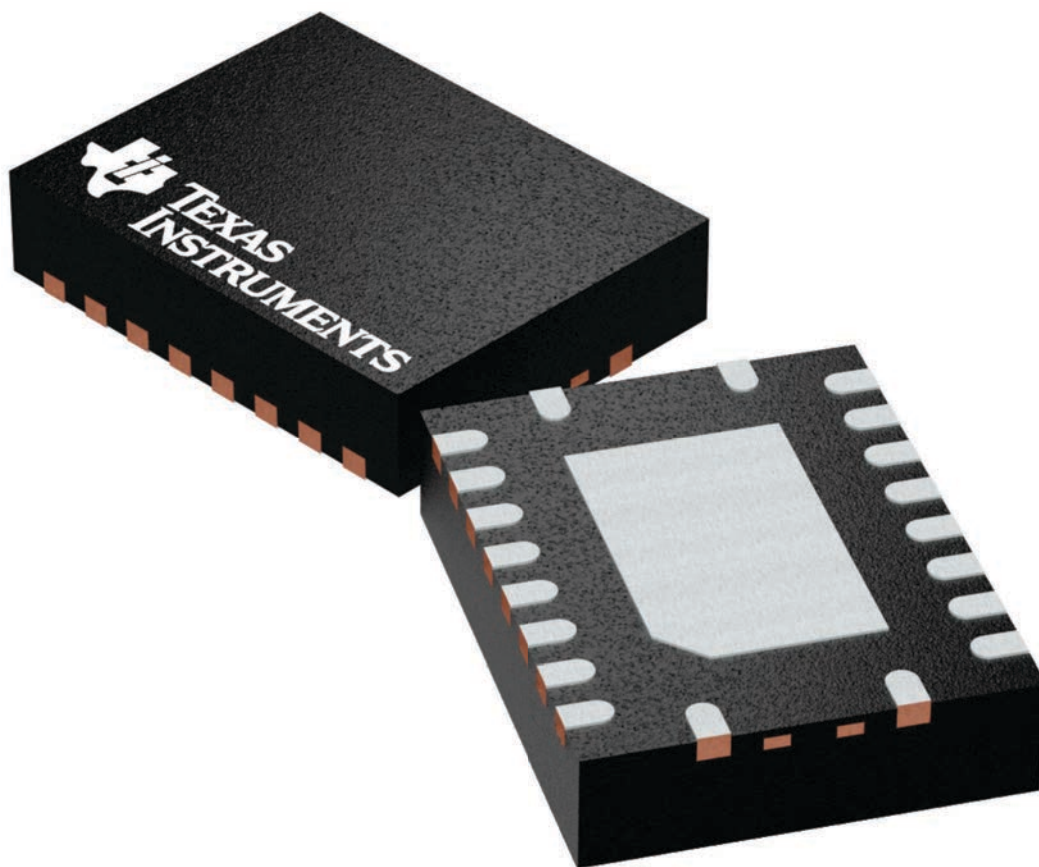
**RGY 20**

**VQFN - 1 mm max height**

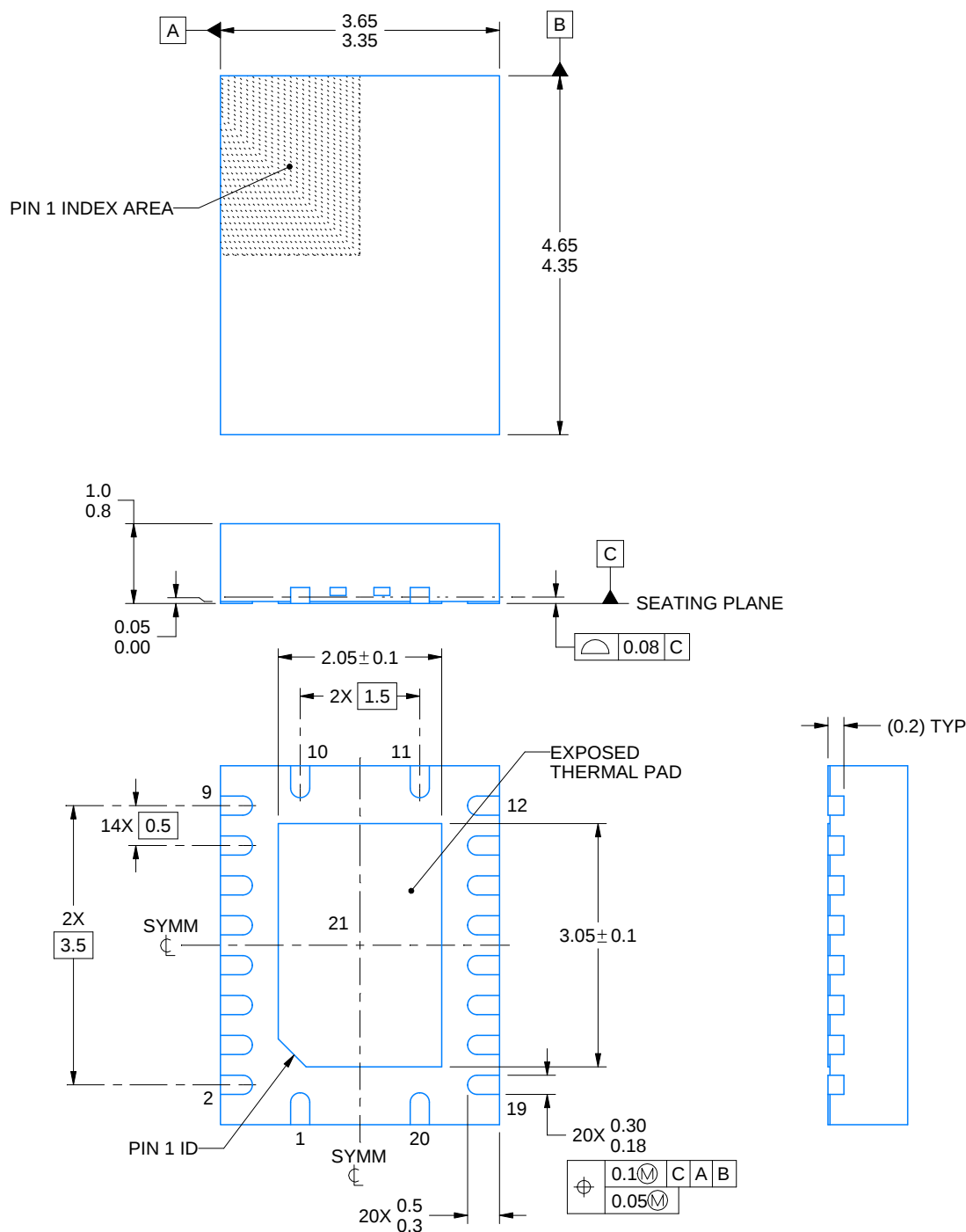
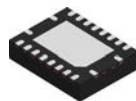
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

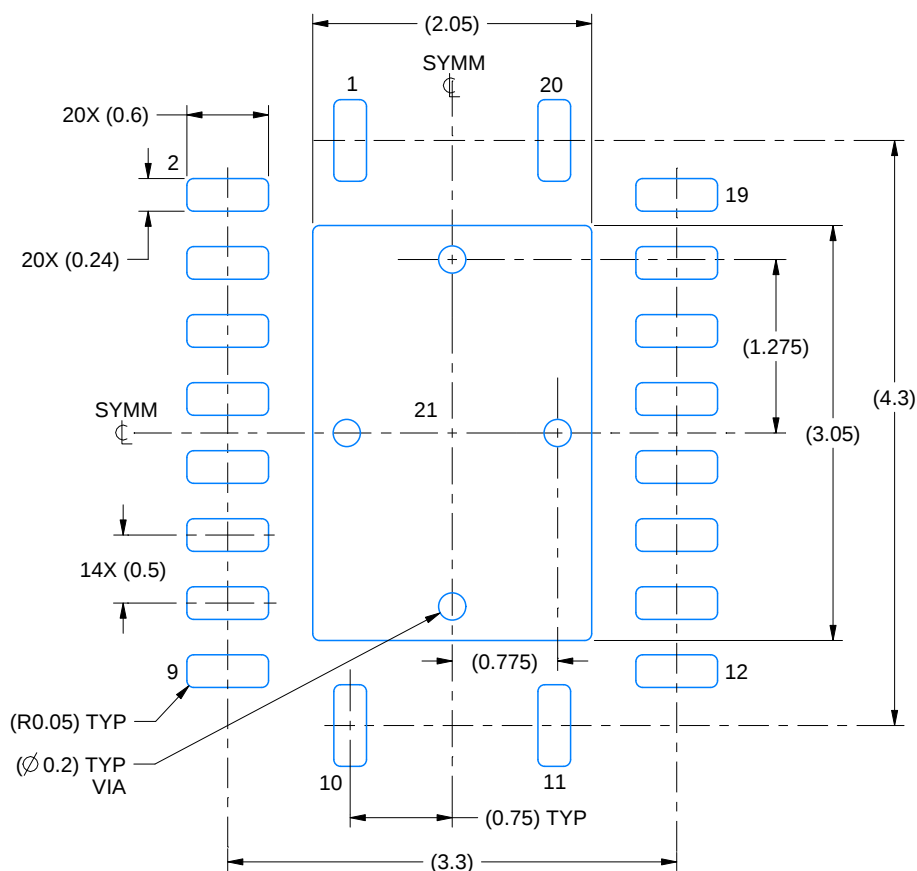
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

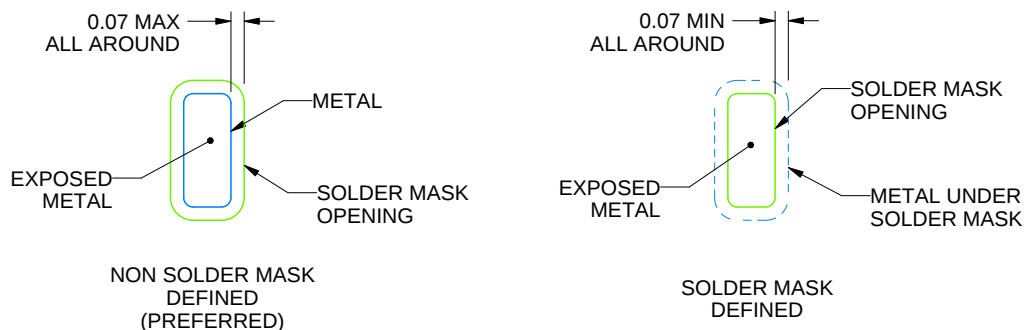
**RGY0020A**

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



## SOLDER MASK DETAILS

4225320/A 09/2019

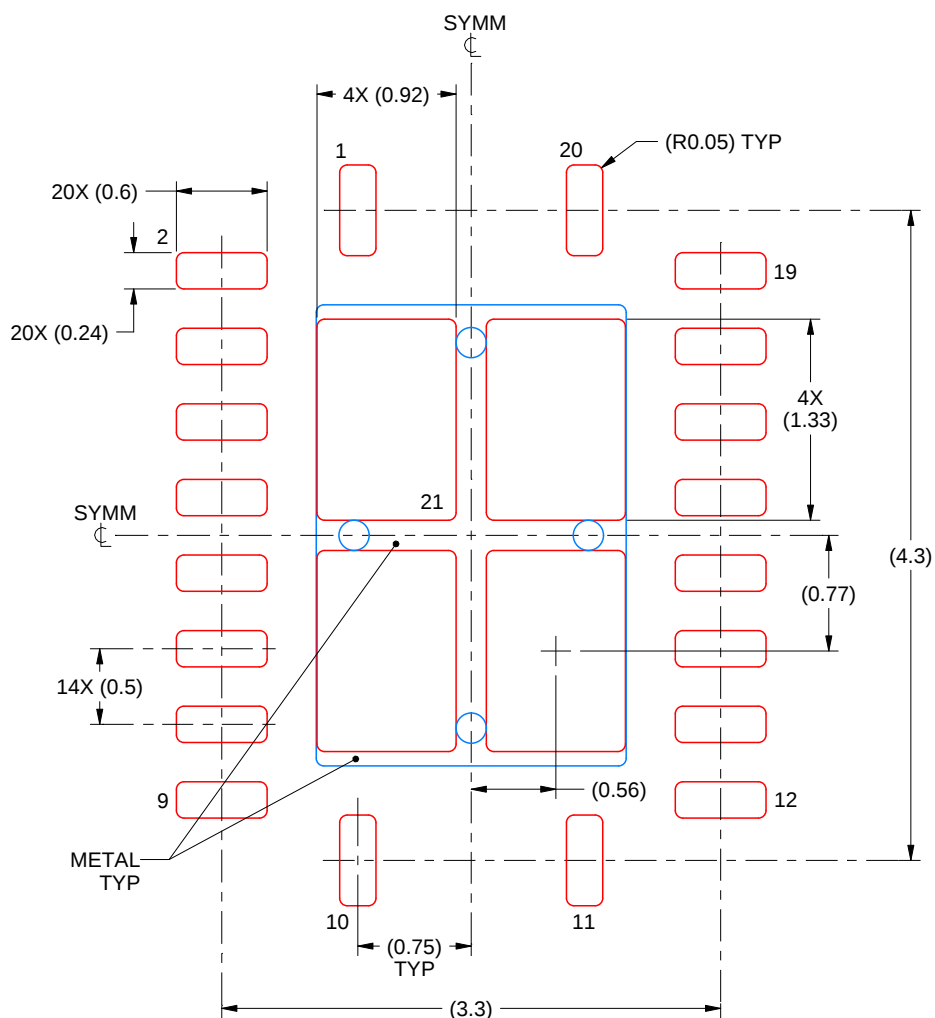
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**RGY0020A**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE

BASED ON 0.125 mm THICK STENCIL

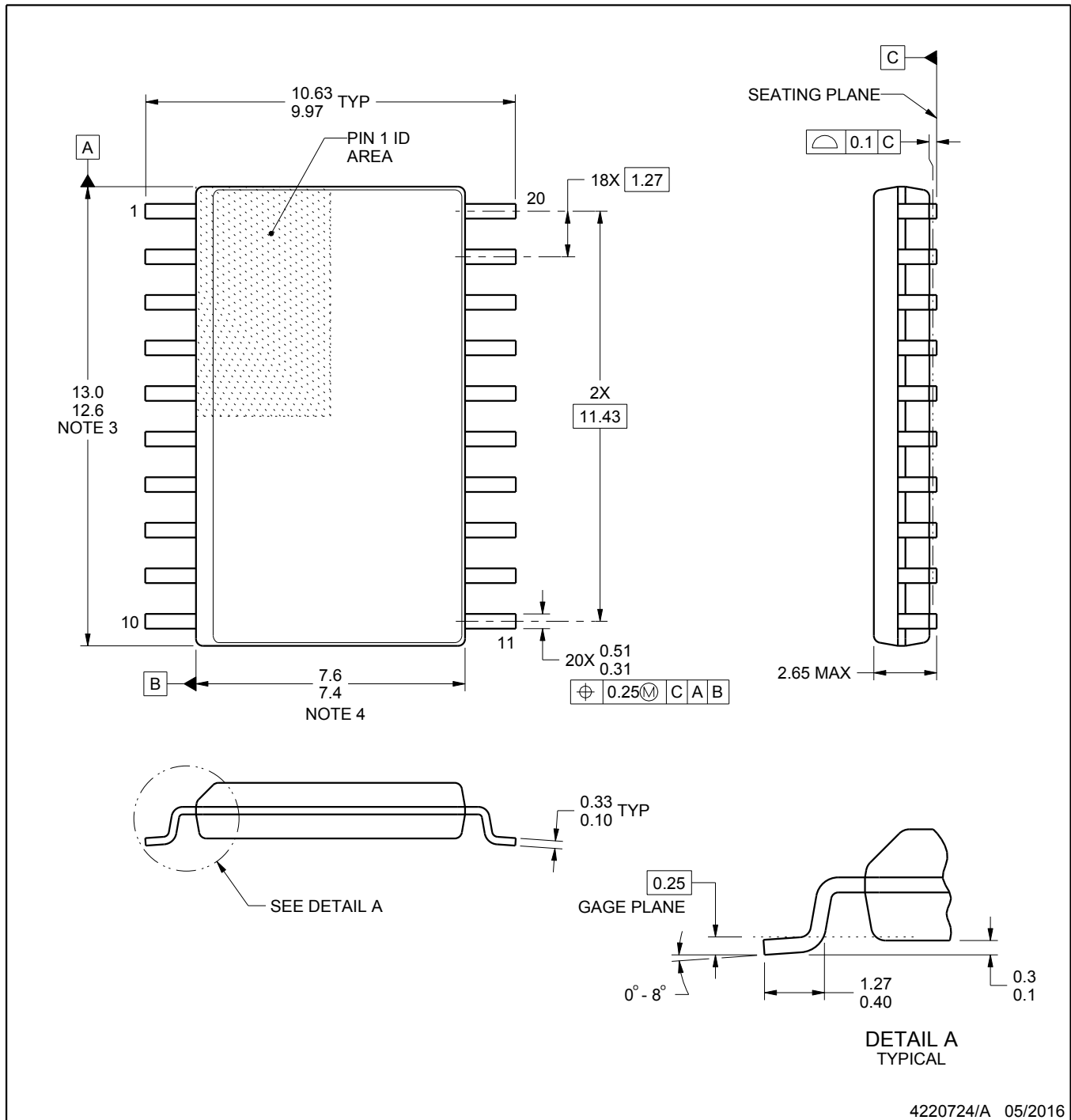
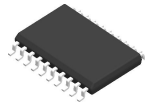
EXPOSED PAD 21

78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220724/A 05/2016

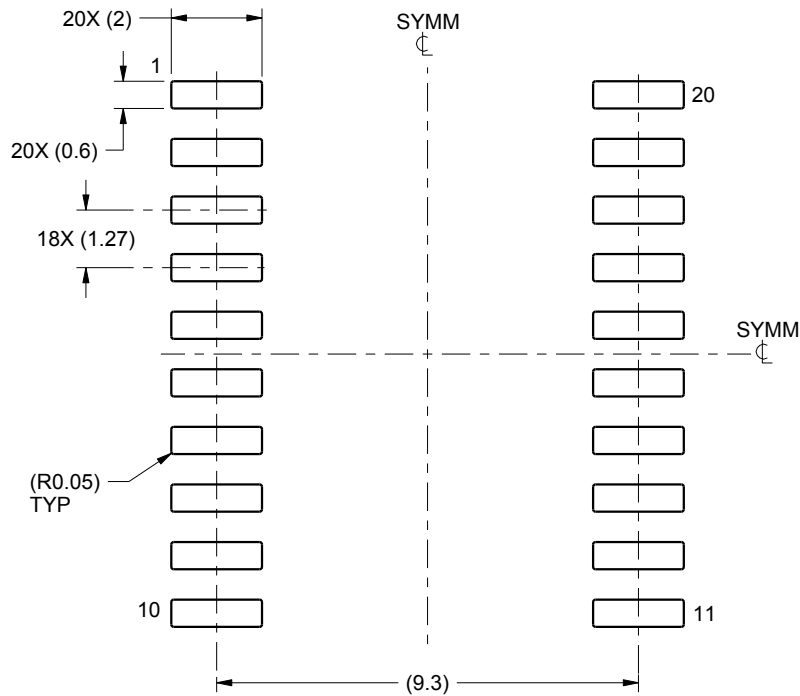
## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

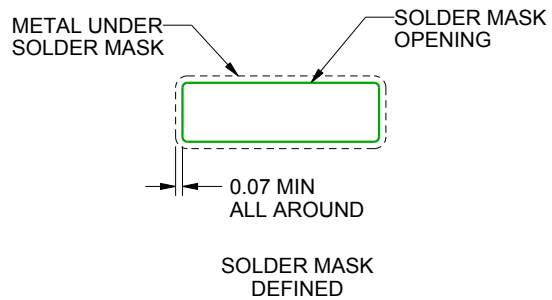
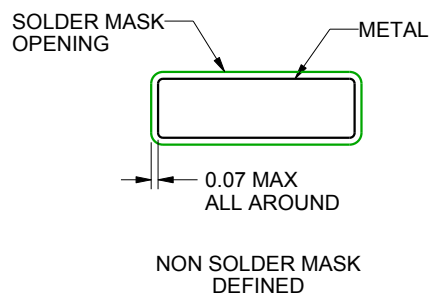
**DW0020A**

**SOIC - 2.65 mm max height**

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated