

# SN74CB3T3306 Dual FET Bus Switch 2.5-V/3.3-V Low-Voltage Bus Switch With 5-V Tolerant Level Shifter

## 1 Features

- Output Voltage Translation Tracks  $V_{CC}$
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
  - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V  $V_{CC}$
  - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V  $V_{CC}$
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 5 \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading ( $C_{io(OFF)} = 4.5 \text{ pF}$  Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 20 \mu\text{A}$  Maximum)
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Digital Applications:
  - Level Translation
  - USB Interface
  - Bus Isolation
- Ideal for Low-Power Portable Equipment

## 2 Applications

- Supports Digital Applications:
  - Level Translation
  - PCI Interface
  - USB Interface
  - Memory Interleaving
  - Bus Isolation

## 3 Description

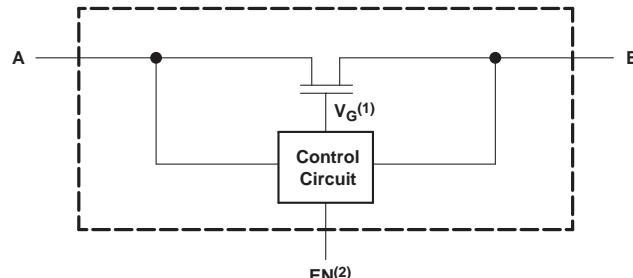
The SN74CB3T3306 device is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks  $V_{CC}$ . The SN74CB3T3306 device supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see [Figure 5](#)).

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CB3T3306DCT	SSOP (8)	2.95 mm x 2.80 mm
SN74CB3T3306DCU	VSSOP (8)	2.30 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Block Diagram



(1) Gate voltage ( $V_G$ ) is approximately equal to  $V_{CC} + V_T$  when the switch is ON and  $V_I > V_{CC} + V_T$ .

(2) EN is the internal enable signal applied to the switch.



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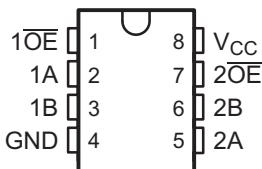
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2012) to Revision C	Page
• Added <i>Applications</i> section, <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

## 5 Pin Configuration and Functions

DCT or DCU Package  
8-Pin SSOP or VSSOP  
Top View



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1OE	1	I	Active-low enable for switch 1
1A	2	I/O	Switch 1 A terminal
1B	3	I/O	Switch 1 B terminal
GND	4	—	Ground
2A	5	I/O	Switch 2 A terminal
2B	6	I/O	Switch 2 B terminal
2OE	7	I	Active-low enable for switch 1
V <sub>CC</sub>	8	—	Supply voltage pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage <sup>(2)</sup>	-0.5	7	V
$V_{IN}$	Control input voltage <sup>(2)(3)</sup>	-0.5	7	V
$V_{I/O}$	Switch I/O voltage <sup>(2)(3)(4)</sup>	-0.5	7	V
$I_{IK}$	Control input clamp current	$V_{IN} < 0$	-50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$	-50	mA
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		$\pm 128$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to ground, unless otherwise specified.
- The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	+2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	+1000

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7	5.5
		$V_{CC} = 2.7$ V to 3.6 V	2	5.5
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3$ V to 2.7 V	0	0.7
		$V_{CC} = 2.7$ V to 3.6 V	0	0.8
$V_{I/O}$	Data input and output voltage	0	5.5	V
$T_A$	Operating free-air temperature	-40	85	°C

- All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74CB3T3306		UNIT
	DCT (SSOP)	DCU (VSSOP)	
	8 PINS	8 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	182.6	209.4	°C/W
$R_{\theta JC(\text{top})}$ Junction-to-case (top) thermal resistance	113.2	75.5	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	95.1	88.9	°C/W
$\Psi_{JT}$ Junction-to-top characterization parameter	39.2	6.4	°C/W
$\Psi_{JB}$ Junction-to-board characterization parameter	94.1	88.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IK}$	$V_{CC} = 3 \text{ V}$ , $I_I = -18 \text{ mA}$ (see <a href="#">Figure 9</a> and <a href="#">Figure 1</a> )			-1.2	V
$V_{OH}$					
$I_{IN}$	Control inputs	$V_{CC} = 3.6 \text{ V}$ , $V_{IN} = 3.6 \text{ V}$ to $5.5 \text{ V}$ or GND		$\pm 10$	$\mu\text{A}$
$I_I$		$V_{CC} = 3.6 \text{ V}$ , Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7 \text{ V}$ to $5.5 \text{ V}$	$\pm 20$	$\mu\text{A}$
			$V_I = 0.7 \text{ V}$ to $V_{CC} - 0.7 \text{ V}$	-40	
			$V_I = 0$ to $0.7 \text{ V}$	$\pm 5$	
$I_{OZ}^{(3)}$		$V_{CC} = 3.6 \text{ V}$ , $V_O = 0$ to $5.5 \text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}$ or GND		$\pm 10$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ , $V_O = 0$ to $5.5 \text{ V}$ , $V_I = 0$		10	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ , $I_{IO} = 0$ , Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND	20	$\mu\text{A}$
			$V_I = 5.5 \text{ V}$	20	
$\Delta I_{CC}^{(4)}$	Control inputs	$V_{CC} = 3 \text{ V}$ to $3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND		300	$\mu\text{A}$
$C_{in}$	Control inputs	$V_{CC} = 3.3 \text{ V}$ , $V_{IN} = V_{CC}$ or GND		3	$\text{pF}$
$C_{io(OFF)}$		$V_{CC} = 3.3 \text{ V}$ , $V_{IO} = 5.5 \text{ V}$ , $3.3 \text{ V}$ , or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND		4.5	$\text{pF}$
$C_{io(ON)}$		$V_{CC} = 3.3 \text{ V}$ , Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{IO} = 5.5 \text{ V}$ or $3.3 \text{ V}$	4	$\text{pF}$
			$V_{IO} = \text{GND}$	15	
$r_{on}^{(5)}$		$V_{CC} = 2.3 \text{ V}$ , TYP at $V_{CC} = 2.5 \text{ V}$ , $V_I = 0$	$I_O = 24 \text{ mA}$	5	$\Omega$
			$I_O = 16 \text{ mA}$	5	
		$V_{CC} = 3 \text{ V}$ , $V_I = 0$	$I_O = 64 \text{ mA}$	5	
			$I_O = 32 \text{ mA}$	5	

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs,  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

(2) All typical values are at  $V_{CC} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

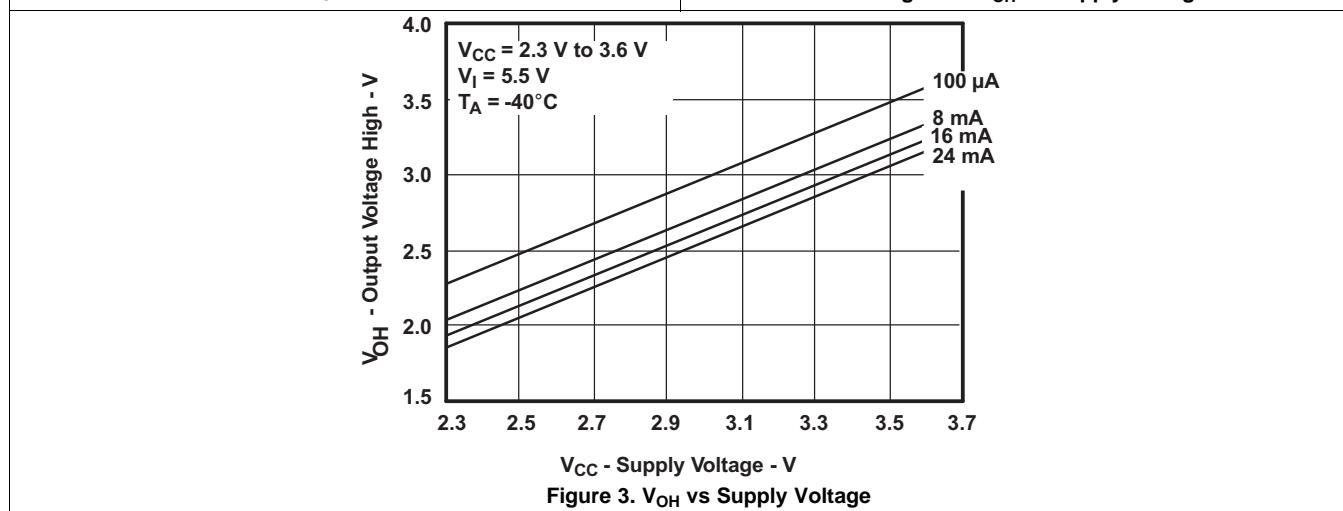
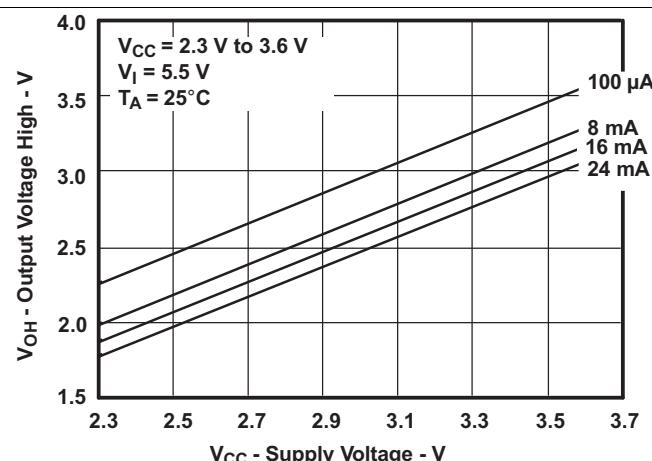
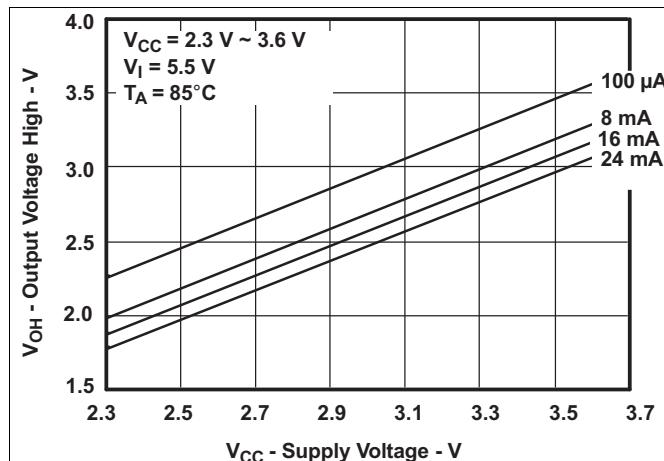
## 6.6 Switching Characteristics

over recommended operating free-air temperature range unless otherwise noted (see Figure 4)

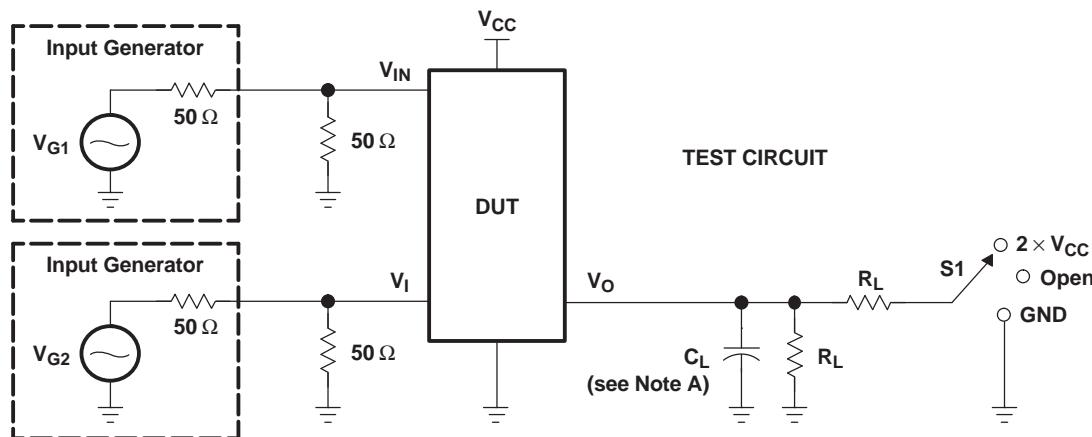
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd}^{(1)}$	A or B	B or A	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	0.15	ns	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.25	ns	
$t_{en}$	$\overline{OE}$	A or B	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1	8.5	ns
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	6.5	ns
$t_{dis}$	$\overline{OE}$	A or B	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1	9	ns
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

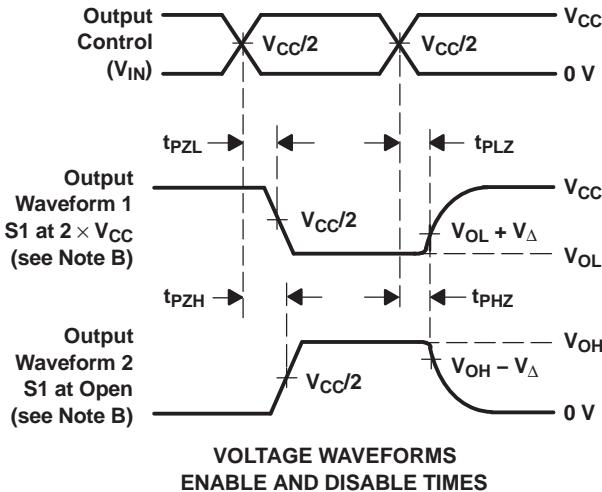
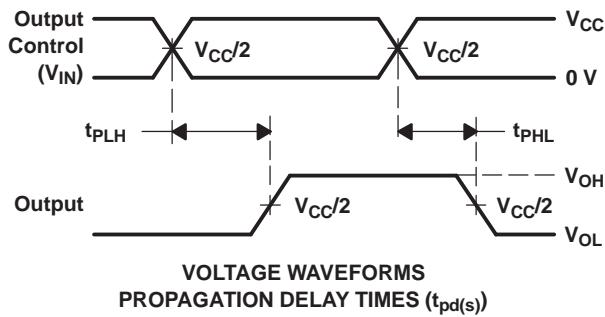
## 6.7 Typical Characteristics



## 7 Parameter Measurement Information



TEST	$V_{CC}$	$S1$	$R_L$	$V_I$	$C_L$	$V_\Delta$
$t_{pd(s)}$	$2.5\ V \pm 0.2\ V$ $3.3\ V \pm 0.3\ V$	Open Open	$500\ \Omega$ $500\ \Omega$	$3.6\ V$ or GND $5.5\ V$ or GND	$30\ pF$ $50\ pF$	
$t_{PLZ}/t_{PZL}$	$2.5\ V \pm 0.2\ V$ $3.3\ V \pm 0.3\ V$	$2 \times V_{CC}$ $2 \times V_{CC}$	$500\ \Omega$ $500\ \Omega$	GND GND	$30\ pF$ $50\ pF$	$0.15\ V$ $0.3\ V$
$t_{PHZ}/t_{PZH}$	$2.5\ V \pm 0.2\ V$ $3.3\ V \pm 0.3\ V$	Open Open	$500\ \Omega$ $500\ \Omega$	$3.6\ V$ $5.5\ V$	$30\ pF$ $50\ pF$	$0.15\ V$ $0.3\ V$



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\ MHz$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\ ns$ ,  $t_f \leq 2.5\ ns$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd(s)}$ . The  $t_{pd}$  propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- All parameters and waveforms are not applicable to all devices.

**Figure 4. Test Circuit and Voltage Waveforms**

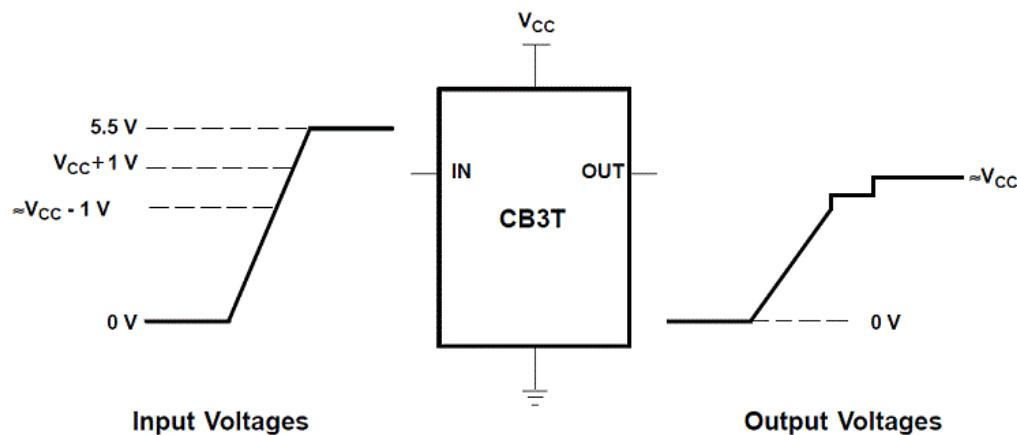
## 8 Detailed Description

### 8.1 Overview

The SN74CB3T3306 device is organized as two 1-bit bus switches with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When  $\overline{OE}$  is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CB3T3306 device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



**Figure 5. Typical DC Voltage-Translation Characteristics**

## 8.2 Functional Block Diagrams

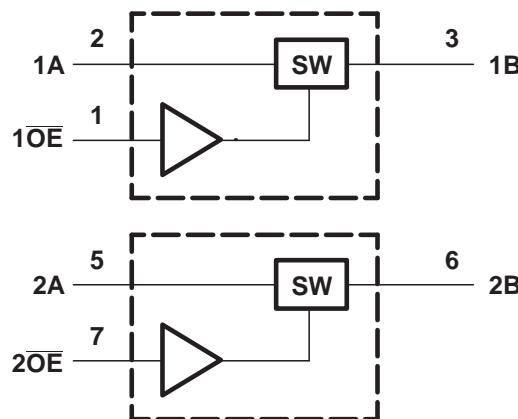
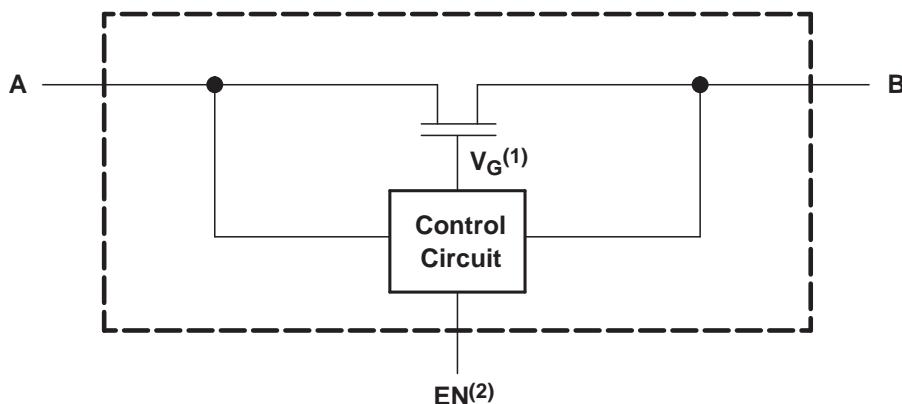


Figure 6. Functional Block Diagram, SN74CB3T3306



- (1) Gate voltage ( $V_G$ ) is approximately equal to  $V_{CC} + V_T$  when the switch is ON and  $V_I > V_{CC} + V_T$ .
- (2) EN is the internal enable signal applied to the switch.

Figure 7. Simplified Schematic, Each FET Switch (SW)

## 8.3 Feature Description

The SN74CB3T3306 is ideal for low-power portable equipment. Power consumption is low by design,  $I_{CC} = 20 \mu A$ . On-state resistance is low ( $r_{on} = 5 \Omega$ ). It has bidirectional data flow with near zero propagation delay. The devices minimizes loading due to the low input/output capacitance  $C_{io(OFF)} = 4.5 \text{ pF Typ}$ . Operating  $V_{CC}$  range from 2.3 V to 3.6 V. The output tracks  $V_{CC}$ . Data and control inputs provide undershoot clamp diodes. Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs. It supports mixed-mode signal operation on all data I/O ports. Data I/Os support 0- to 5-V signaling levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V). The device is protected from damaging current,  $I_{off}$  supports partial shutdown which prevents the current from flowing back through the device when it is powered down. In addition, it has 5-V tolerant I/Os with device powered up or powered down. The device is latch-up resistant with 250 mA exceeding the JESD 17 standard, providing protection from destruction due to latch-up. This device is protected against electrostatic discharge. It is tested per JESD 22 using 2000-V Human-Body Model (A114-B, Class II), and 1000-V Charged-Device Model (C101).

## 8.4 Device Functional Modes

Table 1 lists the functional modes for the SN74CB3T3306.

**Table 1. Function Table**

INPUT OE	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Hi-Z	Disconnect

## 9 Application and Implementation

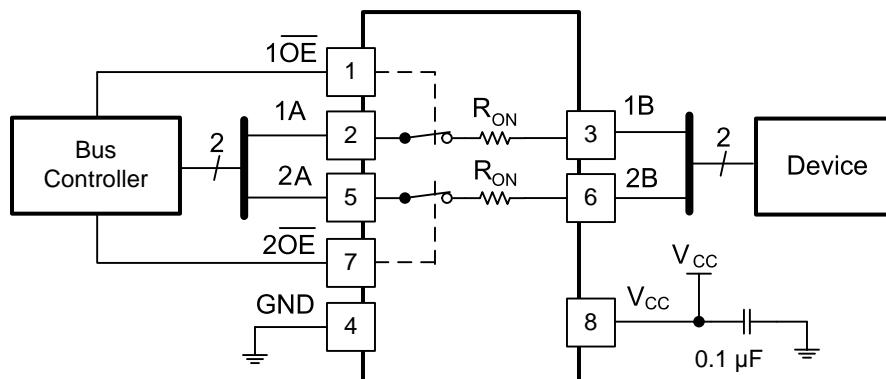
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

This application is specifically to connect a 5-V bus to a 3.3 V device. Ideally, set  $V_{CC}$  to 3.3 V. It is assumed that communication in this particular application is one-directional, going from the bus controller to the device.

### 9.2 Typical Application



**Figure 8. Typical Application Diagram**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

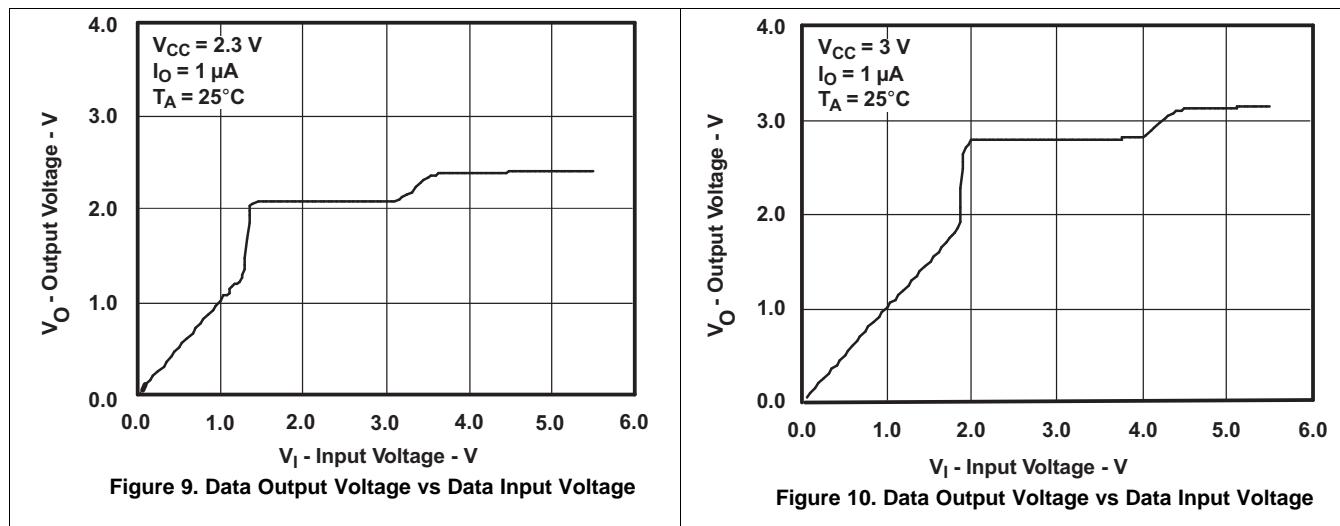
Because this design is for down-translating voltage, no pull-up resistors are required.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input conditions
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in [Recommended Operating Conditions](#)
  - Inputs are overvoltage tolerant allowing them to go as high as 7 V at any valid  $V_{CC}$
2. Recommend output conditions
  - Load currents should not exceed 128 mA on each channel

## Typical Application (continued)

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

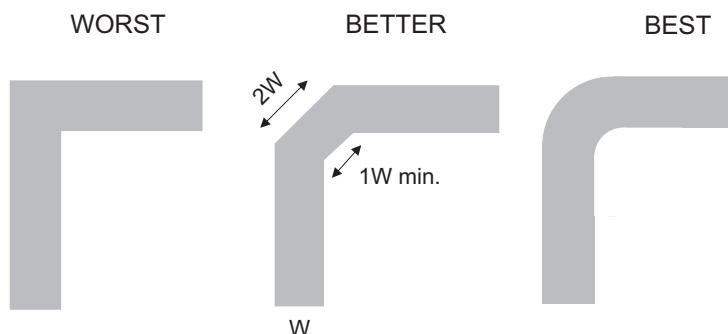
Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F bypass capacitor is recommended. If there are multiple pins labeled  $V_{CC}$ , then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu$ F bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 11](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

## 11.2 Layout Example



**Figure 11. Trace Example**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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### 12.3 Trademarks

E2E is a trademark of Texas Instruments.

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### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

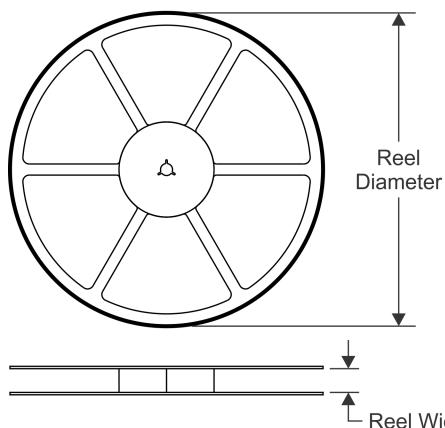
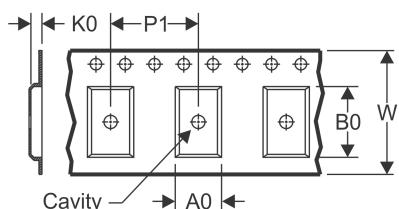
### 12.5 Glossary

[SLYZ022](#) — **TI Glossary.**

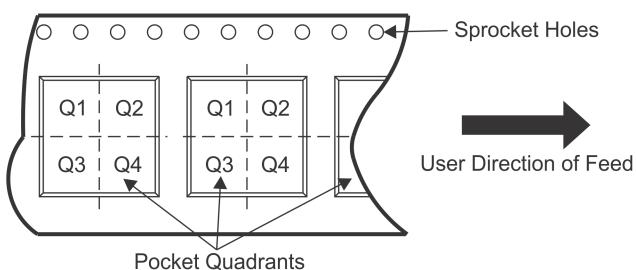
This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3T3306DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3T3306DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74CB3T3306DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3T3306DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3

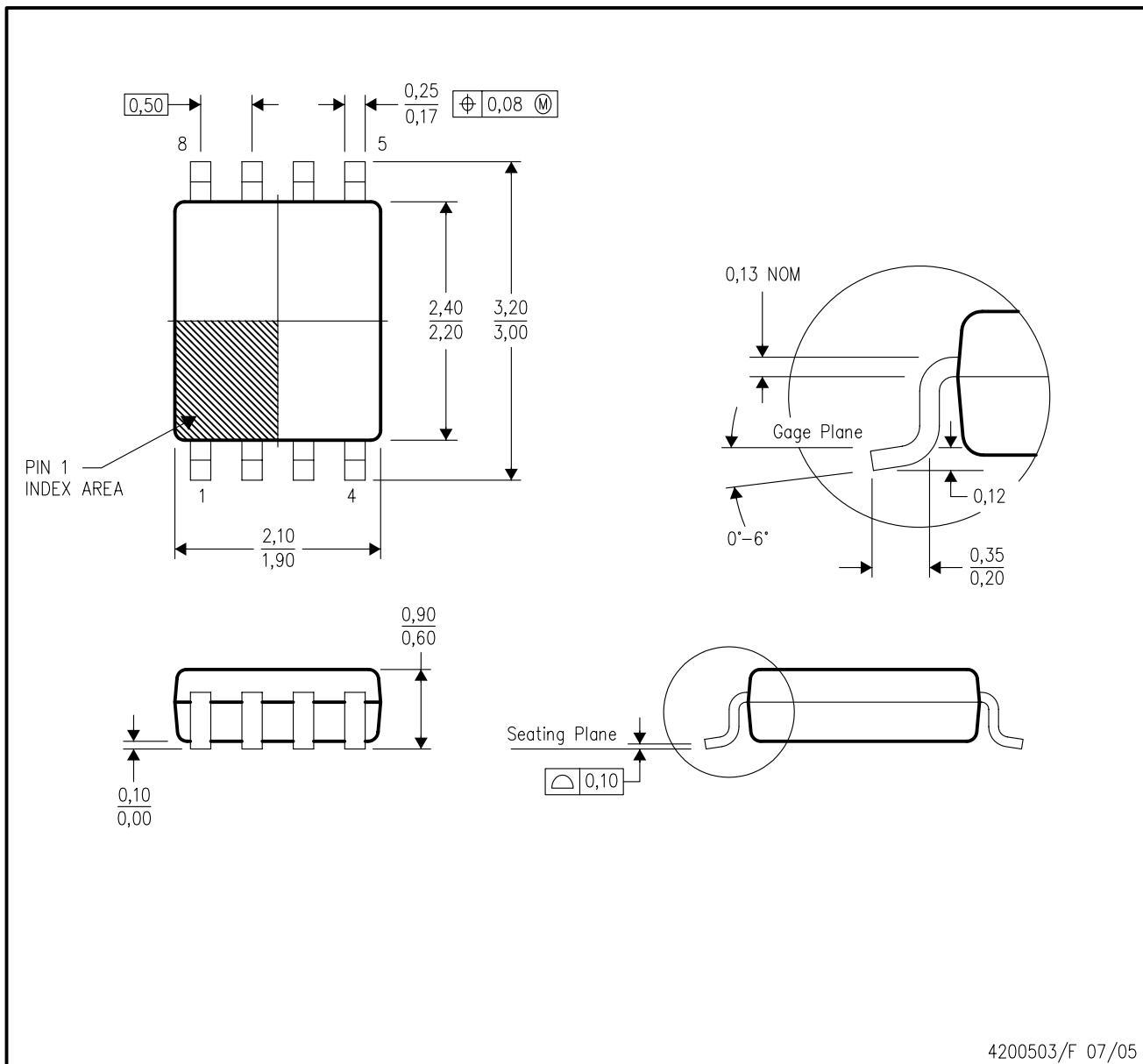
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3T3306DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3T3306DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74CB3T3306DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3T3306DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0

## DCU (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



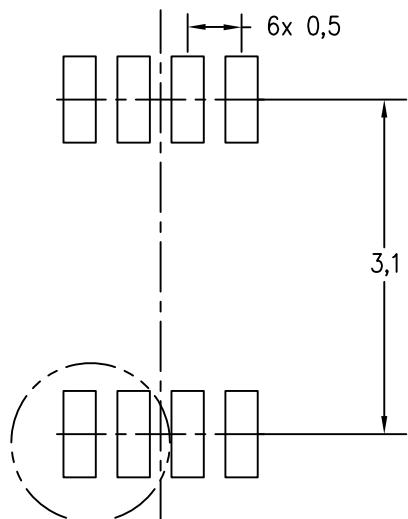
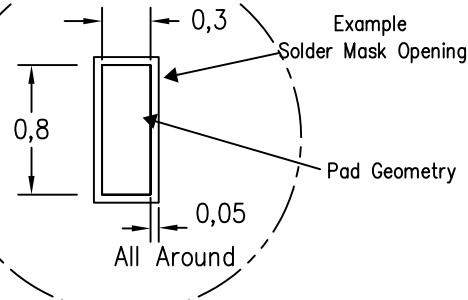
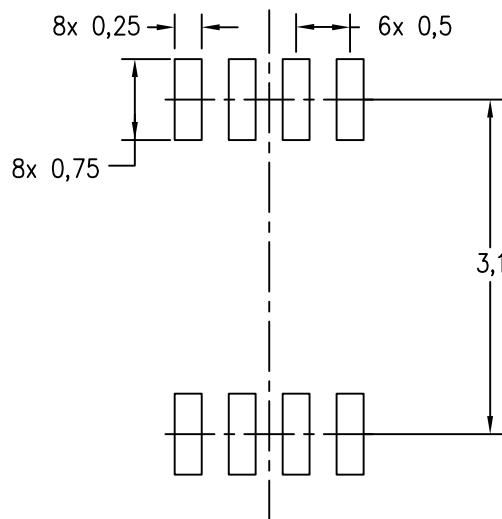
4200503/F 07/05

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

Example Board Layout  
(Note C,E)Example Stencil Design  
(Note D)

4210064/C 04/12

NOTES:

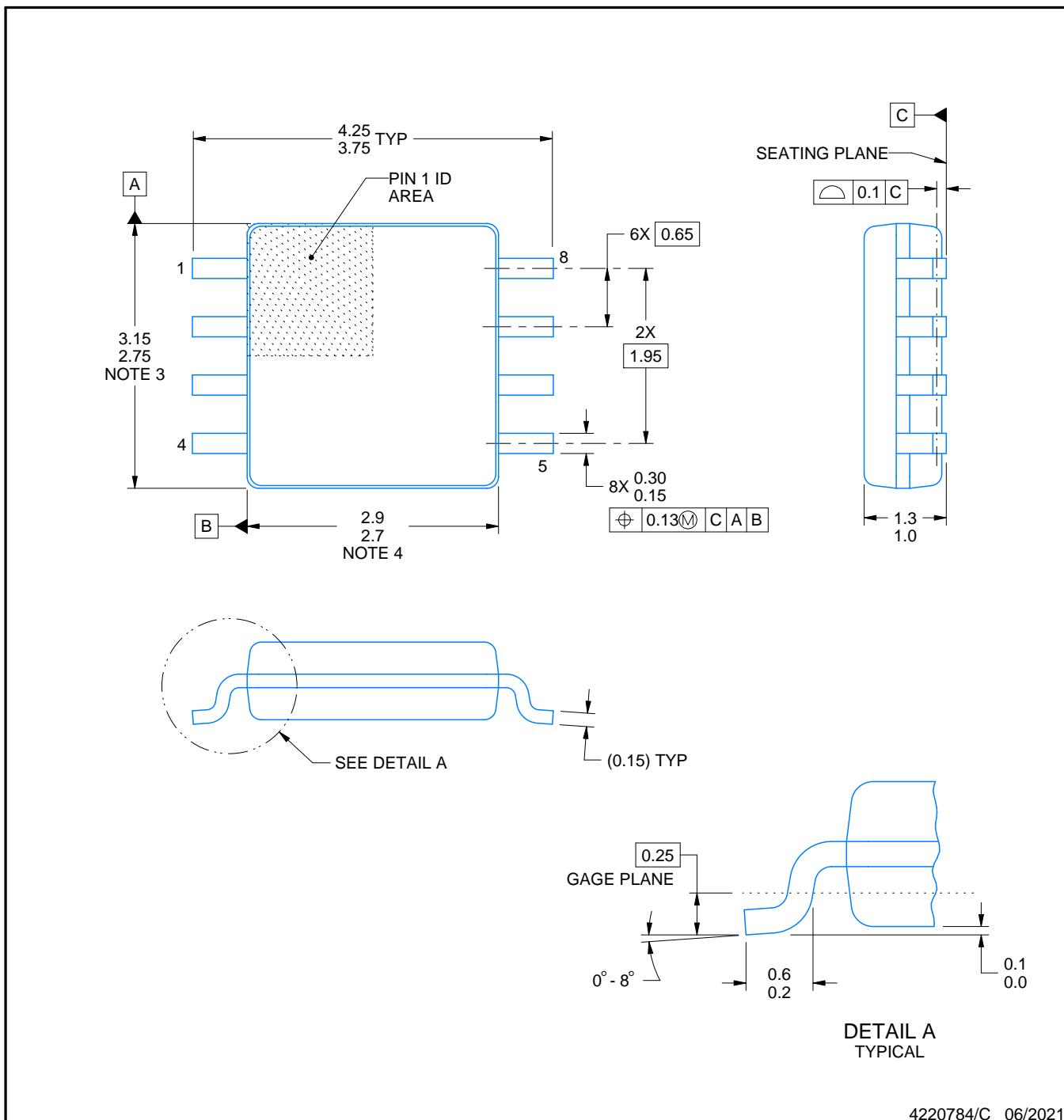
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## PACKAGE OUTLINE

## SSOP - 1.3 mm max height

## SMALL OUTLINE PACKAGE



## NOTES:

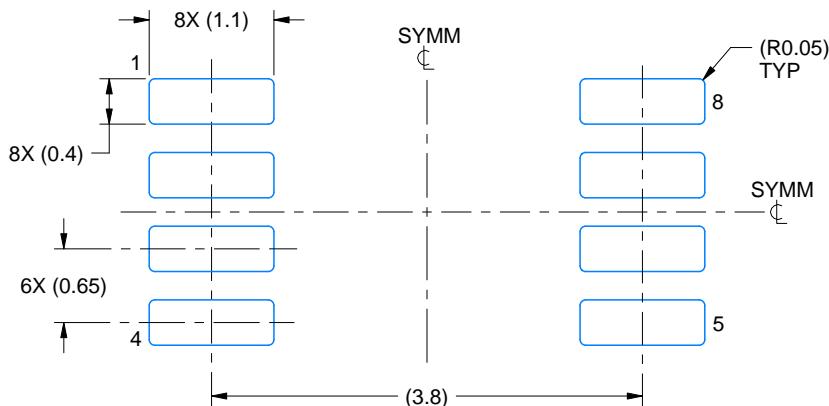
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

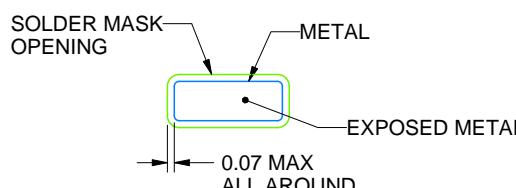
DCT0008A

SSOP - 1.3 mm max height

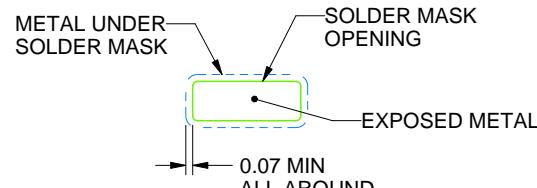
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

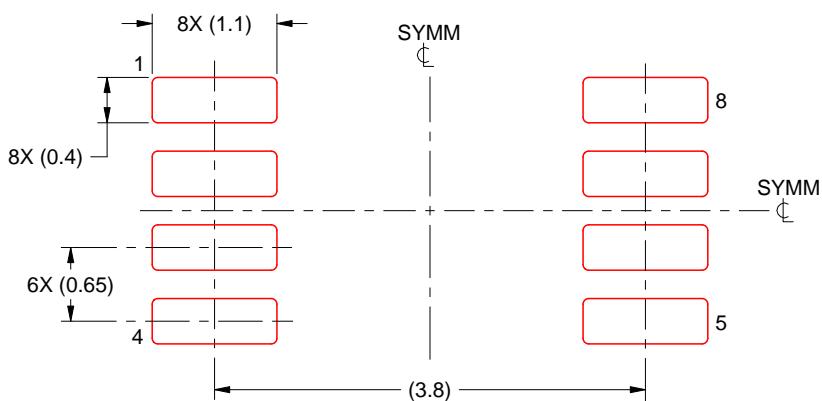
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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