SN74LV1T32 单电源 2 输入正或门 CMOS 逻辑电平转换器

1 特性

- 电压为 5.0/3.3/2.5/1.8V 的单电源电压转换器 V_{CC}
- 1.8V 至 5.5V 的工作电压范围
- 上行转换
  - 1.8V V_{CC} 时，1.2V(1) 至 1.8V
  - 2.5V V_{CC} 时，1.5V(1) 至 2.5V
  - 3.3V V_{CC} 时，1.8V(1) 至 3.3V
  - 5.0V V_{CC} 时，3.3V 至 5.0V
- 下行转换
  - 1.8V V_{CC} 时，3.3V 至 1.8V
  - 2.5V V_{CC} 时，3.3V 至 2.5V
  - 3.3V V_{CC} 时，5.0V 至 3.3V
- 逻辑输出以 V_{CC} 为基准
- 输出驱动
  - 5V 时，8mA 的输出驱动
  - 3.3V 时，7mA 的输出驱动
  - 1.8V 时，3mA 的输出驱动
- 3.3V V_{CC} 时，频率高达 50MHz
- 输入引脚可耐受 5V 电压
- -40°C 至 125°C 工作温度范围
- 采用无铅封装：SC-70 (DCK)
  - 2mm x 2.1mm x 0.65 mm（高度 1.1mm）
- 锁断性能超过 250mA 符合 JESD 17 规范
- 静电放电 (ESD) 性能测试符合 JESD 22 规范
  - 2000V 人体模型（A114-B，II 类）
  - 200V 机器模型 (A115-A)
  - 1000V 充电器件模型 (C101)
- 支持标准逻辑引脚分配
- 与 AUP1G 和 LVC1G 系列兼容的 CMOS 输出 B

(1) 请参考更低 V_{CC} 条件下的 V_{IH}/V_{IL} 和输出驱动。

2 应用范围

- 工业用控制器
- 电信
- 便携式应用
- 服务器
- 个人电脑和笔记本电脑
- 汽车

3 说明

SN74LV1T32 是一款具有较宽电压范围的低压 CMOS 门逻辑电路，用于工业、便携、电信和汽车应用。 输出电平以电源电压为基准，并且能够支持 1.8V/2.5V/3.3V/5V CMOS 电平。

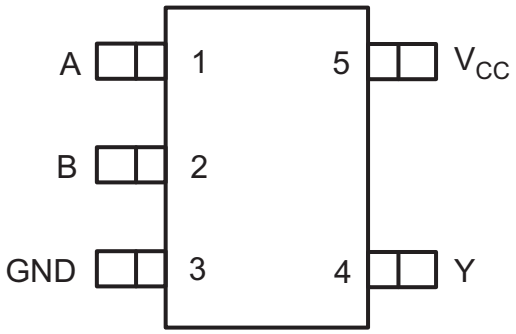
采用了更低阀值电路来设计此输入，以便匹配 V_{CC} = 3.3V 时的 1.8V 输入逻辑，并且可被用于 1.8V 至 3.3V 电平上行转换。 此外，5V 容限输入引脚可实现下行转换（例如，V_{CC} = 2.5V 时的 3.3V 至 2.5V 输出转换）。 1.8V 至 5.5V 的宽 V_{CC} 范围可使所需输出电平的生成接至控制器或处理器。

SN74LV1T32 被设计成具有 8mA 的电流驱动能力，以减少由高驱动输出导致的线路反射、过冲和下冲。

器件信息

订货编号	封装	封装尺寸
SN74LV1T32DBVR	小外形尺寸晶体管封装 (SOT)-23 (5)	2.90mm x 1.60mm
SN74LV1T32DCKR	SC70 (5)	2.00mm x 1.25mm

DCK/DBV/DRL 封装
（顶视图）



目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2013) to Revision A **Page**

- 已更新文档格式。 1
- Updated Electrical Characteristics table. 6
- Updated V_{CC} values for V_{IH} parameter in the ELECTRICAL CHARACTERISTICS table. 6
- Removed I_{OH} = –2.3 mA test condition for V_{OH} parameter. 6
- Removed I_{OH} = –2.3 mA test condition for V_{OL} parameter. 7

Function Table

INPUT (Lower Level Input)		OUTPUT (V_{CC} CMOS)
A	B	Y
H	X	H
X	H	H
L	L	L
SUPPLY V_{CC} = 3.3V		
A	B	Y
V_{IH}(min) =1.35 V V_{IL}(max) =0.08 V		V_{OH}(min) = 2.9 V V_{OL}(max)= 0.2 V

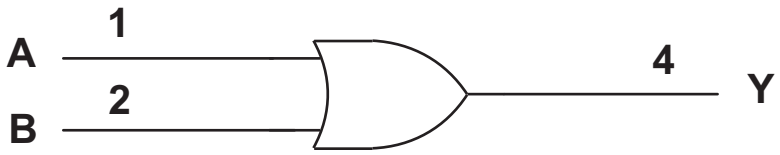


Figure 1. Logic Diagram

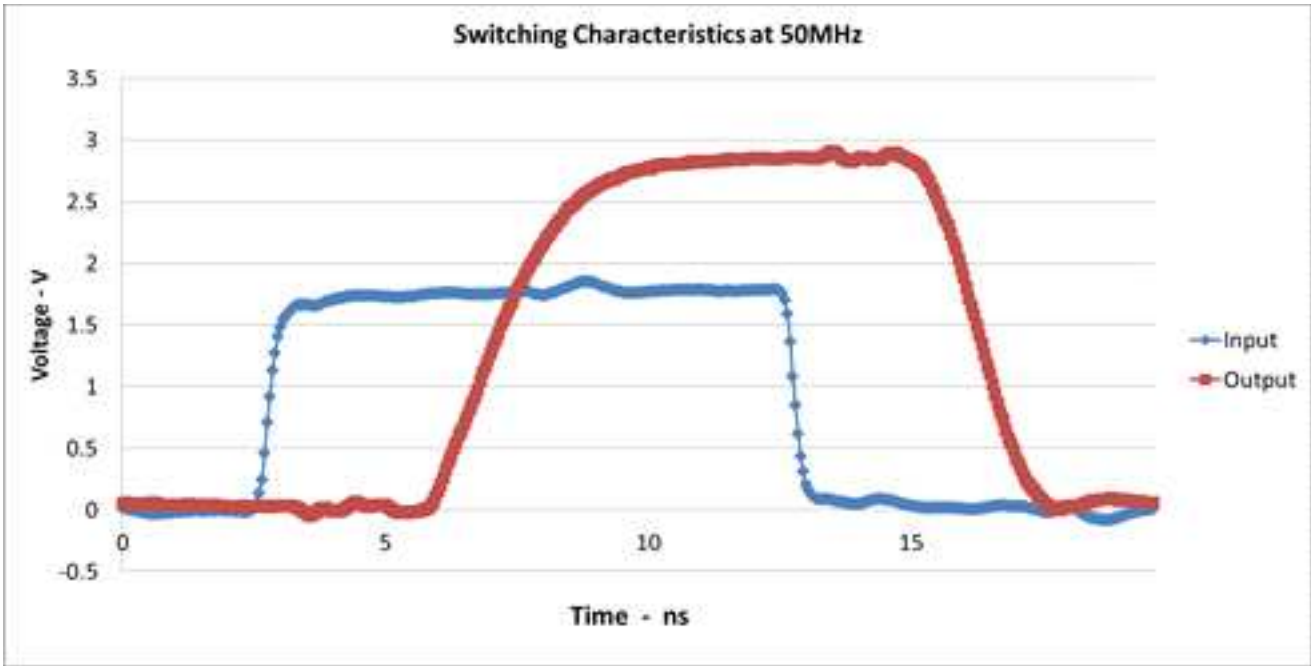


Figure 2. Excellent Signal Integrity (1.8V to 3.3V at 3.3V V_{CC})

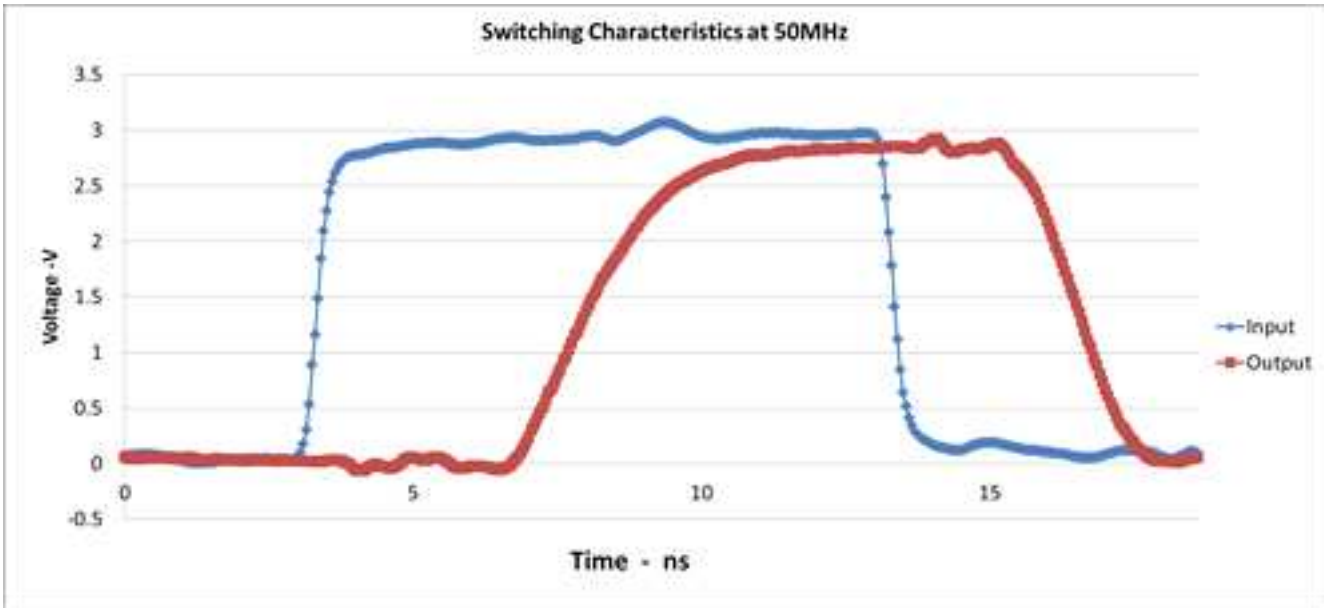


Figure 3. Excellent Signal Integrity (3.3V to 3.3V at 3.3V V_{CC})

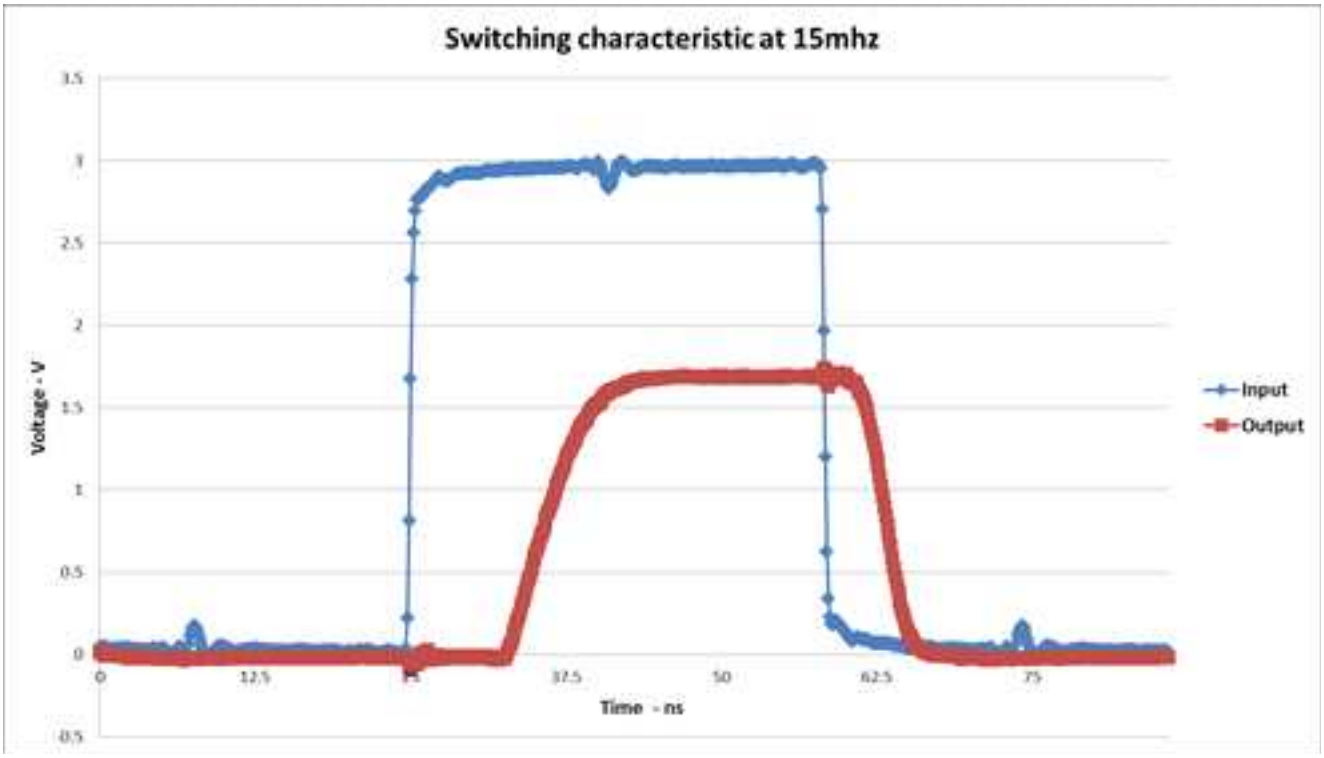


Figure 4. Excellent Signal Integrity (3.3V to 1.8V at 1.8V V_{CC})

4.1 Typical Design Examples

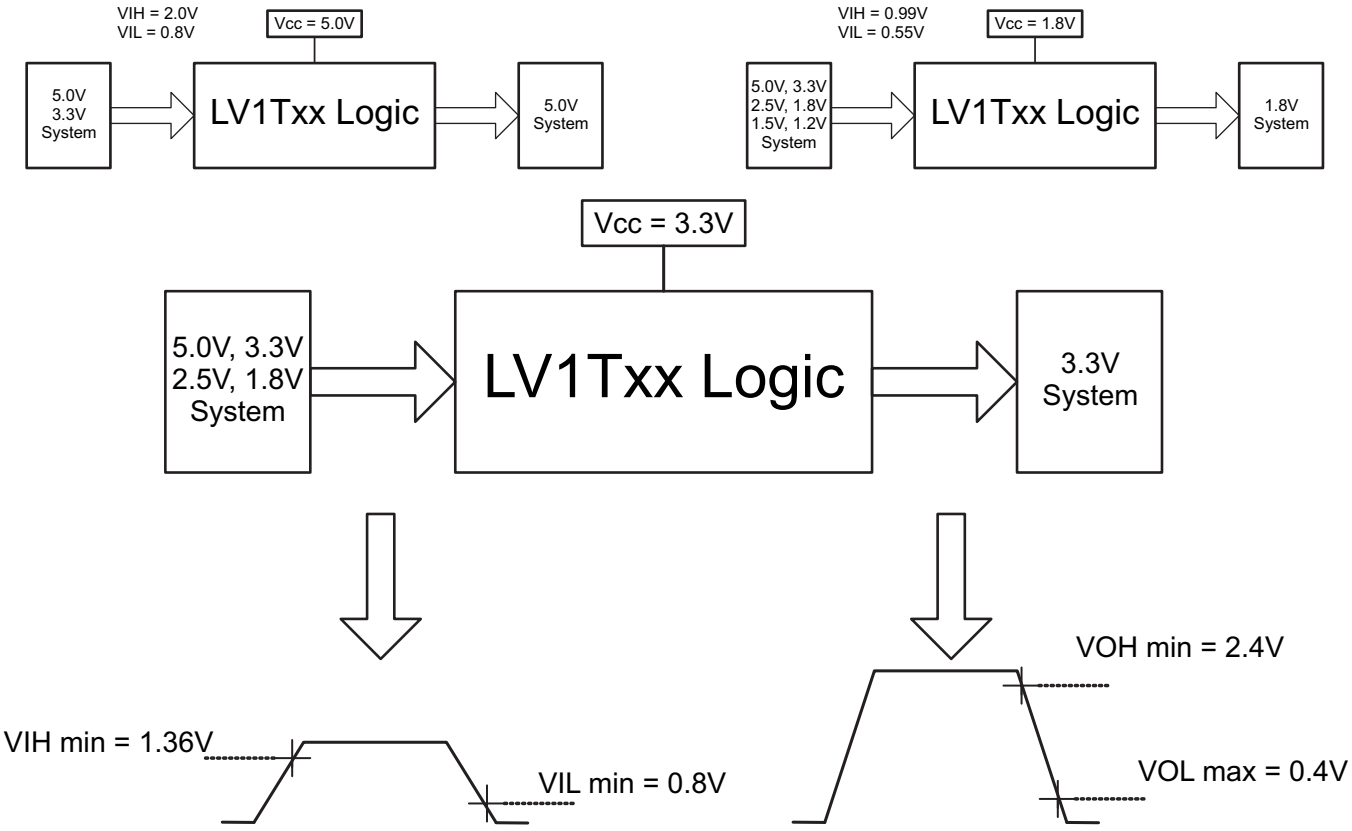


Figure 5. Switching Thresholds for 1.8-V to 3.3-V Translation

4.2 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7.0	V
V_I	Input voltage range(2)		–0.5	7.0	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
	Voltage range applied to any output in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current			±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DBV package		206	°C/W
		DCK package		252	
		DRL package			
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

4.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		–3	mA
		V_{CC} = 2.5 V		–5	
		V_{CC} = 3.3 V		–7	
		V_{CC} = 5.0 V		–8	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		3	mA
		V_{CC} = 2.5 V		5	
		V_{CC} = 3.3 V		7	
		V_{CC} = 5.0 V		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V		20	ns/V
		V_{CC} = 3.3 V or 2.5 V		20	
		V_{CC} = 5.0 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{IH}	High-level input voltage		1.65 V to 1.8 V	0.94			1.0		V
			2.0 V	0.99			1.03		
			2.25 V to 2.5 V	1.135			1.18		
			2.75 V	1.21			1.23		
			3 V to 3.3 V	1.35			1.37		
			3.6 V	1.47			1.48		
			4.5 V to 5.0 V	2.02			2.03		
			5.5 V	2.1			2.11		
V_{IL}	Low-level input voltage		1.65 V to 2.0 V			0.58		0.55	V
			2.25 V to 2.75 V			0.75		0.71	
			3 V to 3.6 V			0.8		0.65	
			4.5 V to 5.5 V			0.8		0.8	
V_{OH}		I_{OH} = –20 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –2.0 mA	1.65 V	1.28			1.21		V
			1.8V	1.5			1.45		
		I_{OH} = –3 mA	2.3V	2.0			1.93		V
		I_{OH} = –3 mA	2.5V	2.25			2.15		V
		I_{OH} = –3.0 mA	3.0 V	2.78			2.7		V
		I_{OH} = –5.5 mA		2.6			2.49		
		I_{OH} = –5.5 mA	3.3 V	2.9			2.8		
		I_{OH} = –4 mA	4.5 V	4.2			4.1		V
		I_{OH} = –8 mA		4.1			3.95		
		I_{OH} = –8 mA	5.0 V	4.6			4.5		

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OL}	I_{OL} = 20 µA	1.65 V to 5.5 V			0.1		0.1	V
	I_{OL} = 2.0 mA	1.65 V			0.2		0.25	
	I_{OH} = 3 mA	2.3V			0.15		0.2	
	I_{OL} = 3 mA	3.0 V			0.1		0.15	
	I_{OL} = 5.5 mA				0.2		0.252	
	I_{OL} = 4 mA	4.5 V			0.15		0.2	
	I_{OL} = 8 mA				0.3		0.35	
I_I A input	V_I = 0 V or V_{CC}	0V, 1.8V, 2.5V, 3.3V, 5.5 V			0.1		±1	µA
I_{CC}	V_I = 0 V or V_{CC}, I_O = 0; open on loading	5.0 V			1		10	µA
		3.3 V			1		10	
		2.5 V			1		10	
		1.8V			1		10	
ΔI_{CC}	One input at 0.3V or 3.4V, Other inputs at 0 or V_{CC}, I_O = 0	5.5 V			1.35		1.5	mA
	One input at 0.3V or 1.1V Other inputs at 0 or V_{CC}, I_O = 0	1.8V			10		10	µA
C_i	V_I = V_{CC} or GND	3.3 V		2	10	2	10	pF
C_o	V_O = V_{CC} or GND	3.3 V		2.5		2.5		pF

4.5 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7)

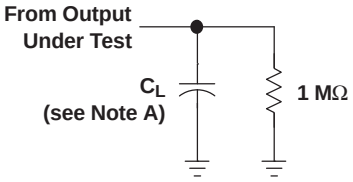
PARAMETER	FROM (INPUT)	TO (OUTPUT)	FREQUENCY (TYP)	V_{CC}	C_L	T_A = 25°C			T_A = –65°C to 125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Any In	Y	DC to 50 MHz	5.0V	15pF		4	5		4	5	ns
					30pF		5.5	7.0		5.5	7.0	
				3.3V	15pF		4.8	5		5	5.5	ns
					30pF		5	5.5		5.5	6.5	
			DC to 25 MHz	2.5V	15pF		6	6.5		7	7.5	ns
					30pF		6.5	7.5		7.5	8.5	
			DC to 15 MHz	1.8V	15pF		10.5	11		11	12	ns
					30pF		12	13		12	14	

4.6 Operating Characteristics

T_A = 25°C

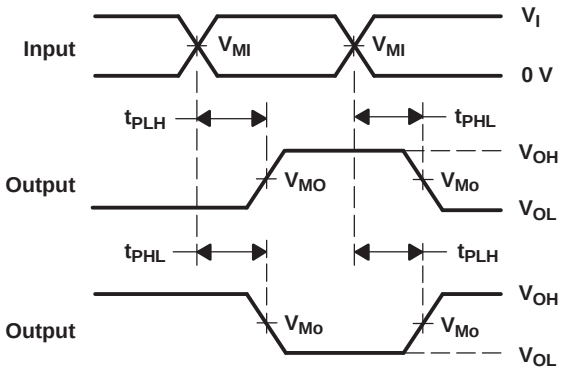
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	f = 1 MHz and 10 MHz	1.8 V ± 0.15 V	14	pF
		2.5 V ± 0.2 V	14	
		3.3 V ± 0.3 V	14	
		5.5 V ± 0.5 V	14	

5 Parameter Measurement Information



LOAD CIRCUIT

	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_{MI}	V_I/2	V_I/2
V_{MO}	V_{CC}/2	V_{CC}/2



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 6. Load Circuit and Voltage Waveforms

5.1 More Product Selection

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T08	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T17	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T50	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV1T126	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV4T125	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs

6 器件和文档支持

6.1 Trademarks

All trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

7 机械，封装和可订购信息

下列封装信息和附录反映了针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV1T32DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(NEG3, NEGJ, NEGS)	Samples
SN74LV1T32DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NEG3	Samples
SN74LV1T32DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(WG3, WGJ, WGS)	Samples
SN74LV1T32DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		WG3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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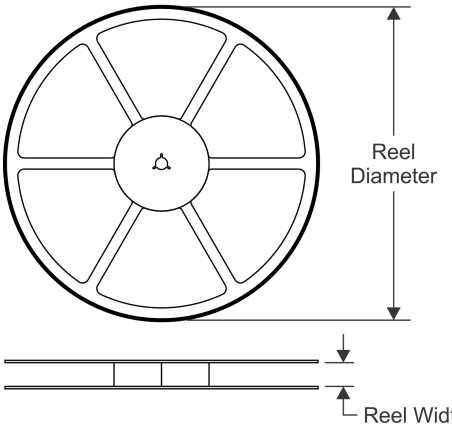
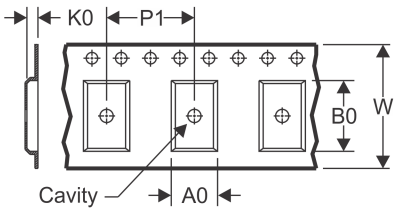
TAPE AND REEL INFORMATION

REEL DIMENSIONS

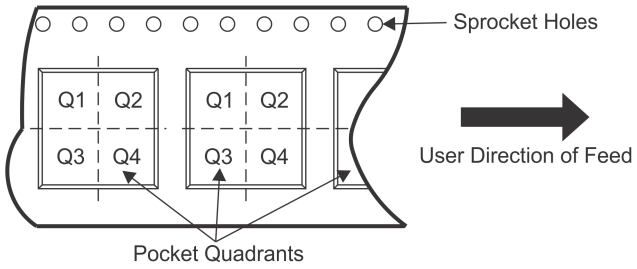


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

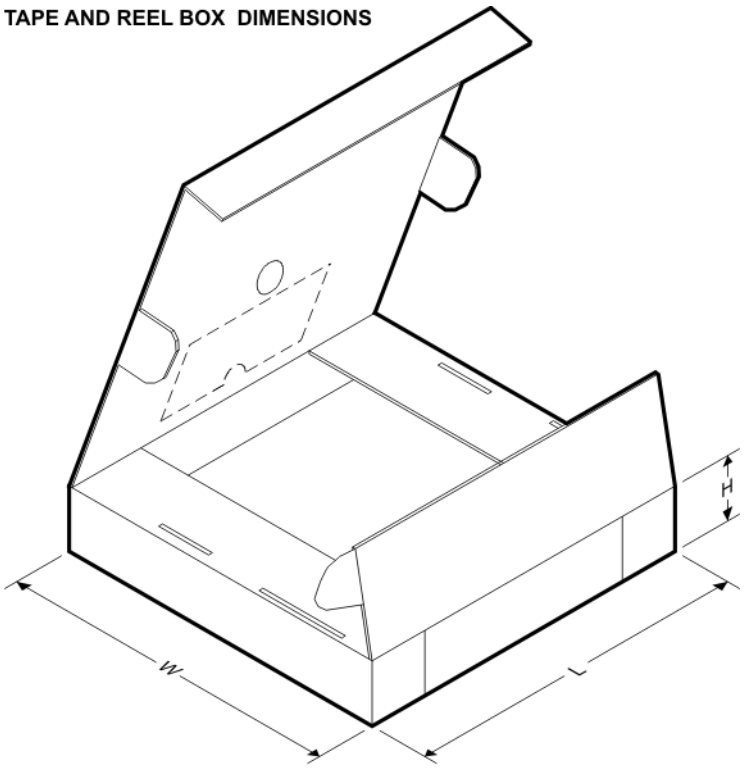
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV1T32DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LV1T32DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LV1T32DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LV1T32DBVRG4	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LV1T32DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LV1T32DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LV1T32DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LV1T32DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

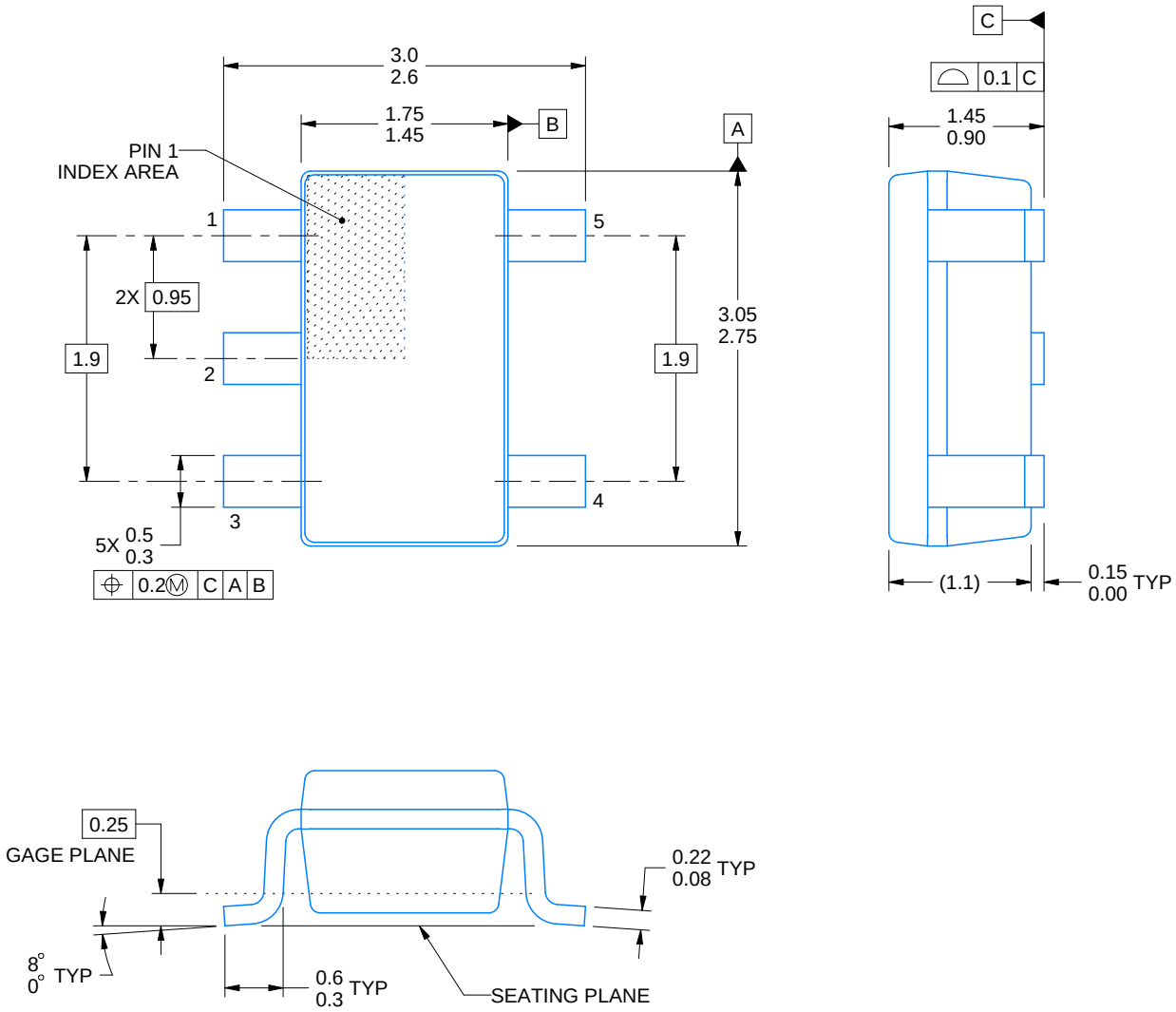
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV1T32DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LV1T32DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T32DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T32DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T32DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LV1T32DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LV1T32DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LV1T32DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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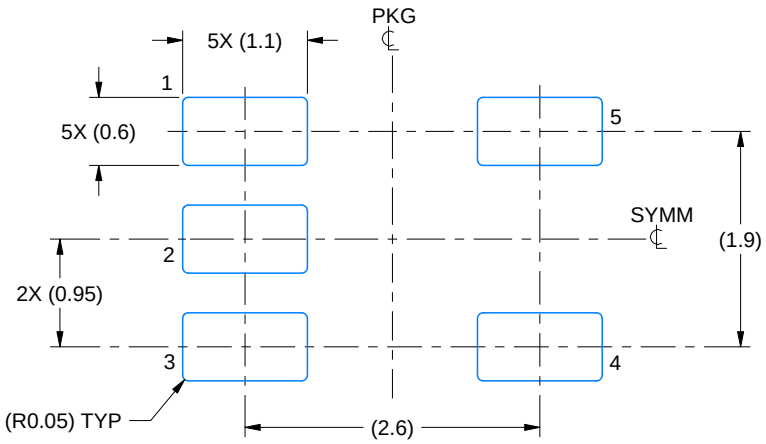
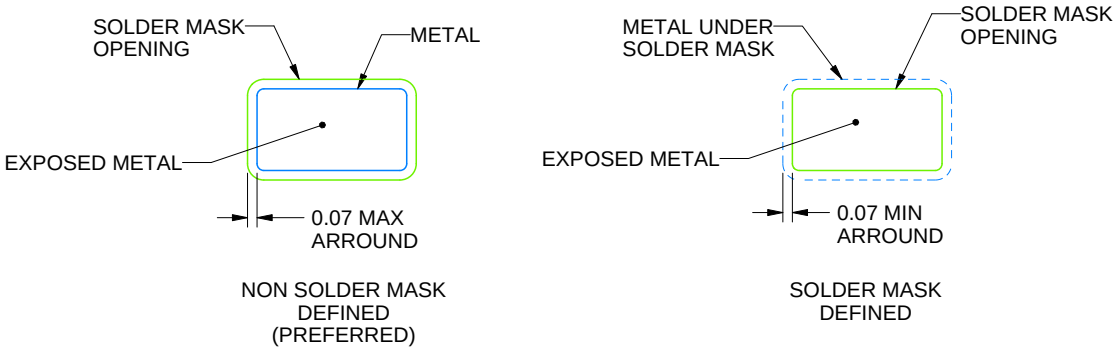
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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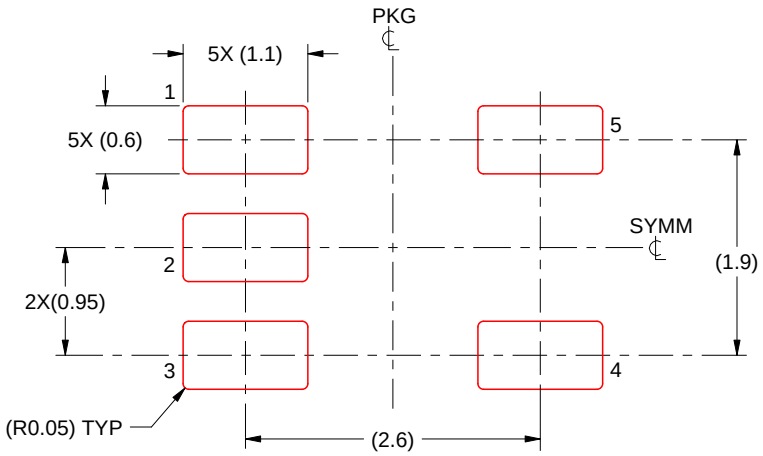
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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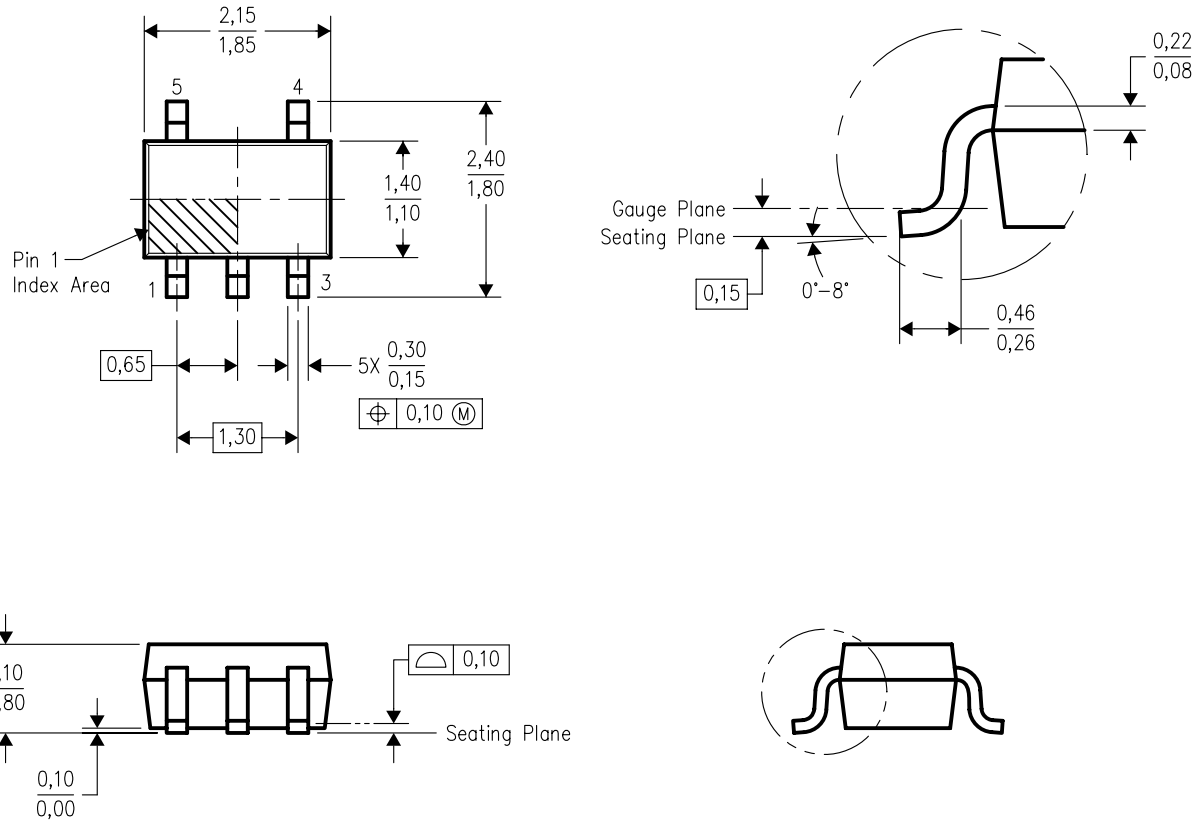
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

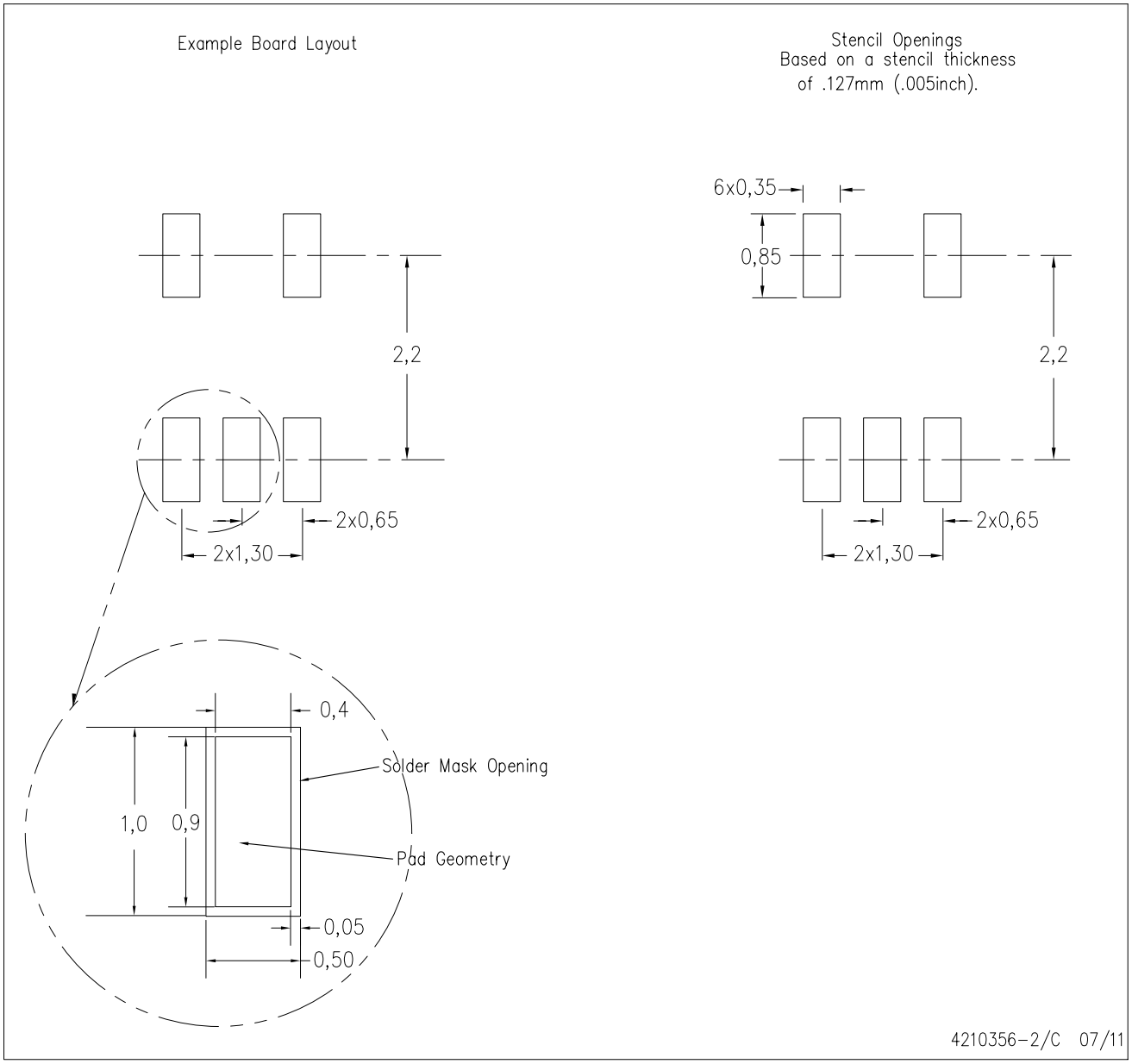
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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