

# TCA9544A 低压 4 通道 I<sup>2</sup>C 和系统管理总线 (SMBus) 复用器, 具有中断逻辑电路

## 1 特性

- 4 选 1 双向转换开关
- 与 I<sup>2</sup>C 总线和 SMBus 兼容
- 四个低电平有效中断输入
- 低电平有效中断输出
- 三个地址引脚, I<sup>2</sup>C 总线上最多支持八个 TCA9544A 器件
- 通过 I<sup>2</sup>C 总线选择通道
- 加电时所有开关通道取消选定
- 低 R<sub>ON</sub> 开关
- 支持 1.8V, 2.5V, 3.3V 和 5V 总线间的电压电平转换
- 加电时无毛刺脉冲
- 支持热插入
- 低待机电流
- 工作电源电压范围: 1.65V 至 5.5V
- 5.5V 耐压输入
- 0 至 400kHz 时钟频率
- 锁断性能超过了 100mA, 符合 JESD 78 规范
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
  - 4000V 人体放电模式 (A114-A)
  - 1500V 充电器件模型 (C101)

## 2 应用

- 服务器
- 路由器 (电信交换设备)
- 工厂自动化
- 具有 I<sup>2</sup>C 从地址冲突 (例如, 多个、完全一样的温度传感器) 的产品

## 3 说明

TCA9544A 是一款四通道双向转换 I<sup>2</sup>C 多路复用器。主 SCL/SDA 信号对可定向到从器件的四个通道 (SC0/SD0-SC3/SD3) 中的任一个。提供四个中断输入 (INT3-INT0), 每个中断输入针对一个下行对。一个中断输出 (INT) 可作为四个中断输入的与 (AND) 操作。

一个加电复位功能使寄存器返回到缺省状态, 并且初始化 I<sup>2</sup>C 状态机, 此时所有通道都取消选定。

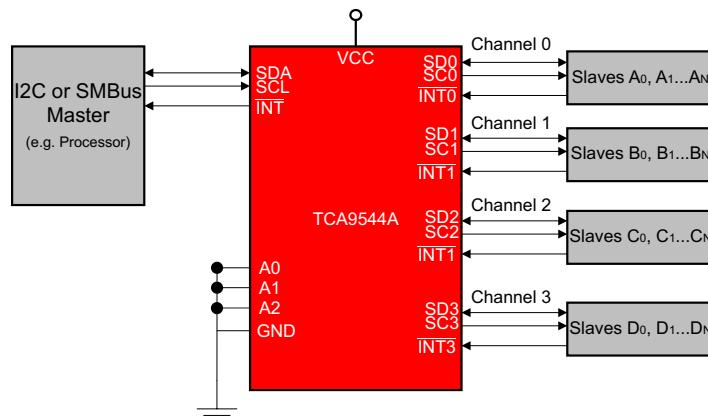
在开关上建有导通栅极, 这样的话, VCC 引脚可被用于限制将由 TCA9544A 传递的最大高压。这允许在每个对上使用不同的总线电压, 以便 1.8V, 2.5V 或 3.3V 部件可以在没有任何额外保护的情况下与 5V 部件通信。对于每个通道, 外部上拉电阻器将总线电压上拉至所需的电压电平。所有 I/O 引脚可耐受 5.5V 电压。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TCA9544A	薄型小外形尺寸封装 (TSSOP) (20)	6.50mm × 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

### 简化原理图



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## 4 修订历史记录

## Changes from Revision B (May 2018) to Revision C Page

• Changed $V_{CC}$ = 1.65 V to 5.5 V To: $V_{CC}$ = 2.5 V in <a href="#">Figure 15</a> .....	16
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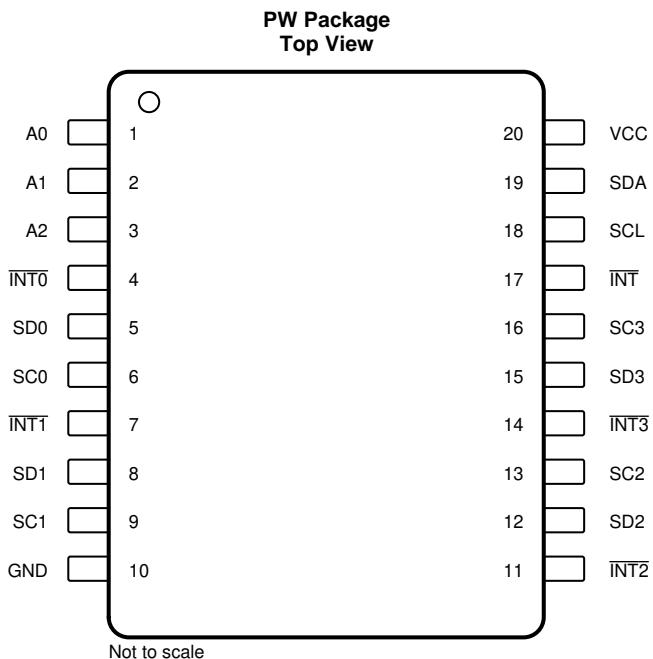
## Changes from Revision A (May 2014) to Revision B Page

• 更改了“说明”中的第一段 .....	1
• Added $T_{stg}$ to the <i>Absolute Maximum Ratings</i> table .....	4
• Changed the first paragraph of the <i>Overview</i> section .....	10
• Changed “switch” to “multiplexer” in the <i>Feature Description</i> section .....	11
• Changed text in the <i>Control Register Definition</i> section From: “One or several SCn/SDn downstream pairs, or channels, are selected...” To: “One SCn/SDn downstream pair, or channel, is selected...” .....	14

## Changes from Original (May 2014) to Revision A Page

• 已将文档从预览更新为生产数据。 .....	1
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## 5 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NO.	
A0	1	Address input 0. Connect directly to $V_{CC}$ or ground.
A1	2	Address input 1. Connect directly to $V_{CC}$ or ground.
A2	3	Address input 2. Connect directly to $V_{CC}$ or ground.
INT0	4	Active-low interrupt input 0. Connect to $V_{DPU0}$ <sup>(1)</sup> through a pull-up resistor.
SD0	5	Serial data 0. Connect to $V_{DPU0}$ <sup>(1)</sup> through a pull-up resistor.
SC0	6	Serial clock 0. Connect to $V_{DPU0}$ <sup>(1)</sup> through a pull-up resistor.
INT1	7	Active-low interrupt input 1. Connect to $V_{DPU1}$ <sup>(1)</sup> through a pull-up resistor.
SD1	8	Serial data 1. Connect to $V_{DPU1}$ <sup>(1)</sup> through a pull-up resistor.
SC1	9	Serial clock 1. Connect to $V_{DPU1}$ <sup>(1)</sup> through a pull-up resistor.
GND	10	Ground
INT2	11	Active-low interrupt input 2. Connect to $V_{DPU2}$ <sup>(1)</sup> through a pull-up resistor.
SD2	12	Serial data 2. Connect to $V_{DPU2}$ <sup>(1)</sup> through a pull-up resistor.
SC2	13	Serial clock 2. Connect to $V_{DPU2}$ <sup>(1)</sup> through a pull-up resistor.
INT3	14	Active-low interrupt input 3. Connect to $V_{DPU3}$ <sup>(1)</sup> through a pull-up resistor.
SD3	15	Serial data 3. Connect to $V_{DPU3}$ <sup>(1)</sup> through a pull-up resistor.
SC3	16	Serial clock 3. Connect to $V_{DPU3}$ <sup>(1)</sup> through a pull-up resistor.
INT	17	Active-low interrupt output. Connect to $V_{DPUM}$ <sup>(1)</sup> through a pull-up resistor.
SCL	18	Serial clock line. Connect to $V_{DPUM}$ <sup>(1)</sup> through a pull-up resistor.
SDA	19	Serial data line. Connect to $V_{DPUM}$ <sup>(1)</sup> through a pull-up resistor.
VCC	20	Supply power

(1)  $V_{DPUX}$  is the pull-up reference voltage for the associated data line.  $V_{DPUM}$  is the master I<sup>2</sup>C reference voltage while  $V_{DPU0}$  —  $V_{DPU3}$  are the slave channel reference voltages.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	-0.5	7	V
$V_I$	Input voltage <sup>(2)</sup>	-0.5	7	V
$I_I$	Input current		±20	mA
$I_O$	Output current		±25	mA
	Continuous current through $V_{CC}$		±100	mA
	Continuous current through GND		±100	mA
$P_{tot}$	Total power dissipation		400	mW
$T_A$	Operating free-air temperature range	-40	85	°C
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		MIN	MAX	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	-4000	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	-1500	1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	5.5	V
$V_{IH}$	High-level input voltage	$0.7 \times V_{CC}$	6	V
		$0.7 \times V_{CC}$	$V_{CC} + 0.5$	
$V_{IL}$	Low-level input voltage	-0.5	$0.3 \times V_{CC}$	V
		-0.5	$0.3 \times V_{CC}$	
$T_A$	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#), literature number SCBA004.

### 6.4 Thermal Information<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC <sup>(1)</sup>	TCA9544A		UNIT	
	PW	20 PIN		
	20 PIN			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.2	°C/W	
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	51.4	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	69.3	°C/W	
$\Psi_{JT}$	Junction-to-top characterization parameter	7.7	°C/W	
$\Psi_{JB}$	Junction-to-board characterization parameter	68.8	v	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
V <sub>PORR</sub>	Power-on reset voltage, V <sub>CC</sub> rising	No load:	V <sub>I</sub> = V <sub>CC</sub> or GND			1.2	1.5	V	
V <sub>PORF</sub>	Power-on reset voltage, V <sub>CC</sub> falling <sup>(3)</sup>	No load:	V <sub>I</sub> = V <sub>CC</sub> or GND		0.8	1		V	
V <sub>pass</sub>	Switch output voltage	V <sub>SWin</sub> = V <sub>CC</sub>	I <sub>SWout</sub> = -100 μA	5 V		3.6		V	
				4.5 to 5.5 V		2.6	4.5		
				3.3 V		1.9			
				3 to 3.6 V		1.6	2.8		
				2.5 V		1.4			
				2.3 to 2.7 V		1.0	1.8		
				1.8 V		0.8			
				1.65 to 1.95 V		0.5	1.1		
I <sub>OH</sub>	INT̄	V <sub>I</sub> = V <sub>CC</sub>		1.65 to 5.5 V		10		μA	
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 to 5.5 V	3	7		mA	
		V <sub>OL</sub> = 0.6 V			6	10			
		INT̄			3				
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 to 5.5 V			±1		μA	
	SC3–SC0, SD3–SD0					±1			
	A2–A0					±1			
	INT3–INT0					±1			
I <sub>CC</sub>	Operating mode	f <sub>SCL</sub> = 400 kHz	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0 t <sub>r,max</sub> = 300 ns	5.5 V		50		μA	
				3.6 V		20			
				2.7 V		11			
				1.65 V		6			
		f <sub>SCL</sub> = 100 kHz		5.5 V		35			
				3.6 V		14			
				2.7 V		5			
				1.65 V		2			
	Standby mode	Low inputs	V <sub>I</sub> = GND I <sub>O</sub> = 0	5.5 V		1.6	2		
				3.6 V		1.0	1.3		
				2.7 V		0.7	1.1		
				1.65 V		0.4	0.55		
		High inputs	V <sub>I</sub> = V <sub>CC</sub> I <sub>O</sub> = 0	5.5 V		1.6	2		
				3.6 V		1.0	1.3		
				2.7 V		0.7	1.1		
				1.65 V		0.4	0.55		
ΔI <sub>CC</sub>	Supply-current change	INT3–INT0	One INT3–INT0 input at 0.6 V, Other inputs at V <sub>CC</sub> or GND	1.65 to 5.5 V		3	20	μA	
						3	20		
		SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V <sub>CC</sub> or GND			2	15		
						2	15		
C <sub>i</sub>	A2–A0 INT3–INT0	V <sub>I</sub> = V <sub>CC</sub> or GND		1.65 to 5.5 V	4.5	6		pF	
					4.5	6			

(1) For operation between specified voltage ranges, refer to the worst-case parameter in both applicable ranges.

(2) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V<sub>CC</sub>), T<sub>A</sub> = 25°C.

(3) The power-on reset circuit resets the I<sup>2</sup>C bus logic when V<sub>CC</sub> < V<sub>PORF</sub>.

## Electrical Characteristics<sup>(1)</sup> (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
C <sub>IO(OFF)</sub> <sup>(4)</sup>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	Switch OFF	1.65 to 5.5 V	15	19		pF
	SC3–SC0, SD3–SD0				6	8		
R <sub>ON</sub>	Switch-on resistance	V <sub>O</sub> = 0.4 V	I <sub>O</sub> = 15 mA	4.5 to 5.5 V	10	16		Ω
				3 to 3.6 V	13	20		
		V <sub>O</sub> = 0.4 V	I <sub>O</sub> = 10 mA	2.3 to 2.7 V	16	45		
				1.65 to 1.95 V	25	70		

(4) C<sub>IO(ON)</sub> depends on device capacitance and load that is downstream from the device.

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		STANDARD-MODE I <sup>2</sup> C BUS		FAST-MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
t <sub>SCH</sub>	I <sup>2</sup> C clock high time	4		0.6		μs
t <sub>SCL</sub>	I <sup>2</sup> C clock low time	4.7		1.3		μs
t <sub>SP</sub>	I <sup>2</sup> C spike time		50		50	ns
t <sub>SDS</sub>	I <sup>2</sup> C serial-data setup time	250		100		ns
t <sub>SDH</sub>	I <sup>2</sup> C serial-data hold time	0 <sup>(1)</sup>		0 <sup>(1)</sup>		μs
t <sub>ICR</sub>	I <sup>2</sup> C input rise time		1000	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>ICF</sub>	I <sup>2</sup> C input fall time		300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>OCF</sub>	I <sup>2</sup> C output fall time (10-pF to 400-pF bus)		300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>BUF</sub>	I <sup>2</sup> C bus free time between stop and start	4.7		1.3		μs
t <sub>STS</sub>	I <sup>2</sup> C start or repeated start condition setup	4.7		0.6		μs
t <sub>STH</sub>	I <sup>2</sup> C start or repeated start condition hold	4		0.6		μs
t <sub>SPS</sub>	I <sup>2</sup> C stop condition setup	4		0.6		μs
t <sub>VdL(Data)</sub>	Valid-data time (high to low) <sup>(3)</sup>	SCL low to SDA output low valid	1		1	μs
t <sub>VdH(Data)</sub>	Valid-data time (low to high) <sup>(3)</sup>	SCL low to SDA output high valid	0.6		0.6	μs
t <sub>Vd(ack)</sub>	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low	1		1	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V<sub>IH</sub> min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.

(2) C<sub>b</sub> = total bus capacitance of one bus line in pF

(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see [Figure 5](#)).

## 6.7 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see [Figure 5](#))

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT	
t <sub>PD</sub> <sup>(1)</sup>	Propagation delay time	R <sub>ON</sub> = 20 Ω, C <sub>L</sub> = 15 pF	SDA or SCL	SDn or SCn	0.3	ns	
					1		
t <sub>IV</sub>	Interrupt valid time <sup>(2)</sup>	$\overline{\text{INTn}}$		$\overline{\text{INT}}$		4	
t <sub>IR</sub>	Interrupt reset delay time <sup>(2)</sup>	$\overline{\text{INTn}}$		$\overline{\text{INT}}$		2	

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) Data taken using a 4.7-kΩ pullup resistor and 100-pF load (see [Figure 6](#)).

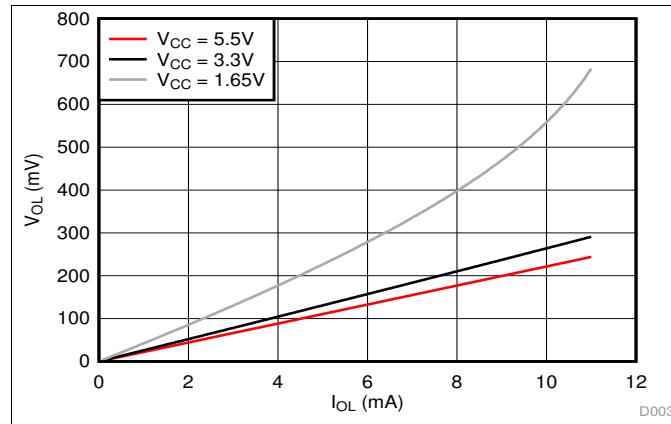
## 6.8 Interrupt Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

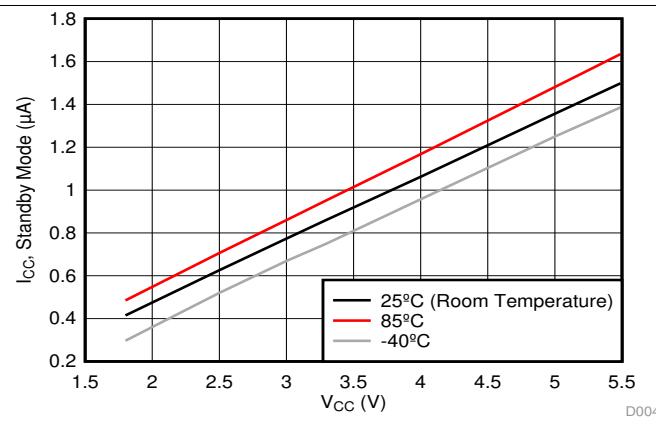
PARAMETER		MIN	MAX	UNIT
t <sub>PWRL</sub>	Low-level pulse duration rejection of INT <sub>n</sub> inputs <sup>(1)</sup>	1		μs
t <sub>PWRH</sub>	High-level pulse duration rejection of INT <sub>n</sub> inputs <sup>(1)</sup>	0.5		μs

(1) Data taken using a 4.7-kΩ pullup resistor and 100-pF load (see Figure 6).

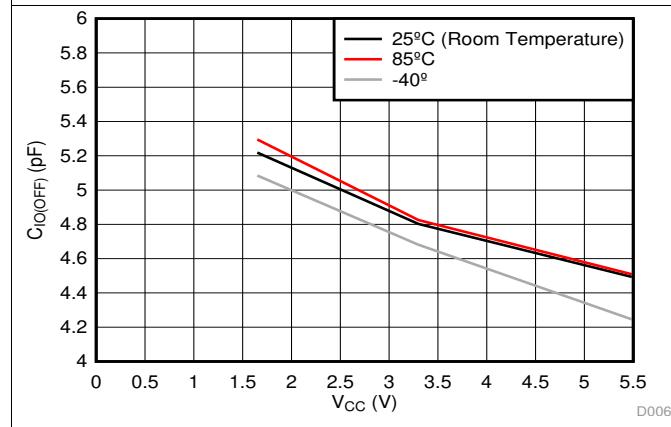
## 6.9 Typical Characteristics



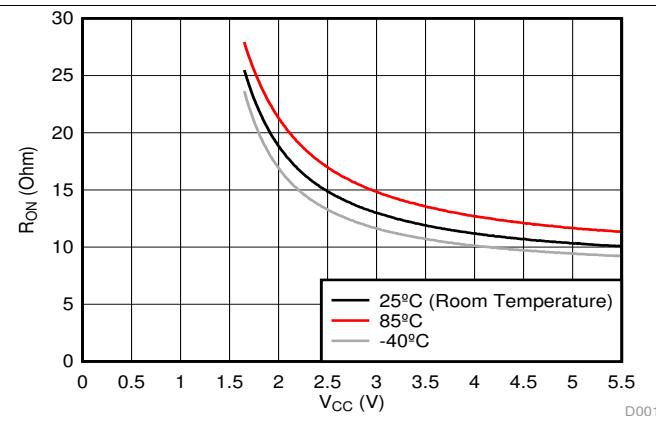
**Figure 1. SDA Output Low Voltage ( $V_{OL}$ ) vs Load Current ( $I_{OL}$ ) at Three  $V_{CC}$  Levels**



**Figure 2. Standby Current ( $I_{CC}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperature Points**

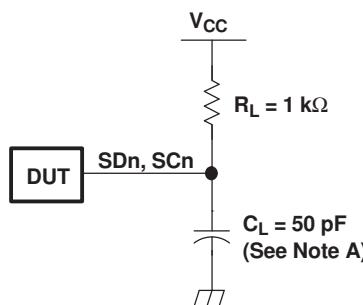
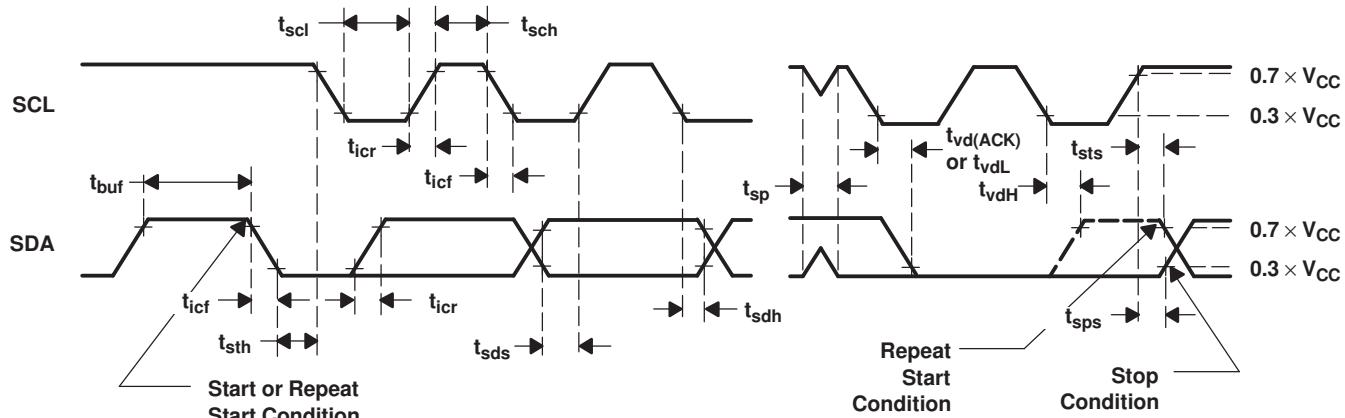
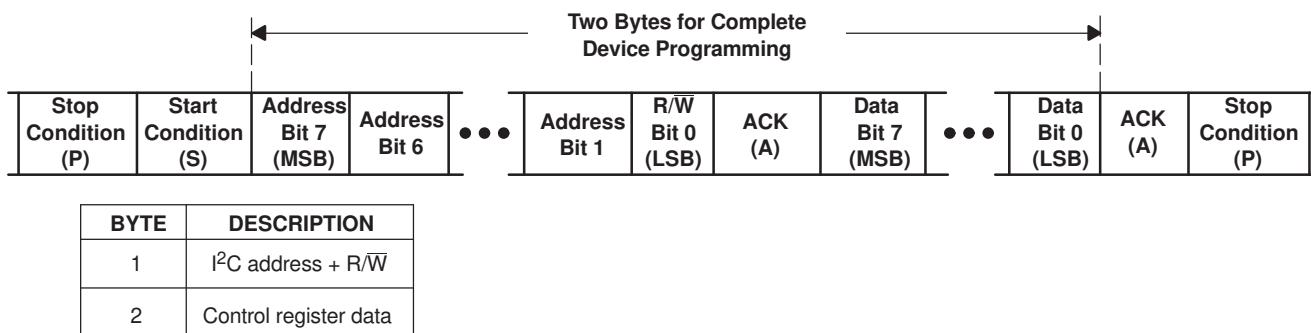


**Figure 3. Slave channel (SC<sub>n</sub>/SD<sub>n</sub>) capacitance ( $C_{IO(OFF)}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperature Points**



**Figure 4. ON-Resistance ( $R_{ON}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperatures**

## 7 Parameter Measurement Information

I<sup>2</sup>C-PORT LOAD CONFIGURATION

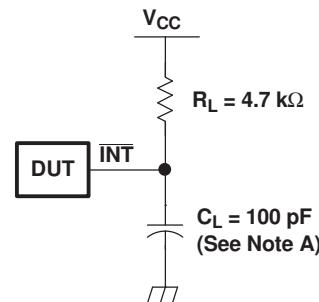
VOLTAGE WAVEFORMS

NOTES:

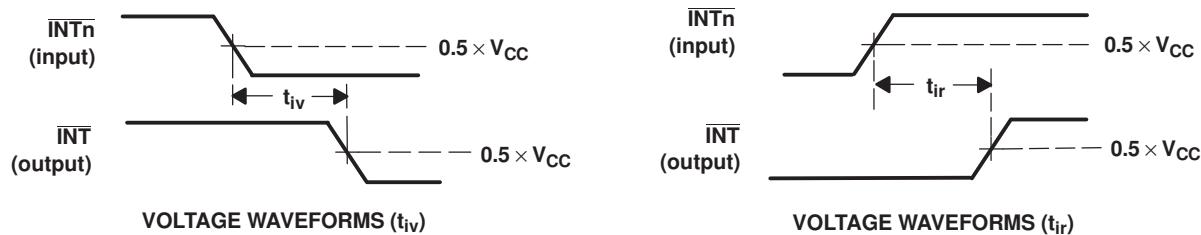
- $C_L$  includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r/t_f \leq 30\text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.

Figure 5. I<sup>2</sup>C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

### Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.

**Figure 6. Interrupt Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

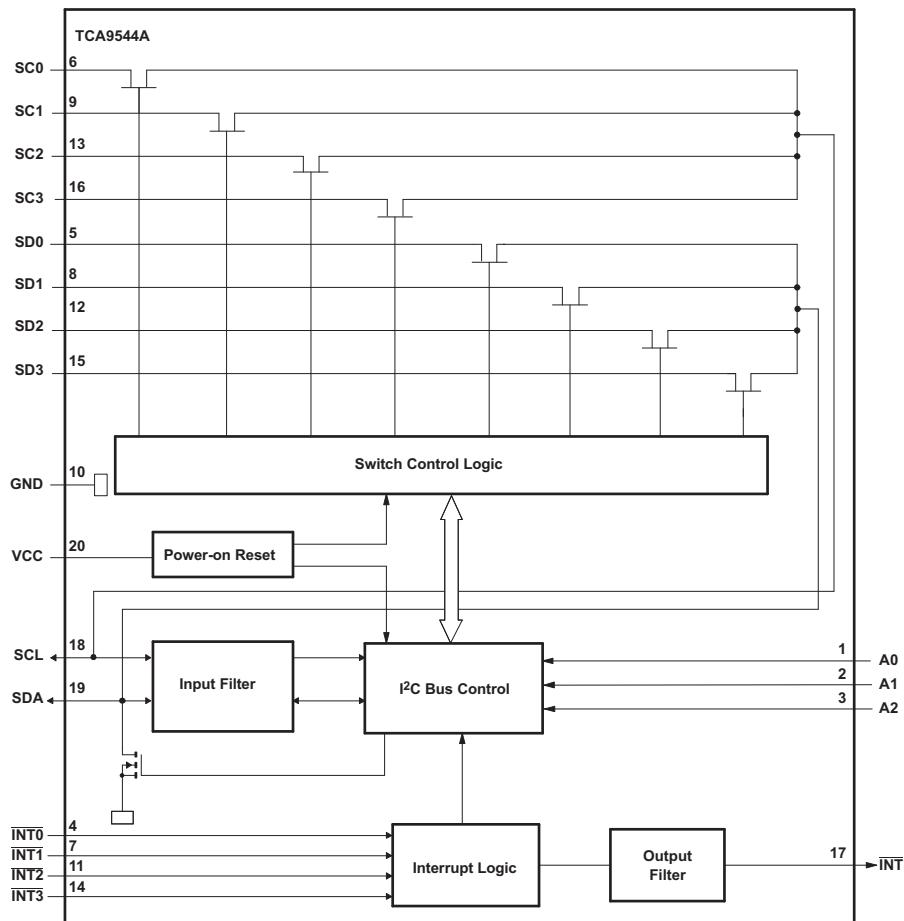
The TCA9544A is a 4-channel, bidirectional translating I<sup>2</sup>C Multiplexer. The master SCL/SDA signal pair is directed to one of the four channels of slave devices, SC0/SD0-SC3/SD3. Four interrupt inputs (INT3–INT0), one for each of the downstream pairs, are provided. One interrupt output (INT) acts as an AND of the four interrupt inputs.

The device can be reset by cycling the power supply, V<sub>CC</sub>, also known as a power-on reset (POR), which resets the state machine and allows the TCA9544A to recover should one of the downstream I<sup>2</sup>C buses get stuck in a low state. A POR event will cause all channels to be deselected.

The connections of the I<sup>2</sup>C data path are controlled by the same I<sup>2</sup>C master device that is switched to communicate with multiple I<sup>2</sup>C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0-A2 pins), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The TCA9544A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

The TCA9544A is a 4-channel, bidirectional translating multiplexer for I<sup>2</sup>C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The TCA9544A features I<sup>2</sup>C control using a single 8-bit control register in which the three least significant bits control the enabling and disabling of the 4 switch channels of I<sup>2</sup>C data flow. The TCA9544A also supports interrupt signals for each slave channel and this data is held in the four most significant bits of the control register. Depending on the application, voltage translation of the I<sup>2</sup>C bus can also be achieved using the TCA9544A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I<sup>2</sup>C bus enters a fault state, the TCA9544A can be reset to resume normal operation by means of a power-on reset which results from cycling power to the device.

## 8.4 Device Functional Modes

### 8.4.1 Power-On Reset

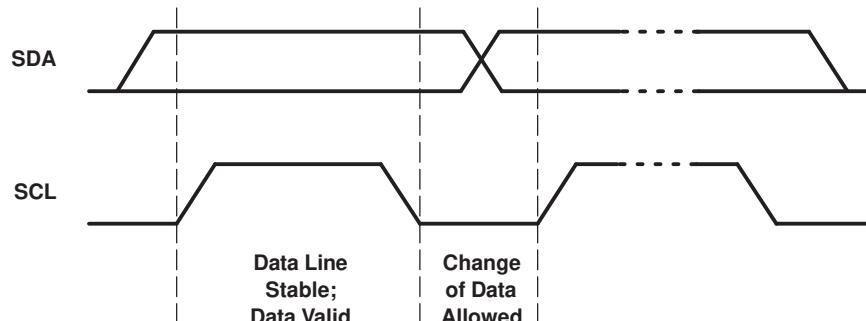
When power is applied to  $V_{CC}$ , an internal power-on reset holds the TCA9544A in a reset condition until  $V_{CC}$  has reached  $V_{PORR}$ . At this point, the reset condition is released, and the TCA9544A registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter,  $V_{CC}$  must be lowered below  $V_{PORF}$  to reset the device.

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C Interface

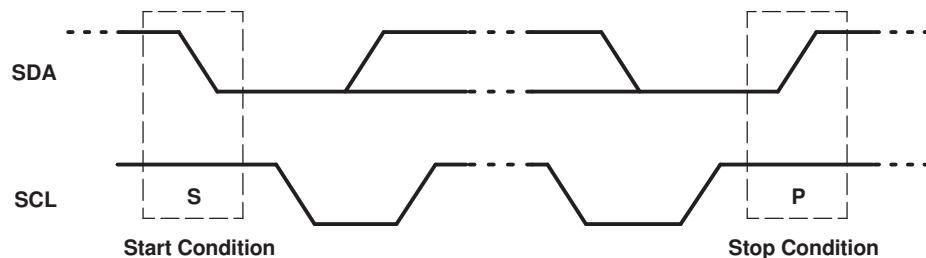
The I<sup>2</sup>C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see [Figure 7](#)).



**Figure 7. Bit Transfer**

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see [Figure 8](#)).



**Figure 8. Definition of Start and Stop Conditions**

## Programming (continued)

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 9).

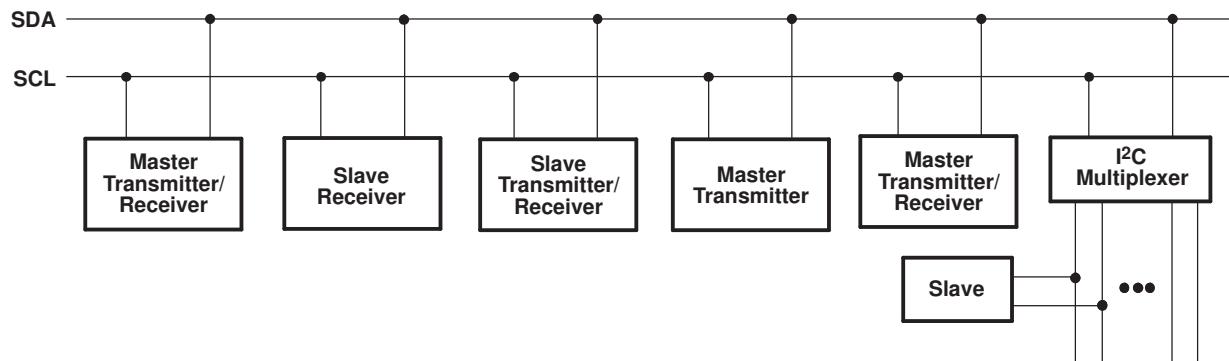


Figure 9. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an acknowledge (ACK) after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 10). Setup and hold times must be taken into account.

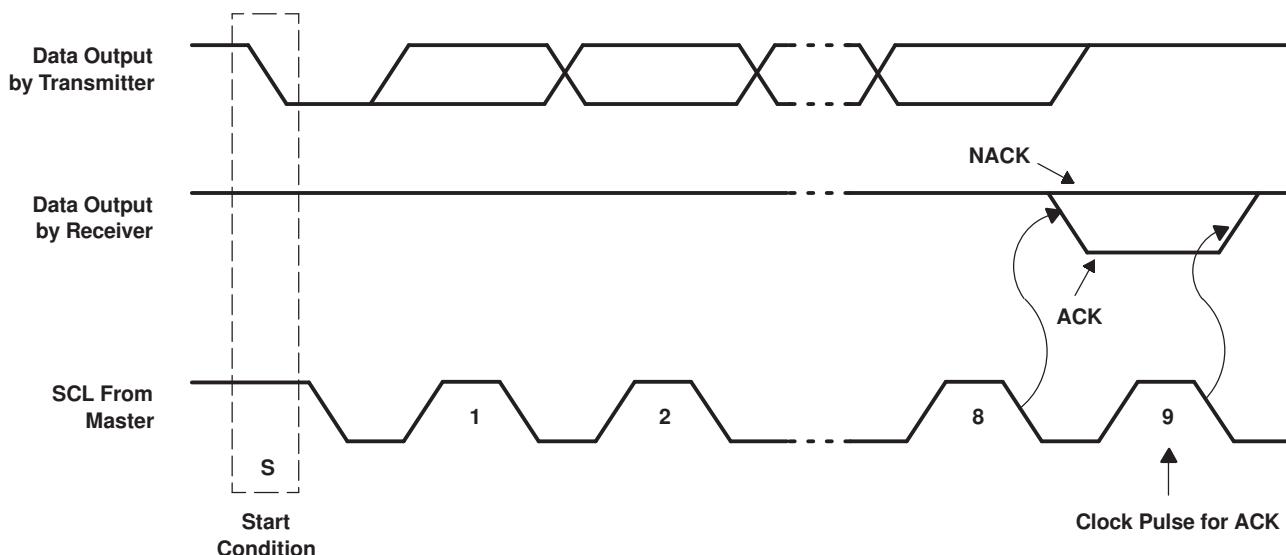


Figure 10. Acknowledgment on the I<sup>2</sup>C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Data is transmitted to the TCA9544A control register using the write mode shown in Figure 11.

## Programming (continued)

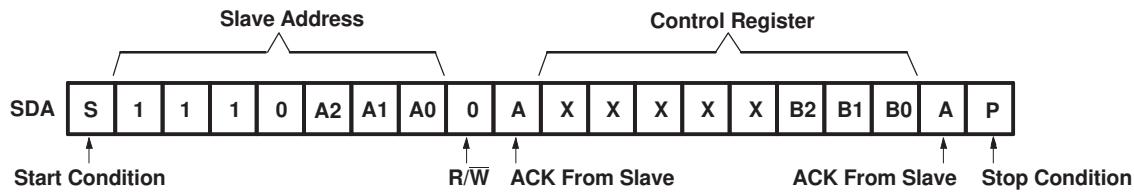


Figure 11. Write Control Register

Data is read from the TCA9544A control register using the read mode shown in Figure 12.

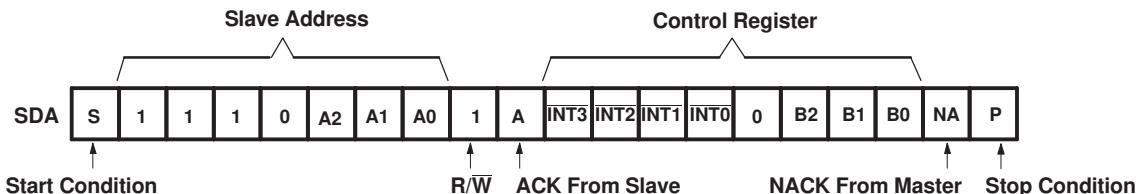


Figure 12. Read Control Register

## 8.6 Control Register

### 8.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the TCA9544A is shown in Figure 13. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low.

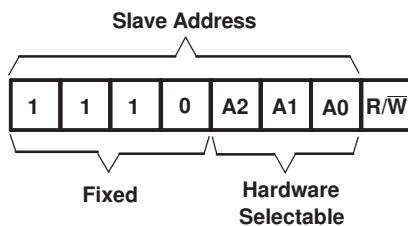


Figure 13. TCA9544A Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

## Control Register (continued)

### 8.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TCA9544A, which is stored in the control register. If multiple bytes are received by the TCA9544A, it saves the last byte received. This register can be written and read via the I<sup>2</sup>C bus.

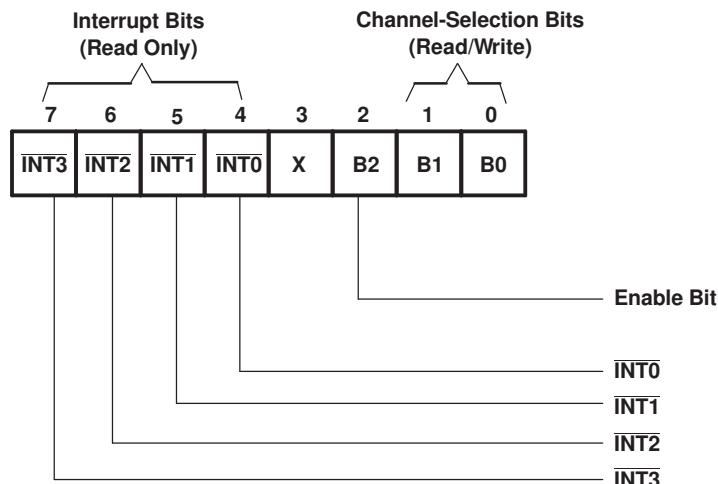


Figure 14. Control Register

### 8.6.3 Control Register Definition

Only one SCn/SDn downstream pair, or channel, can be selected by the contents of the control register (see Table 1). This register is written after the TCA9544A has been addressed. The three LSBs of the control byte are used to determine which channel (or channels) is to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I<sup>2</sup>C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)<sup>(1)</sup>

INT3	INT2	INT1	INT0	D3	B2	B1	B0	COMMAND
X	X	X	X	X	0	X	X	No channel selected
X	X	X	X	X	1	0	0	Channel 0 enabled
X	X	X	X	X	1	0	1	Channel 1 enabled
X	X	X	X	X	1	1	0	Channel 2 enabled
X	X	X	X	X	1	1	1	Channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up default state

(1) Only one channel may be selected at a time.

#### 8.6.4 Interrupt Handling

The TCA9544A provides four interrupt inputs (one for each channel) and one open-drain interrupt output. When an interrupt is generated by any device, it is detected by the TCA9544A, and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register (see Table 2).

Bits 4–7 of the control register correspond to channels 0–3 of the TCA9544A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 causes bit 4 of the control register to be set on the read. The master then can address the TCA9544A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can reconfigure the TCA9544A to select this channel and locate the device generating the interrupt and clear it. Once the device responsible for the interrupt clears, the interrupt clears.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to  $V_{CC}$ .

**Table 2. Control Register Read (Interrupt)<sup>(1)</sup>**

<b>INT3</b>	<b>INT2</b>	<b>INT1</b>	<b>INT0</b>	<b>D3</b>	<b>B2</b>	<b>B1</b>	<b>B0</b>	<b>COMMAND</b>
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
X	0	X	X	X	X	X	X	No interrupt on channel 2
	1							Interrupt on channel 2
0	X	X	X	X	X	X	X	No interrupt on channel 3
1								Interrupt on channel 3

(1) Several interrupts can be active at the same time. For example,  $\overline{INT3} = 0$ ,  $\overline{INT2} = 1$ ,  $\overline{INT1} = 1$ ,  $\overline{INT0} = 0$  means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Applications of the TCA9544A will contain an I<sup>2</sup>C (or SMBus) master device and up to four I<sup>2</sup>C slave devices. The downstream channels are ideally used to resolve I<sup>2</sup>C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I<sup>2</sup>C master can move on and read the next channel.

In an application where the I<sup>2</sup>C bus will contain many additional slave devices that do not result in I<sup>2</sup>C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See *Design Requirements* and *Detailed Design Procedure*).

### 9.2 Typical Application

A typical application of the TCA9544A contains anywhere from 1 to 5 separate data pull-up voltages,  $V_{DPUX}$ , one for the master device ( $V_{DPUM}$ ) and one for each of the selectable slave channels ( $V_{DPU0} – V_{DPU3}$ ). In the event where the master device and all slave devices operate at the same voltage, then the supply voltage can be  $V_{CC} = V_{DPUX}$ . In an application where voltage translation is necessary, additional design requirements must be considered (See *Design Requirements*).

Figure 15 shows an application in which the TCA9544A can be used.

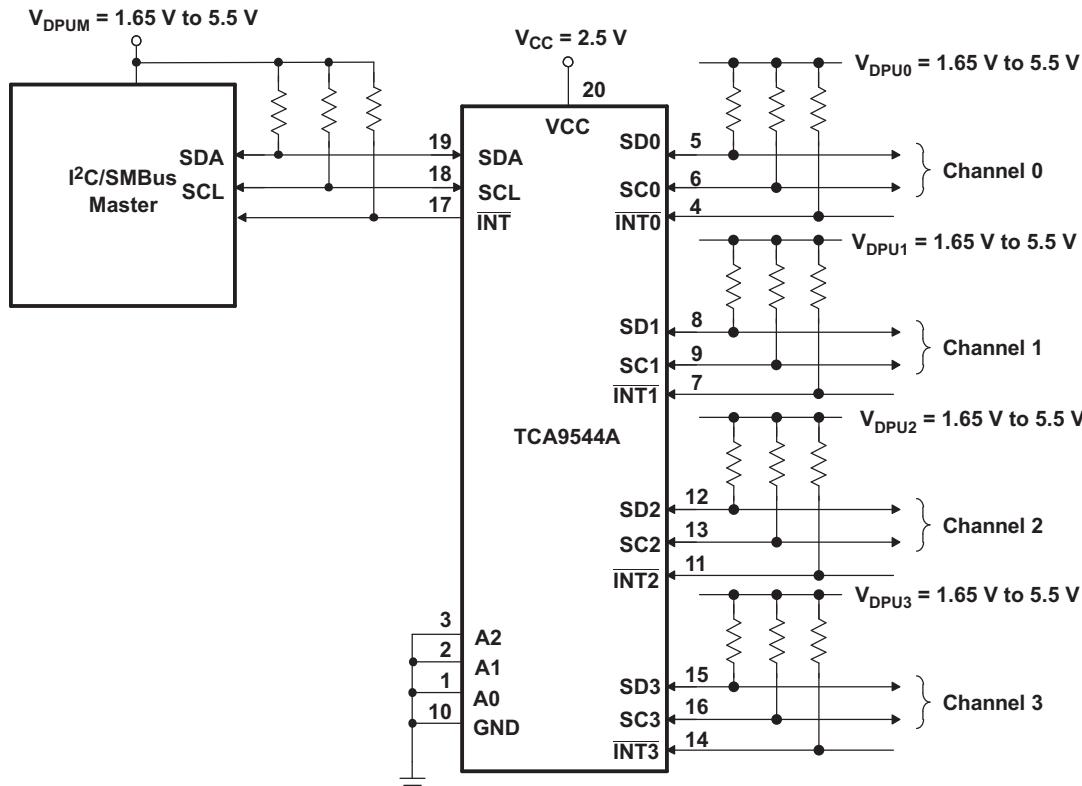


Figure 15. Typical Application Schematic

## Typical Application (continued)

### 9.2.1 Design Requirements

The pull-up resistors on the INT3-INT0 pins in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

The A0 and A1 pins are hardware selectable to control the slave address of the TCA9544A. These pins may be tied directly to GND or  $V_{CC}$  in the application.

If multiple slave channels will be activated simultaneously in the application, then the total  $I_{OL}$  from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors,  $R_p$ .

The pass-gate transistors of the TCA9544A are constructed such that the  $V_{CC}$  voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C bus to another.

Figure 16 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the [Electrical Characteristics](#) section of this data sheet). In order for the TCA9544A to act as a voltage translator, the  $V_{pass}$  voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V,  $V_{pass}$  must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 16,  $V_{pass(max)}$  is 2.7 V when the TCA9544A supply voltage is 4 V or lower, so the TCA9544A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 15).

### 9.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors,  $R_p$ , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of  $V_{DPUX}$ ,  $V_{OL(max)}$ , and  $I_{OL}$ :

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

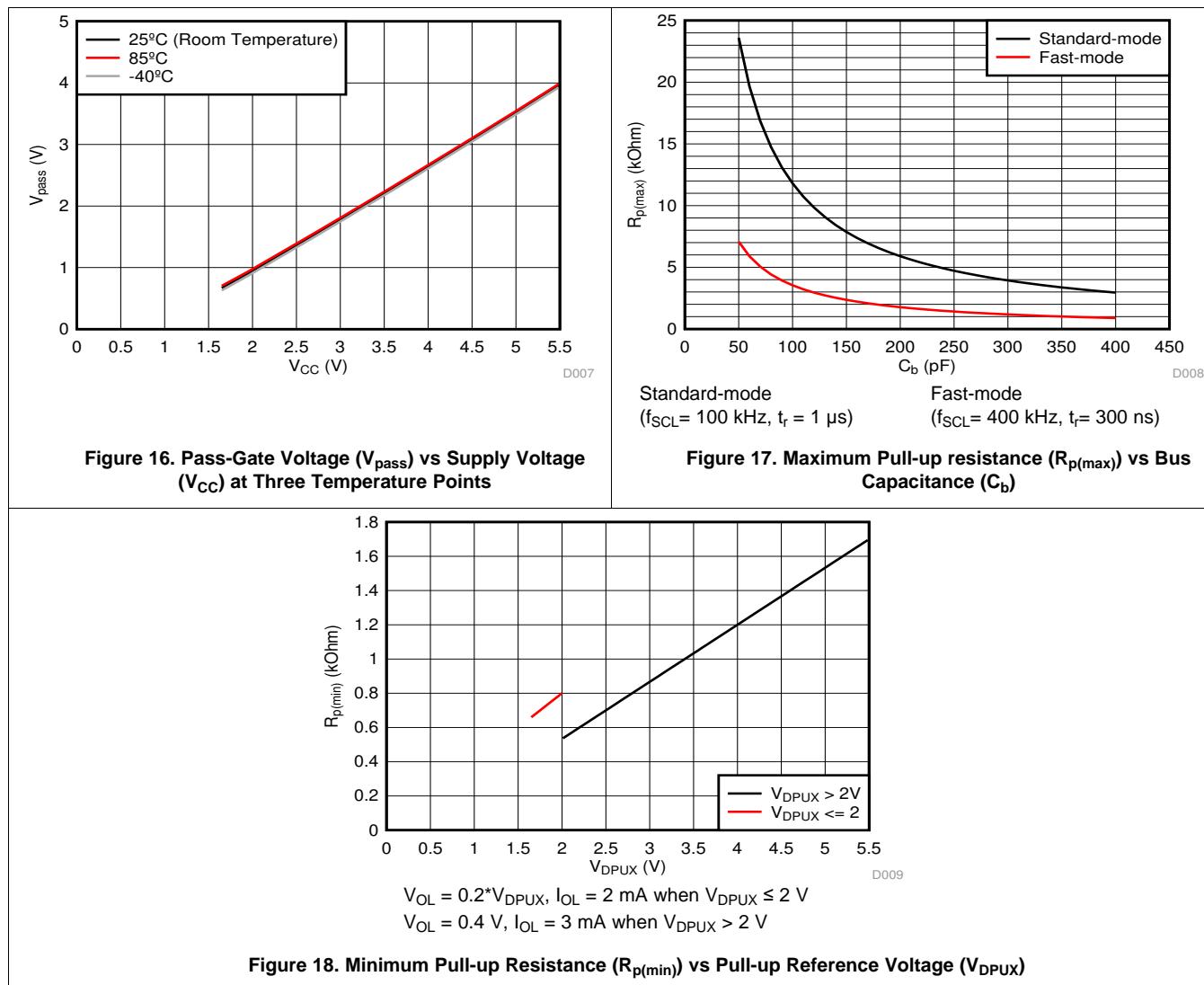
The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$ :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9544A,  $C_{io(OFF)}$ , the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

## Typical Application (continued)

### 9.2.3 TCA9544A Application Curves



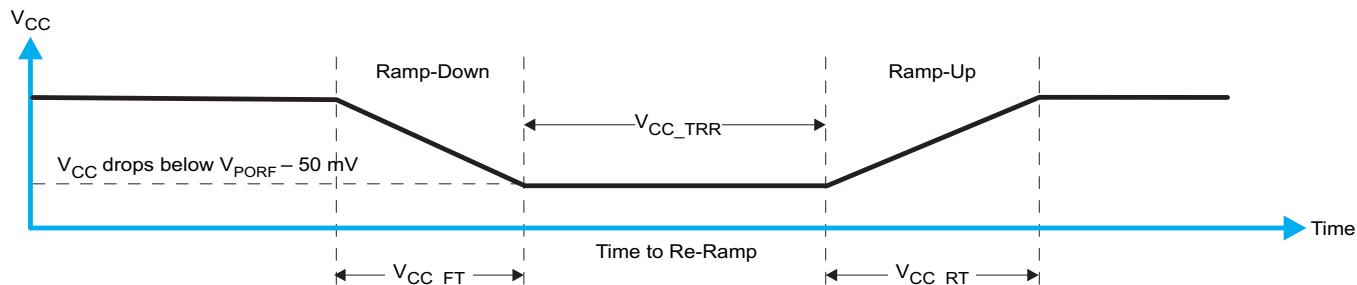
## 10 Power Supply Recommendations

The operating power-supply voltage range of the TCA9544A is 1.65 V to 5.5 V applied at the VCC pin. When the TCA9544A is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I<sup>2</sup>C bus logic is initialized properly.

### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9544A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in Figure 19.



**Figure 19. V<sub>CC</sub> is Lowered Below the POR Threshold, Then Ramped Back Up to V<sub>CC</sub>**

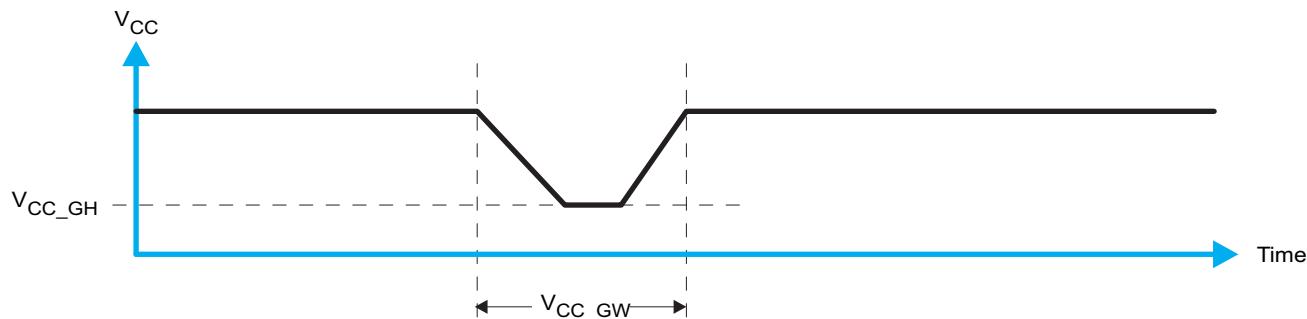
Table 3 specifies the performance of the power-on reset feature for TCA9544A for both types of power-on reset.

**Table 3. Recommended Supply Sequencing And Ramp Rates<sup>(1)</sup>**

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>CC_FT</sub>	Fall time	See Figure 19	1		ms
V <sub>CC_RT</sub>	Rise time	See Figure 19	0.1		ms
V <sub>CC_TRR</sub>	Time to re-ramp (when V <sub>CC</sub> drops below V <sub>PORF(min)</sub> – 50 mV or when V <sub>CC</sub> drops to GND)	See Figure 19	40		μs
V <sub>CC_GH</sub>	Level that V <sub>CC</sub> can glitch down to, but not cause a functional disruption when V <sub>CC_GW</sub> = 1 μs	See Figure 20		1.2	V
V <sub>CC_GW</sub>	Glitch width that will not cause a functional disruption when V <sub>CC_GH</sub> = 0.5 × V <sub>CC</sub>	See Figure 20		10	μs
V <sub>PORF</sub>	Voltage trip point of POR on falling V <sub>CC</sub>	See Figure 21	0.8	1.25	V
V <sub>PORR</sub>	Voltage trip point of POR on rising V <sub>CC</sub>	See Figure 21	1.05	1.5	V

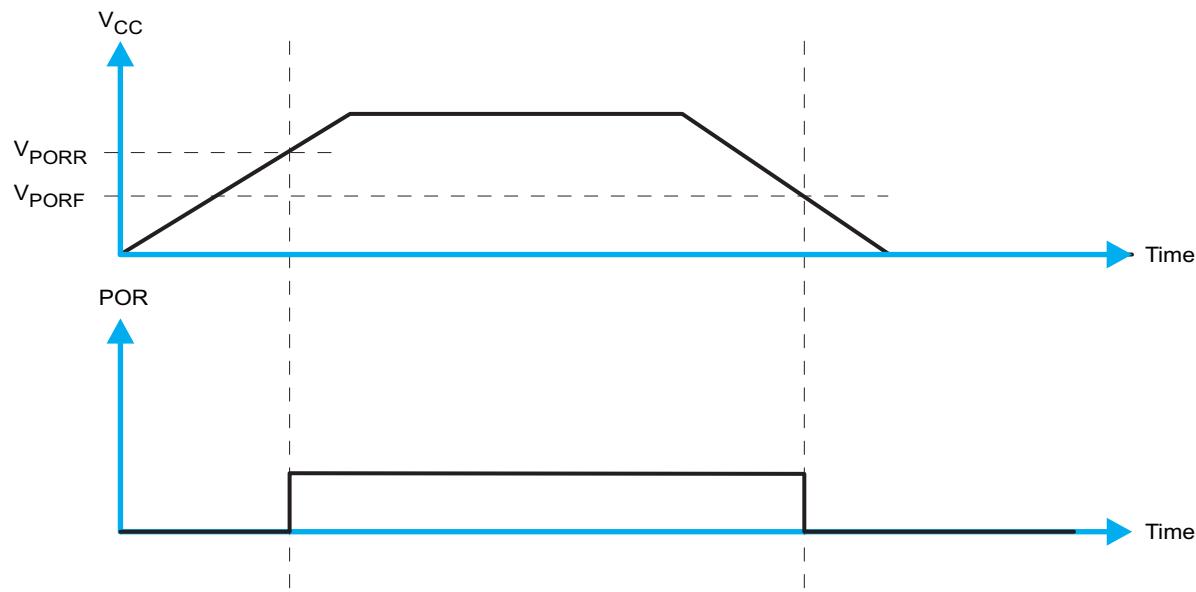
(1) All supply sequencing and ramp rate values are measured at T<sub>A</sub> = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 20](#) and [Table 3](#) provide more information on how to measure these specifications.



**Figure 20. Glitch Width and Glitch Height**

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. [Figure 21](#) and [Table 3](#) provide more details on this specification.



**Figure 21.  $V_{POR}$**

## 11 Layout

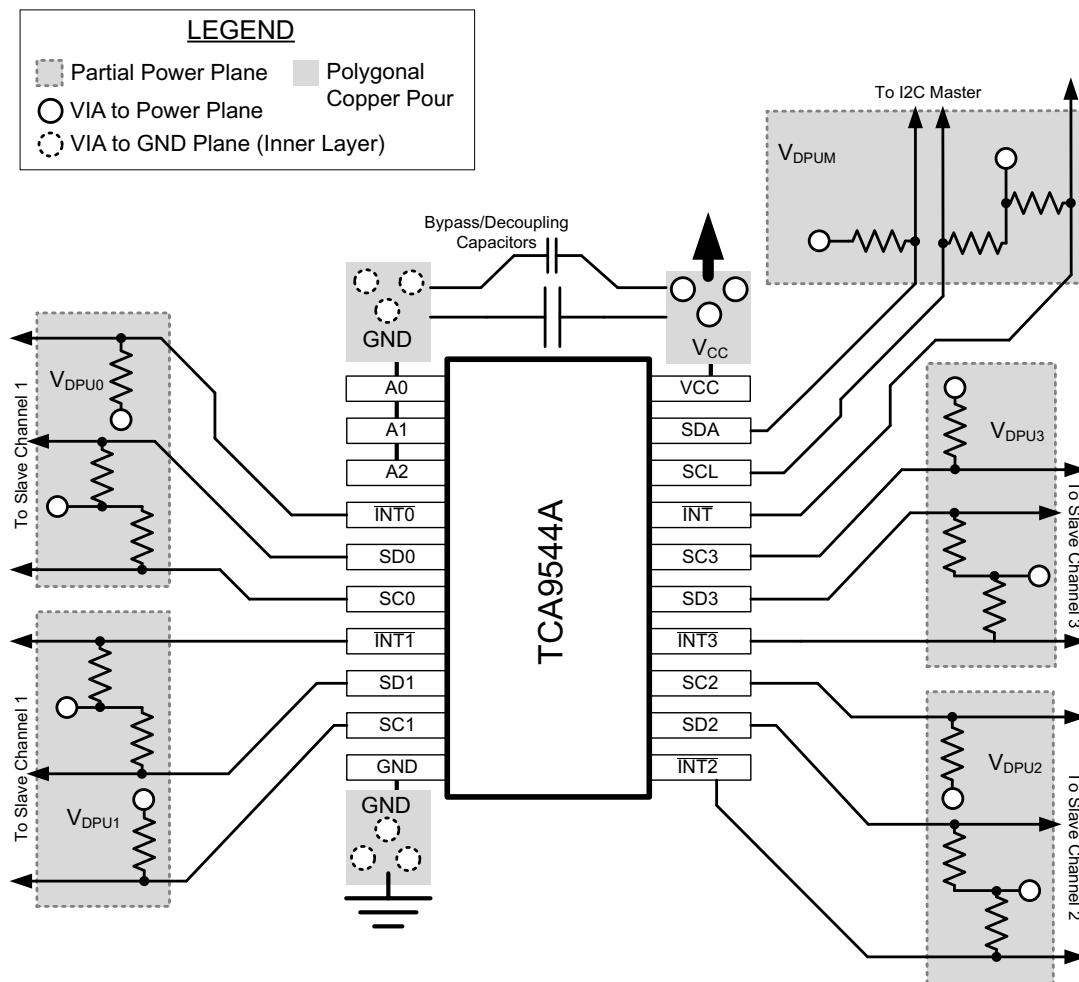
### 11.1 Layout Guidelines

For PCB layout of the TCA9544A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V<sub>DPUX</sub> voltages and V<sub>CC</sub> could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V<sub>DPUM</sub>, V<sub>DPU0</sub>, V<sub>DPU1</sub>, V<sub>DPU2</sub>, and V<sub>DPU3</sub> may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I<sup>2</sup>C bus capacitance added by PCB parasitics, data lines (S<sub>Cn</sub>, S<sub>Dn</sub> and INT<sub>n</sub>) should be as short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

### 11.2 Layout Example



## 12 器件和文档支持

### 12.1 接收文档更新通知

要接收文档更新通知, 请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的通知我进行注册, 即可每周接收产品信息更改摘要。有关更改的详细信息, 请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.3 商标

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### 12.4 静电放电警告

 这些装置包含有限的内置 ESD 保护。 存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

### 12.5 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更, 恕不另行通知, 且不会对此文档进行修订。如需获取此数据表的浏览器版本, 请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9544APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW544A	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

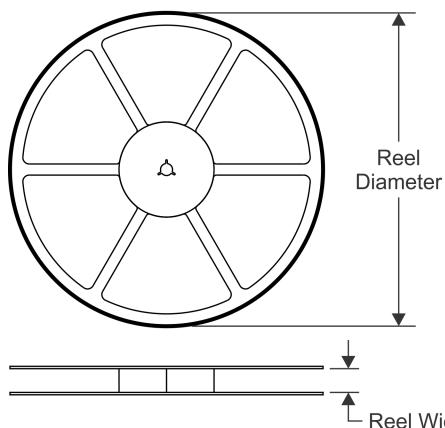
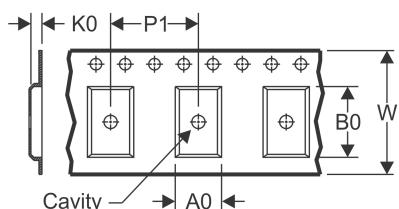
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

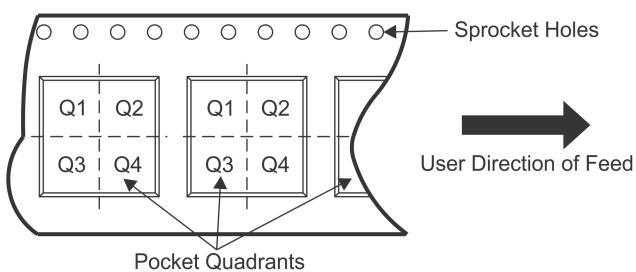
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9544APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9544APWR	TSSOP	PW	20	2000	853.0	449.0	35.0

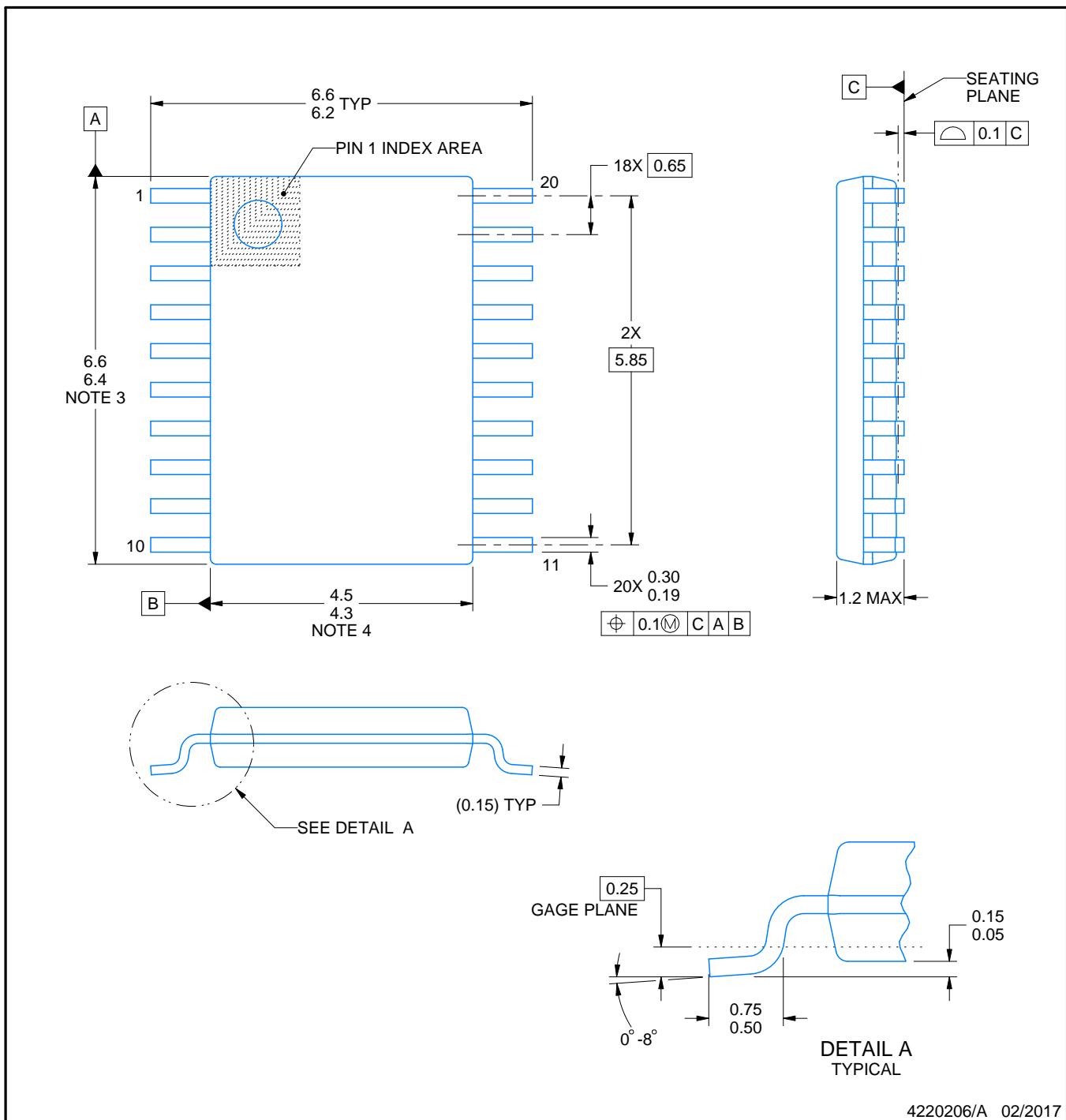
## PACKAGE OUTLINE

**PW0020A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

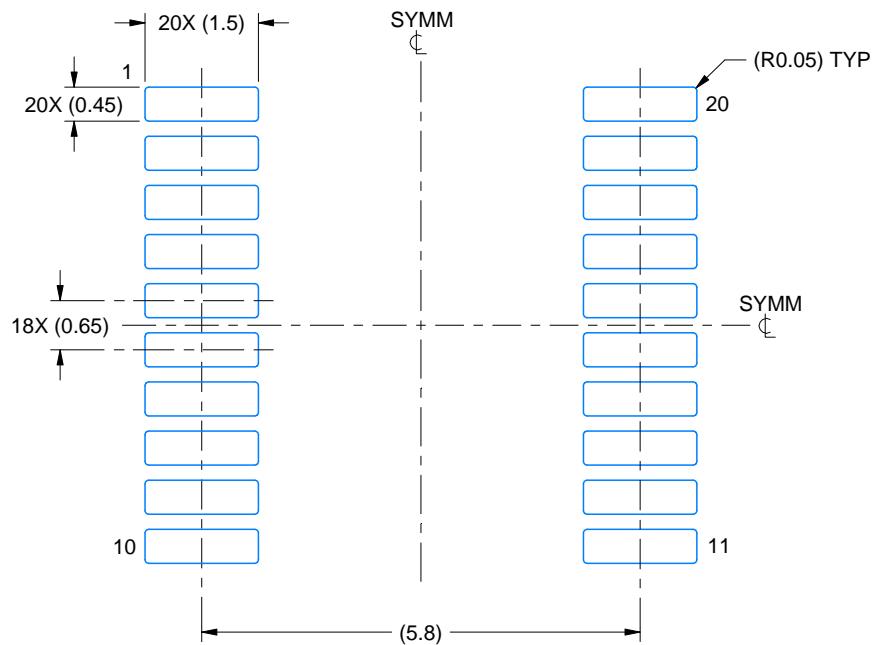
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

## EXAMPLE BOARD LAYOUT

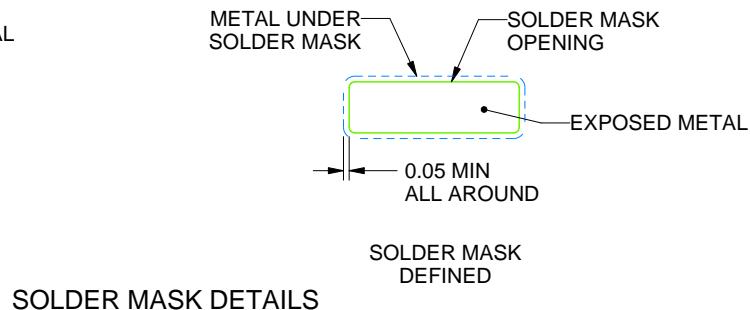
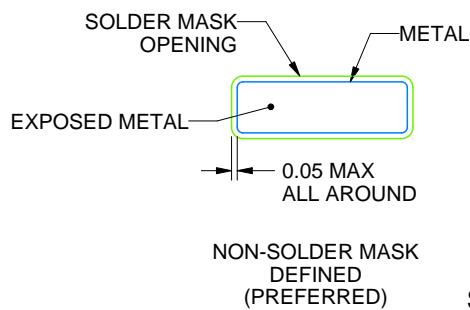
**PW0020A**

## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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#### NOTES: (continued)

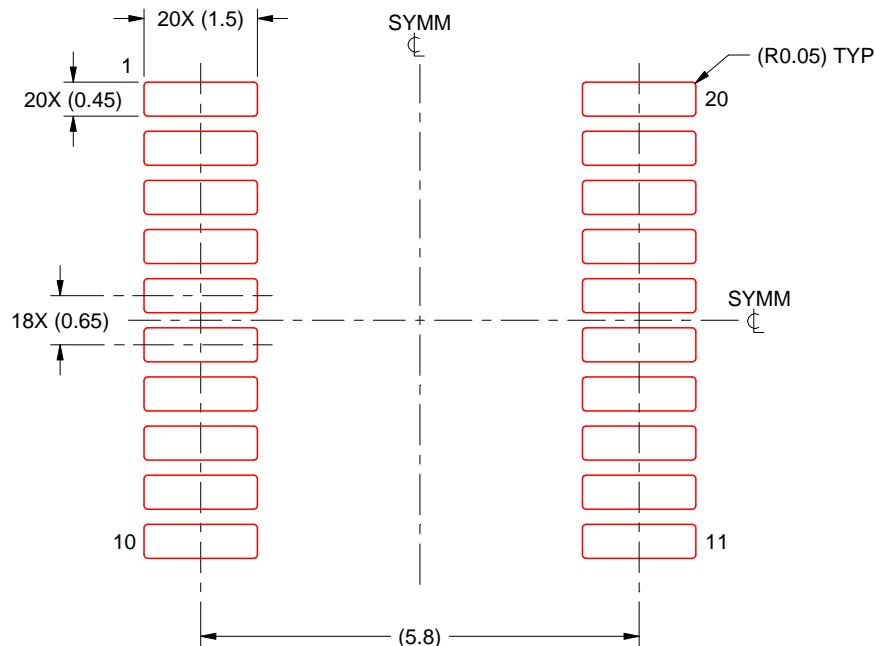
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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