适用于成本敏感型系统的 TLV900x 低功耗、RRIO、1MHz 运算放大器

1 特性

- 可扩展 CMOS 放大器，适用于低成本应用
- 轨至轨输入和输出
- 低输入失调电压：±0.4mV
- 单位带宽增益积：1MHz
- 低宽带噪声：27nV/ $\sqrt{Hz}$
- 低输入偏置电流：5pA
- 低静态电流：60μA/通道
- 单位增益稳定
- 内置 RFI 和 EMI 滤波器
- 可在电源电压低至 1.8V 的情况下运行
- 由于具有电阻式开环输出阻抗，因此可在更高的容性负载下更轻松地实现稳定
- 工作温度范围：–40°C 至 125°C

2 应用

- 传感器信号调节
- 电源模块
- 有源滤波器
- 低侧电流检测
- 烟雾探测器
- 运动检测器
- 可穿戴设备
- 大型和小型家用电器
- EPOS
- 条形码扫描仪
- 个人电子产品
- HVAC：暖通空调
- 电机控制：交流感应

3 说明

TLV900x 系列包括单通道 (TLV9001)、双通道 (TLV9002)、和四通道 (TLV9004) 低电压（1.8V 至 5.5V）运算放大器，具有轨至轨输入和输出摆幅能力。这些运算放大器为空间受限、需要低压运行和高容性负载驱动的应用（例如烟雾探测器、可穿戴电子产品和小型电器）提供了具有成本效益的解决方案。TLV900x 系列的电容负载驱动器具有 500pF 的电容，而电阻式开环输出阻抗使其能够在更高的电容负载下更轻松地实现稳定。这些运算放大器专为低工作电压 (1.8V 至 5.5V)而设计，性能规格类似于 TLV600x 器件。

TLV900x 系列稳健耐用的设计可简化电路设计。这些运算放大器具有单位增益稳定性，集成了 RFI 和 EMI 抑制滤波器，并且在过驱情况下不会出现相位反转。

TLV900x 器件具有关断模式（TLV9001S、TLV9002S 和 TLV9004S），允许放大器切换至典型电流消耗低于 1μA 的待机模式。

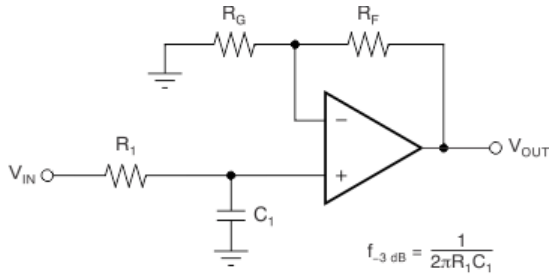
针对所有通道型号（单通道、双通道和四通道）提供微型封装（如 SOT-553 和 WSON）以及行业标准封装（如 SOIC、MSOP、SOT-23 和 TSSOP 封装）。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
TLV9001	SOT-23 (5)	1.60mm × 2.90mm
	SC70 (5)	1.25mm × 2.00mm
	SOT-553 (5)(2)	1.65mm × 1.20mm
	X2SON (5)	0.80mm × 0.80mm
TLV9001S	SOT-23 (6)	1.60mm × 2.90mm
	SC70 (6)	1.25mm × 2.00mm
TLV9002	SOIC (8)	3.91mm × 4.90mm
	WSON (8)	2.00mm × 2.00mm
	VSSOP (8)	3.00mm × 3.00mm
	SOT-23 (8)	1.60mm × 2.90mm
	TSSOP (8)	3.00mm × 4.40mm
TLV9002S	VSSOP (10)	3.00mm × 3.00mm
	X2QFN (10)	1.50mm x 2.00mm
	DSBGA (9)	1.00mm x 1.00mm
TLV9004	SOIC (14)	8.65mm × 3.91mm
	SOT-23 (14)	4.20 mm × 2.00 mm
	TSSOP (14)	4.40mm × 5.00mm
	WQFN (16)	3.00mm × 3.00mm
	X2QFN (14)	2.00mm × 2.00mm
TLV9004S	WQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 仅表示封装为预发布。



单极低通滤波器

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision Q (June 2021) to Revision R (November 2021) — **Page**

- 向*器件信息*表中添加了 SOT-23 (14) 封装 1
- Added SOT-23 DYY package to *Device Comparison Table* 6
- Added SOT-23 (14) package to *Pin Configuration and Functions* section 7
- Added DYY (SOT-23) package thermal information to the *Thermal Information: TLV9004* table 16

Changes from Revision P (April 2021) to Revision Q (June 2021) — **Page**

- Changed supply voltage (V+) – (V–) MAX from 6 V to 7 V in the *Absolute Maximum Ratings* table 14

Changes from Revision O (April 2020) to Revision P (April 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 向*器件信息*表中添加了 9 引脚 DSBGA 封装 1
- Added 9-pin DSBGA package to *Device Comparison Table* 6
- Added TLV9002S 9-pin DSBGA package to *Pin Configuration and Functions* section 7
- Added TLV9002S 9-pin DSBGA package to *Thermal Information: TLV9002S* 16
- Deleted the *Related Links* section from the *Device and Documentation Support* section 37

Changes from Revision N (January 2020) to Revision O (April 2020) — **Page**

- 删除了 TLV9001S 上的“预发布”标识 1
- Deleted TLV9001SIDCK (6-pin SC70) package preview note 7
- Added DCK (SC70) data to the Thermal Information: TLV9001S table 15

Changes from Revision M (September 2019) to Revision N (January 2020) **Page**

- 向*器件信息*表中添加了 6 引脚 SC70 封装 1
- Added 6-pin SC70 package to *Device Comparison Table* 6
- Added TLV9001SIDCK (6-Pin SC70) package pinout 7
- Added TLV9001S 6-pin SC70 package to *Pin Configuration and Functions* section 7
- Added 6-pin SC70 pinout to *Pin Functions: TLV9001S* 7
- Added TLV9001S 6-pin SC70 package to *Thermal Information: TLV9001S* table 15

Changes from Revision L (May 2019) to Revision M (September 2019) **Page**

- Deleted preview notations for SOT-23-8 (DDF) package 6
- Added link to *Shutdown* section in all $\overline{\text{SHDN}}$ pin function rows 7
- Added *EMI Rejection* section to the *Feature Description* section 27
- Changed the *Shutdown* section to add more clarity regarding internal pull-up resistor 28

Changes from Revision K (March 2019) to Revision L (May 2019) **Page**

- 向*器件信息*表中添加了 SOT-23 (8) 信息 1
- Added SOT-23 DDF package to *Device Comparison Table* 6
- Added SOT-23 (DDF) to *Pin Configuration and Functions* section 7
- Added DDF (SOT-23) *Thermal Information: TLV9002* table 15

Changes from Revision J (January 2019) to Revision K (March 2019) **Page**

- Changed TLV9002S *ESD Ratings* heading to include all TLV9002S packages 14
- Deleted preview notation from TLV9002SIRUG in *Thermal Information* table 16

Changes from Revision I (November 2018) to Revision J (January 2019) **Page**

- 删除了 TLV9002SIRUGR 的预发布符号 1
- 将 TLV9004 WQFN(14) 封装标识符更改为 X2QFN(14) 封装标识符 1
- Added RUG package to *Device Comparison Table* 6
- Added DGS package to *Device Comparison Table* 6
- Added shutdown devices to *Device Comparison Table* 6
- Changed TLV9001 DRL package pinout drawing 7
- Changed TLV9001 DRL package pin functions 7
- Deleted package preview note from TLV9002SIRUGR (X2QFN) pinout drawing 7
- Added TLV9004IRUC Thermal Information 16
- Changed legend of Closed-Loop Gain vs Frequency plot 20

Changes from Revision H (October 2018) to Revision I (November 2018) **Page**

- Added TLV9002SIDGS to *ESD Ratings* table 14

Changes from Revision G (September 2018) to Revision H (October 2018) **Page**

- Changed From: TLV9001 DCK Package To: TLV9001T DCK Package 7

Changes from Revision F (August 2018) to Revision G (September 2018) **Page**

- Added *Device Comparison Table* 6
- Changed pin names for all devices and all packages 7
- Changed pin names and I/O designation on some TLV9001 pins 7
- Changed the pin number for V+ in the *SOIC, TSSOP* column of the *Pin Functions: TLV9004* table 7

Changes from Revision E (July 2018) to Revision F (August 2018) **Page**

- 添加了“可扩展 CMOS 放大器，适用于低成本应用”特性 1

- 删除了采用 TSSOP 封装的 TLV9002 和 TLV9004 器件上的“预发布”标识。 1
- Added TLV9001U DBV (SOT-23) pinout drawing to *Pin Configuration and Functions* section 7
- Added SOT-23 U Pinout to *Pin Functions* section 7

Changes from Revision D (June 2018) to Revision E (July 2018) **Page**

- 更正了*说明*部分中的拼写错误..... 1
- 向*器件信息*表中添加了 TLV9001 5 引脚 X2SON 封装..... 1
- 向*器件信息*表中添加了 TLV9001S 6 引脚 SOT-23 封装..... 1
- 向*器件信息*表中添加了 TLV9004 14 引脚和 16 引脚 WQFN 封装..... 1
- Added TLV9001 DPW (X2SON) pinout drawing to *Pin Configuration and Functions* section..... 7
- Added TLV9001S 6-pin SOT-23 package to *Pin Configuration and Functions* section..... 7
- Added TLV9004 RTE pinout information to *Pin Configuration and Functions* section 7
- Added DPW (X2SON) and DRL (SOT-553) packages to *Thermal Information: TLV9001* table..... 15
- Added *Thermal Information: TLV9001S* table to *Specifications* section..... 15
- Added RUG (X2QFN) package to *Thermal Information: TLV9002* table..... 15
- Added RTE (WQFN) and RUC (WQFN) packages to *Thermal Information: TLV9004* table..... 16

Changes from Revision C (May 2018) to Revision D (June 2018) **Page**

- 向*说明*部分添加了关断文本..... 1
- 向*器件信息*表中添加了 TLV9002S 和 TLV9004S 器件..... 1
- 向*器件信息*表中添加了 TLV9002S 10 引脚 X2QFN 封装..... 1
- Added TLV9002S DGS package pinout information to *Pin Configurations and Functions* section..... 7
- Added *Thermal Information: TLV9001* table to *Specifications* section..... 15
- Added *Thermal Information: TLV9004* table to *Specifications* section..... 16
- Added shutdown section to *Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V –) = 1.8 V to 5.5 V* table..... 17
- Added *Shutdown* section..... 28

Changes from Revision B (March 2018) to Revision C (May 2018) **Page**

- 向*器件信息*表中添加了 TLV9002 16 引脚 TSSOP 封装..... 1
- 向*器件信息*表中添加了 TLV9002 10 引脚 X2QFN 封装..... 1
- Added TLV9002S DGS package pinout drawing in *Pin Configurations and Functions* section..... 7
- Added TLV9004 pinout diagram and pin configuration table to *Pin Configuration and Functions* section 7
- Added TLV9004S pinout diagram and pin configuration table to *Pin Configuration and Functions* section 7
- Changed TLV9002 D (SOIC) junction-to-ambient thermal resistance value from 147.4°C/W to 207.9°C/W... 15
- Changed TLV9002 D (SOIC) junction-to-case (top) thermal resistance from 94.3°C/W to 92.8°C/W..... 15
- Changed TLV9002 D (SOIC) junction-to-board thermal resistance from 89.5°C/W to 129.7°C/W..... 15
- Changed TLV9002 D (SOIC) junction-to-top characterization parameter from 47.3°C/W to 26°C/W..... 15
- Changed TLV9002 D (SOIC) junction-to-board characterization parameter from 89°C/W to 127.9°C/W..... 15
- Added DGK (VSSOP) thermal information to *Thermal Information: TLV9002* table 15
- Added TLV9002 PW (TSSOP) thermal information to *Thermal Information: TLV9002* table..... 15
- Added PW (TSSOP) thermal information to *Thermal Information: TLV9002* table 16

Changes from Revision A (December 2017) to Revision B (March 2018) **Page**

- 在*器件信息*表中，向 TLV9001 封装、TLV9004 封装和 TLV9002 8 引脚 VSSOP 封装添加了封装预发布说明. 1
- Added package preview notes to TLV9001, TLV9004 and TLV9002 VSSOP package pinout drawings in *Pin Configuration and Functions* section 7
- Deleted package preview note from TLV9002 DSG (WSON) pinout drawing in Pin Configurations and Functions section..... 7
- Deleted package preview note from TLV9002 RUG (X2QFN) pinout drawing in *Pin Configurations and Functions* section..... 7

- Added DSG (WSON) package thermal information to the *Thermal Information: TLV9002* table..... 15
- Deleted package preview note from DSG (WSON) package in *Thermal Information: TLV9002* table..... 15
- Added D (SOIC) package thermal information to the *Thermal Information: TLV9004* table..... 16

Changes from Revision * (October 2017) to Revision A (December 2017) **Page**

- 将器件状态从“预告信息”更改为“量产数据/混合状态”..... 1

5 Device Comparison Table

DEVICE	NO. OF CH.	PACKAGE LEADS														
		SC70 DCK	SOIC D	SOT-23 DBV	SOT-23 DYY	SOT-553 DRL	TSSOP PW	VSSOP DGK	SOT-23 DDF	WQFN RTE	WSON DSG	X2QFN RUC	X2SON DPW	X2QFN RUG	VSSOP DGS	DSBGA YCK
TLV9001	1	5	—	5	—	5	—	—	—	—	—	—	5	—	—	—
TLV9001S		6	—	6	—	—	—	—	—	—	—	—	—	—	—	—
TLV9002	2	—	8	—	—	—	8	8	8	—	8	—	—	—	—	—
TLV9002S		—	—	—	—	—	—	—	—	—	—	—	—	10	10	9
TLV9004	4	—	14	—	14	—	14	—	—	16	—	14	—	—	—	—
TLV9004S		—	—	—	—	—	—	—	—	16	—	—	—	—	—	—

6 Pin Configuration and Functions

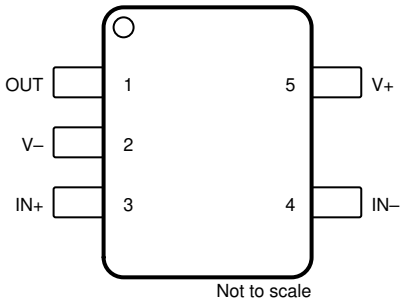


图 6-1. TLV9001 DBV, TLV9001T DCK Package
5-Pin SOT-23, SC70
Top View

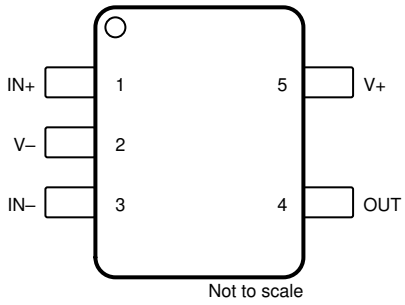


图 6-2. TLV9001 DCK Package, TLV9001 DRL Package, TLV9001U DBV Package
5-Pin SC70, SOT-553, SOT-23
Top View

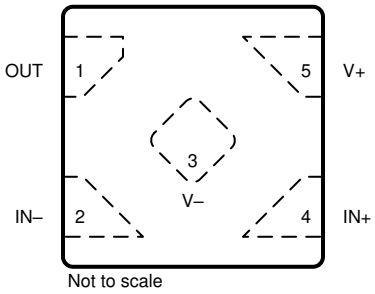


图 6-3. TLV9001 DPW Package
5-Pin X2SON
Top View

表 6-1. Pin Functions: TLV9001

PIN				I/O	DESCRIPTION
NAME	SOT-23, SC70(T)	SC70, SOT-23(U), SOT-553	X2SON		
IN –	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V –	2	2	3	I or —	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	I	Positive (high) supply

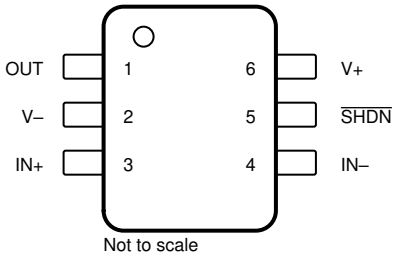


图 6-4. TLV9001S DBV Package
6-Pin SOT-23
Top View

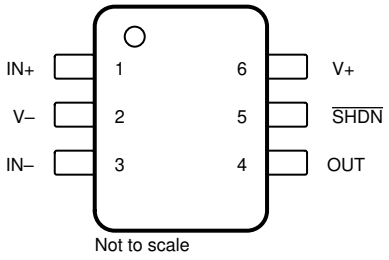


图 6-5. TLV9001S DCK Package
6-Pin SC70
Top View

表 6-2. Pin Functions: TLV9001S

PIN			I/O	DESCRIPTION
NAME	SOT-23	SC70		
IN –	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
$\overline{SHDN}$	5	5	I	Shutdown: low = amp disabled, high = amp enabled. See 节 8.5 for more information.
V –	2	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	6	6	I	Positive (high) supply

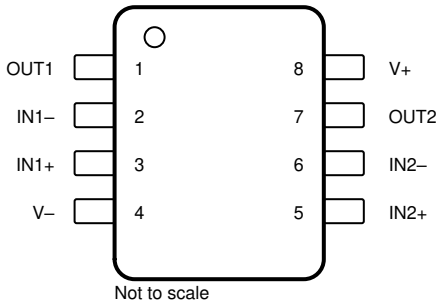
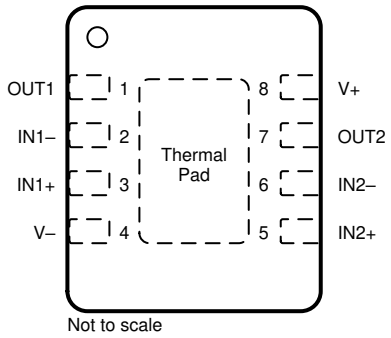


图 6-6. TLV9002 D, DGK, PW, DDF Package
8-Pin SOIC, VSSOP, TSSOP, SOT-23
Top View



A. Connect thermal pad to V – .

图 6-7. TLV9002 DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View

表 6-3. Pin Functions: TLV9002

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 –	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 –	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V –	4	I or —	Negative (low) supply or ground (for single-supply operation)

表 6-3. Pin Functions: TLV9002 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
V+	8	I	Positive (high) supply

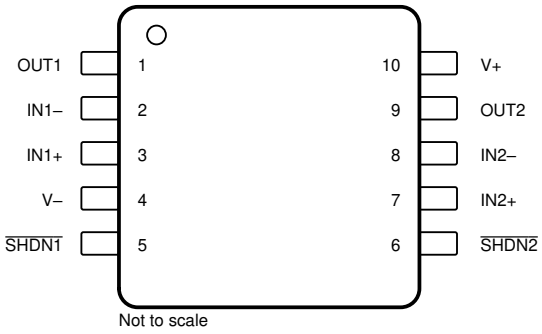


图 6-8. TLV9002S DGS Package
10-Pin VSSOP
Top View

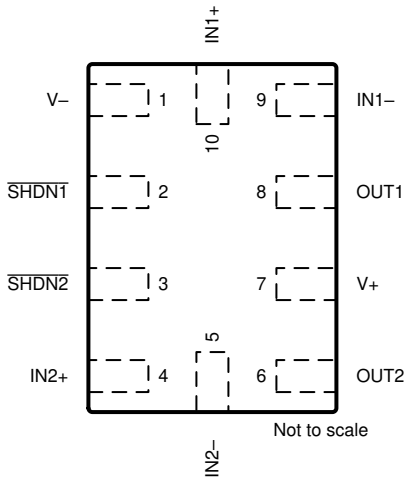


图 6-9. TLV9002S RUG Package
10-Pin X2QFN
Top View

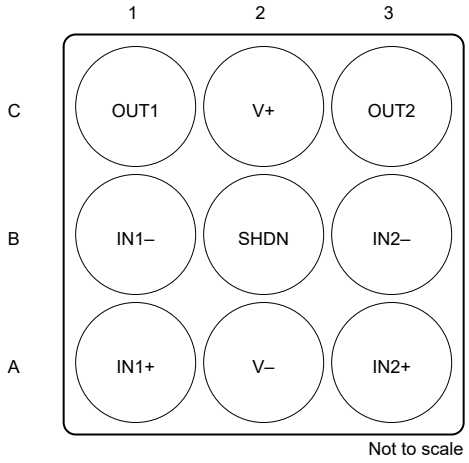


图 6-10. TLV9002S YCK Package
9-Pin DSBGA (WCSP)
Bottom View

表 6-4. Pin Functions: TLV9002S

PIN				I/O	DESCRIPTION
NAME	VSSOP	X2QFN	DSBGA (WCSP)		
IN1 –	2	9	B1	I	Inverting input, channel 1
IN1+	3	10	A1	I	Noninverting input, channel 1
IN2 –	8	5	B3	I	Inverting input, channel 2

表 6-4. Pin Functions: TLV9002S (continued)

PIN				I/O	DESCRIPTION
NAME	VSSOP	X2QFN	DSBGA (WCSP)		
IN2+	7	4	A3	I	Noninverting input, channel 2
OUT1	1	8	C1	O	Output, channel 1
OUT2	9	6	C3	O	Output, channel 2
$\overline{SHDN1}$	5	2	—	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. See 节 8.5 for more information.
$\overline{SHDN2}$	6	3	—	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. See 节 8.5 for more information.
$\overline{SHDN}$	—	—	B2		Shutdown: low = both amplifiers disabled, high = both amplifiers enabled
V –	4	1	A2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	10	7	C2	I	Positive (high) supply

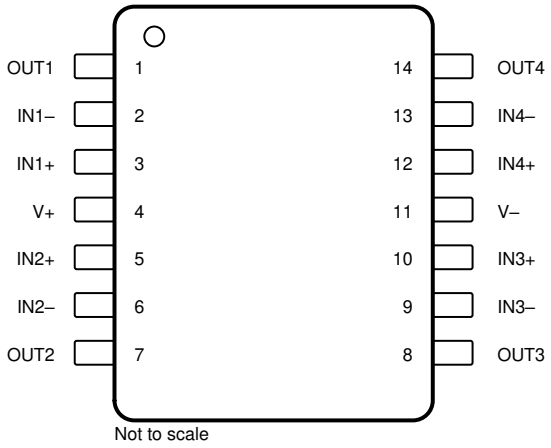


图 6-11. TLV9004 D, DYY, PW Package
14-Pin SOIC, SOT-23 (14), TSSOP
Top View

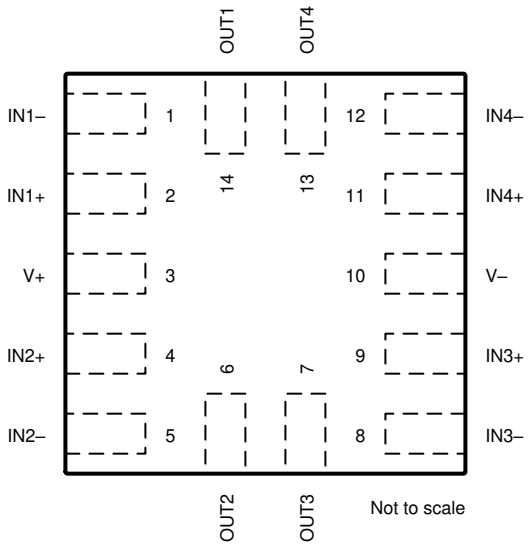
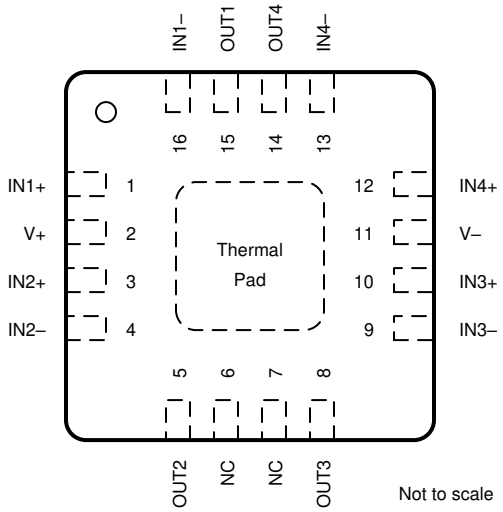


图 6-12. TLV9004 RUC Package
14-Pin X2QFN
Top View



A. Connect thermal pad to V – .

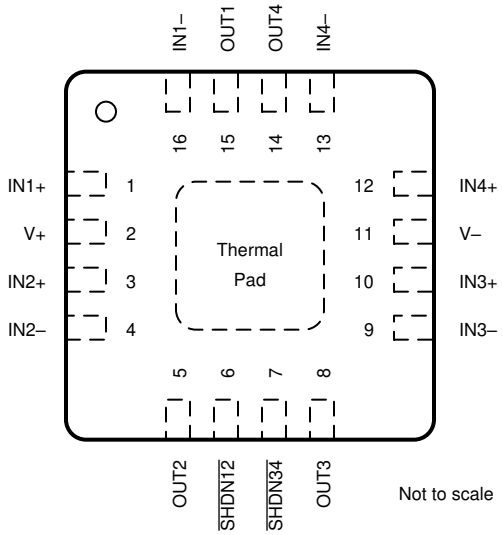
图 6-13. TLV9004 RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View

表 6-5. Pin Functions: TLV9004

PIN				I/O	DESCRIPTION
NAME	SOIC, SOT-23 (14), TSSOP	WQFN	X2QFN		
IN1 –	2	16	1	I	Inverting input, channel 1
IN1+	3	1	2	I	Noninverting input, channel 1
IN2 –	6	4	5	I	Inverting input, channel 2
IN2+	5	3	4	I	Noninverting input, channel 2

表 6-5. Pin Functions: TLV9004 (continued)

PIN				I/O	DESCRIPTION
NAME	SOIC, SOT-23 (14), TSSOP	WQFN	X2QFN		
IN3 –	9	9	8	I	Inverting input, channel 3
IN3+	10	10	9	I	Noninverting input, channel 3
IN4 –	13	13	12	I	Inverting input, channel 4
IN4+	12	12	11	I	Noninverting input, channel 4
NC	—	6, 7	—	—	No internal connection
OUT1	1	15	14	O	Output, channel 1
OUT2	7	5	6	O	Output, channel 2
OUT3	8	8	7	O	Output, channel 3
OUT4	14	14	13	O	Output, channel 4
V –	11	11	10	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	2	3	I	Positive (high) supply



A. Connect thermal pad to V – .

图 6-14. TLV9004S RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View

表 6-6. Pin Functions: TLV9004S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input
IN1 –	16	I	Inverting input
IN2+	3	I	Noninverting input
IN2 –	4	I	Inverting input
IN3+	10	I	Noninverting input
IN3 –	9	I	Inverting input
IN4+	12	I	Noninverting input
IN4 –	13	I	Inverting input
$\overline{\text{SHDN12}}$	6	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. See 节 8.5 for more information.
$\overline{\text{SHDN34}}$	7	I	Shutdown: low = amp disabled, high = amp enabled, channel 3 and 4. See 节 8.5 for more information.
OUT1	15	O	Output
OUT2	5	O	Output
OUT3	8	O	Output
OUT4	14	O	Output
V –	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	2	I	Positive (high) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage (V+) – (V–)				7	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		
Operating, T_A			–55	150	°C
Junction, T_J				150	°C
Storage, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

TLV9002S PACKAGE			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
ALL OTHER PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

7.4 Thermal Information: TLV9001

THERMAL METRIC[1]		TLV9001				UNIT
		DBV (SOT-23)	DCK (SC70)	DPW (X2SON)	DRL (SOT-553)[2]	
		5 PINS	5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.9	239.6	470.0	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153.8	148.5	211.9	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.9	82.3	334.8	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	77.2	54.5	29.8	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.4	81.8	333.2	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) This package option for TLV9001 is preview only.

7.5 Thermal Information: TLV9001S

THERMAL METRIC[1]		TLV9001S		UNIT
		DBV (SOT-23)	DCK (SC70)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.9	215.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153.8	146.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.9	72.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	77.2	55.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.4	71.7	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.6 Thermal Information: TLV9002

THERMAL METRIC[1]		TLV9002						UNIT
		D (SOIC)	DGK (VSSOP)	DGS (VSSOP)	DSG (WSON)	PW (TSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	10 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	207.9	201.2	169.5	103.2	200.7	183.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.8	85.7	84.1	120.1	95.4	112.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	129.7	122.9	113	68.8	128.6	98.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26	21.2	15.8	14.7	27.2	18.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	127.9	121.4	111.6	68.5	127.2	97.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.7 Thermal Information: TLV9002S

THERMAL METRIC(1)		TLV9002S			UNIT
		DGS (VSSOP)	RUG (X2QFN)	YCK (DSBGA)	
		10 PINS	10 PINS	9 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.5	194.2	101.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.1	90.3	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	113	122.2	33.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.8	3.5	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	111.6	118.8	33.8	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.8 Thermal Information: TLV9004

THERMAL METRIC(1)		TLV9004					UNIT
		D (SOIC)	DYY (SOT-23)	PW (TSSOP)	RTE (WQFN)	RUC (X2QFN)	
		14 PINS	14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.1	154.3	148.3	66.4	205.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.8	86.8	68.1	69.3	72.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	67.9	92.7	41.7	150.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	10.1	16.9	5.7	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.1	67.5	91.8	41.5	149.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.9 Thermal Information: TLV9004S

THERMAL METRIC(1)		TLV9004S	UNIT
		RTE (WQFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.5	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.10 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.4	±1.6	mV
		V_S = 5 V, T_A = –40°C to 125°C			±2	
dV_{OS}/dT	V_{OS} vs temperature	T_A = –40°C to 125°C		±0.6		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 to 5.5 V, V_{CM} = (V–)	80	105		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C		86		dB
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C		95		
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to 125°C	63	77		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to 125°C		68		
INPUT BIAS CURRENT						
I_B	Input bias current	V_S = 5 V		±5		pA
I_{OS}	Input offset current			±2		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, V_S = 5 V		4.7		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz, V_S = 5 V		30		nV/√Hz
		f = 10 kHz, V_S = 5 V		27		
i_n	Input current noise density	f = 1 kHz, V_S = 5 V		23		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			1.5		pF
C_{IC}	Common-mode			5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	117		dB
		V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		100		
		V_S = 1.8 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 2 kΩ		115		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 5 V		1		MHz
ϕ_m	Phase margin	V_S = 5.5 V, G = 1		78		°
SR	Slew rate	V_S = 5 V		2		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step, G = +1, C_L = 100 pF		2.5		µs
		To 0.01%, V_S = 5 V, 2-V step, G = +1, C_L = 100 pF		3		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.85		µs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, 80-kHz measurement BW		0.004%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ		10	20	mV
		V_S = 5.5 V, R_L = 2 kΩ		35	55	
I_{SC}	Short-circuit current	V_S = 5.5 V		±40		mA

7.10 Electrical Characteristics (continued)

For V_S = (V+) – (V –) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_O	Open-loop output impedance	V_S = 5 V, f = 1 MHz		1200		Ω

7.10 Electrical Characteristics (continued)

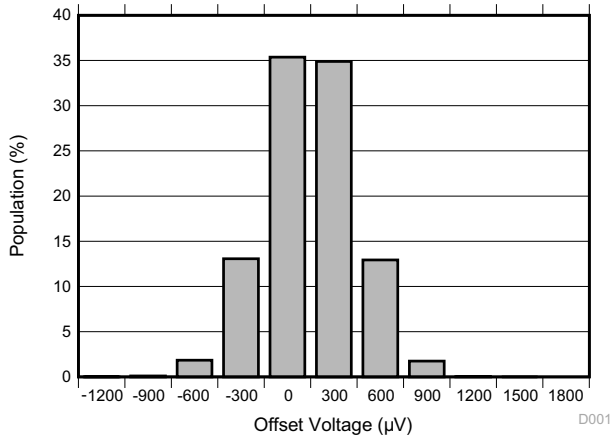
For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_S	Specified voltage range			1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	TLV9002, TLV9002S TLV9004, TLV9004S	I_O = 0 mA, V_S = 5.5 V		60	75	µA
		TLV9001, TLV9001S	I_O = 0 mA, V_S = 5.5 V		60	77	
		I_O = 0 mA, V_S = 5.5 V, T_A = –40°C to 125°C				85	
SHUTDOWN(1)							
I_{QSD}	Quiescent current per amplifier	V_S = 1.8 V to 5.5 V, all amplifiers disabled, $\overline{SHDN}$ = V_S –			0.5	1.5	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 1.8 V to 5.5 V, amplifier disabled			10 || 2		GΩ || pF
	High level voltage shutdown threshold (amplifier enabled)	V_S = 1.8 V to 5.5 V			(V–) + 0.9	(V–) + 1.1	V
	Low level voltage shutdown threshold (amplifier disabled)	V_S = 1.8 V to 5.5 V		(V–) + 0.2 V	(V–) + 0.7 V		V
t_{ON}	Amplifier enable time (full shutdown)	V_S = 1.8 V to 5.5 V, full shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2, R_L connected to V–			70		µs
	Amplifier enable time (partial shutdown)	V_S = 1.8 V to 5.5 V, partial shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2, R_L connected to V–			50		
t_{OFF}	Amplifier disable time	V_S = 1.8 V to 5.5 V, G = 1, V_{OUT} = 0.1 × V_S / 2, R_L connected to V–			4		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≥ $\overline{SHDN}$ ≥ (V+) – 0.8 V			40		nA
		V_S = 1.8 V to 5.5 V, V– ≤ $\overline{SHDN}$ ≤ V– + 0.8 V			150		

(1) Specified by design and characterization; not production tested.

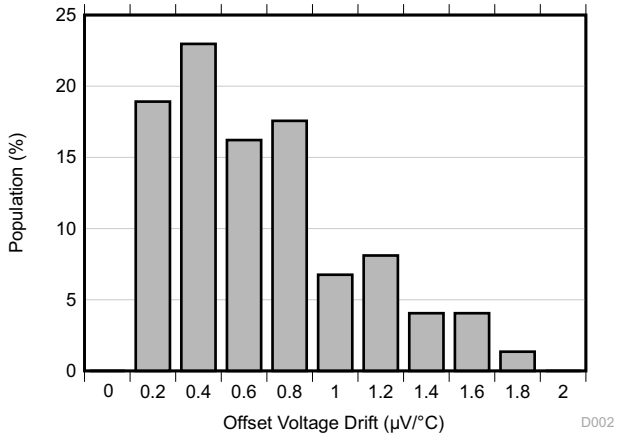
7.11 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5 V

图 7-1. Offset Voltage Distribution Histogram



V_S = 5 V, T_A = –40°C to 125°C

图 7-2. Offset Voltage Drift Distribution Histogram

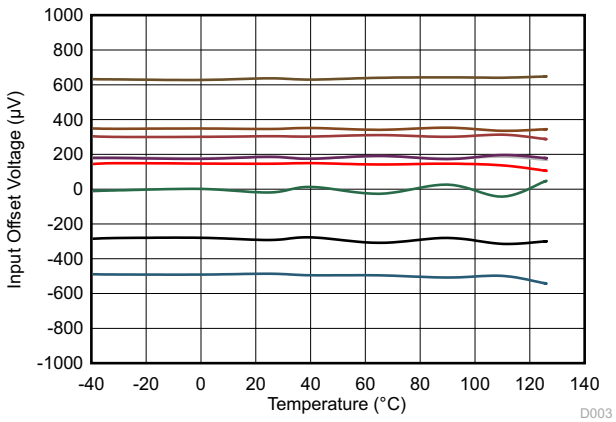


图 7-3. Input Offset Voltage vs Temperature

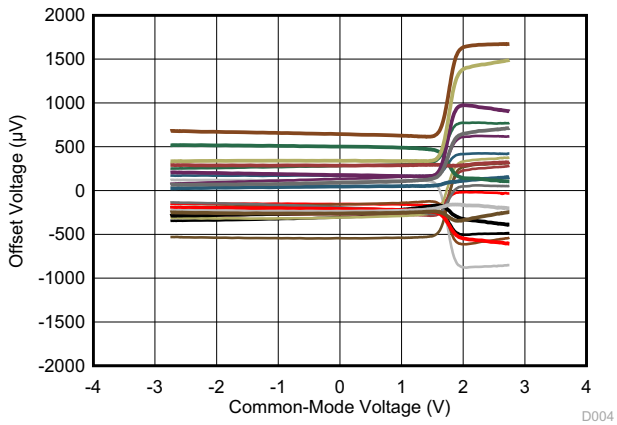


图 7-4. Offset Voltage vs Common-Mode

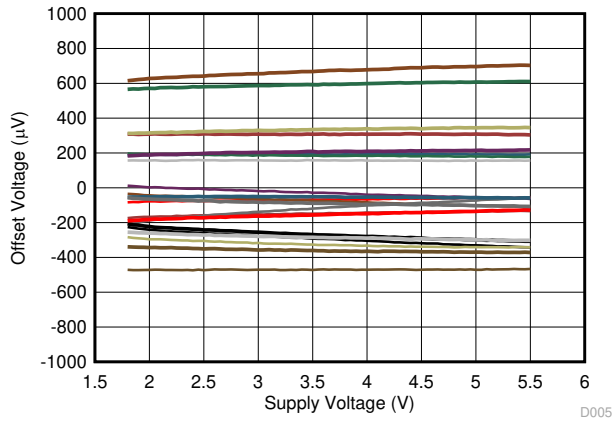


图 7-5. Offset Voltage vs Supply Voltage

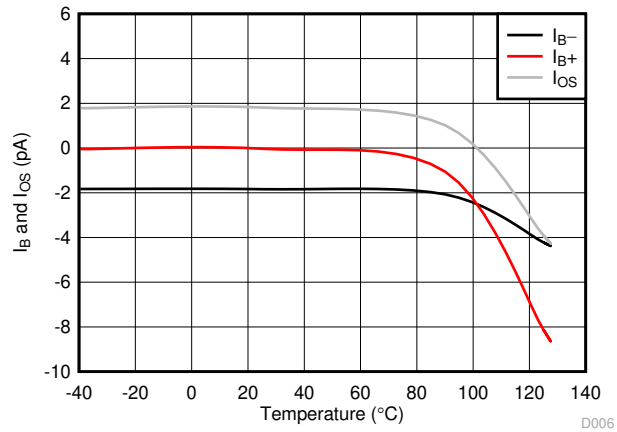


图 7-6. I_B and I_{OS} vs Temperature

7.11 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

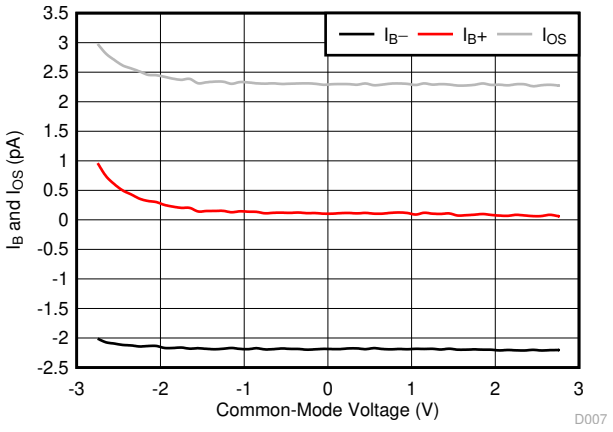


图 7-7. I_B and I_{OS} vs Common-Mode Voltage

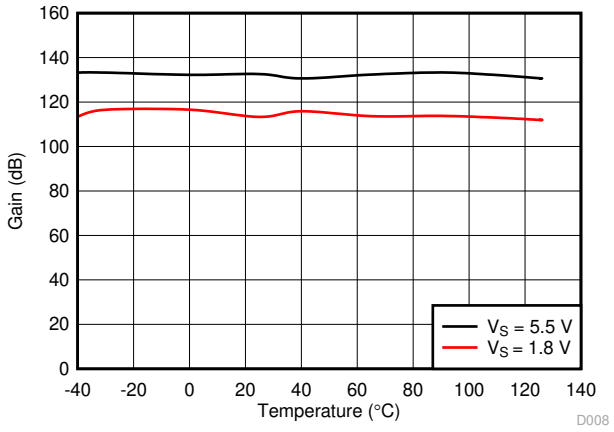
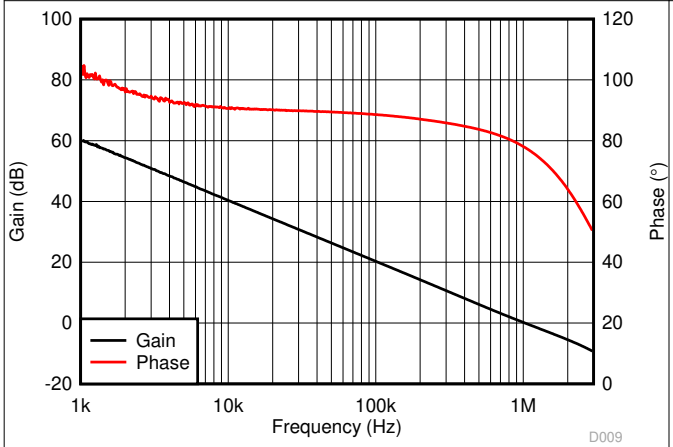


图 7-8. Open-Loop Gain vs Temperature



C_L = 10 pF

图 7-9. Open-Loop Gain and Phase vs Frequency

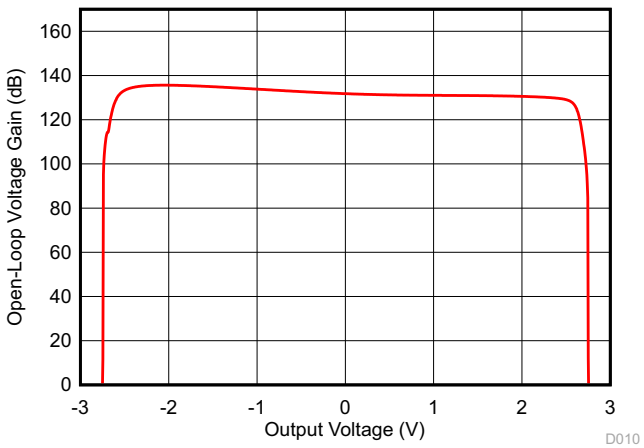
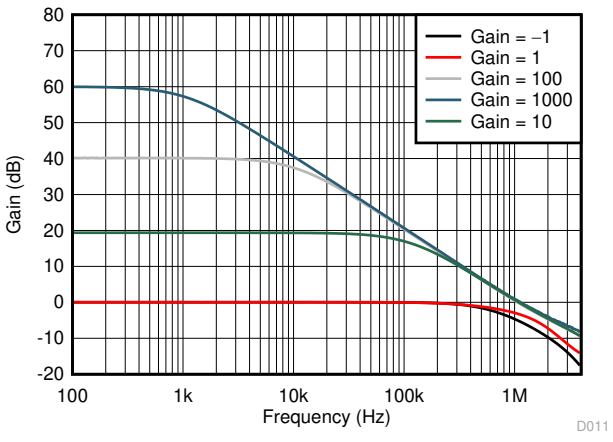


图 7-10. Open-Loop Gain vs Output Voltage



C_L = 10 pF

图 7-11. Closed-Loop Gain vs Frequency

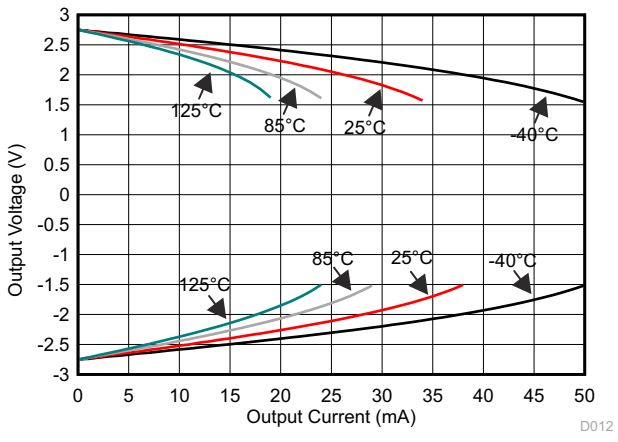


图 7-12. Output Voltage vs Output Current (Claw)

7.11 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

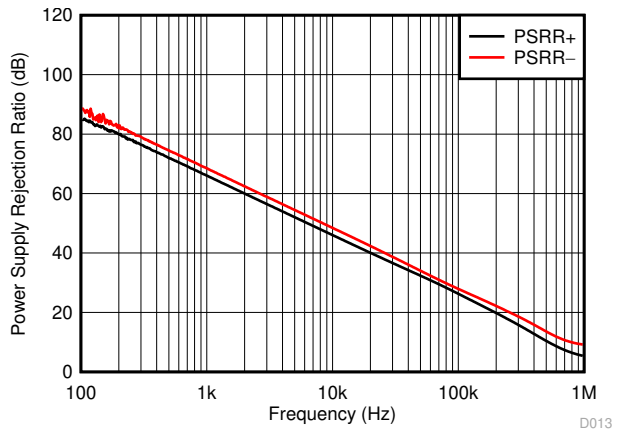
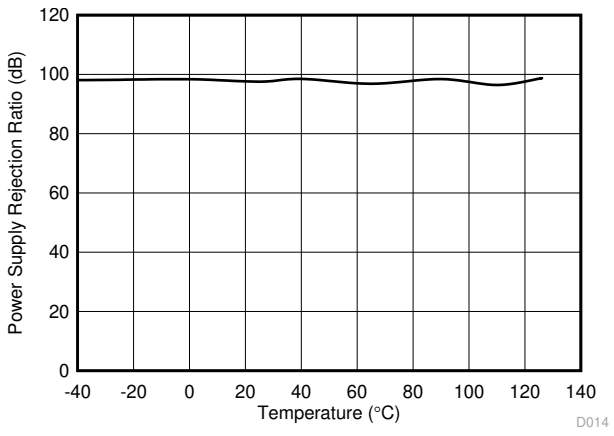


图 7-13. PSRR vs Frequency



V_S = 1.8 V to 5.5 V

图 7-14. DC PSRR vs Temperature

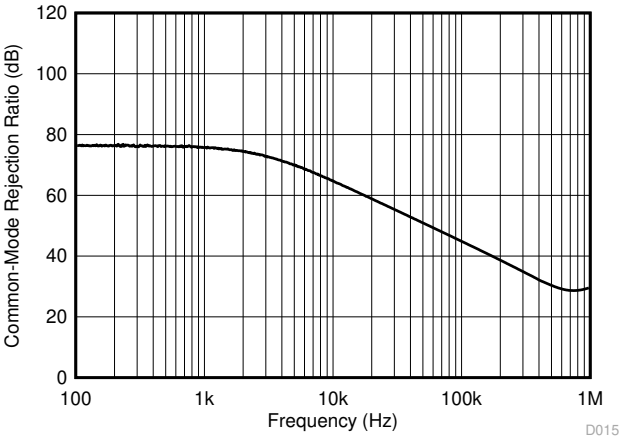
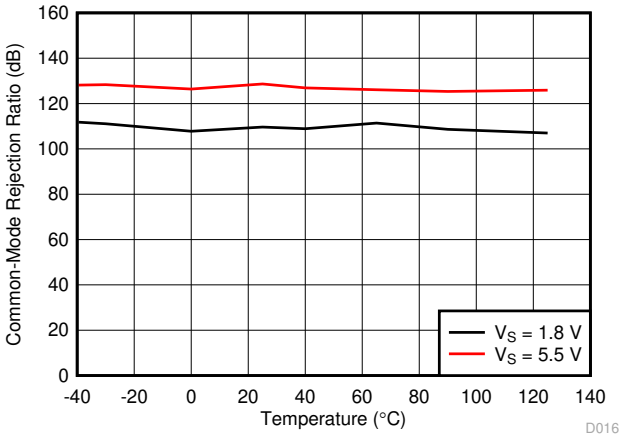


图 7-15. CMRR vs Frequency



V_{CM} = (V–) – 0.1 V to (V+) – 1.4 V

图 7-16. DC CMRR vs Temperature

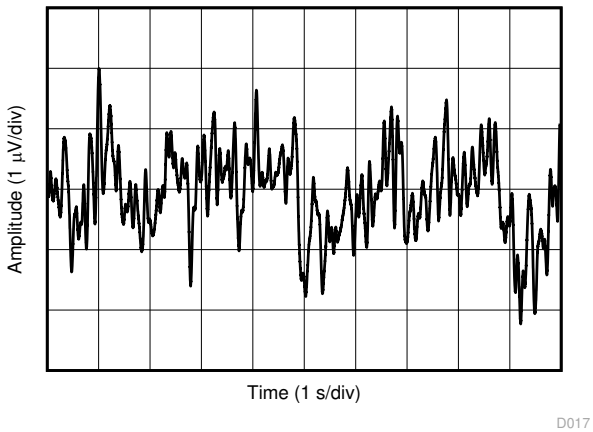


图 7-17. 0.1-Hz to 10-Hz Integrated Voltage Noise

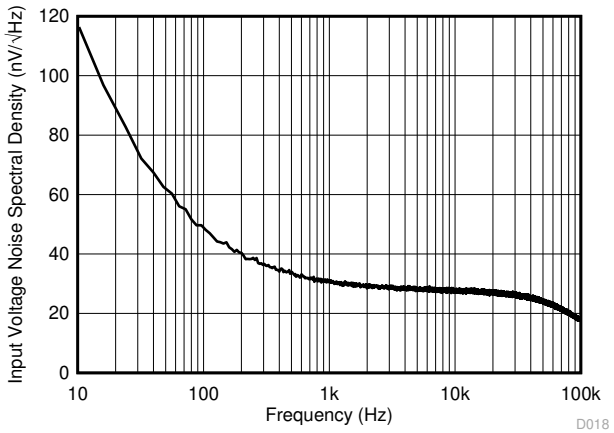
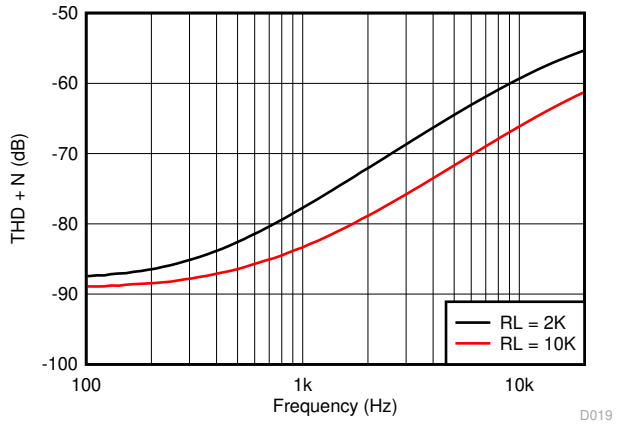


图 7-18. Input Voltage Noise Spectral Density

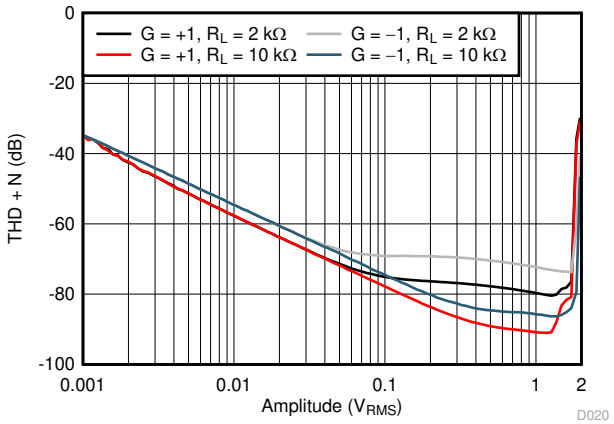
7.11 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V V_{CM} = 2.5 V G = 1
BW = 80 kHz V_{OUT} = 0.5 V_{RMS}

图 7-19. THD + N vs Frequency



V_S = 5.5 V V_{CM} = 2.5 V f = 1 kHz
G = 1 BW = 80 kHz

图 7-20. THD + N vs Amplitude

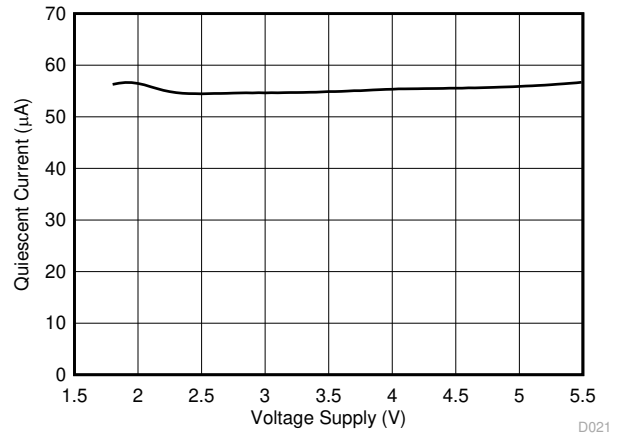


图 7-21. Quiescent Current vs Supply Voltage

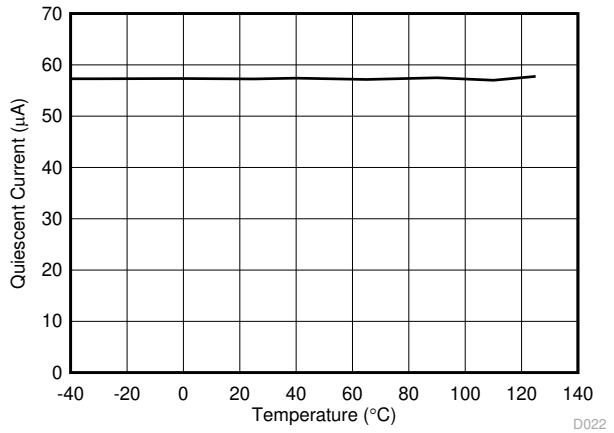


图 7-22. Quiescent Current vs Temperature

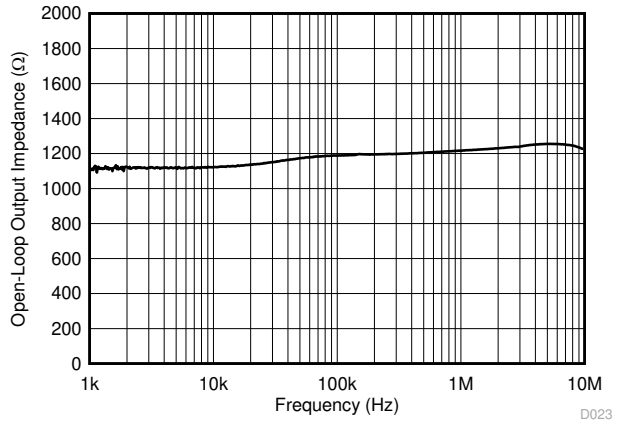
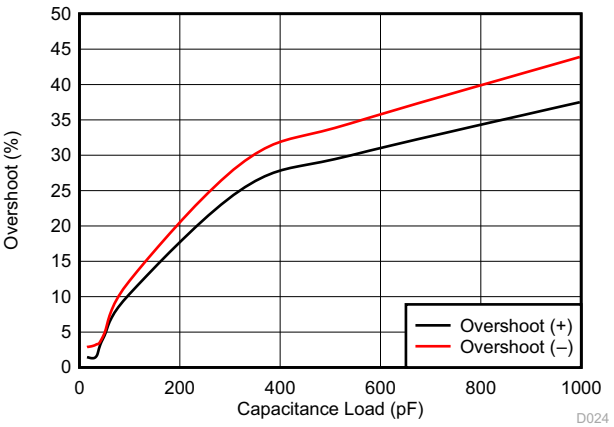


图 7-23. Open-Loop Output Impedance vs Frequency

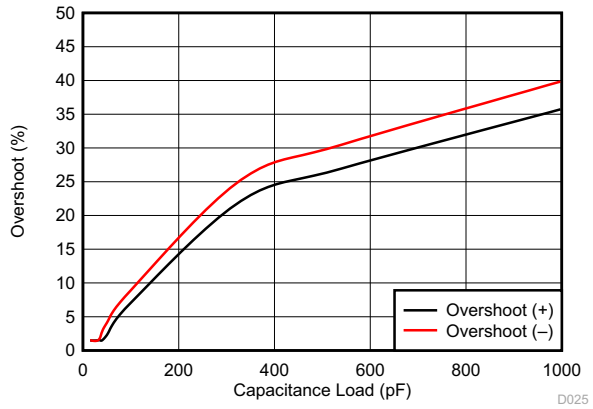


G = 1 V_{IN} = 100 mVpp

图 7-24. Small Signal Overshoot vs Capacitive Load

7.11 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = –1 V_{IN} = 100 mVpp

图 7-25. Small Signal Overshoot vs Capacitive Load

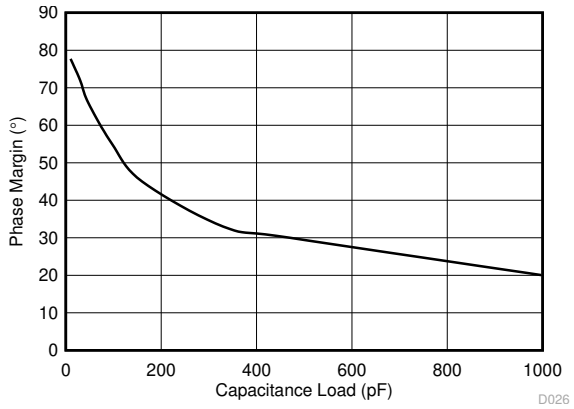
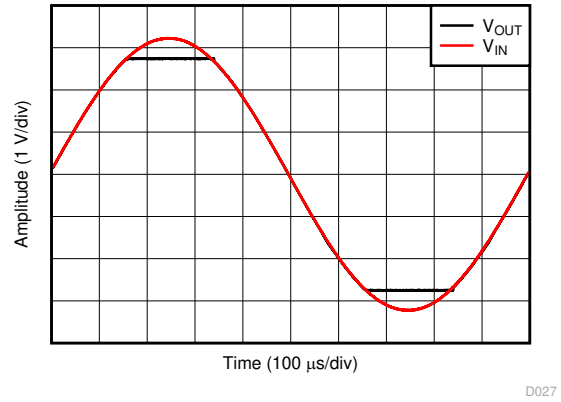
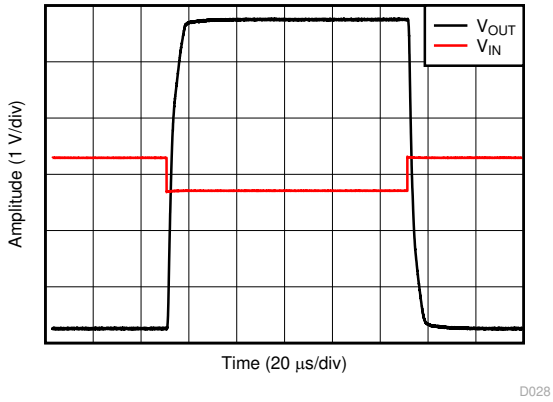


图 7-26. Phase Margin vs Capacitive Load



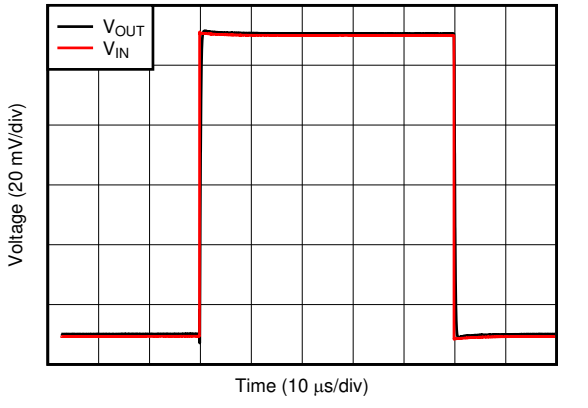
G = 1 V_{IN} = 6.5 V_{PP}

图 7-27. No Phase Reversal



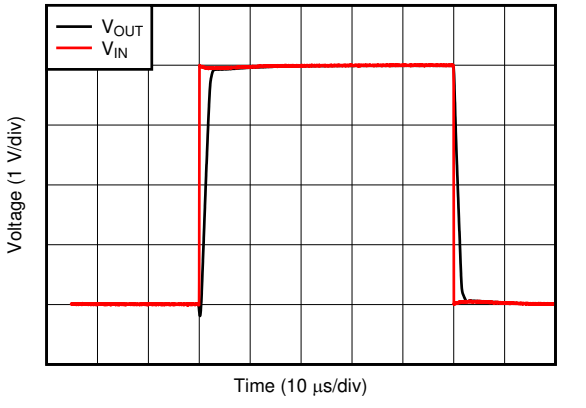
G = –10 V_{IN} = 600 mV_{PP}

图 7-28. Overload Recovery



G = 1 V_{IN} = 100 mV_{PP} C_L = 10 pF

图 7-29. Small-Signal Step Response



G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

图 7-30. Large-Signal Step Response

7.11 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

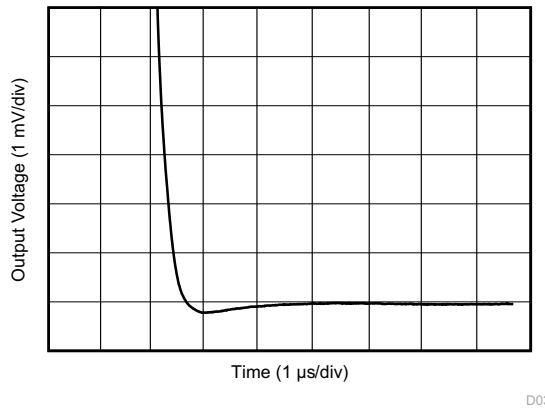


图 7-31. Large-Signal Settling Time (Negative)

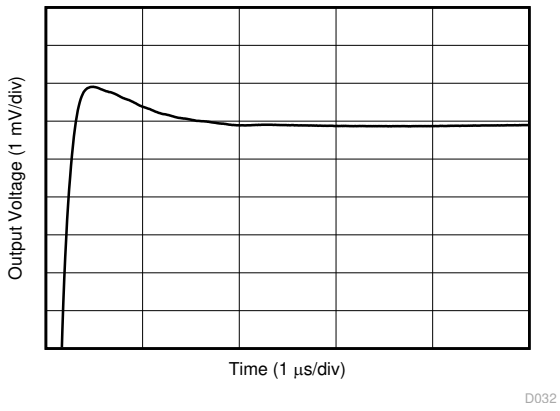


图 7-32. Large-Signal Settling Time (Positive)

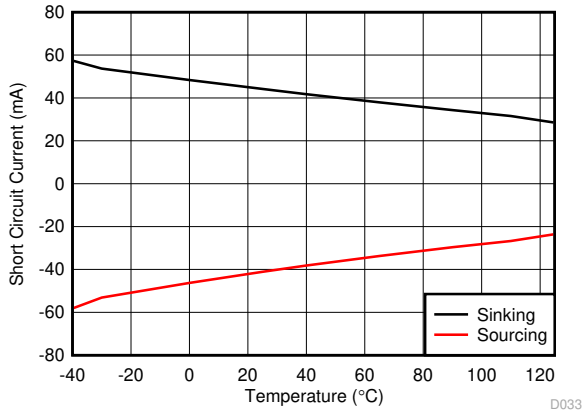


图 7-33. Short-Circuit Current vs Temperature

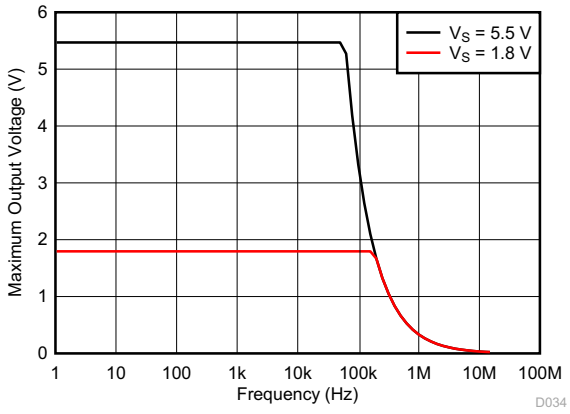


图 7-34. Maximum Output Voltage vs Frequency

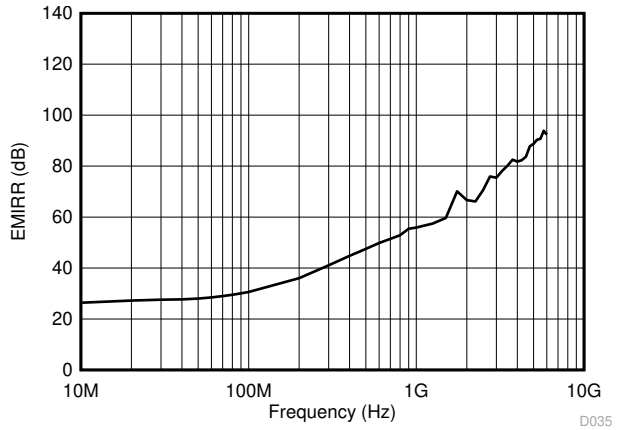


图 7-35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

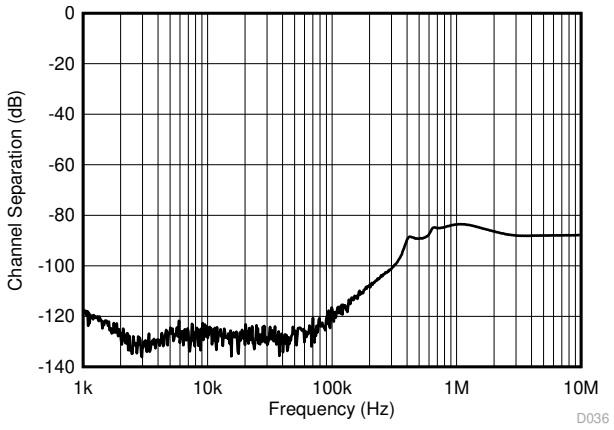


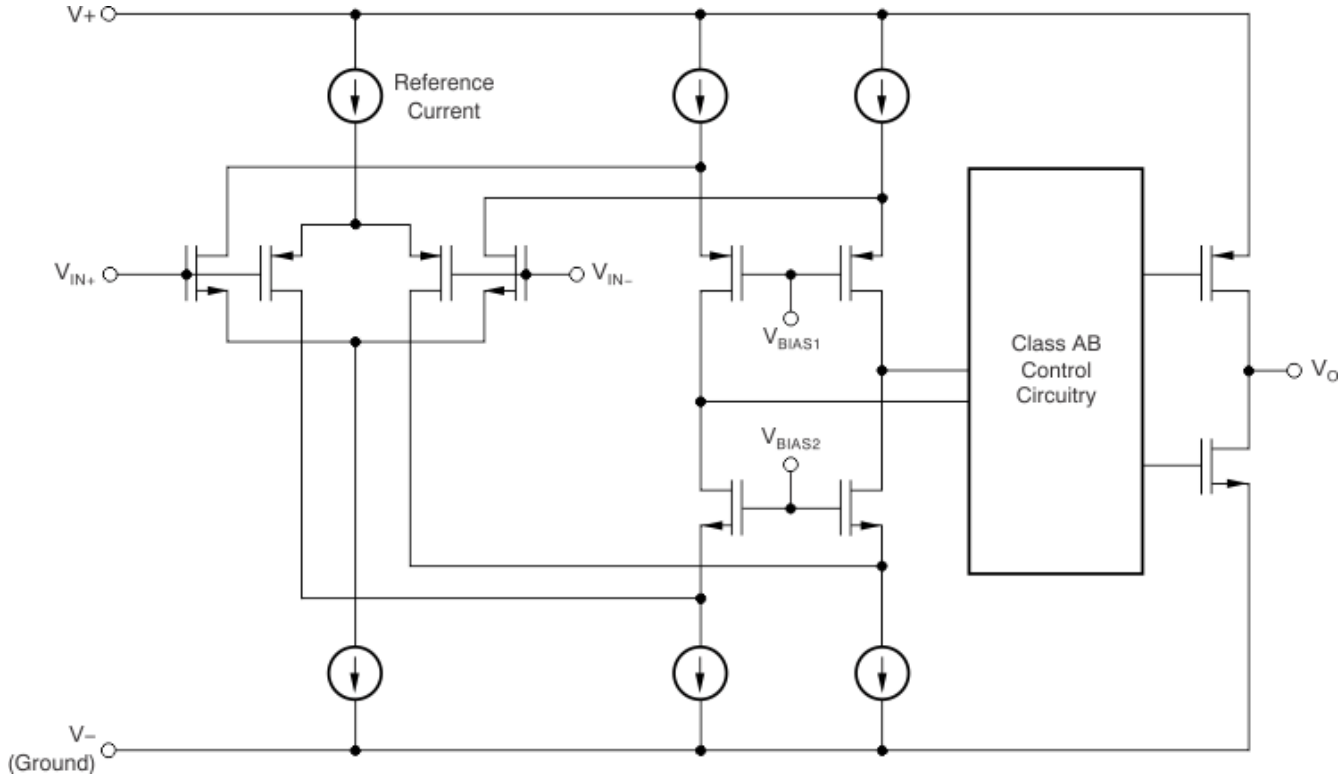
图 7-36. Channel Separation

8 Detailed Description

8.1 Overview

The TLV900x is a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV900x family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV900x family of op amps are for operation from 1.8 V to 5.5 V. In addition, many specifications such as input offset voltage, quiescent current, offset current, and short circuit current apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in 节 7.11.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV900x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in 节 8.2. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 100-mV transition region can vary up to 100 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV900x family delivers a robust output drive capability. A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 20 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 EMI Rejection

The TLV900x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV900x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 8-1 shows the results of this testing on the TLV900x. 表 8-1 shows the EMIRR IN+ values for the TLV900x at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

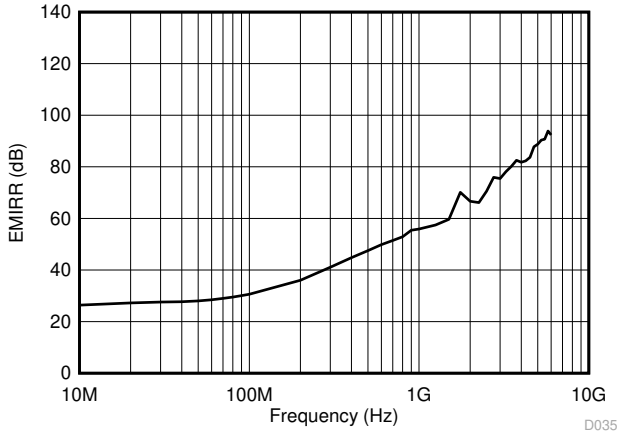


图 8-1. EMIRR Testing

表 8-1. TLV900x EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB

8.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV900x family is approximately 850 ns.

8.5 Shutdown

The TLV9001S, TLV9002S, and TLV9004S devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1 µA. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 620 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V – and V – + 0.2 V. A valid logic high is defined as a voltage between V – + 1.2 V and V+. The shutdown pin circuitry includes a pull-up resistor, which will inherently pull the voltage of the pin to the positive supply rail if not driven. Thus, to enable the amplifier, the $\overline{\text{SHDN}}$ pins should either be left floating or driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. While we highly recommend that the shutdown pin be connected to a valid high or a low voltage or driven, we have included a pull-up resistor connected to VCC. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5 V. Exceeding this voltage level will damage the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 70 µs for full shutdown of all channels; disable time is 4 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV9002S and TLV9004S to operate as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the TLV9001S, TLV9002S, or TLV9004S without a load, the resulting turnoff time significantly increases.

8.6 Device Functional Modes

The TLV900x family has a single functional mode. The devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV900x family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable applications. The devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10-kΩ loads connected to any point between V+ and V–. The input common-mode voltage range includes both rails, and allows the TLV900x devices to be used in any single-supply application.

9.2 Typical Application

9.2.1 TLV900x Low-Side, Current Sensing Application

图 9-1 shows the TLV900x configured in a low-side current sensing application.

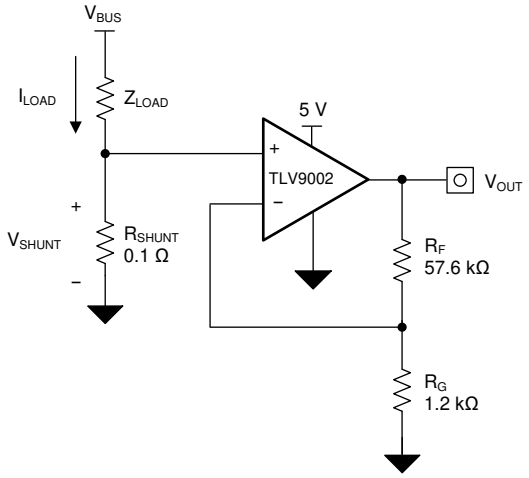


图 9-1. TLV900x in a Low-Side, Current-Sensing Application

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 9-1 is given in 方程式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is shown using 方程式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using 方程式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV900x to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the TLV900x to produce the necessary output voltage is calculated using 方程式 3.

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \tag{3}$$

Using 方程式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 方程式 4 sizes the resistors R_F and R_G, to set the gain of the TLV900x to 49 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{4}$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49 V/V. 图 9-2 shows the measured transfer function of the circuit shown in 图 9-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

9.2.1.3 Application Curve

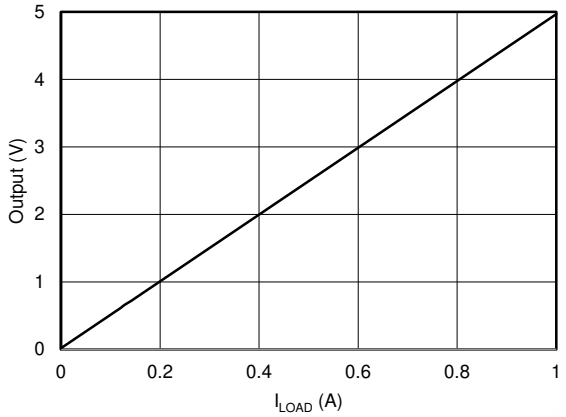


图 9-2. Low-Side, Current-Sense Transfer Function

9.2.2 Single-Supply Photodiode Amplifier

Photodiodes are used in many applications to convert light signals to electrical signals. The current through the photodiode is proportional to the photon energy absorbed, and is commonly in the range of a few hundred picoamps to a few tens of microamps. An amplifier in a transimpedance configuration is typically used to convert the low-level photodiode current to a voltage signal for processing in an MCU. The circuit shown in 图 9-3 is an example of a single-supply photodiode amplifier circuit using the TLV9002.

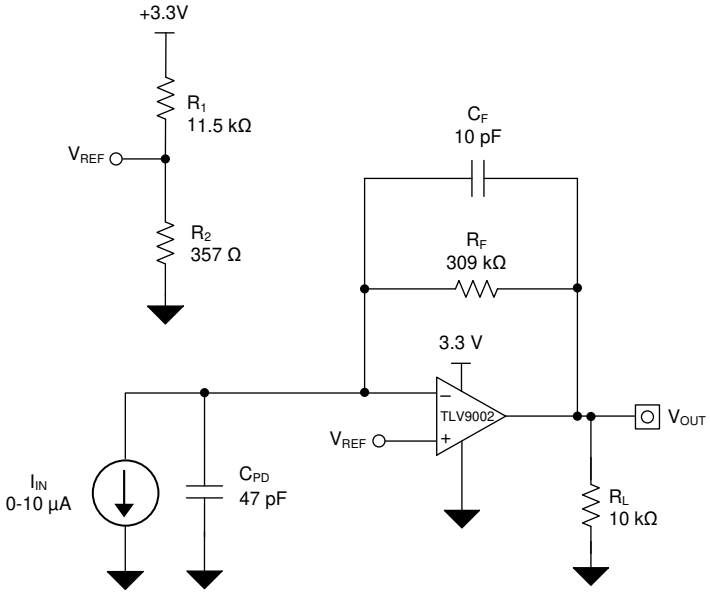


图 9-3. Single-Supply Photodiode Amplifier Circuit

9.2.2.1 Design Requirements

The design requirements for this design are:

- Supply voltage: 3.3 V
- Input: 0 µA to 10 µA
- Output: 0.1 V to 3.2 V
- Bandwidth: 50 kHz

9.2.2.2 Detailed Design Procedure

The transfer function between the output voltage (V_{OUT}), the input current, (I_{IN}) and the reference voltage (V_{REF}) is defined in 方程式 5.

$$V_{OUT} = I_{IN} \times R_F + V_{REF} \tag{5}$$

Where:

$$V_{REF} = V_+ \times \left(\frac{R_1 \times R_2}{R_1 + R_2} \right) \tag{6}$$

Set V_{REF} to 100 mV to meet the minimum output voltage level by setting R1 and R2 to meet the required ratio calculated in 方程式 7.

$$\frac{V_{REF}}{V_+} = \frac{0.1\ V}{3.3\ V} = 0.0303 \tag{7}$$

The closest resistor ratio to meet this ratio sets R1 to 11.5 kΩ and R2 to 357 Ω.

The required feedback resistance can be calculated based on the input current and desired output voltage.

$$R_F = \frac{V_{OUT} - V_{REF}}{I_{IN}} = \frac{3.2\ V - 0.1\ V}{10\ \mu A} = 310 \frac{kV}{A} \approx 309\ k\Omega \tag{8}$$

Calculate the value for the feedback capacitor based on R_F and the desired –3-dB bandwidth, (f_{-3dB}) using 方程式 9.

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_{-3dB}} = \frac{1}{2 \times \pi \times 309\ k\Omega \times 50\ kHz} = 10.3\ pF \approx 10\ pF \tag{9}$$

The minimum op amp bandwidth required for this application is based on the value of R_F, C_F, and the capacitance on the INx– pin of the TLV9002 which is equal to the sum of the photodiode shunt capacitance, (CPD) the common-mode input capacitance, (CCM) and the differential input capacitance (CD) as 方程式 10 shows.

$$C_{IN} = C_{PD} + C_{CM} + C_D = 47\ pF + 5\ pF + 1\ pF = 53\ pF \tag{10}$$

The minimum op amp bandwidth is calculated in 方程式 11.

$$f_{-BGW} \geq \frac{C_{IN} + C_F}{2 \times \pi \times R_F \times C_F^2} \geq 324\ kHz \tag{11}$$

The 1-MHz bandwidth of the TLV900x meets the minimum bandwidth requirement and remains stable in this application configuration.

9.2.2.3 Application Curves

The measured current-to-voltage transfer function for the photodiode amplifier circuit is shown in 图 9-4. The measured performance of the photodiode amplifier circuit is shown in 图 9-5.

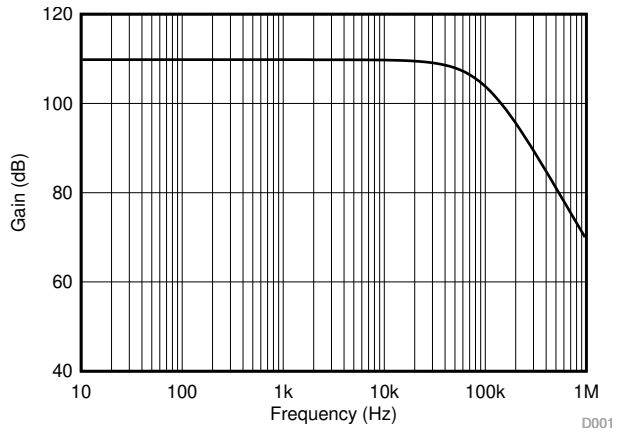


图 9-4. Photodiode Amplifier Circuit AC Gain Results

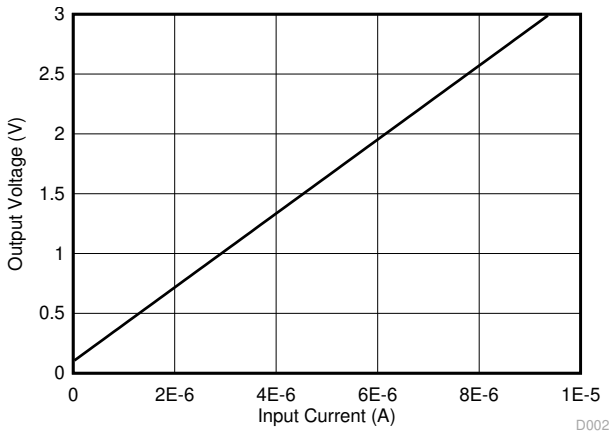


图 9-5. Photodiode Amplifier Circuit DC Results

10 Power Supply Recommendations

The TLV900x family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. 节 7.11 presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see 节 7.1.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see 节 11.1.

10.1 Input and ESD Protection

The TLV900x family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA. 图 10-1 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

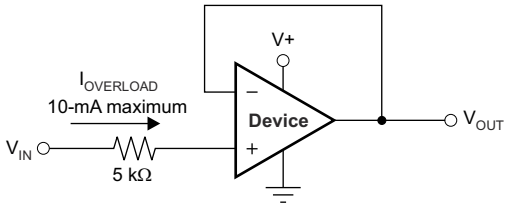


图 10-1. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in 图 11-2. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

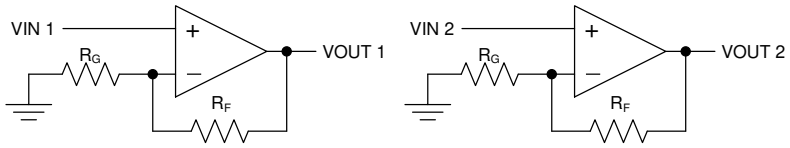


图 11-1. Schematic Representation

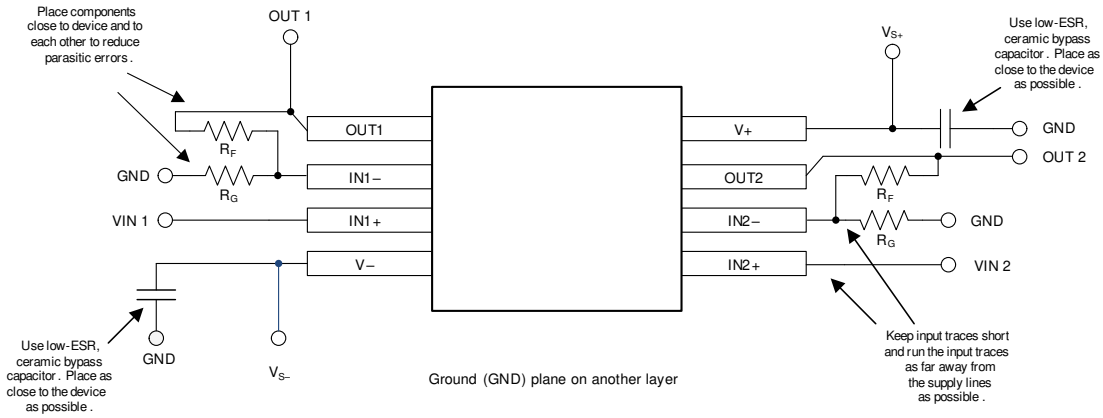


图 11-2. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9001IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OGF	Samples
TLV9001IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1BZ	Samples
TLV9001IDPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DF	Samples
TLV9001SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OJF	Samples
TLV9001SIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1F8	Samples
TLV9001TIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1D6	Samples
TLV9001UIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ODF	Samples
TLV9002IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T902	Samples
TLV9002IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1GNX	Samples
TLV9002IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1GNX	Samples
TLV9002IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TL9002	Samples
TLV9002IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GMH	Samples
TLV9002IDSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GMH	Samples
TLV9002IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	9002	Samples
TLV9002SIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1GDX	Samples
TLV9002SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ENF	Samples
TLV9002SIYCKR	ACTIVE	DSBGA	YCK	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	JK	Samples
TLV9004IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9004	Samples
TLV9004IDYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9004I	Samples
TLV9004IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TLV9004	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9004IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9004	Samples
TLV9004IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1DC	Samples
TLV9004SIRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9004S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV9002, TLV9004 :

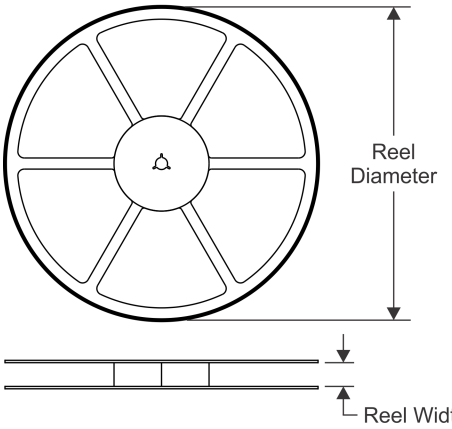
- Automotive : TLV9002-Q1, TLV9004-Q1

NOTE: Qualified Version Definitions:

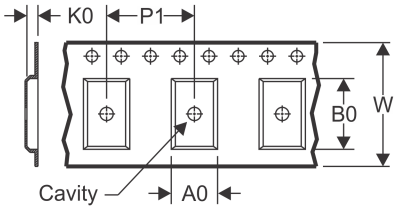
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

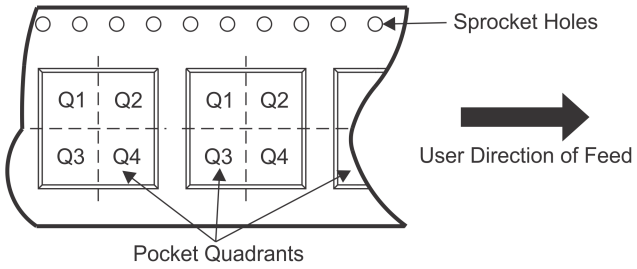


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

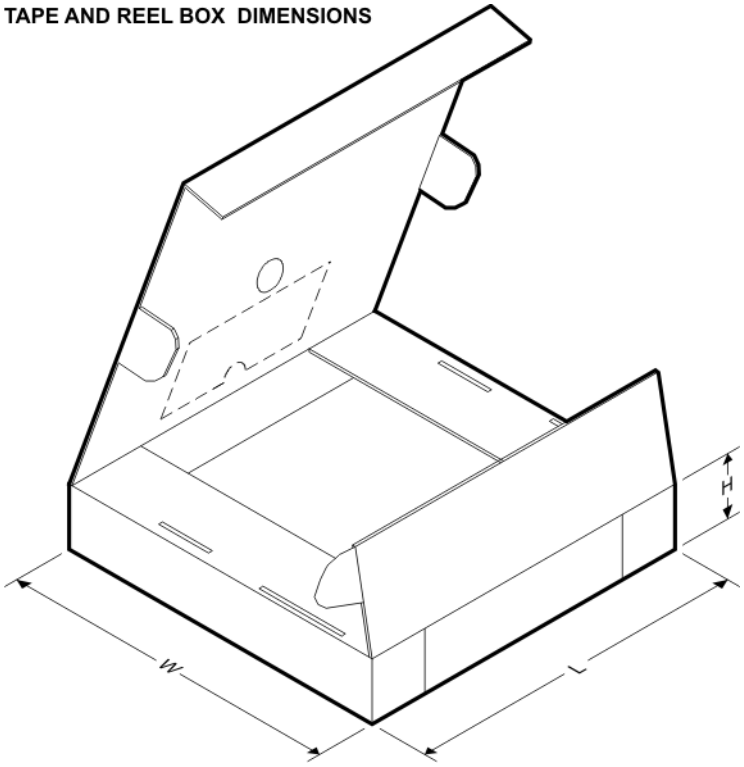


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9001IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9001IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9001IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9001SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9001SIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9001TIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9001UIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9002IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9002IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9002IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9002IDR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9002IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9002IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9002IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9002IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9002SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9002SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9002SIYCKR	DSBGA	YCK	9	3000	180.0	8.4	1.1	1.1	0.4	2.0	8.0	Q1
TLV9004IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9004IDR	SOIC	D	14	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9004IDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV9004IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9004IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9004IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9004SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

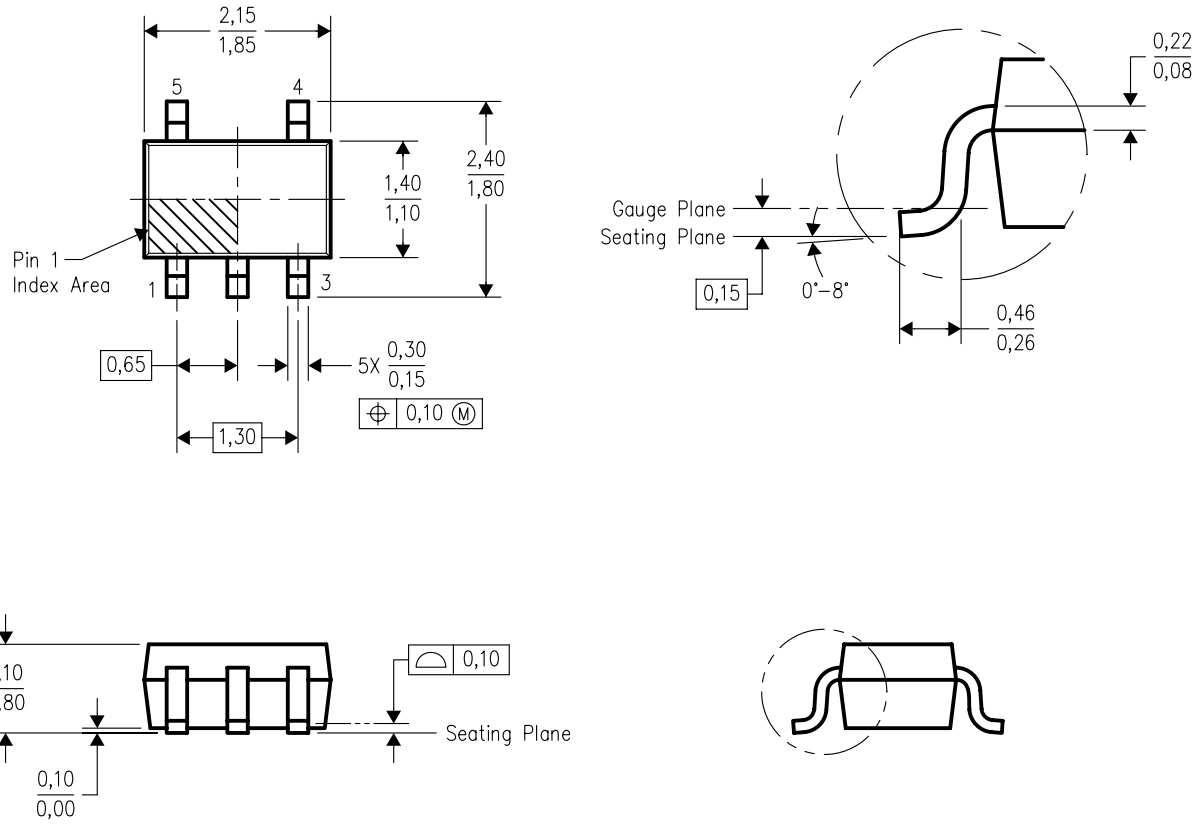


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9001IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9001IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9001IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9001SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9001SIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV9001TIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9001UIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9002IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9002IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9002IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV9002IDR	SOIC	D	8	2500	336.6	336.6	41.3
TLV9002IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9002IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
TLV9002IPWR	TSSOP	PW	8	2000	366.0	364.0	50.0
TLV9002IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV9002SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9002SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9002SIYCKR	DSBGA	YCK	9	3000	182.0	182.0	20.0
TLV9004IDR	SOIC	D	14	2500	853.0	449.0	35.0
TLV9004IDR	SOIC	D	14	2500	336.6	336.6	41.3
TLV9004IDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV9004IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TLV9004IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV9004IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9004SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

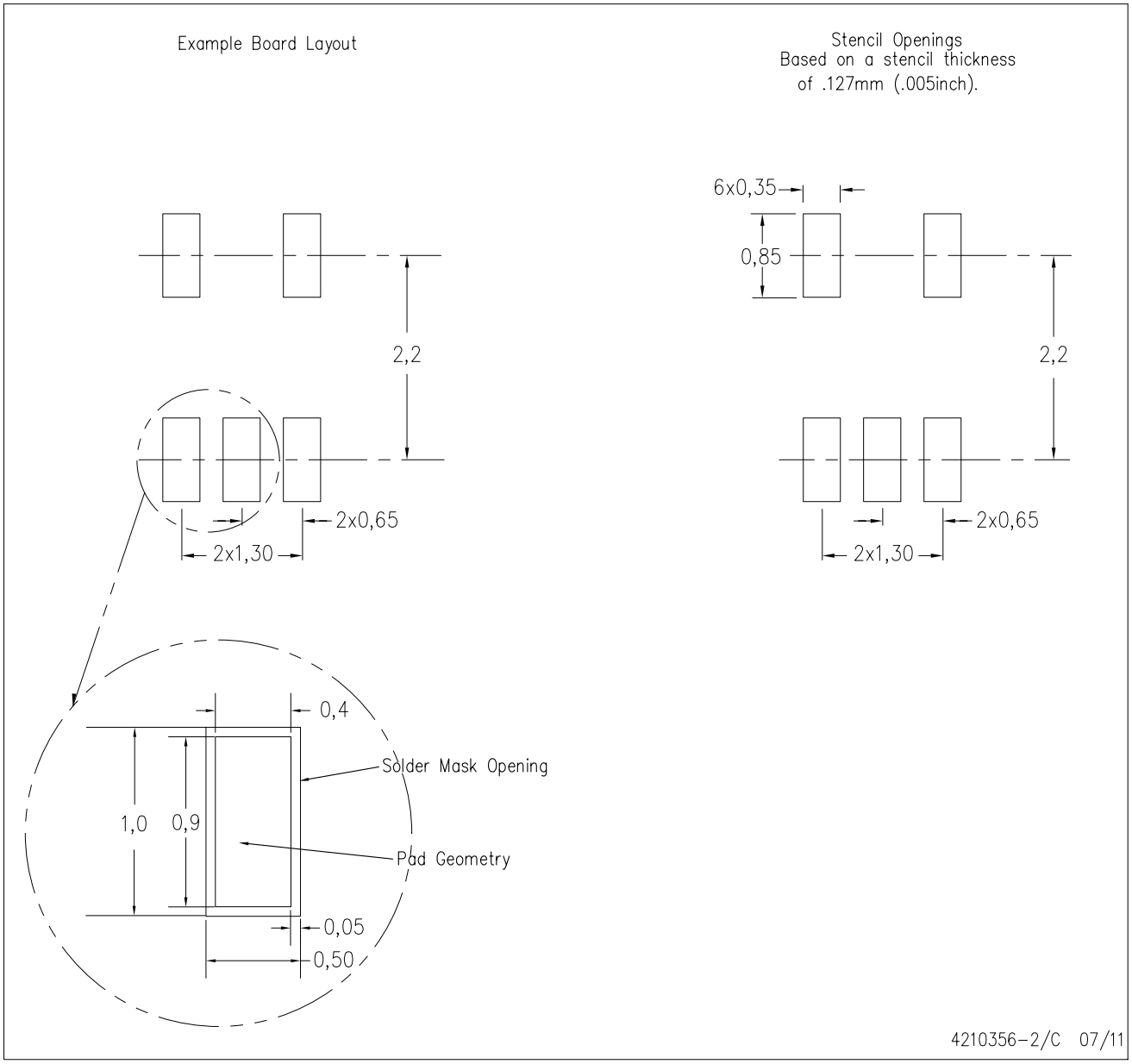
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



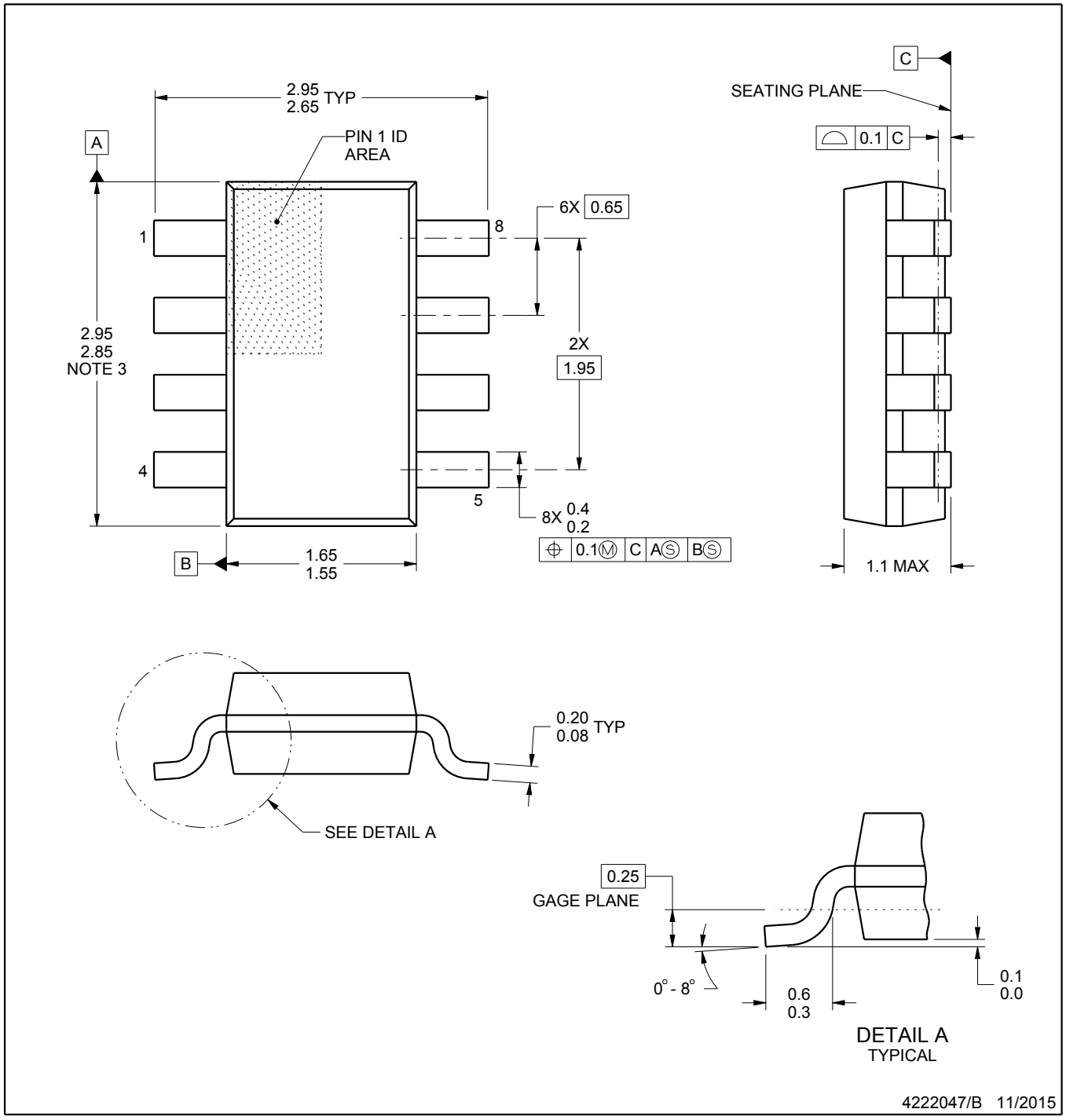
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DDF0008A

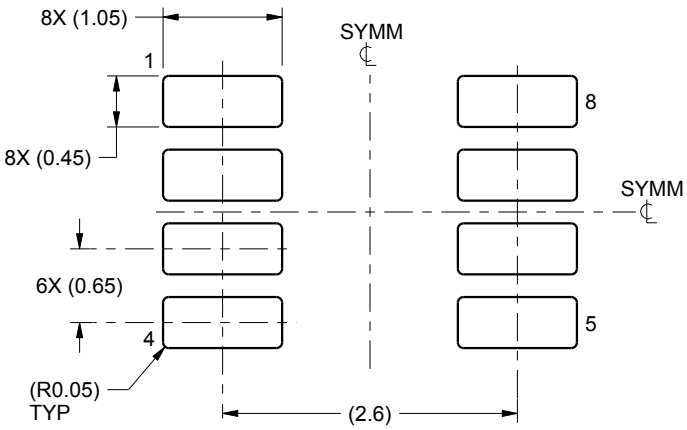
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

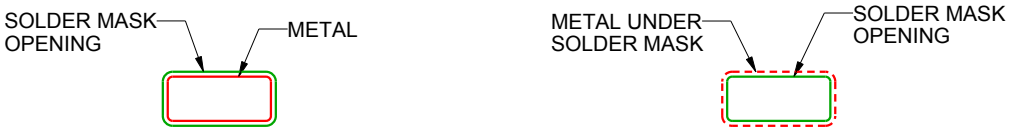


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

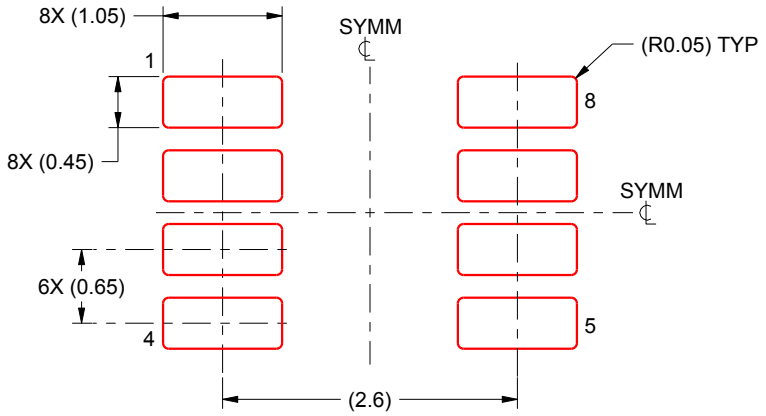
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

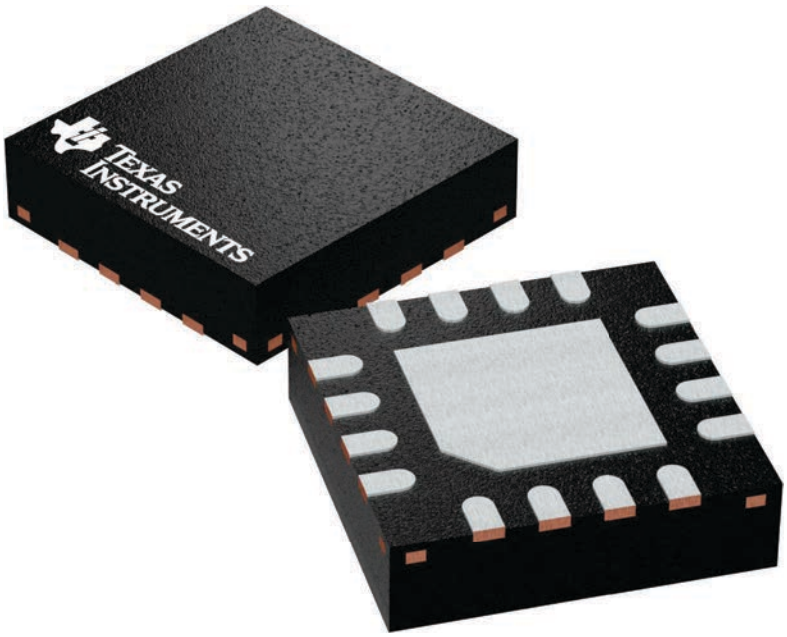
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

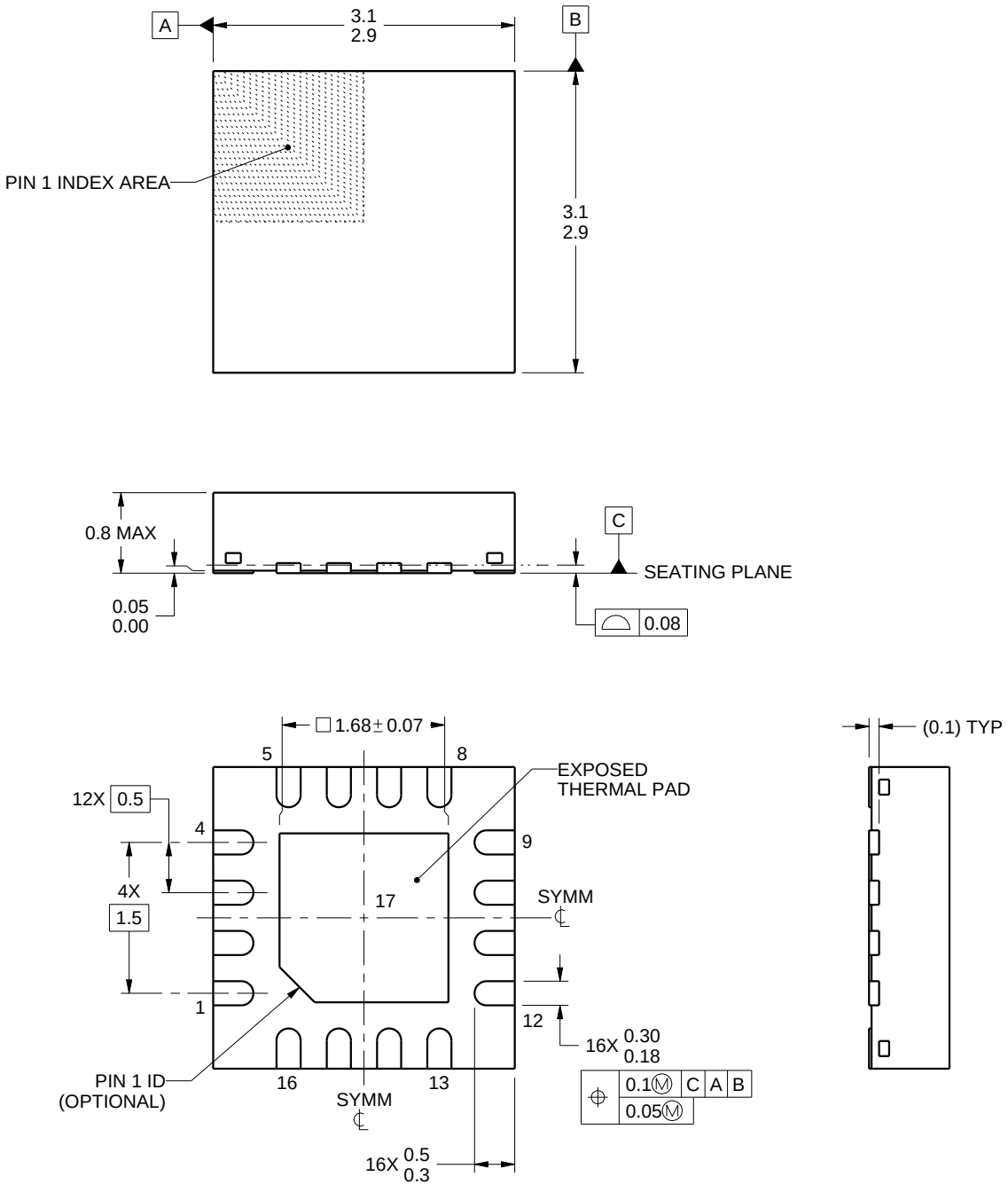


PACKAGE OUTLINE

RTE0016C

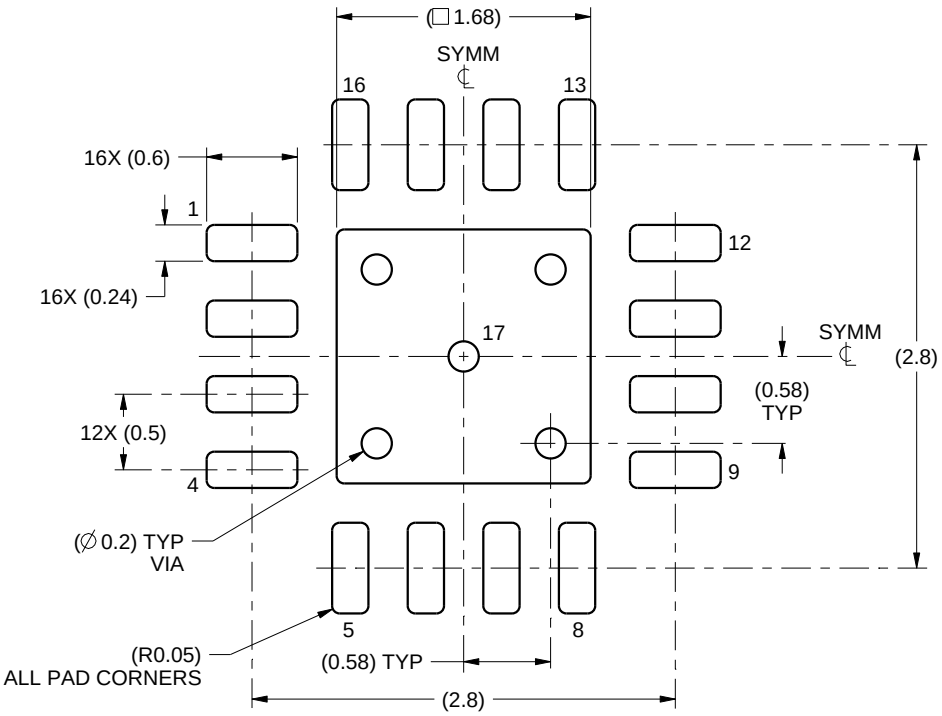
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

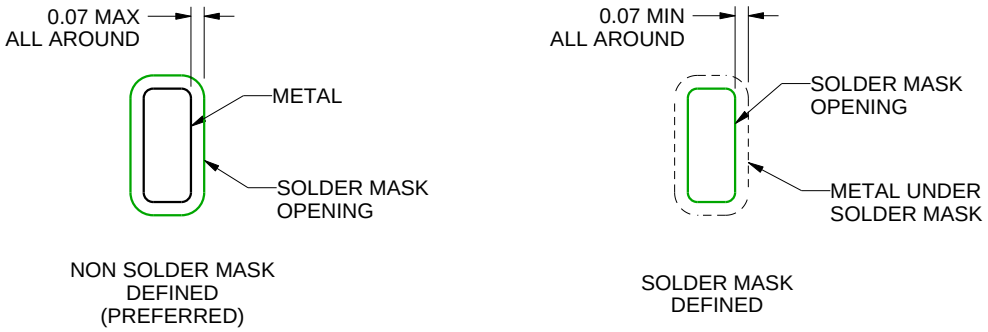


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

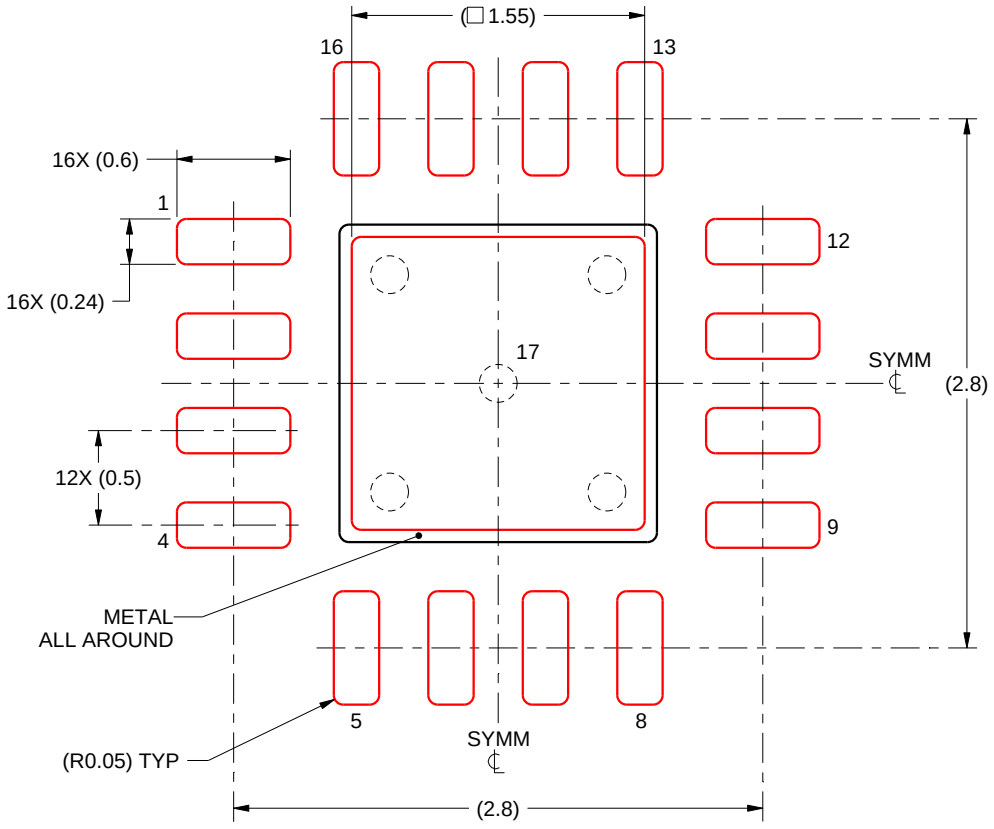


SOLDER MASK DETAILS

4219117/A 09/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/A 09/2016

NOTES: (continued)

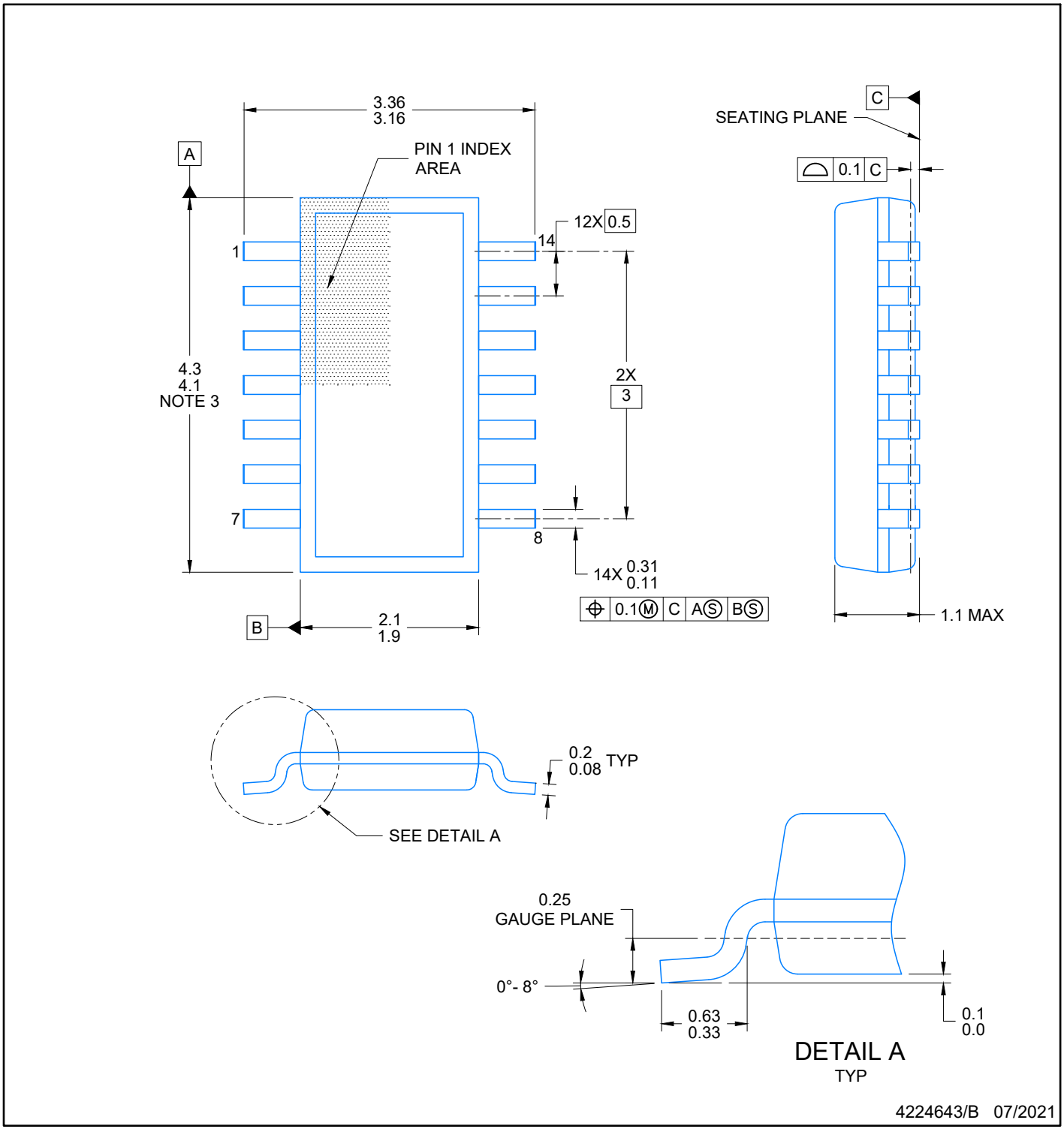
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0014A

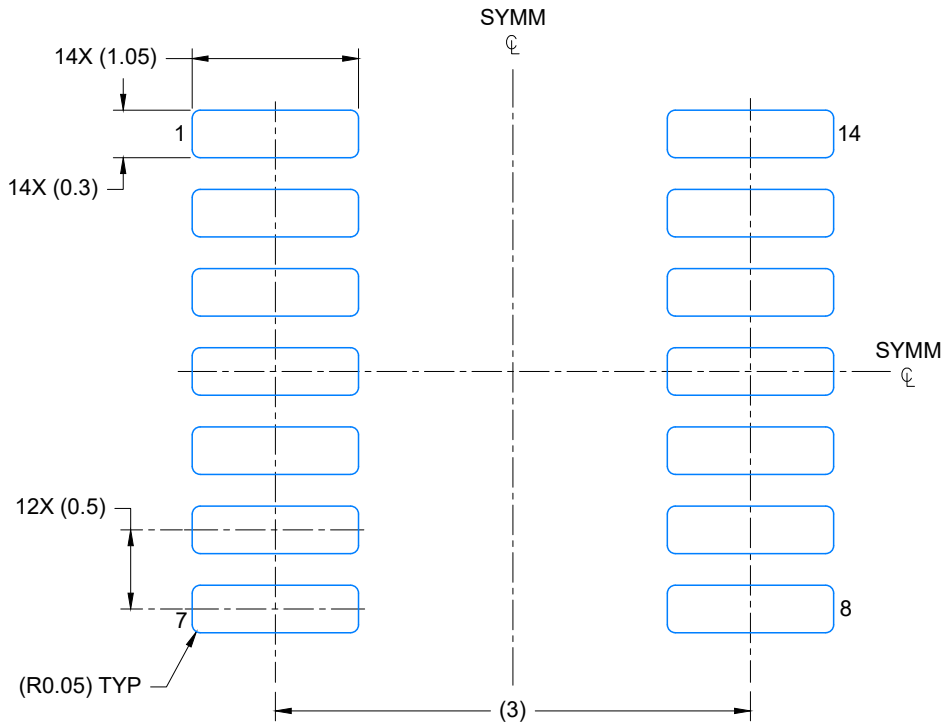
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

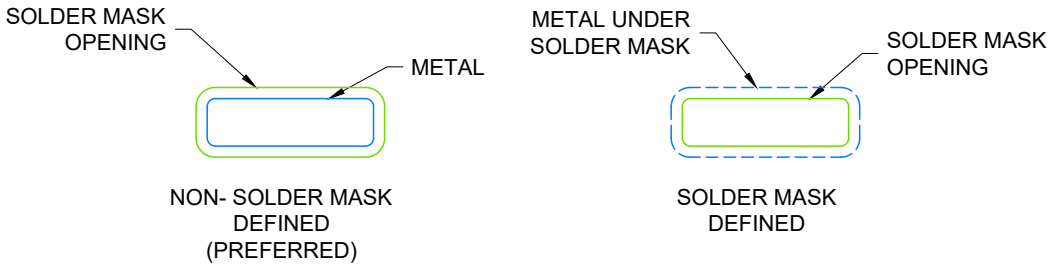


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

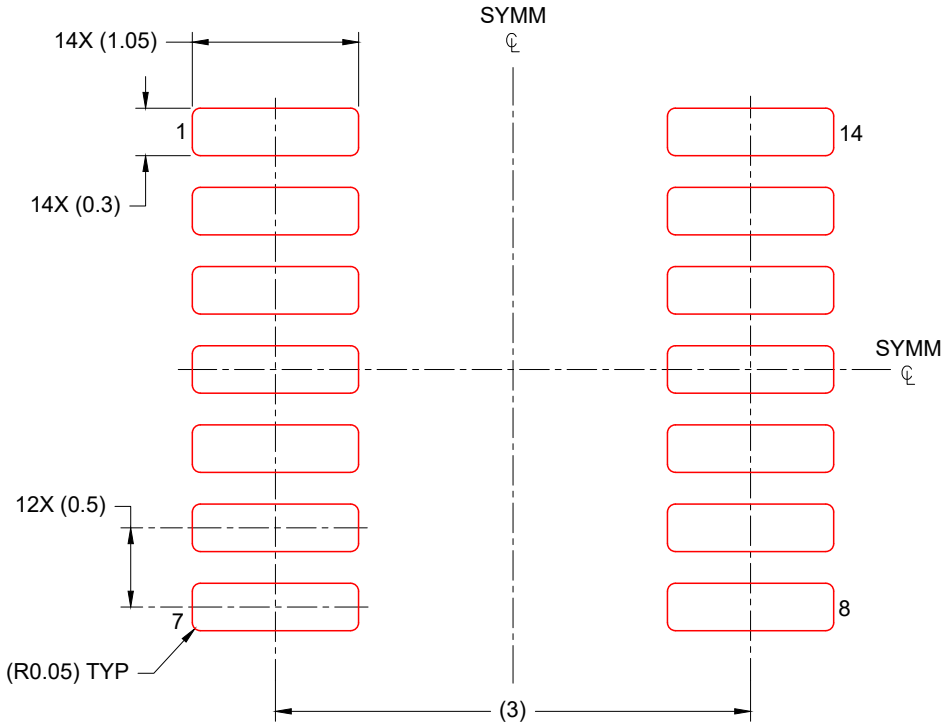


SOLDER MASK DETAILS

4224643/B 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

NOTES: (continued)

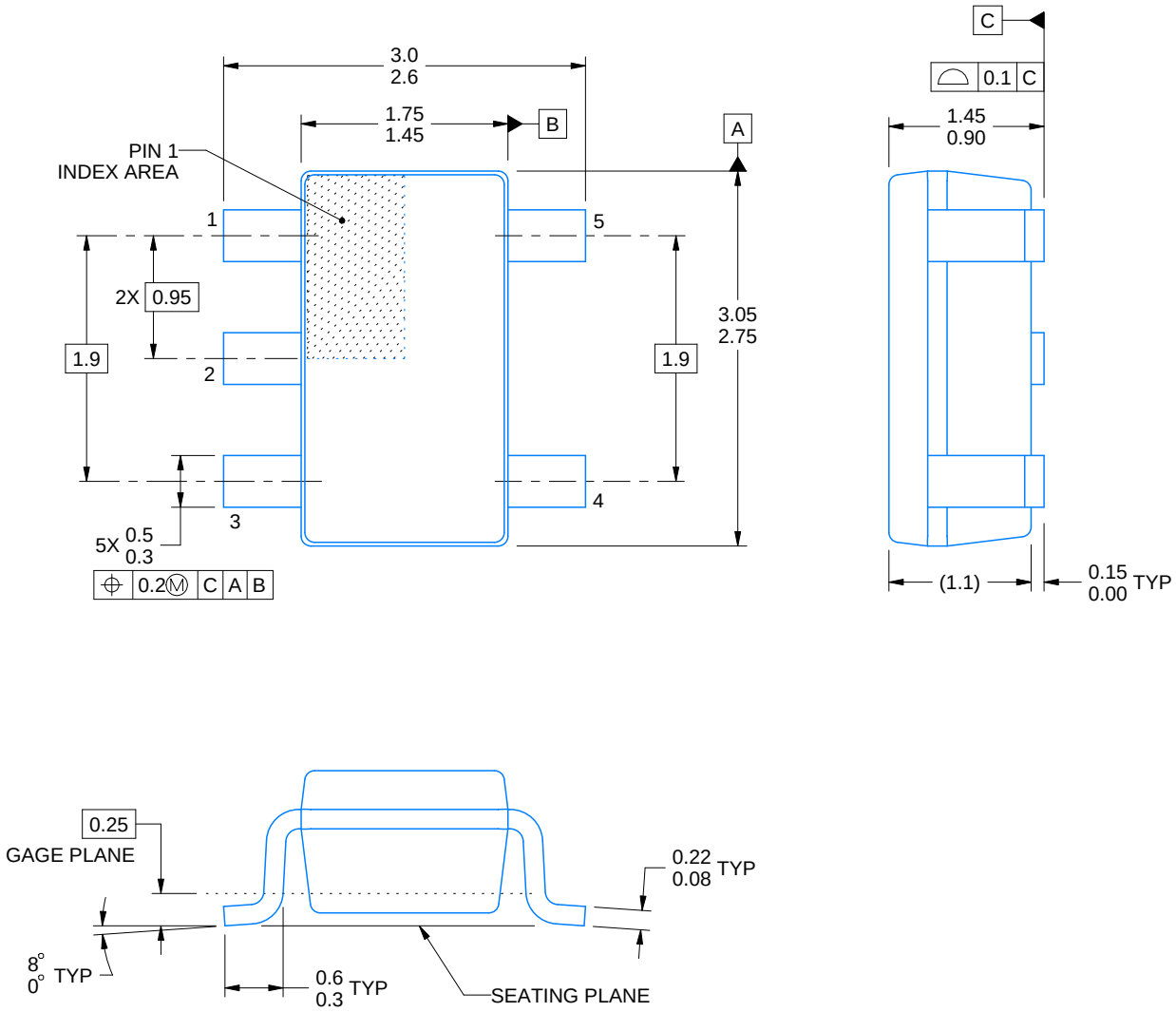
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

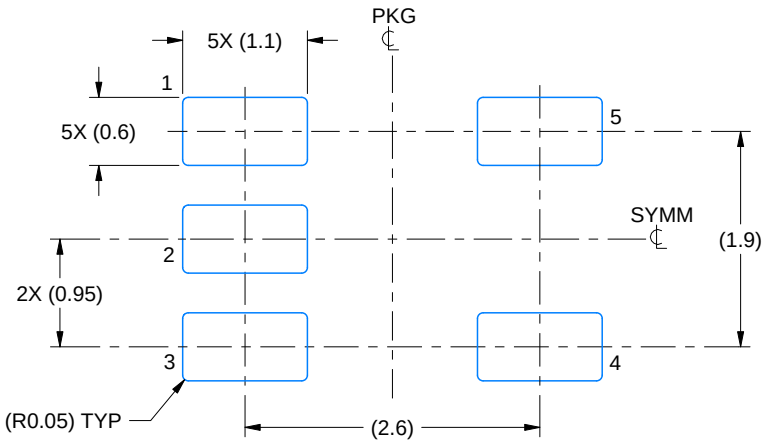
SMALL OUTLINE TRANSISTOR



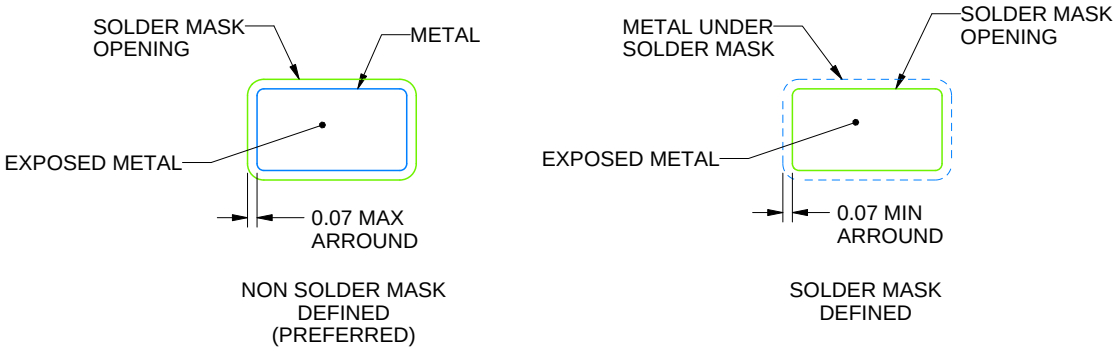
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

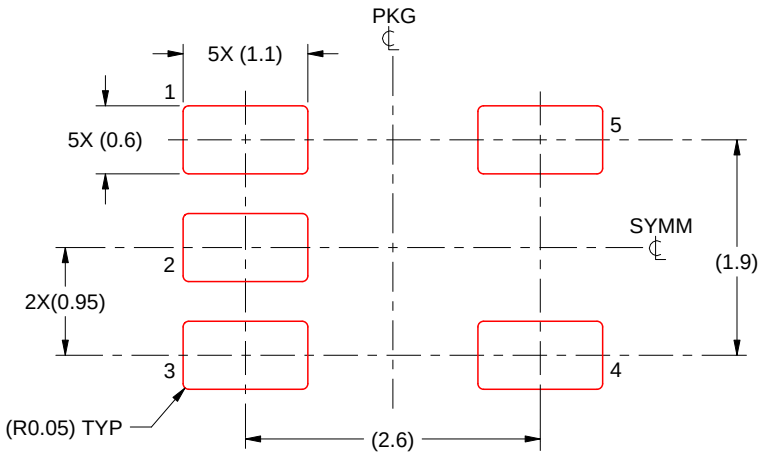


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

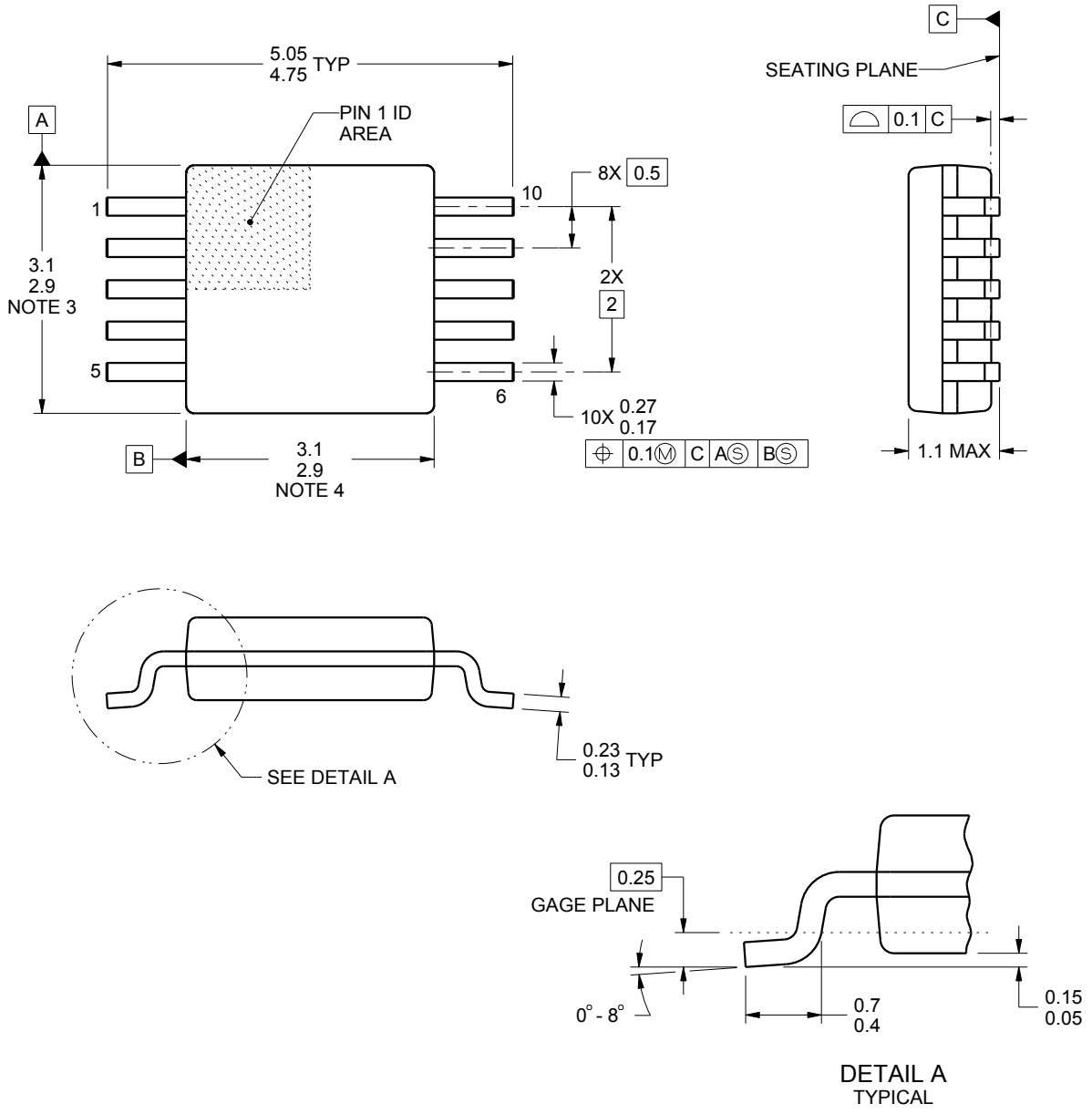
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

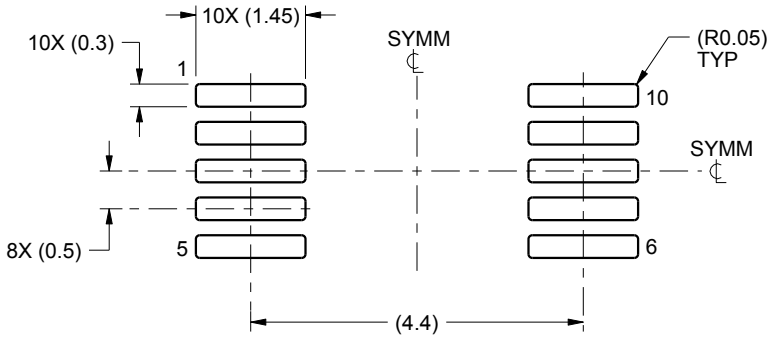
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

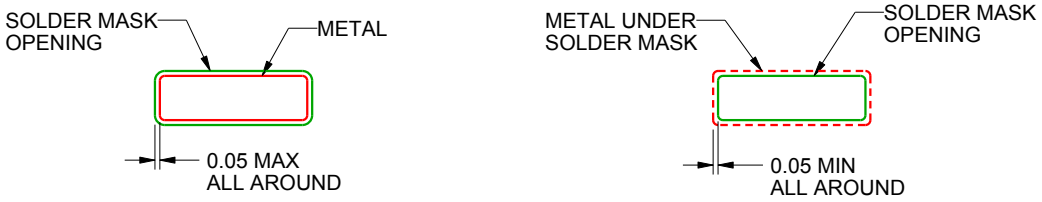


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

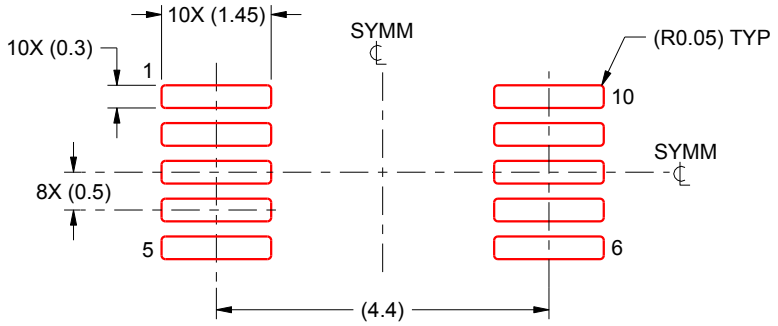


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



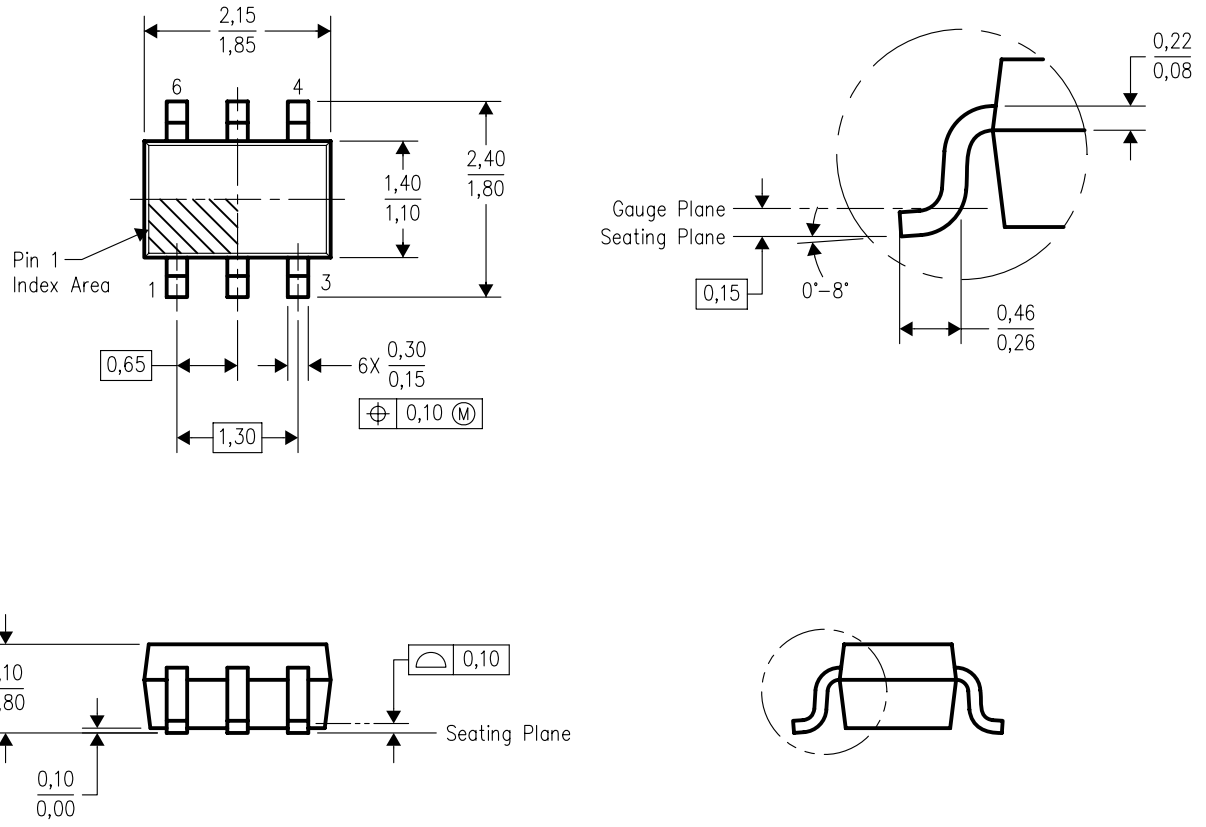
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

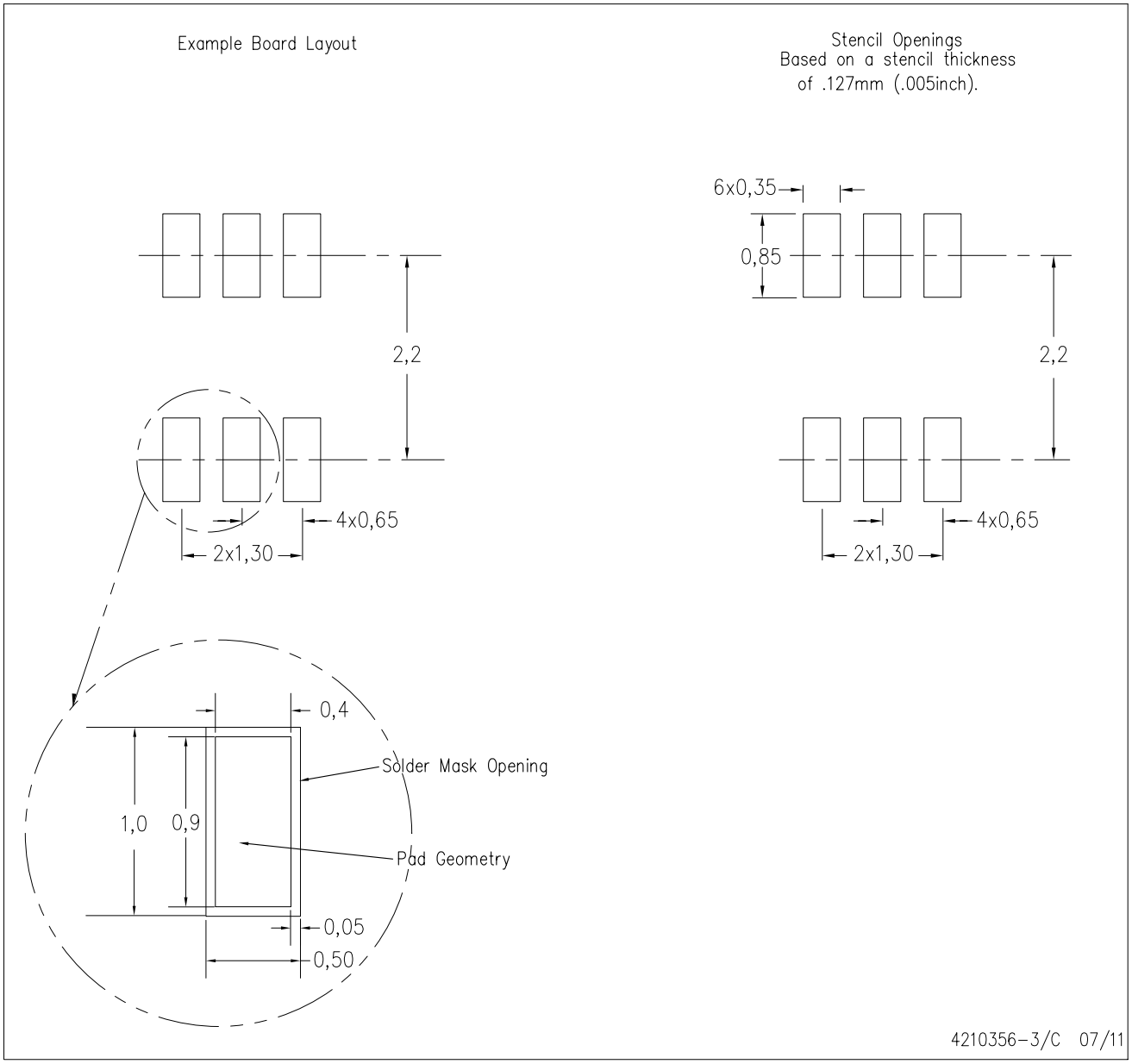
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

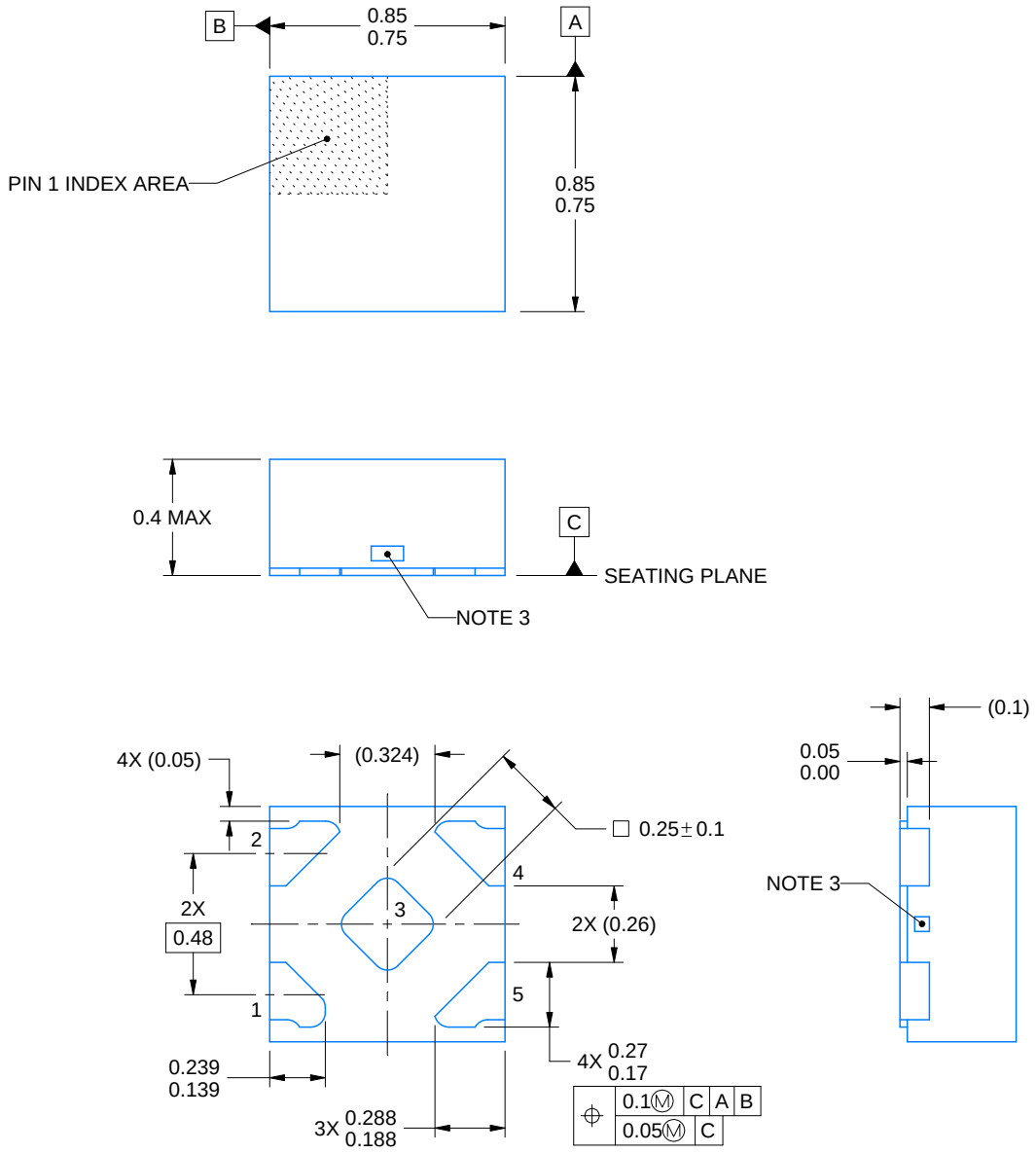
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

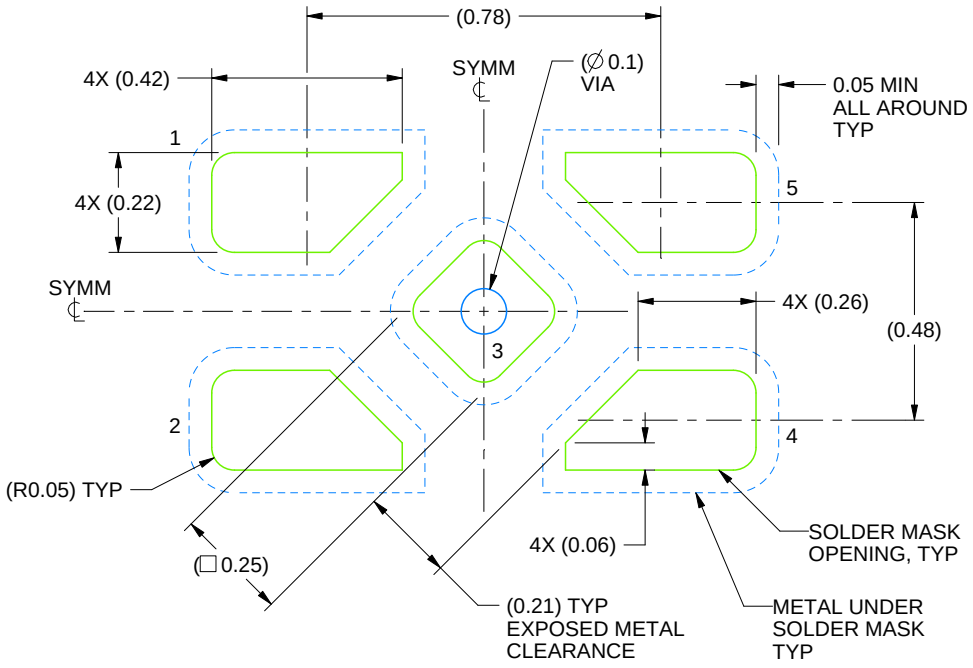
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

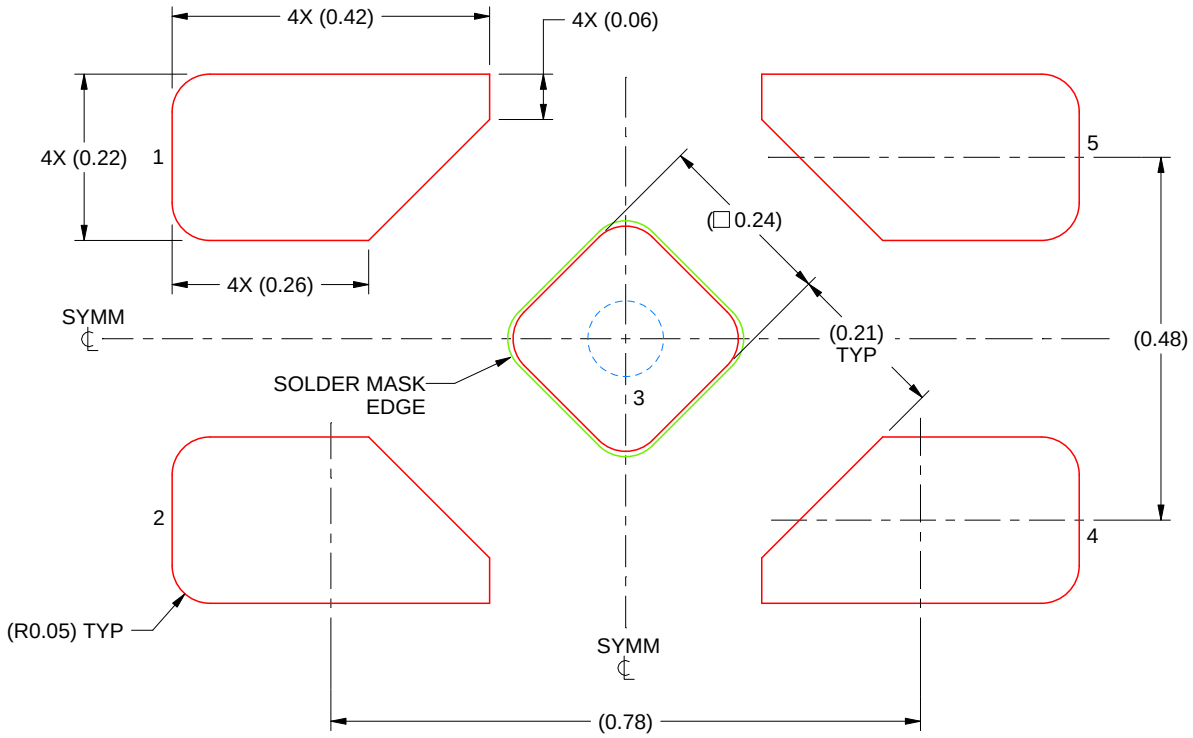
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

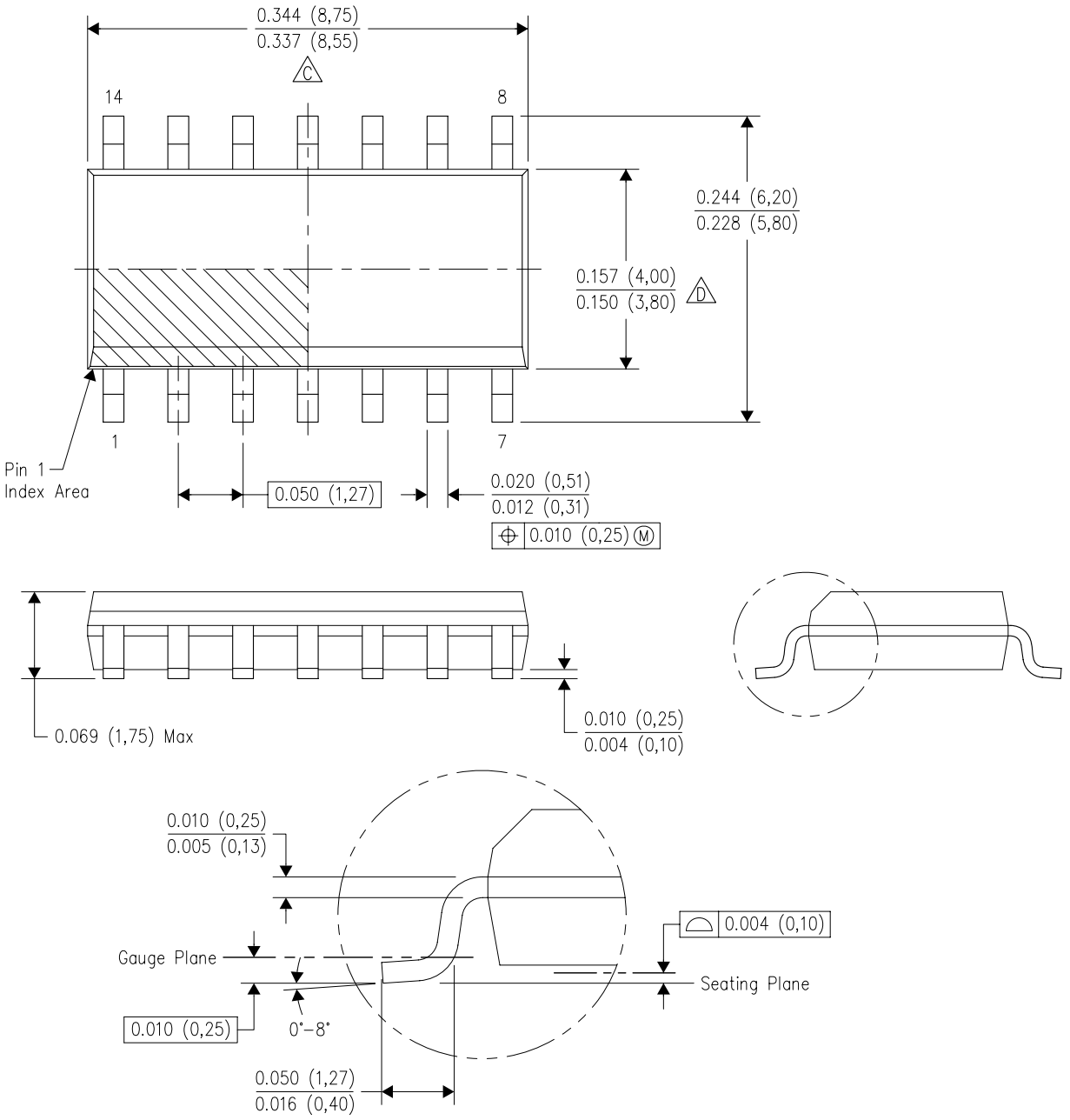
EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

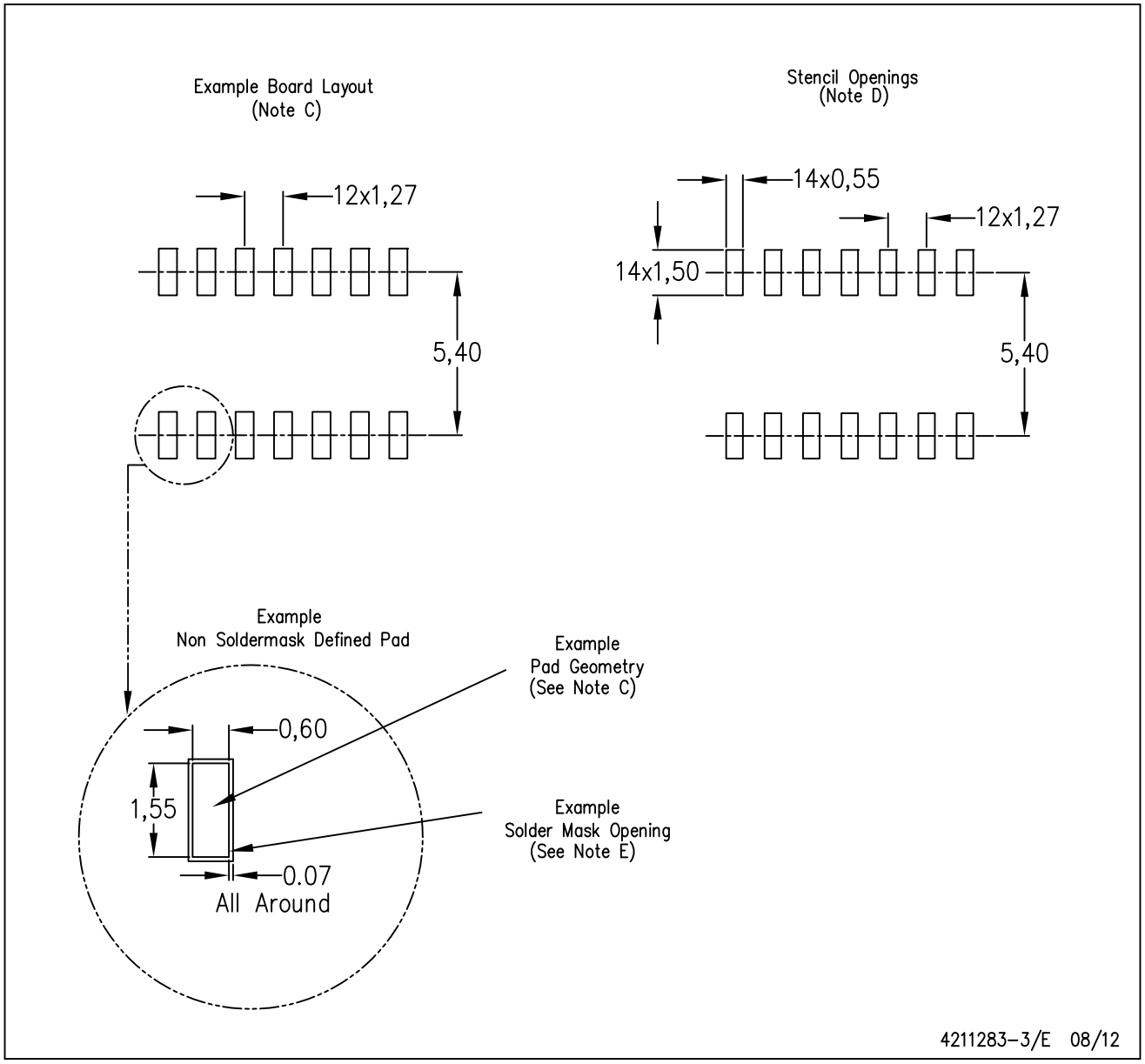
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

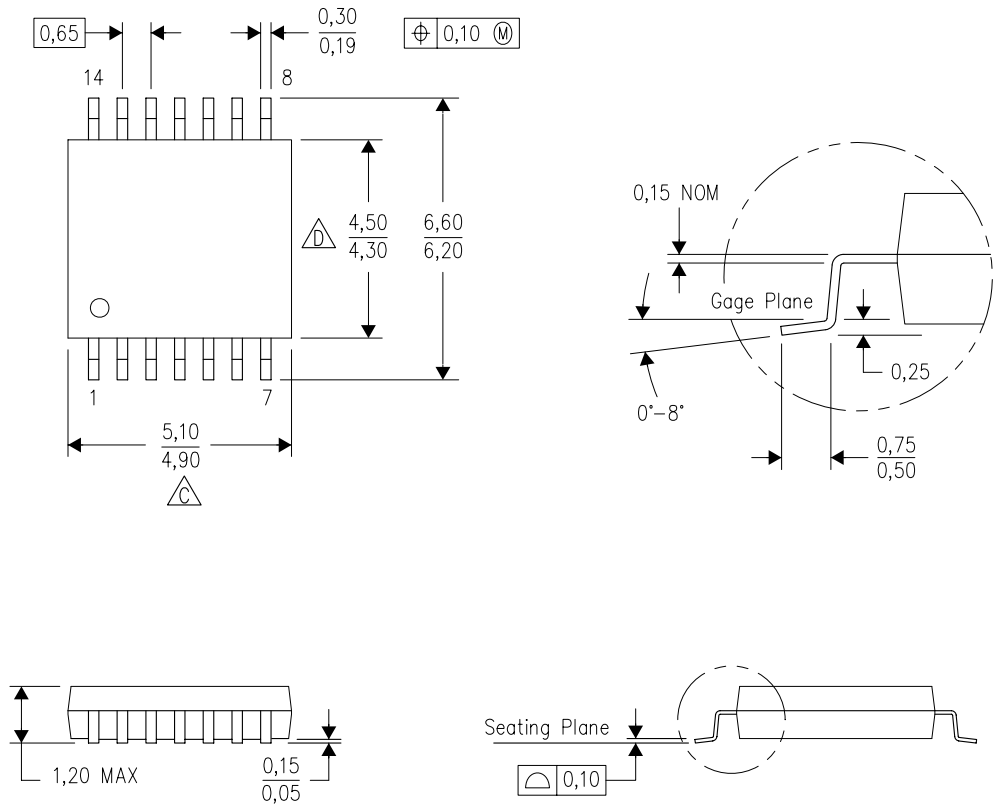
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

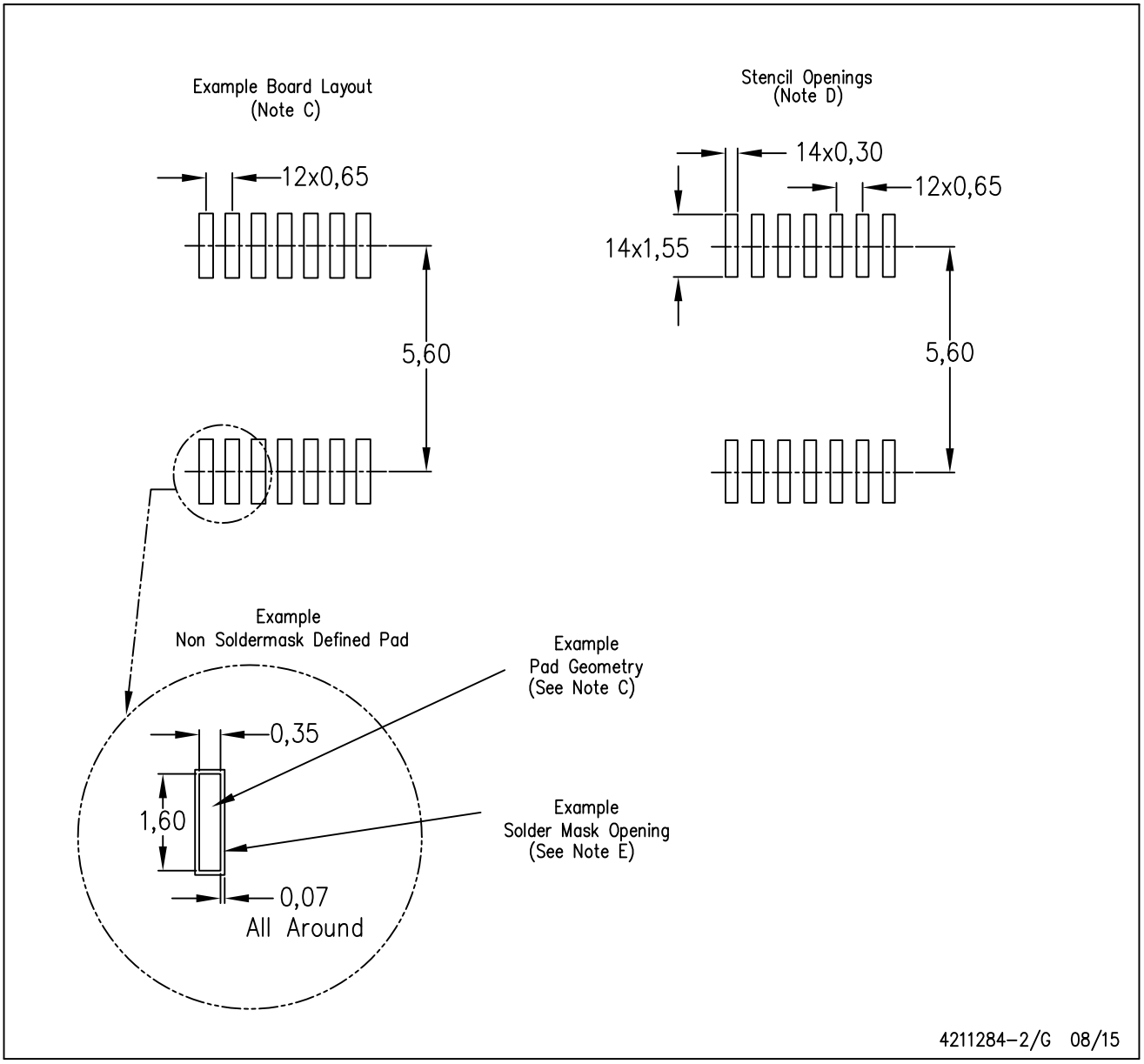
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

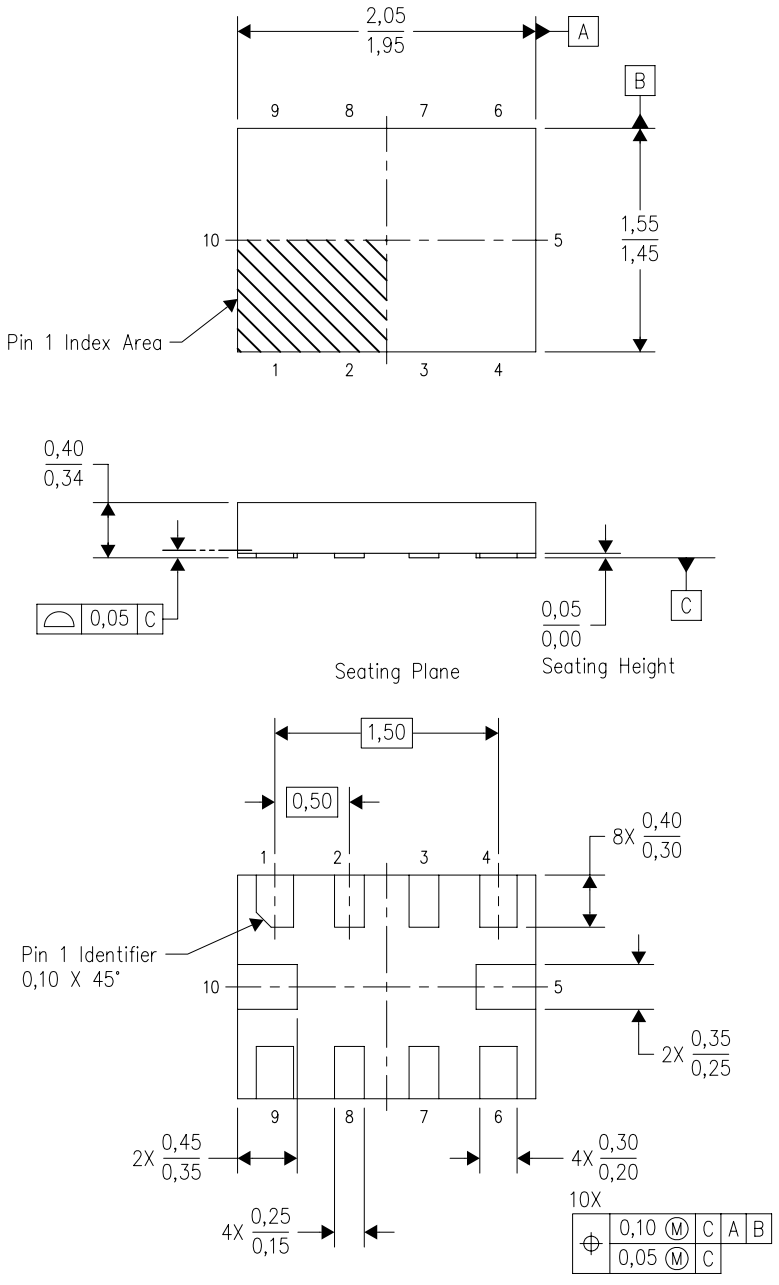
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

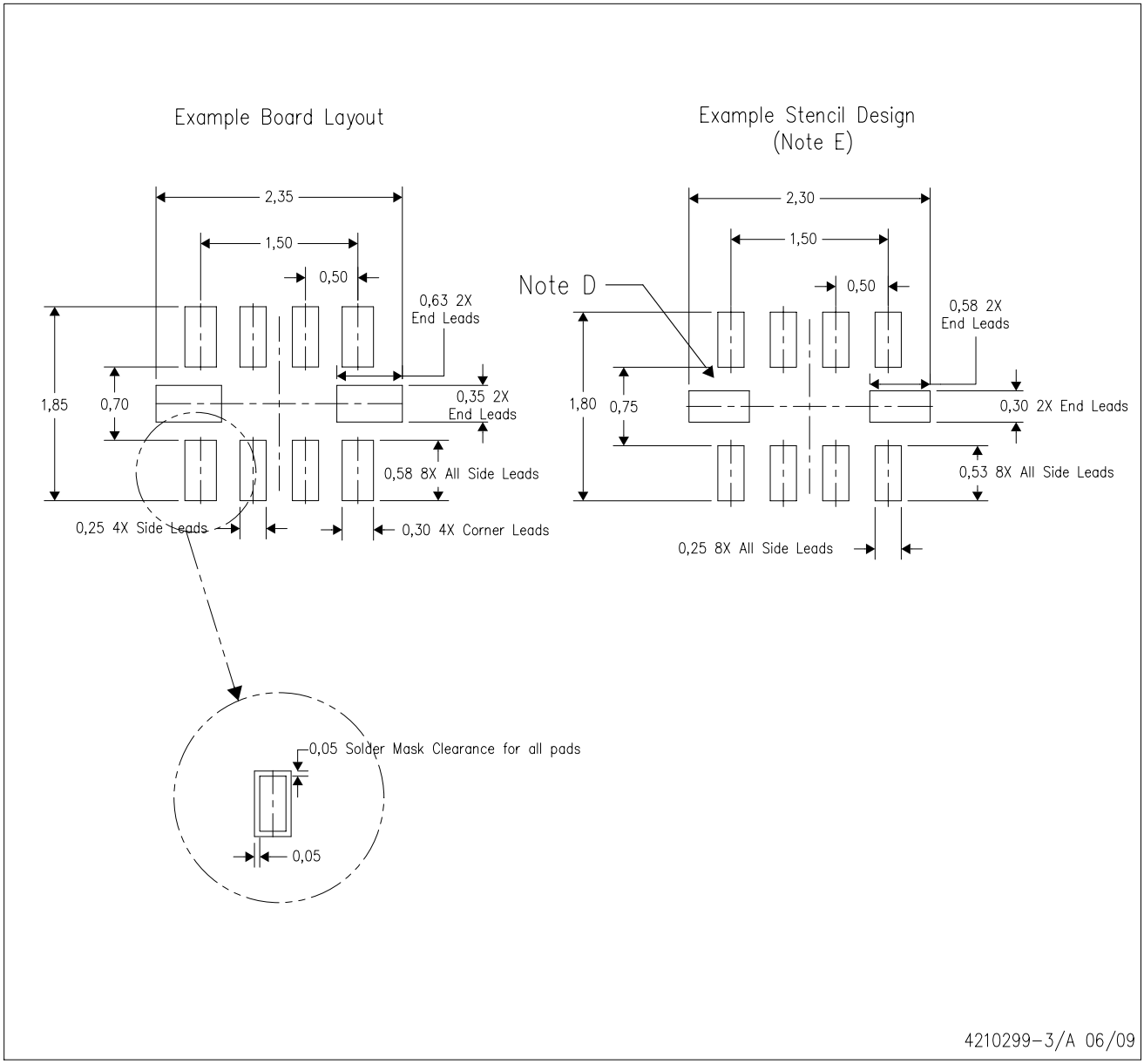
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



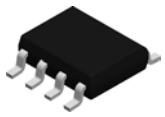
4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

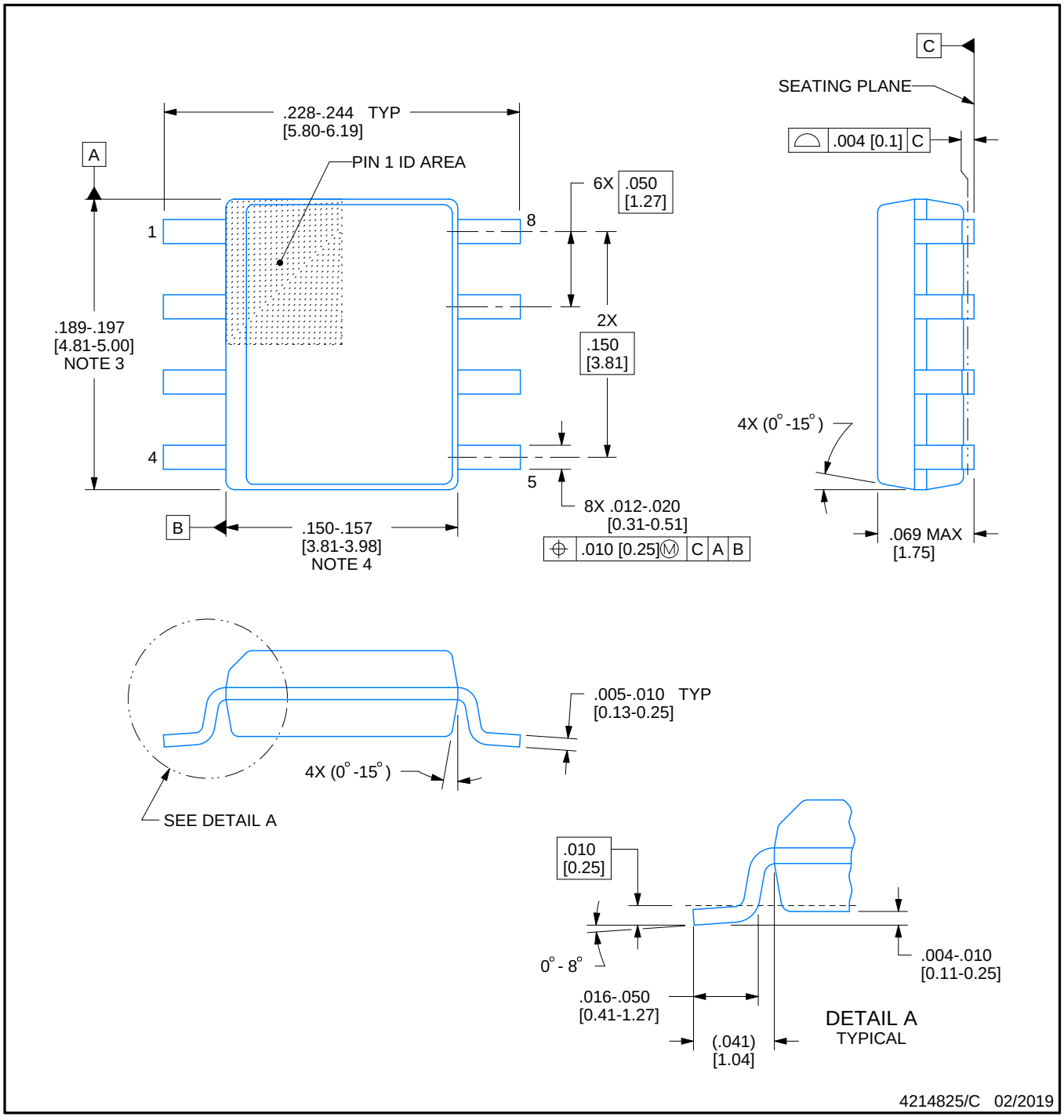


PACKAGE OUTLINE

D0008A

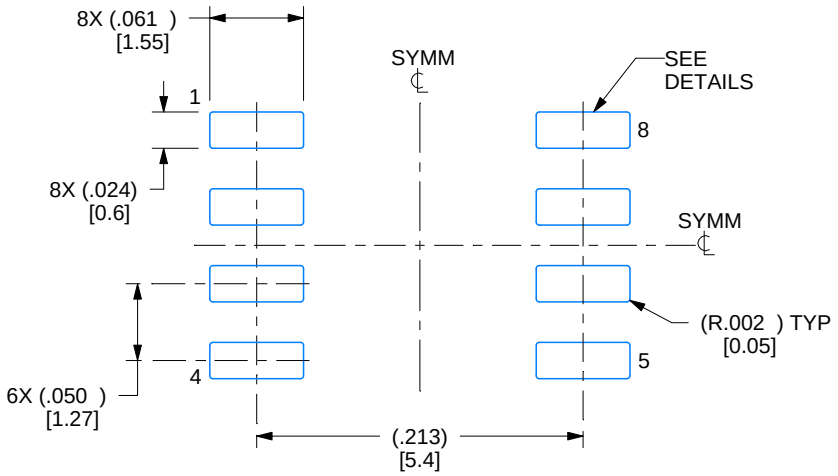
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

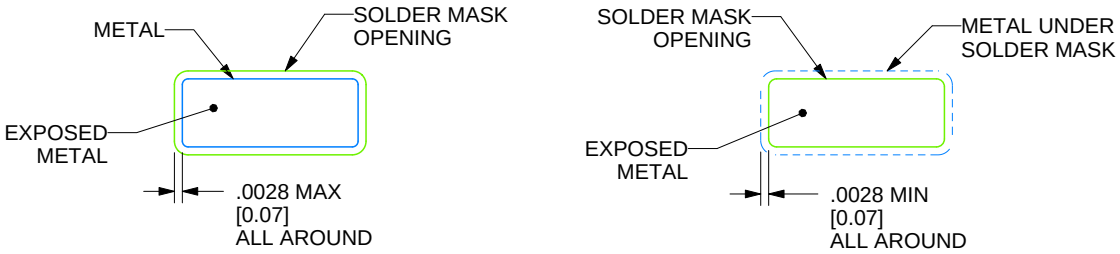


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

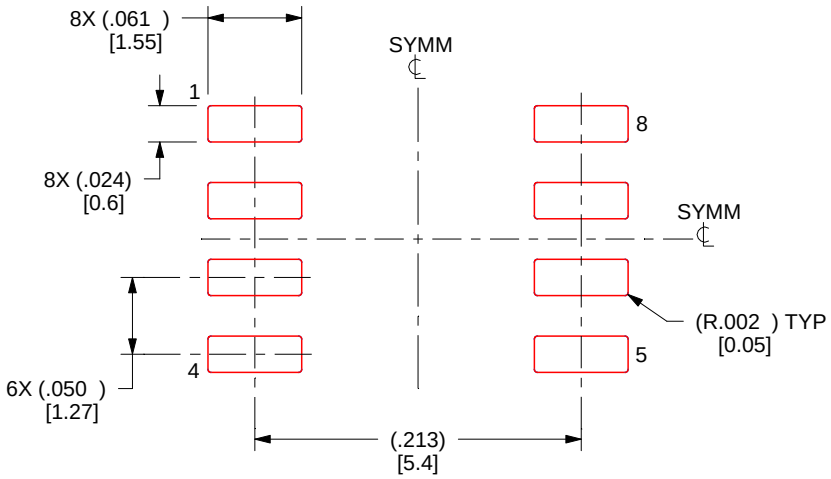
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

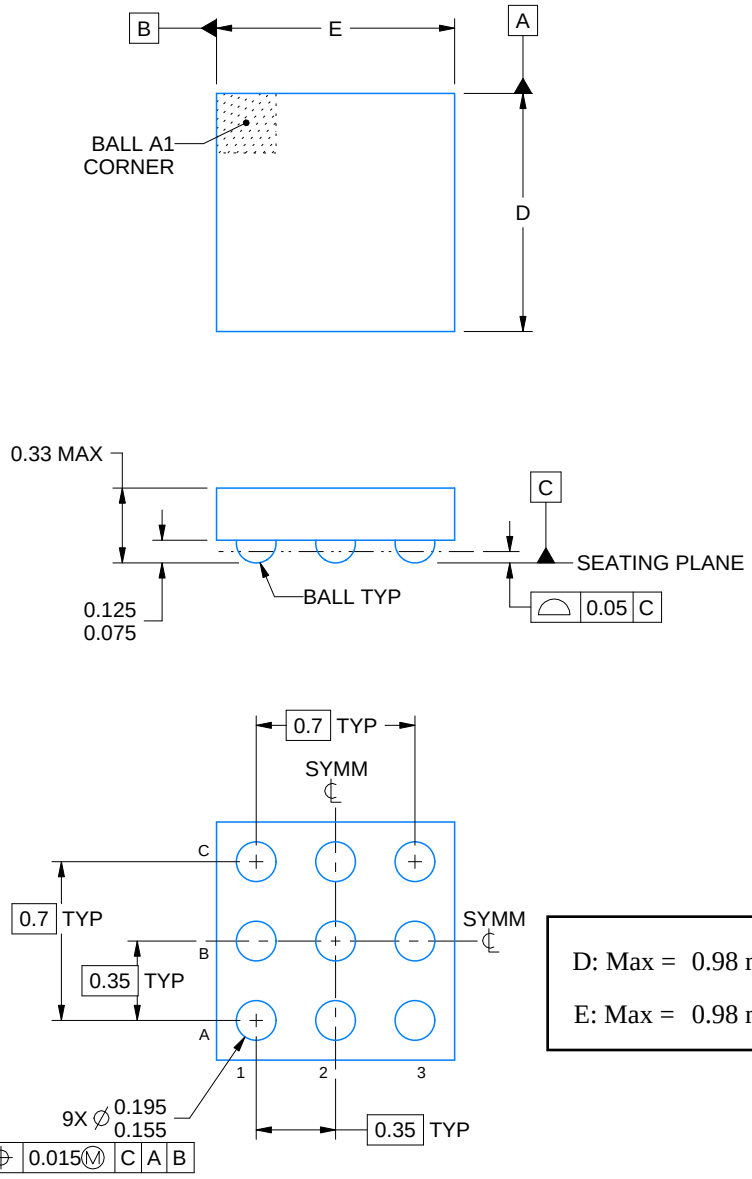
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

YCK0009

PACKAGE OUTLINE

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.98 mm, Min = 0.92 mm

E: Max = 0.98 mm, Min = 0.92 mm

4225837/A 04/2020

NOTES:

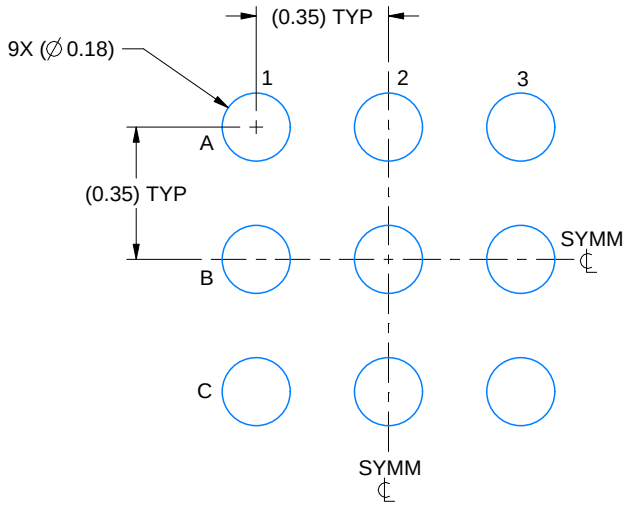
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

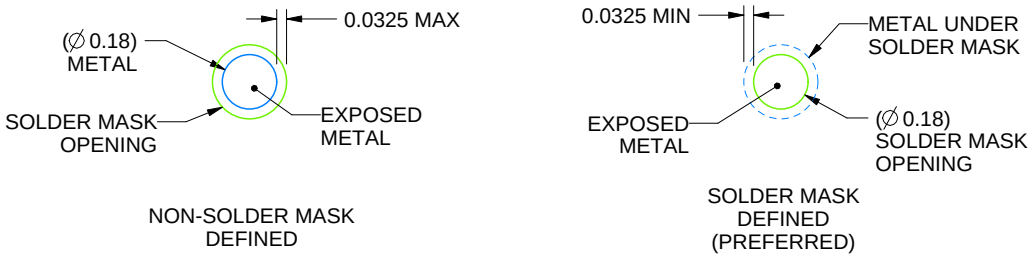
YCK0009

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4225837/A 04/2020

NOTES: (continued)

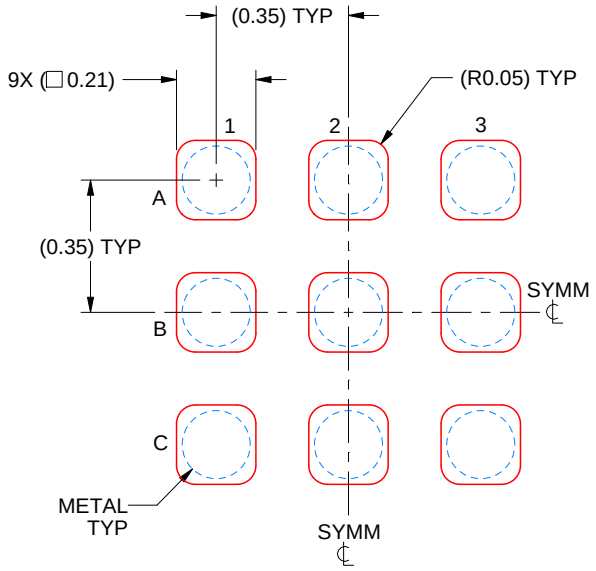
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCK0009

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4225837/A 04/2020

NOTES: (continued)

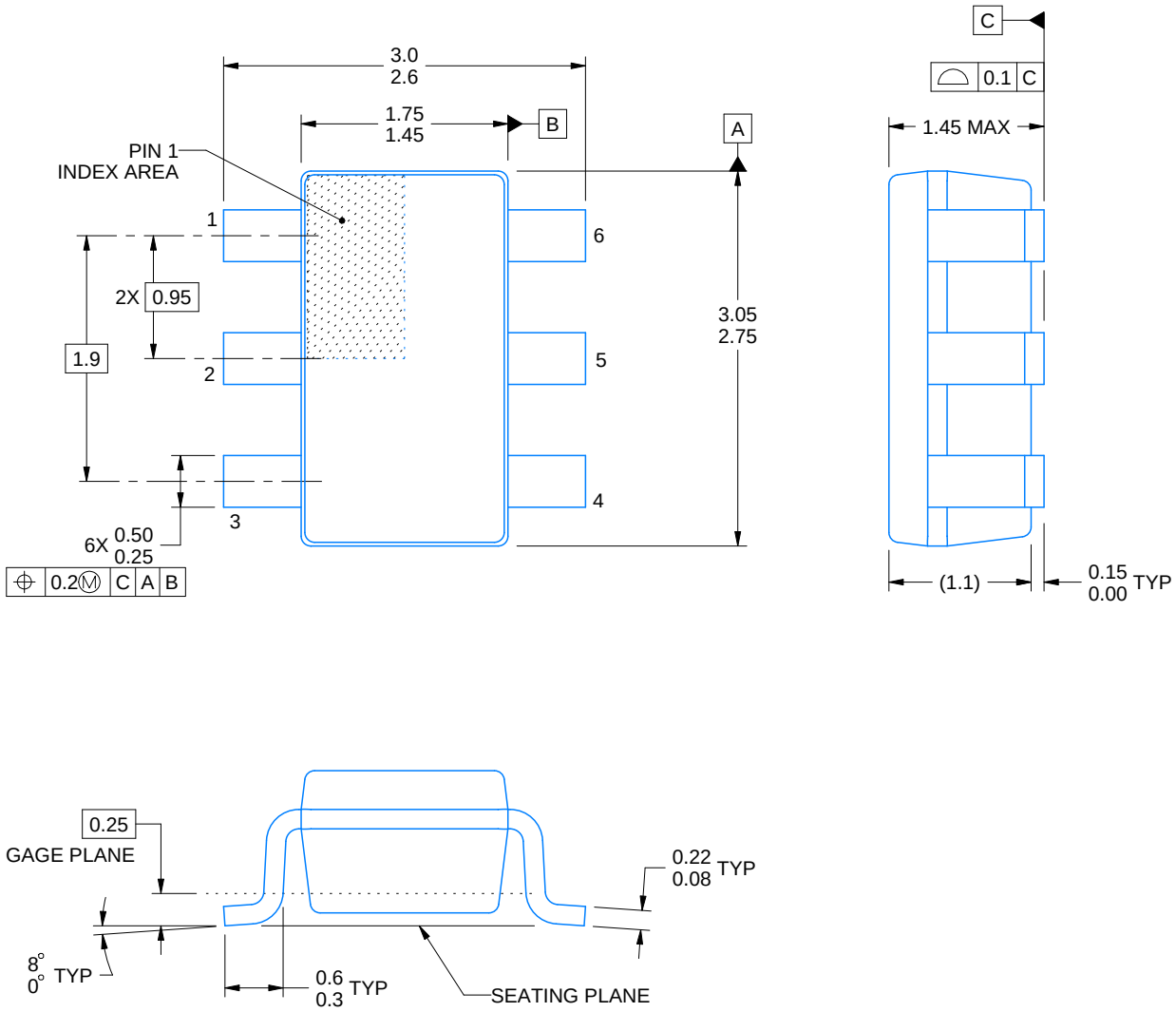
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

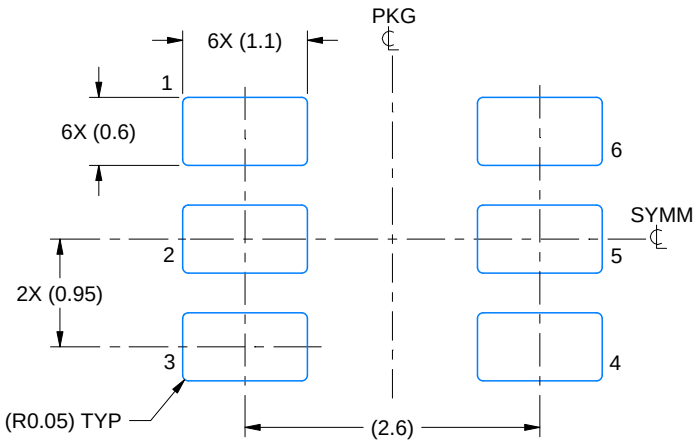
SMALL OUTLINE TRANSISTOR



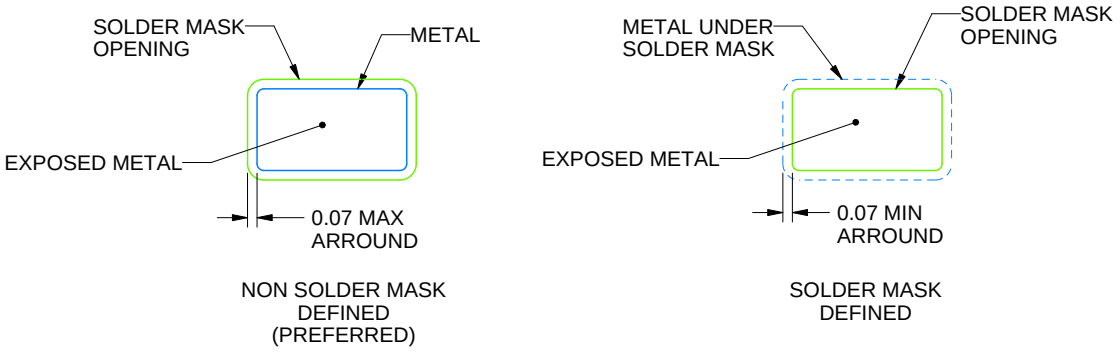
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

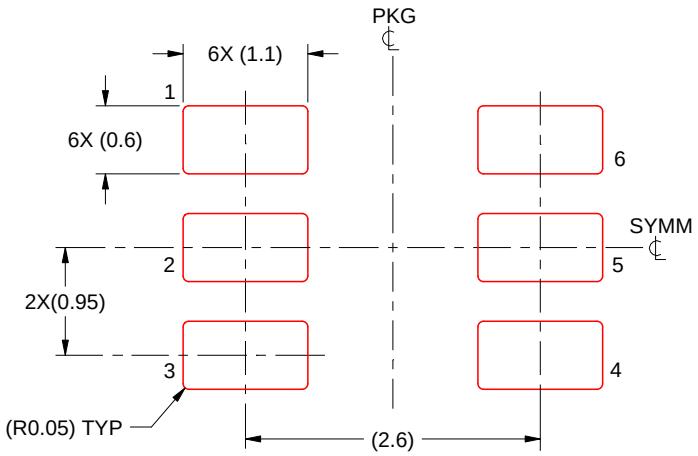


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



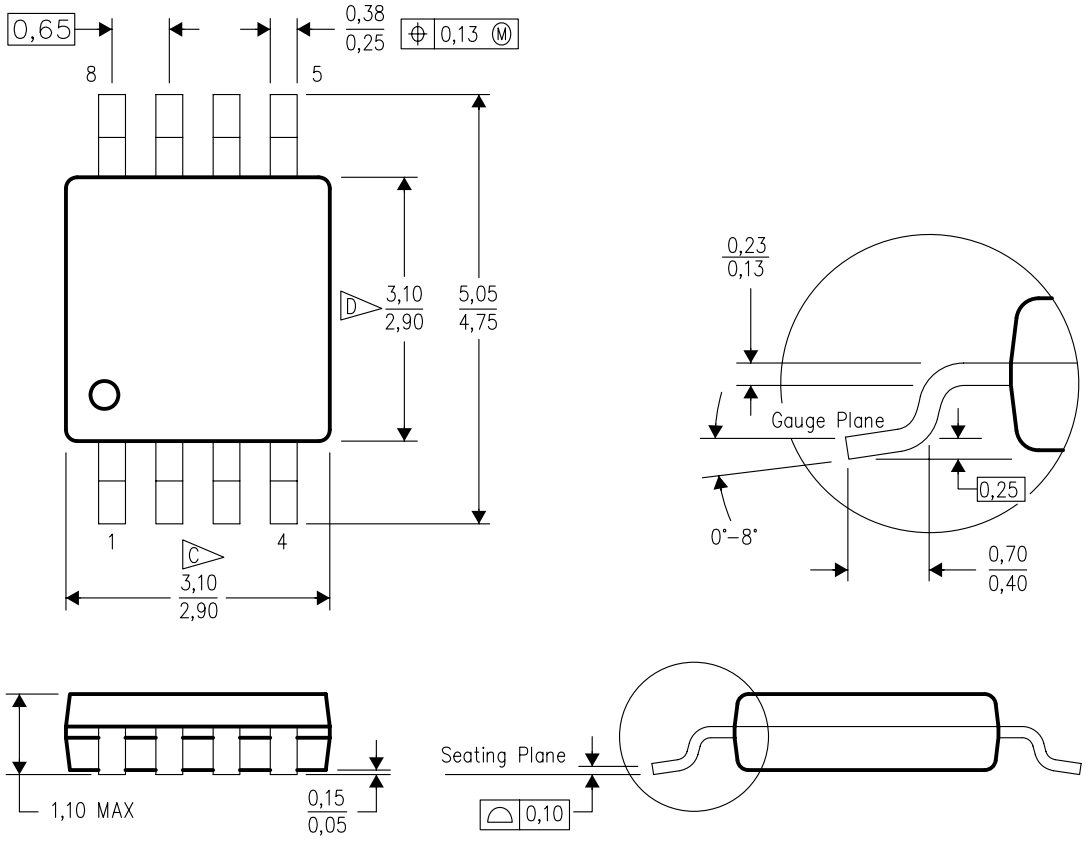
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

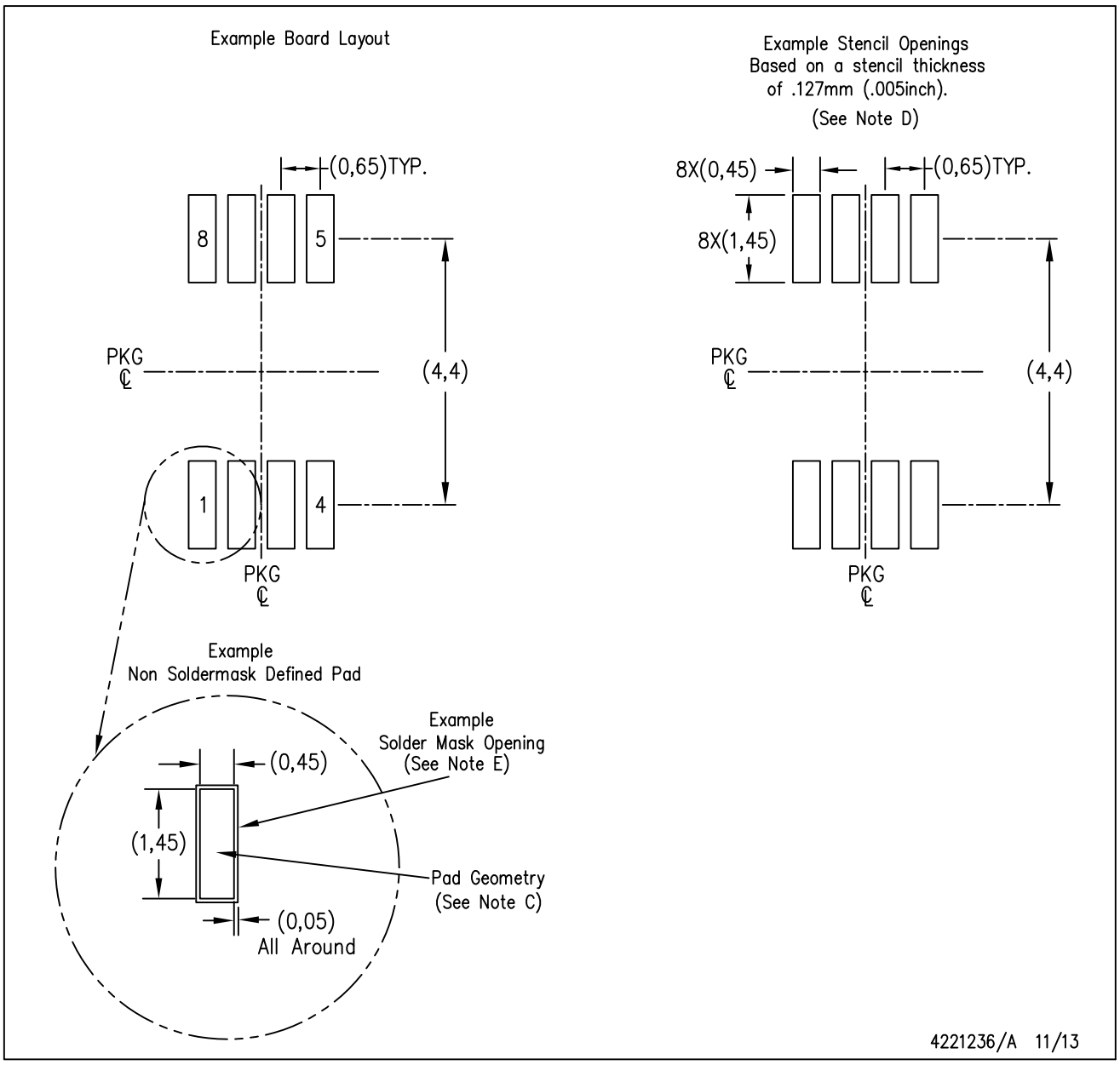
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

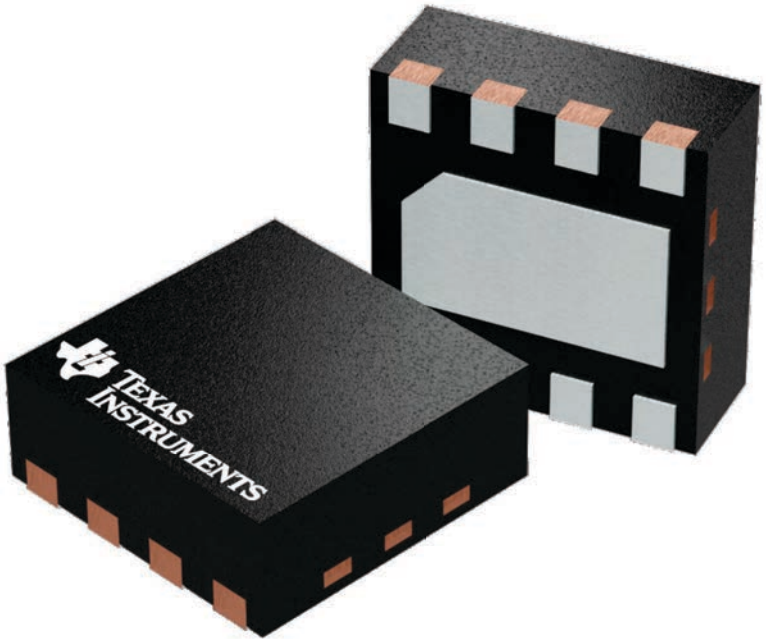
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



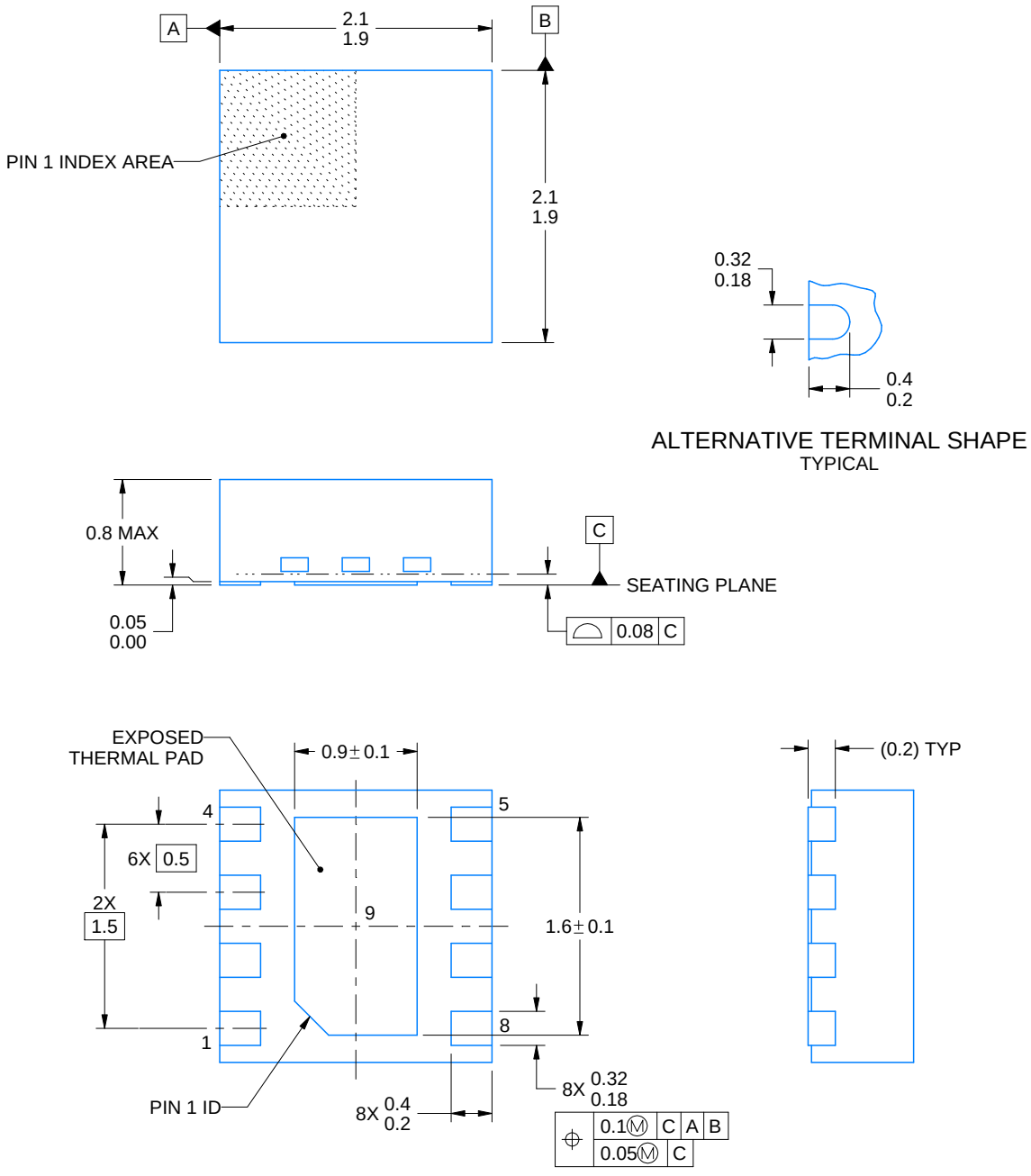
4224783/A

PACKAGE OUTLINE

DSG0008A

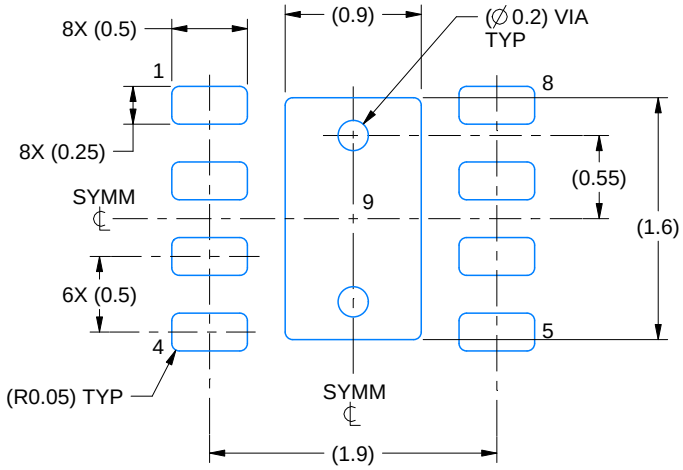
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

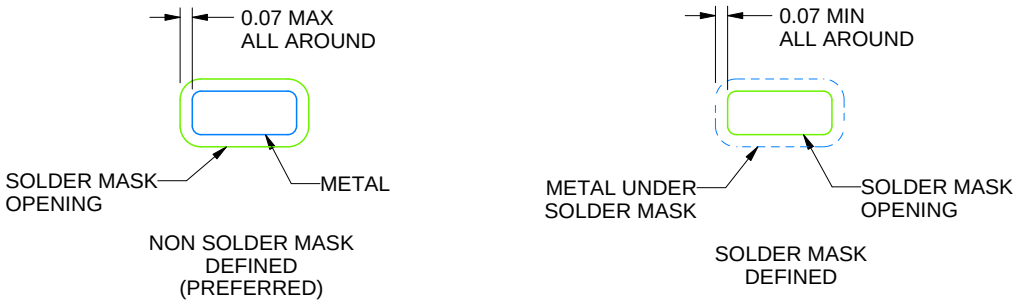


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

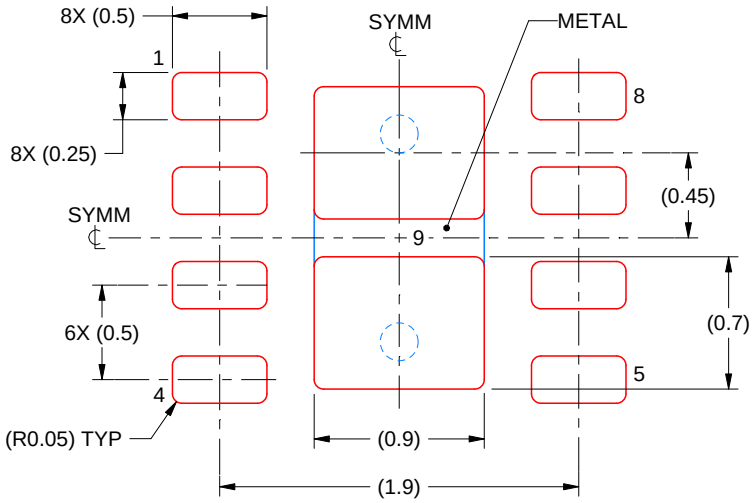
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

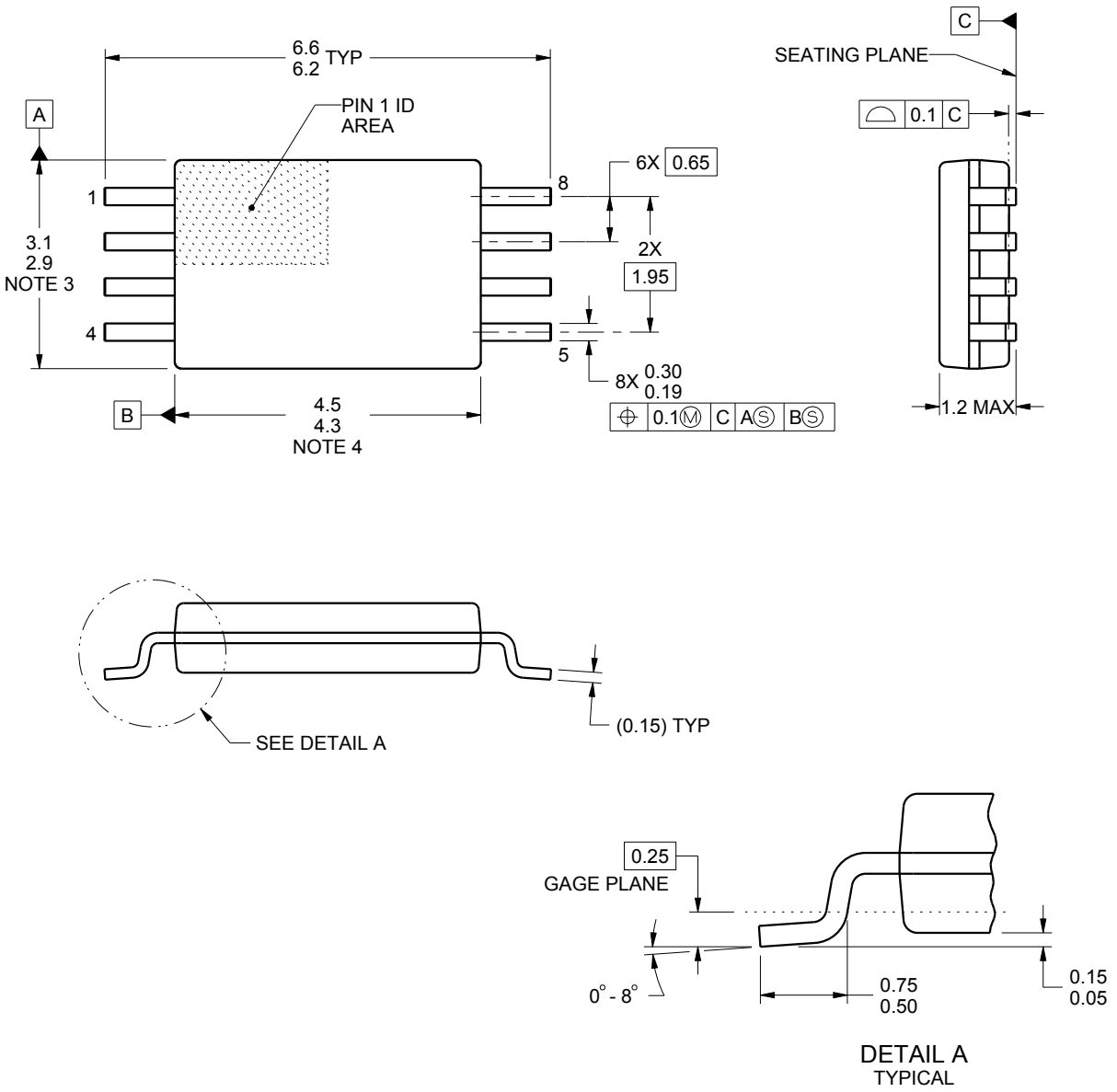
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

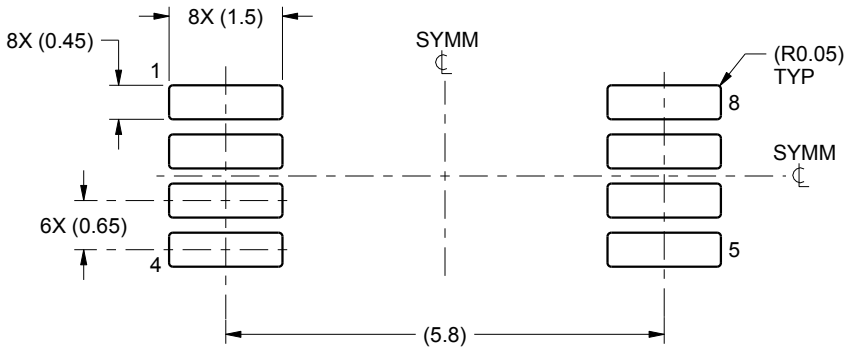
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

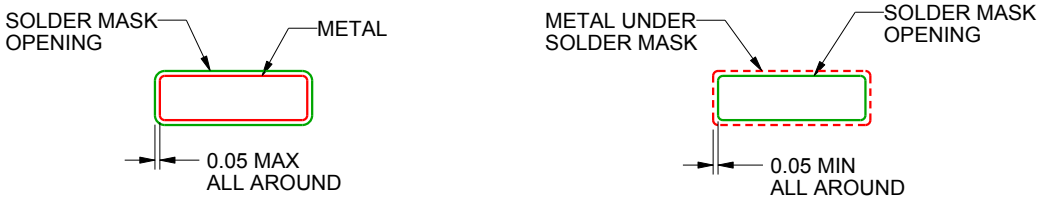


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

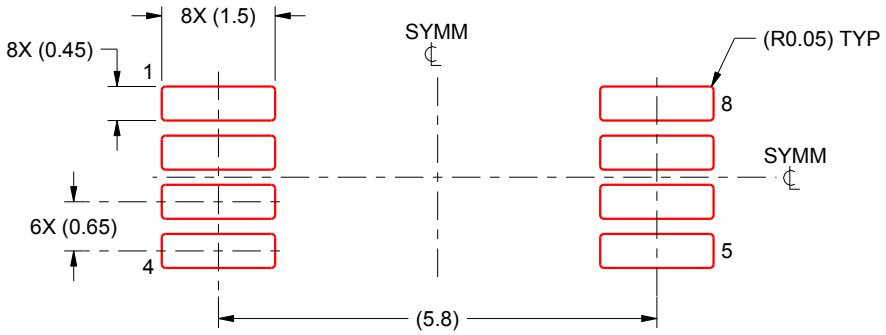


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

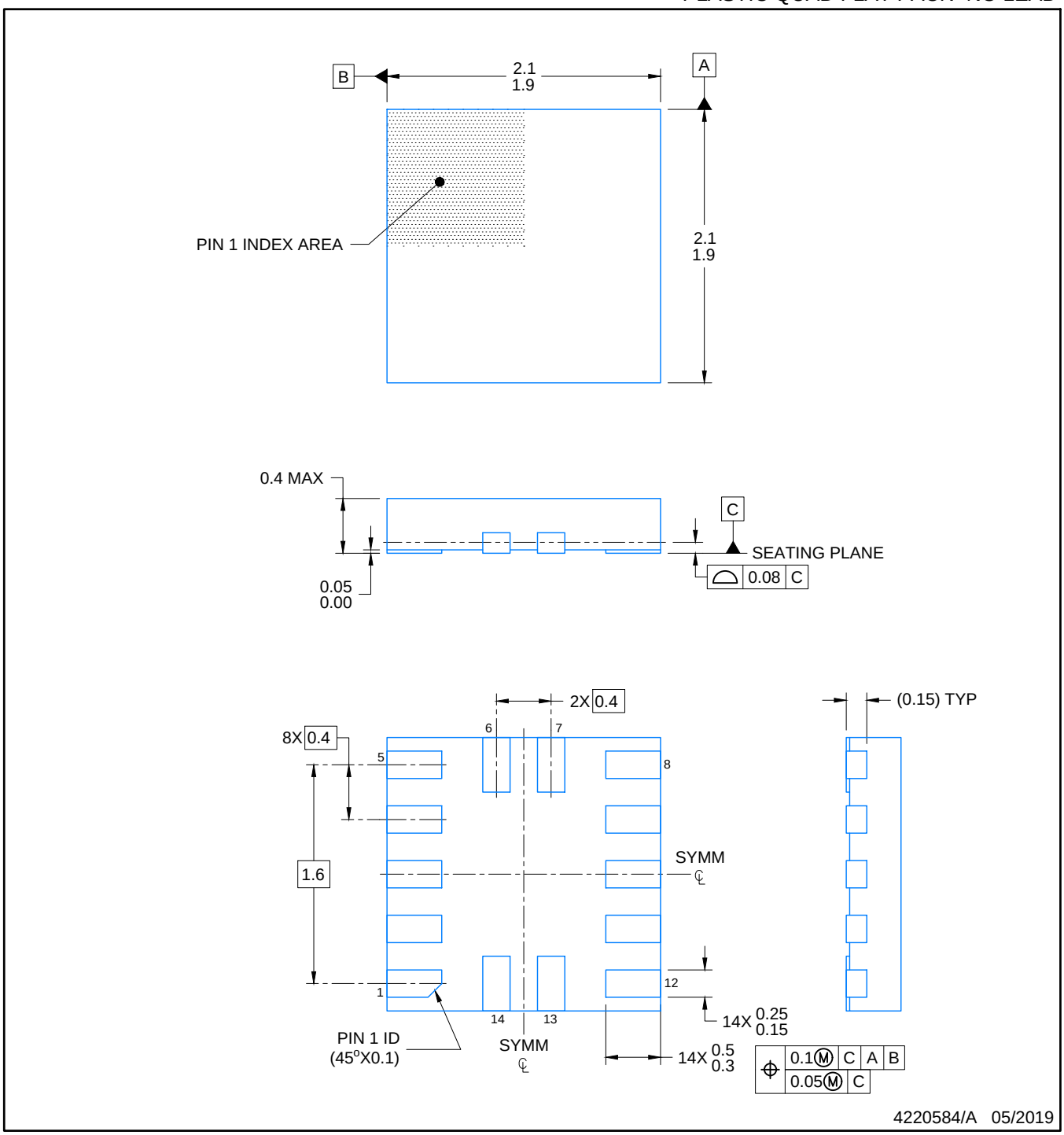
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RUC0014A

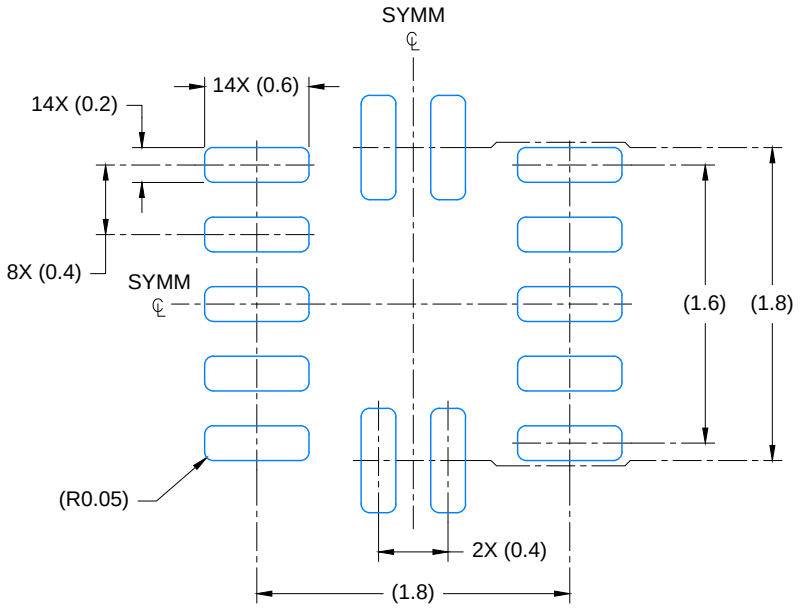
X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

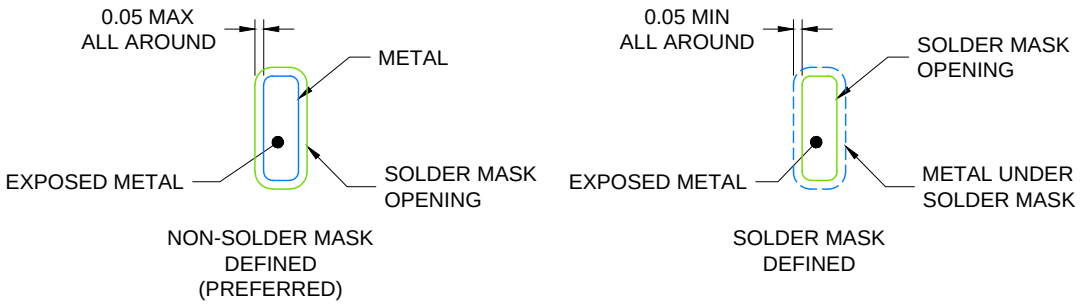


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

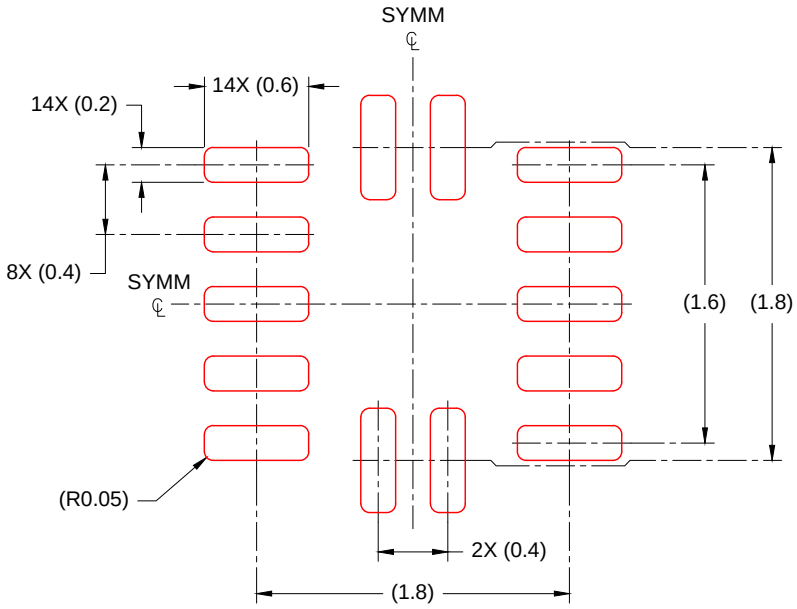


SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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