LMV331 单路、LMV393 双路、LMV339 四路通用低电压比较器

1 特性

- 2.7V 和 5V 性能
- 低电源电流
  - LMV331 130 μA（典型值）
  - LMV393 210 μA（典型值）
  - LMV339 410 μA（典型值）
- 输入共模电压范围包括接地
- 低输出饱和电压：200mV（典型值）
- 集电极开路输出可实现更大的灵活性

2 应用

- 迟滞比较器
- 振荡器
- 窗口比较器
- 工业设备
- 测试和测量

3 说明

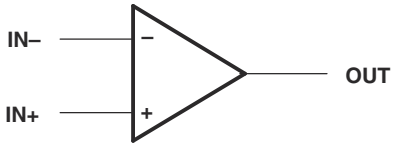
LMV393 和 LMV339 器件分别是双路和四路比较器的低电压（2.7V 至 5.5V）版本，它们的工作电压范围为 5V 至 30V。LMV331 是单路比较器。

LMV331、LMV339 和 LMV393 是颇具成本效益的解决方案，适用于在便携式消费类电子产品的电路设计中要求低电压运行、低功耗和节省空间的应用。无需消耗全部的电源电流，这类器件便可达到或超出常见 LM339 和 LM393 器件的规格。

器件信息

器件型号	封装（引脚）(1)	封装尺寸（标称值）
LMV339	SOIC (14)	8.65mm x 3.90mm
LMV393	SOIC (8)	4.90mm x 3.90mm
LMV331	SC70 (5)	2.00mm x 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision T (January 2015) to Revision U (October 2020)	Page
• 更新了整个文档的表、图和交叉参考的编号格式。	1

Changes from Revision S (October 2012) to Revision T (January 2015)	Page
• 添加了*应用*、*器件信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*典型特性*、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• 删除了*订购信息* 表	1

Changes from Revision R (May 2012) to Revision S (October 2012)	Page
• Updated operating temperature range	4

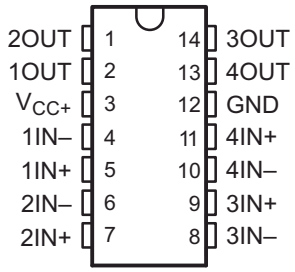
Changes from Revision N (April 2011) to Revision O (February 2012)	Page
• Changed V_I in the *Absolute Maximum Ratings* from 5.5 V to V_{CC+}	4

Changes from Revision M (November 2005) to Revision N (April 2011)	Page
• 将文档格式从 Quicksilver 变更为 DocZone	1
• Added RUC package pin out drawing	3

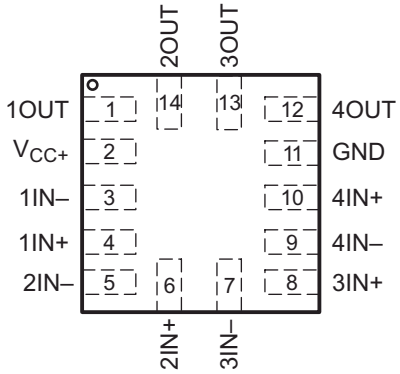
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5 Pin Configuration and Functions

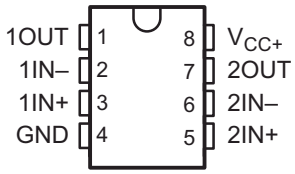
LMV339 . . . D OR PW PACKAGE
(TOP VIEW)



LMV339 . . . RUC PACKAGE
(TOP VIEW)



LMV393 . . . D, DDU, DGK OR PW PACKAGE
(TOP VIEW)



LMV331 . . . DBV OR DCK PACKAGE
(TOP VIEW)

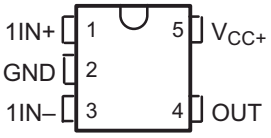


表 5-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	LMV331	LMV393	LMV339			
	DBV or DCK	D, DDU, DGK or PW	D or PW	RUC		
1IN – , 2IN – , 3IN – , 4IN –	3	2, 6	4, 6, 8, 10	3, 5, 7, 9	I	Comparator(s) negative input pin(s)
1IN+ , 2IN+, 3IN+, 4IN+	1	3, 5	5, 7, 9, 11	4, 6, 8, 10	I	Comparator(s) positive input pin(s)
GND	2	4	12	11	I	Ground
1OUT, 2OUT, 3OUT, 4OUT	4	1, 7	2, 1, 14, 13	1, 14, 13, 12	O	Comparator(s) output pin(s)
V_{CC+}	5	8	3	2	I	Supply Pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			5.5	V
V_{ID}	Differential input voltage(3)			±5.5	V
V_I	Input voltage range (either input)		0	V_{CC+}	V
	Duration of output short circuit (one amplifier) to ground(4)	At or below T_A = 25°C, V_{CC} ≤ 5.5 V	Unlimited		
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.

(3) Differential voltages are at IN+ with respect to IN –.

(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)	2.7	5.5	V
V_{OUT}	Output voltage		V_{CC+} + 0.3	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMV339			LMV393				LMV331		UNIT
		D	PW	RUC	D	DDU	DGK	PW	DBV	DCK	
		14 PINS			8 PINS				5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	113	216	97	210	172	149	206	252	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	51.3	—	—	—	—	—	—	
$R_{\theta JB}$	Junction-to-board thermal resistance	—	—	59.0	—	—	—	—	—	—	
ψ_{JT}	Junction-to-top characterization parameter	—	—	1.2	—	—	—	—	—	—	
ψ_{JB}	Junction-to-board characterization parameter	—	—	59.0	—	—	—	—	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics, V_{CC+} = 2.7 V

V_{CC+} = 2.7 V, GND = 0 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1.7	7	mV
α_{VIO}	Average temperature coefficient of input offset voltage		–40°C to 125°C		5		µV/°C
I_{IB}	Input bias current		25°C		15	250	nA
			–40°C to 125°C			400	
I_{IO}	Input offset current		25°C		5	50	nA
			–40°C to 125°C			150	
I_O	Output current (sinking)	$V_O \leqslant$ 1.5 V	25°C	5	23		mA
	Output Leakage Current		25°C		0.003		µA
			–40°C to 125°C			1	
V_{ICR}	Common-mode input voltage range		25°C		–0.1 to 2		V
V_{SAT}	Saturation voltage	$I_O \leqslant$ 1.5 mA	25°C		200		mV
I_{CC}	Supply current	LMV331	25°C		40	100	µA
		LMV393 (both comparators)	25°C		70	140	
		LMV339 (all four comparators)	25°C		140	200	

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6.6 Electrical Characteristics, V_{CC+} = 5 V

V_{CC+} = 5 V, GND = 0 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1.7	7	mV
			–40°C to 125°C			9	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C		5		µV/°C
I_{IB}	Input bias current		25°C		25	250	nA
			–40°C to 125°C			400	
I_{IO}	Input offset current		25°C		2	50	nA
			–40°C to 125°C			150	
I_O	Output current (sinking)	$V_O \leq$ 1.5 V	25°C	10	84		mA
	Output Leakage Current		25°C		0.003		µA
			–40°C to 125°C			1	
V_{ICR}	Common-mode input voltage range		25°C		–0.1 to 4.2		V
A_{VD}	Large-signal differential voltage gain		25°C	20	50		V/mV
V_{SAT}	Saturation voltage	$I_O \leq$ 4 mA	25°C		200	400	mV
			–40°C to 125°C			700	
I_{CC}	Supply current	LMV331	25°C		60	120	µA
			–40°C to 125°C			150	
		LMV393 (both comparators)	25°C		100	200	
			–40°C to 125°C			250	
		LMV339 (all four comparators)	25°C		170	300	
			–40°C to 125°C			350	

6.7 Switching Characteristics, V_{CC+} = 2.7 V

T_A = 25°C, V_{CC+} = 2.7 V, R_L = 5.1 kΩ, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PHL}	Propagation delay high to low level output switching	Input overdrive = 10 mV	1000	ns
		Input overdrive = 100 mV	350	
t_{PLH}	Propagation delay low to high level output switching	Input overdrive = 10 mV	500	ns
		Input overdrive = 100 mV	400	

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6.8 Switching Characteristics, V_{CC+} = 5 V

T_A = 25°C, V_{CC+} = 5 V, R_L = 5.1 kΩ, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PHL}	Propagation delay high to low level output switching	Input overdrive = 10 mV	600	ns
		Input overdrive = 100 mV	200	
t_{PLH}	Propagation delay low to high level output switching	Input overdrive = 10 mV	450	ns
		Input overdrive = 100 mV	300	

6.9 Typical Characteristics

Unless otherwise specified, VS = +5V, single supply, TA = 25°C

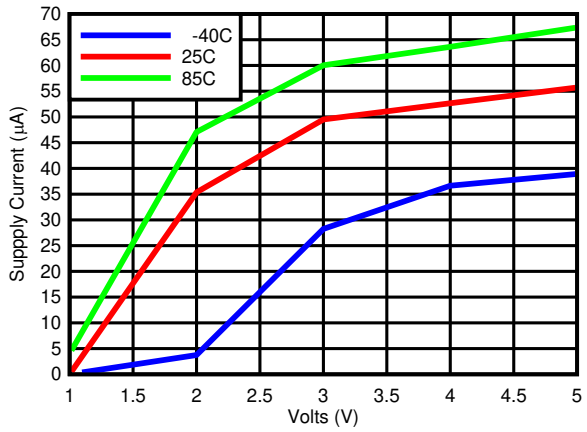


图 6-1. Supply Current vs Supply Voltage Output High (LMV33x)

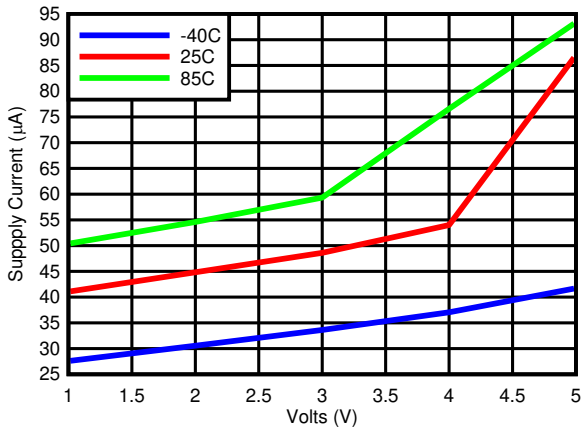


图 6-2. Supply Current vs Supply Voltage Output Low (LMV33x)

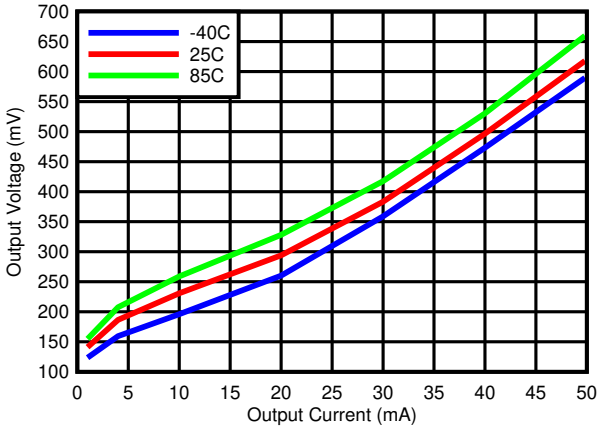


图 6-3. Output Voltage vs Output Current

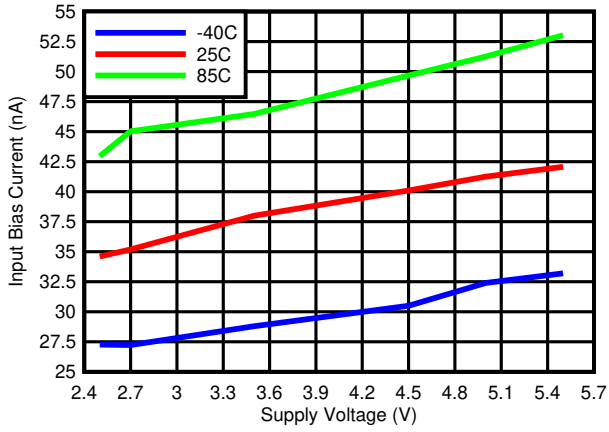


图 6-4. Input Bias Current vs Supply Voltage

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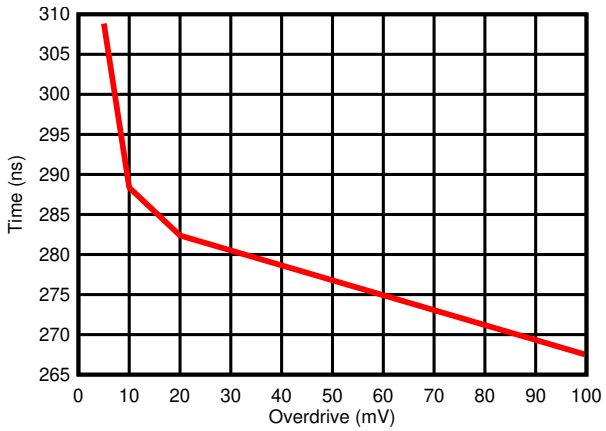


图 6-5. Response Time vs Input Overdrives Negative Transition (V_{CC}=5 V)

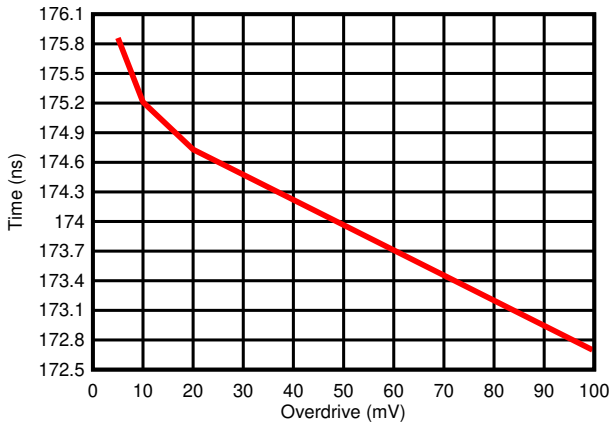


图 6-6. Response Time vs Input Overdrives Positive Transition (V_{CC} = 5 V)

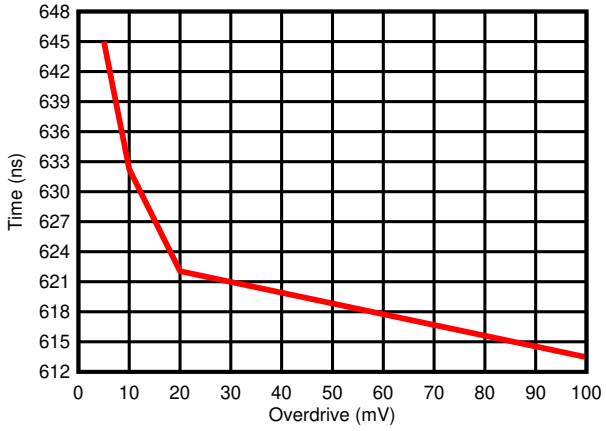


图 6-7. Response Time vs Input Overdrives Negative Transition (V_{CC} = 2.7 V)

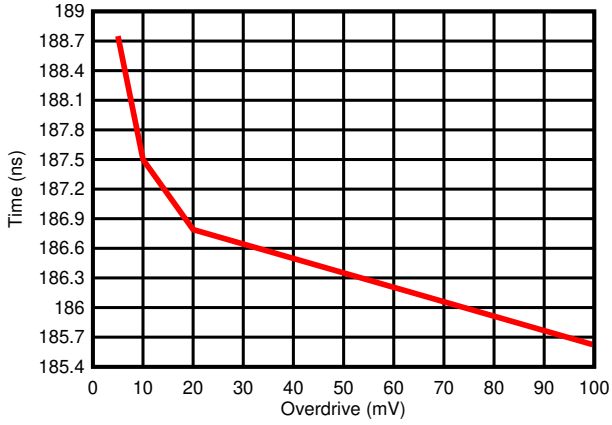


图 6-8. Response Time vs Input Overdrives Positive Transition (V_{CC} = 2.7 V)

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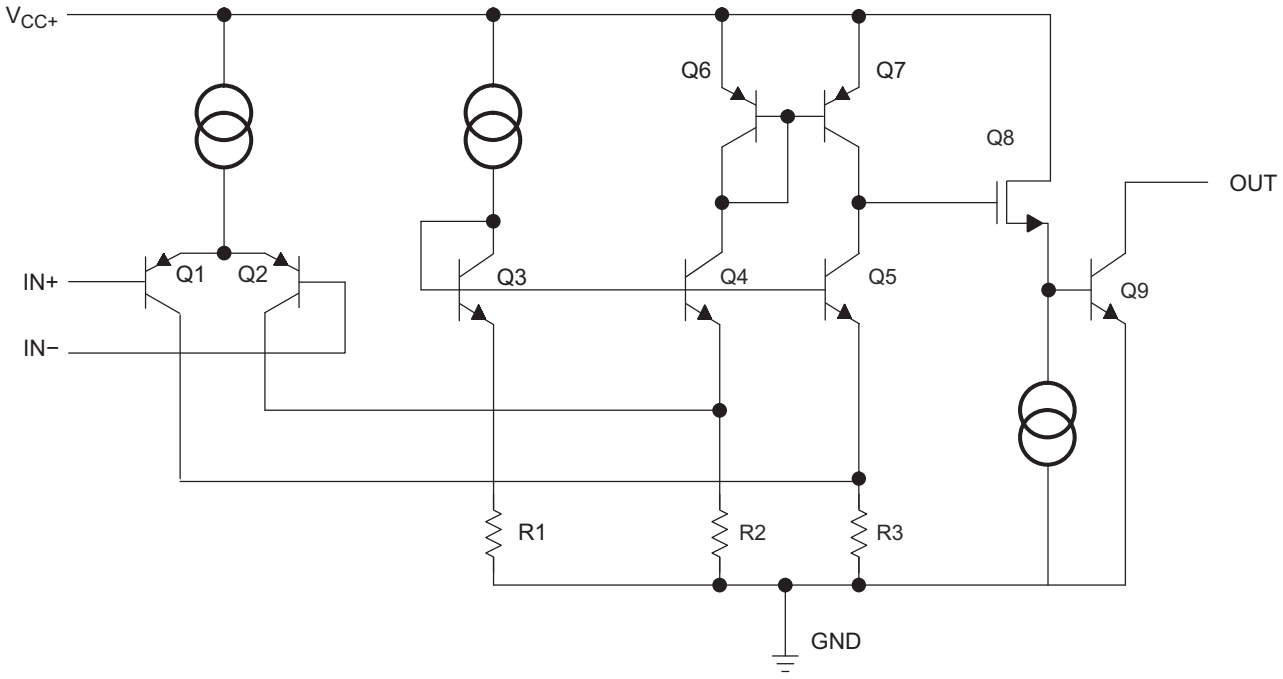
7 Detailed Description

7.1 Overview

The LMV331, LMV393 and LMV339 family of comparators have the ability to operate up to 5 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to it's low Iq and fast response.

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

7.2 Functional Block Diagram



7.3 Feature Description

The LMV331, LMV393 and LMV339 consists of a PNP input, whose Vbe creates a limit on the input common mode voltage capability, allowing LMV33x to accurately function from ground to V_{CC} – Vbe(~700mV) differential input. This enables much head room for modern day supplies of 3.3 V and 5.0 V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the positive input voltage is higher than the negative input voltage and the offset voltage. The V_{OL} is resistive and will scale with the output current. Please see 图 6-3 for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The LMV33x operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputs a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LMV331, LMV393, and LMV339 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LMV331, LMV393, and LMV33 optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

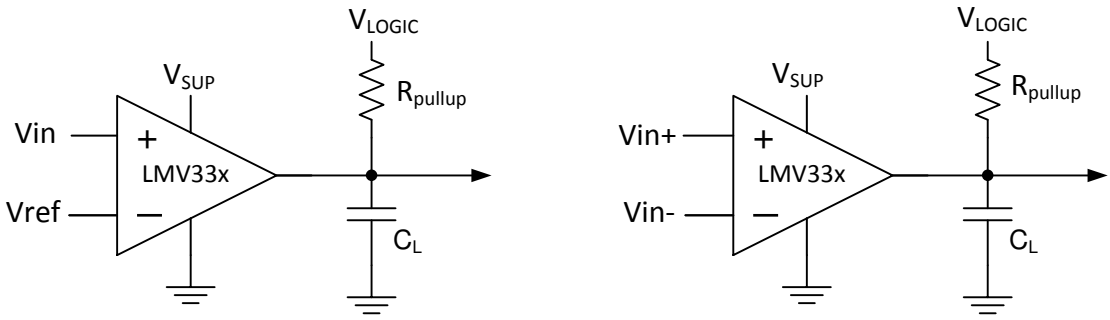


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to 4.2 V
Supply Voltage	2.7 V to 5V
Logic Supply Voltage (R_{PULLUP} Voltage)	1 V to 5 V
Output Current (V_{LOGIC}/R_{PULLUP})	1 µA to 20 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using LMV331, LMV393, and LMV33 in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

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8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If operating temperature is above or below 25°C the V_{ICR} can range from 0 V to V_{CC} – 0.7 V. This limits the input voltage range to as high as V_{CC} – 0.7 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a possible list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). In order to make an accurate comparison; the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 图 8-2 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the pull-up resistance (Rpullup) and Vlogic voltage, refer to 图 8-1. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use 图 6-3 to determine V_{OL} based on the output current.

The output current can also effect the transient response. More will be explained in the next section.

8.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The positive response time (τ_p) is approximately $\tau_P \sim R_{PULLUP} \times C_L$
- The negative response time (τ_N) is approximately $\tau_N \sim R_{CE} \times C_L$
  - R_{CE} can be determine by taking the slope of 图 6-3 in it's linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1 kΩ, and 50 pF scope probe.

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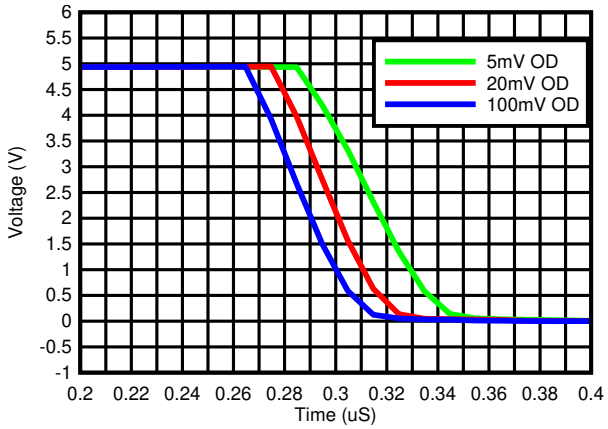


图 8-2. Response Time for Various Overdrives (Negative Transition)

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation cause temporary fluctuations in the comparator's input common mode range and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

10.2 Layout Example

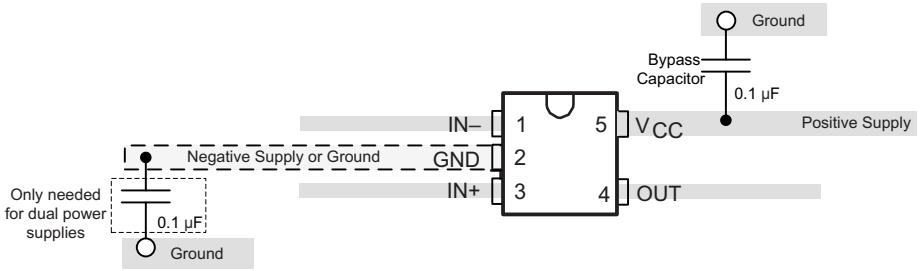


图 10-1. LMV331 Layout Example

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV331	Click here	Click here	Click here	Click here	Click here
LMV393	Click here	Click here	Click here	Click here	Click here
LMV339	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

所有商标均为其各自所有者的财产。

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV331IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)	Samples
LMV331IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)	Samples
LMV331IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)	Samples
LMV331IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)	Samples
LMV331IDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)	Samples
LMV331IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)	Samples
LMV331IDCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)	Samples
LMV331IDCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)	Samples
LMV331IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R2C, R2F, R2R)	Samples
LMV331IDCKTE4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2C, R2F, R2R)	Samples
LMV331IDCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2C, R2F, R2R)	Samples
LMV339ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV339I	Samples
LMV339IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV339I	Samples
LMV339IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I	Samples
LMV339IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I	Samples
LMV339IPWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I	Samples
LMV339IPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I	Samples
LMV339IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(RT, RTR)	Samples
LMV393ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I	Samples
LMV393IDDUR	ACTIVE	VSSOP	DDU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RABR	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV393IDDURG4	ACTIVE	VSSOP	DDU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RABR	Samples
LMV393IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R9B, R9Q, R9R)	Samples
LMV393IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R9B, R9Q, R9R)	Samples
LMV393IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	MV393I	Samples
LMV393IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I	Samples
LMV393IPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I	Samples
LMV393IPWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I	Samples
LMV393IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I	Samples
LMV393IPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

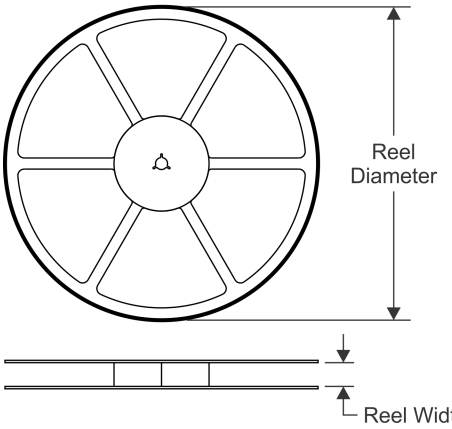
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

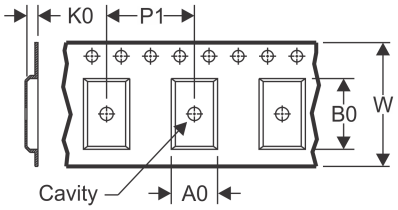
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

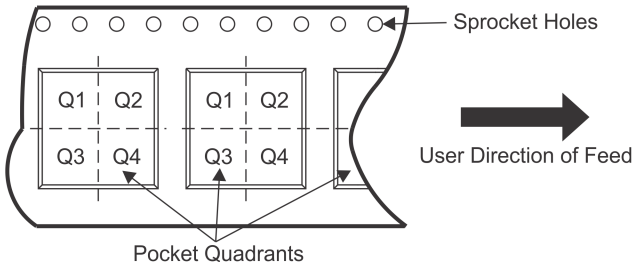


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

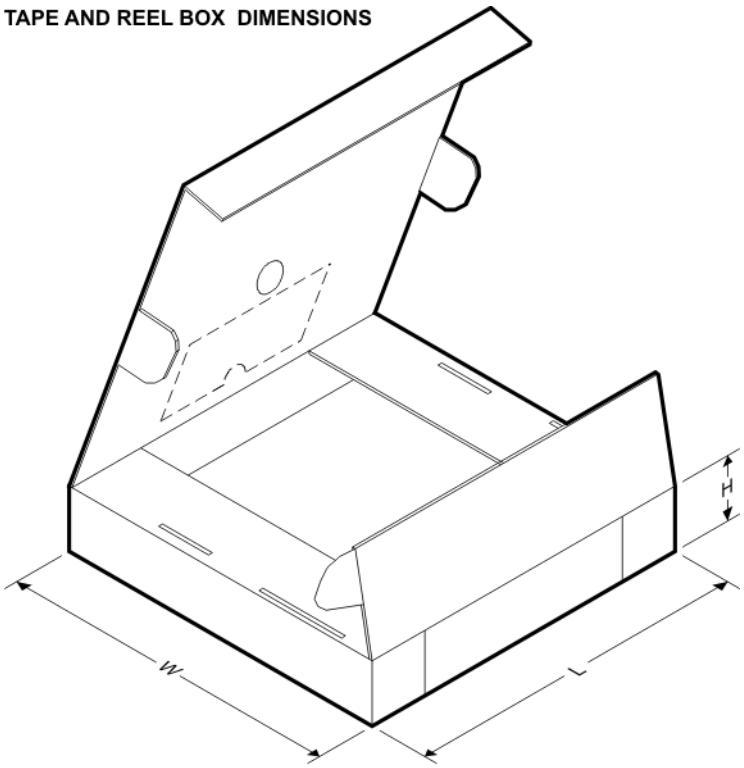
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV331IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV331IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV331IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV331IDCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV331IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV339IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV339IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV339IRUCR	QFN	RUC	14	3000	180.0	8.4	2.3	2.3	0.55	4.0	8.0	Q2
LMV393IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LMV393IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393IDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

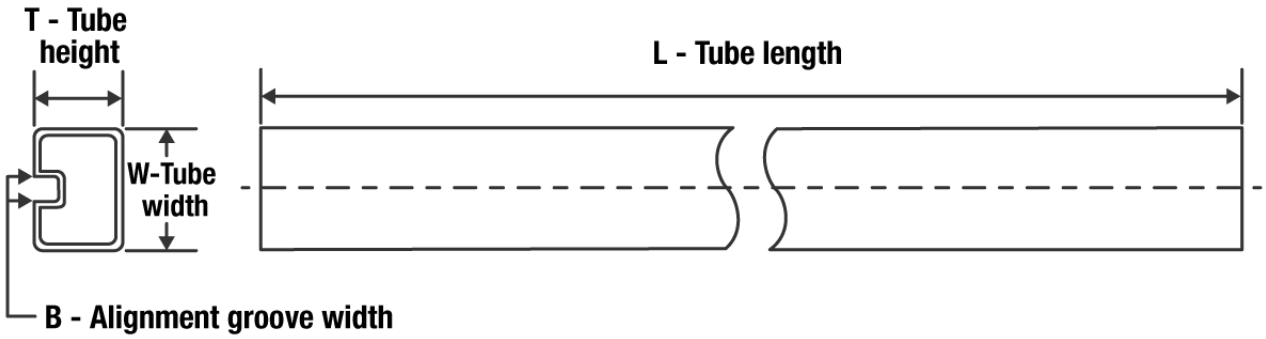
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV331IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LMV331IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV331IDCKT	SC70	DCK	5	250	205.0	200.0	33.0
LMV331IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
LMV339IDR	SOIC	D	14	2500	853.0	449.0	35.0
LMV339IPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
LMV339IRUCR	QFN	RUC	14	3000	202.0	201.0	28.0
LMV393IDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LMV393IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LMV393IDR	SOIC	D	8	2500	364.0	364.0	27.0
LMV393IDR	SOIC	D	8	2500	340.5	336.1	25.0
LMV393IDRG4	SOIC	D	8	2500	340.5	336.1	25.0
LMV393IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

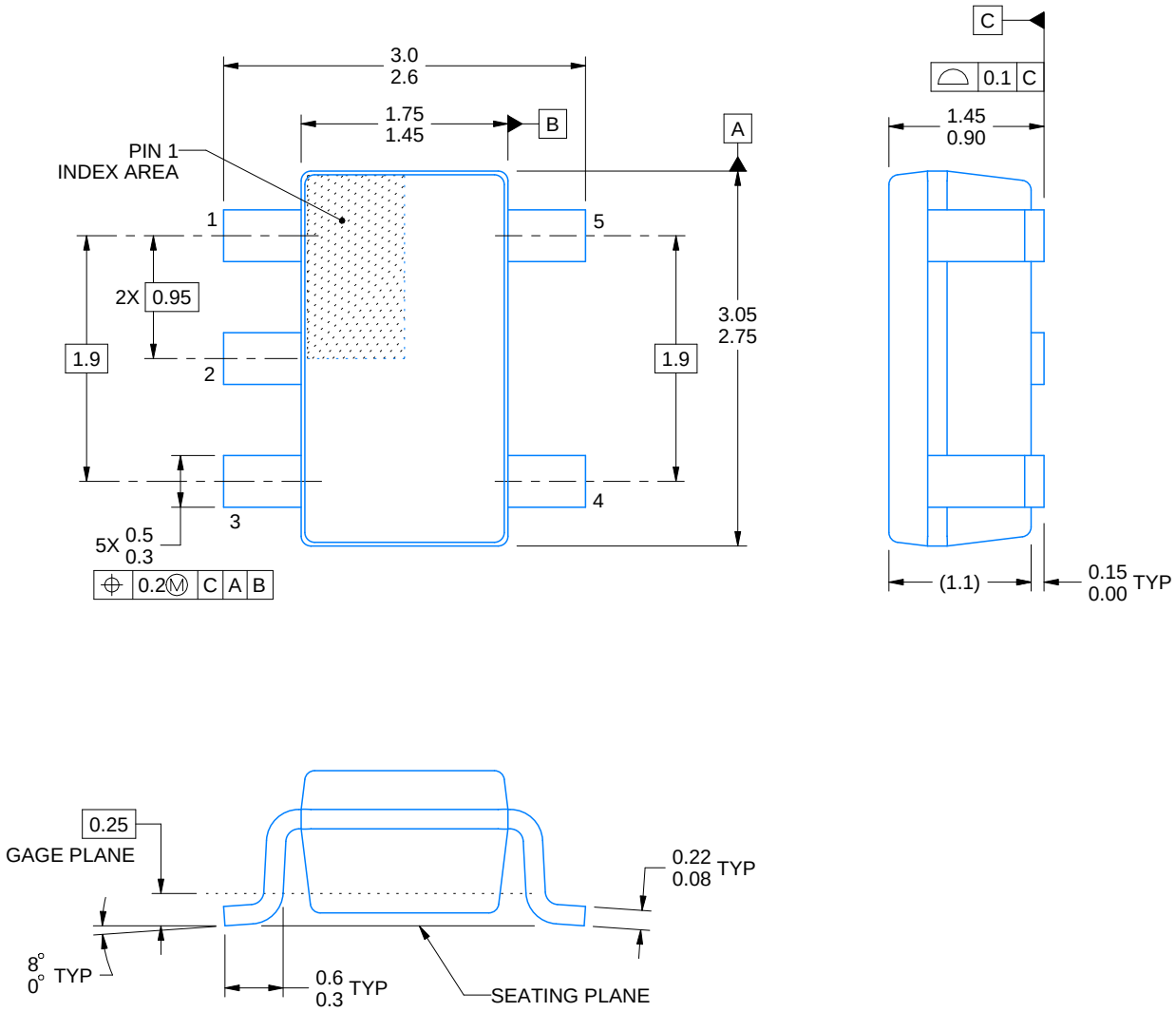
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV339ID	D	SOIC	14	50	506.6	8	3940	4.32
LMV339IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
LMV393ID	D	SOIC	8	75	507	8	3940	4.32
LMV393IPW	PW	TSSOP	8	150	530	10.2	3600	3.5
LMV393IPWG4	PW	TSSOP	8	150	530	10.2	3600	3.5

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

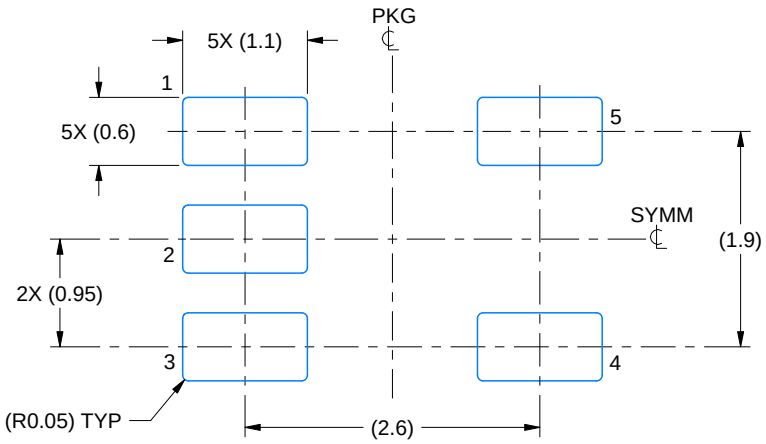
SMALL OUTLINE TRANSISTOR



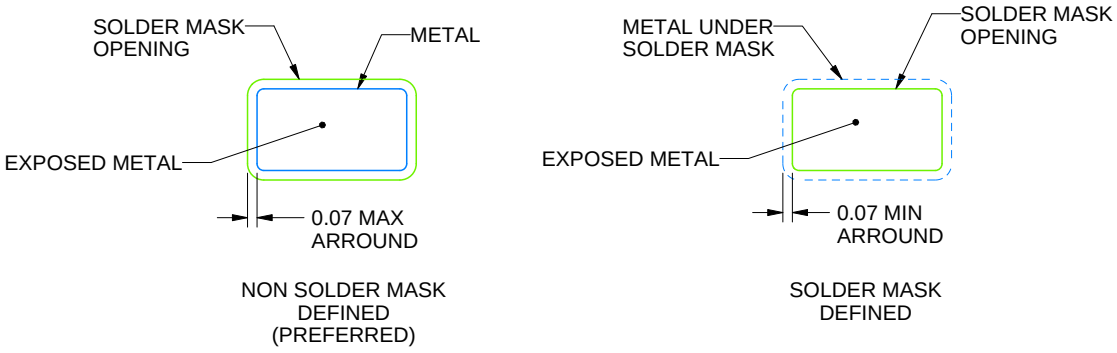
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

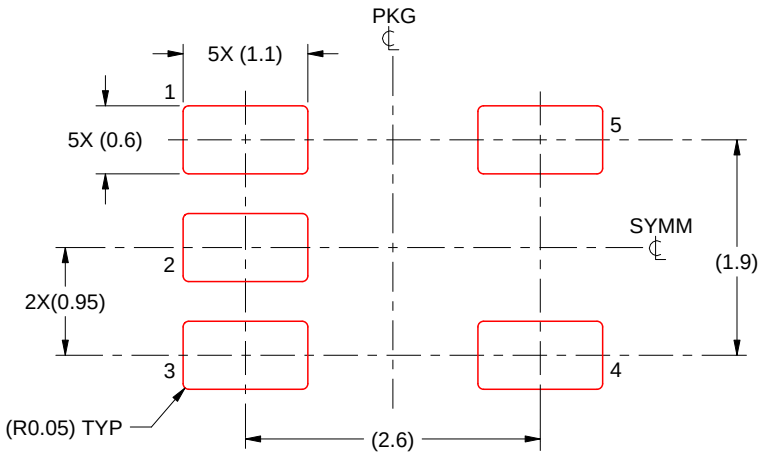


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



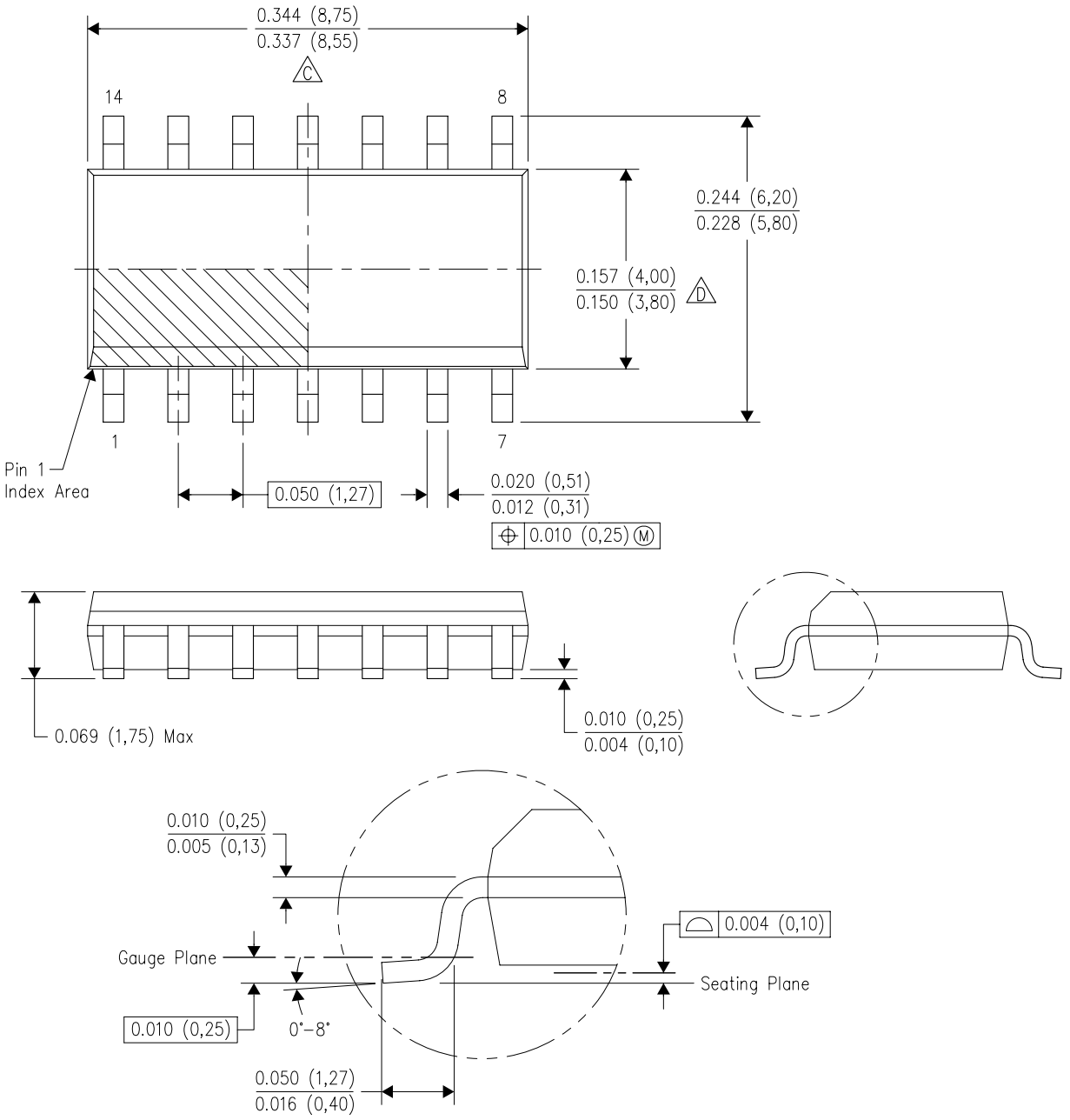
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

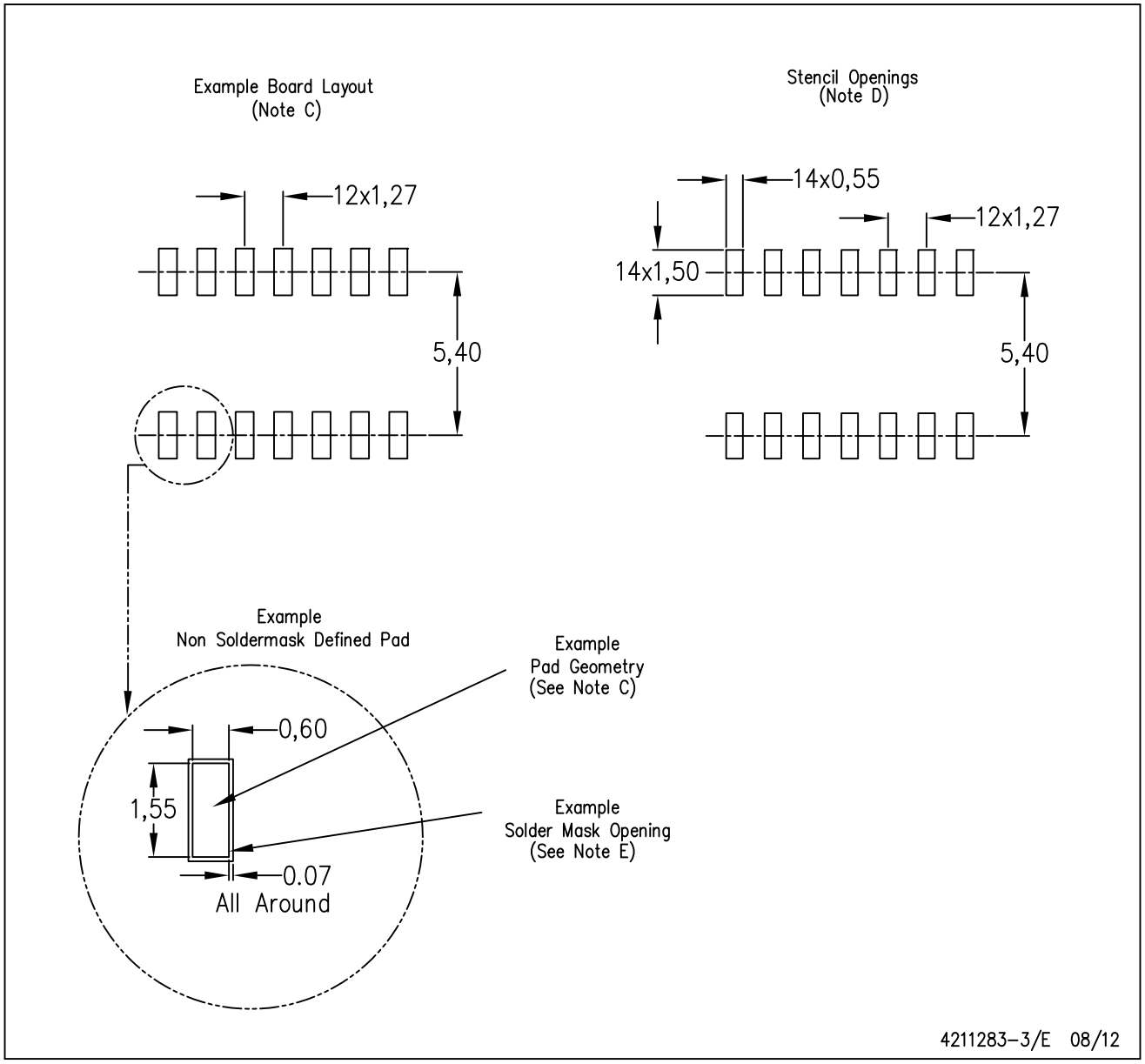
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

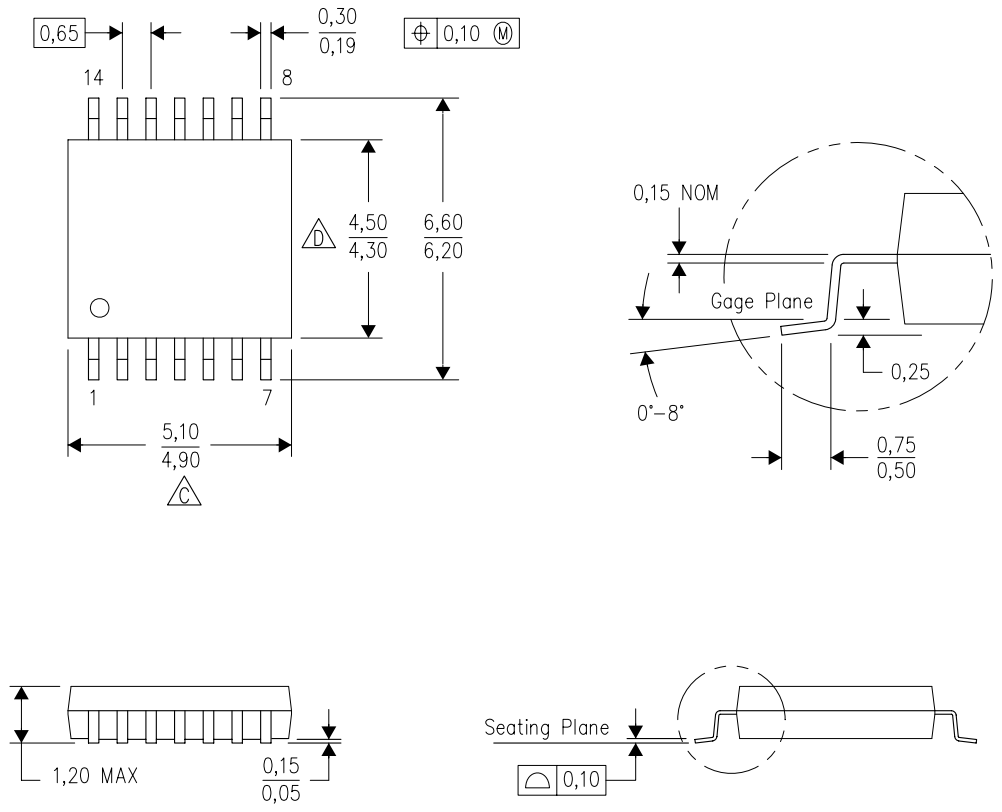
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

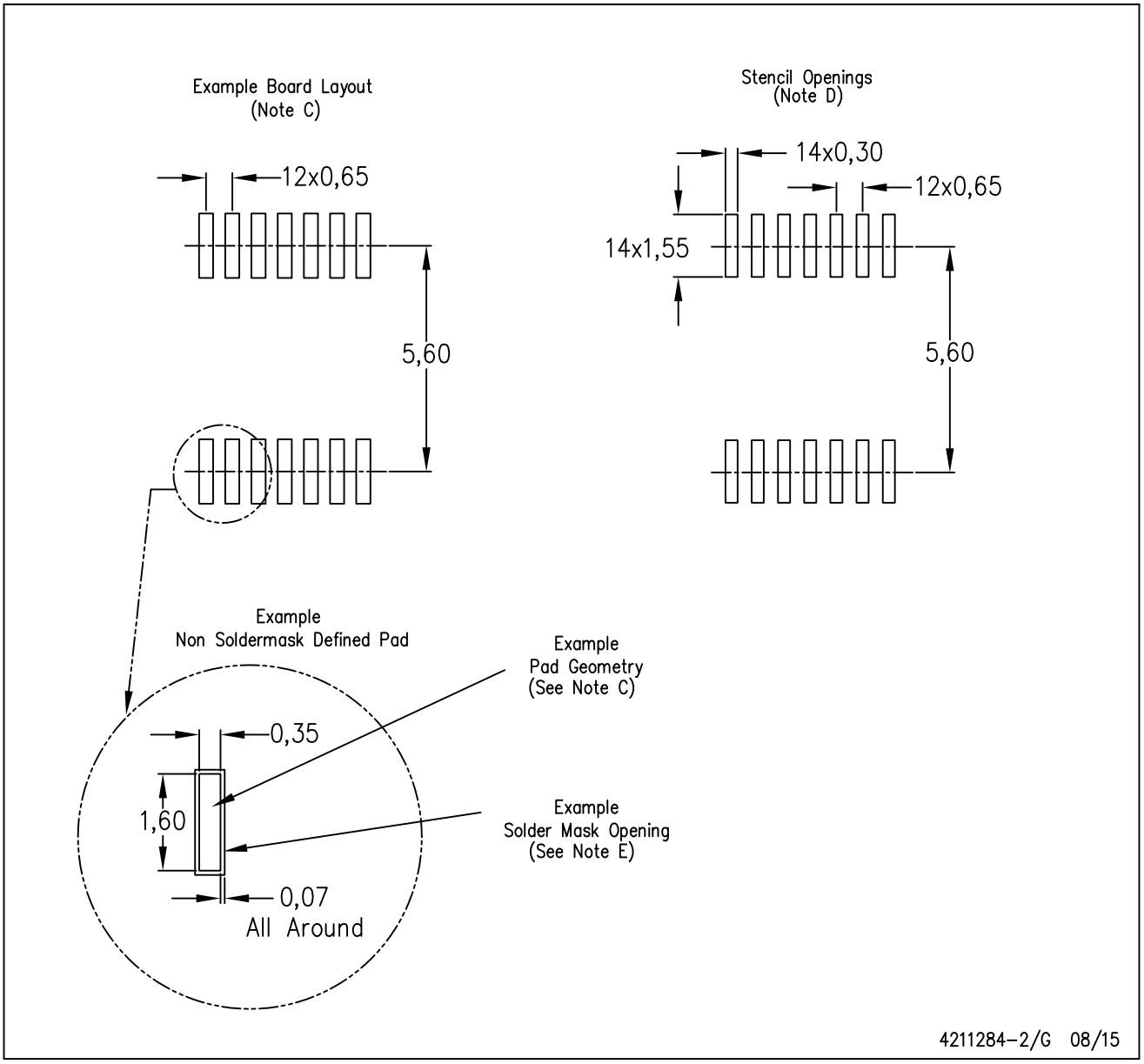
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



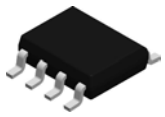
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

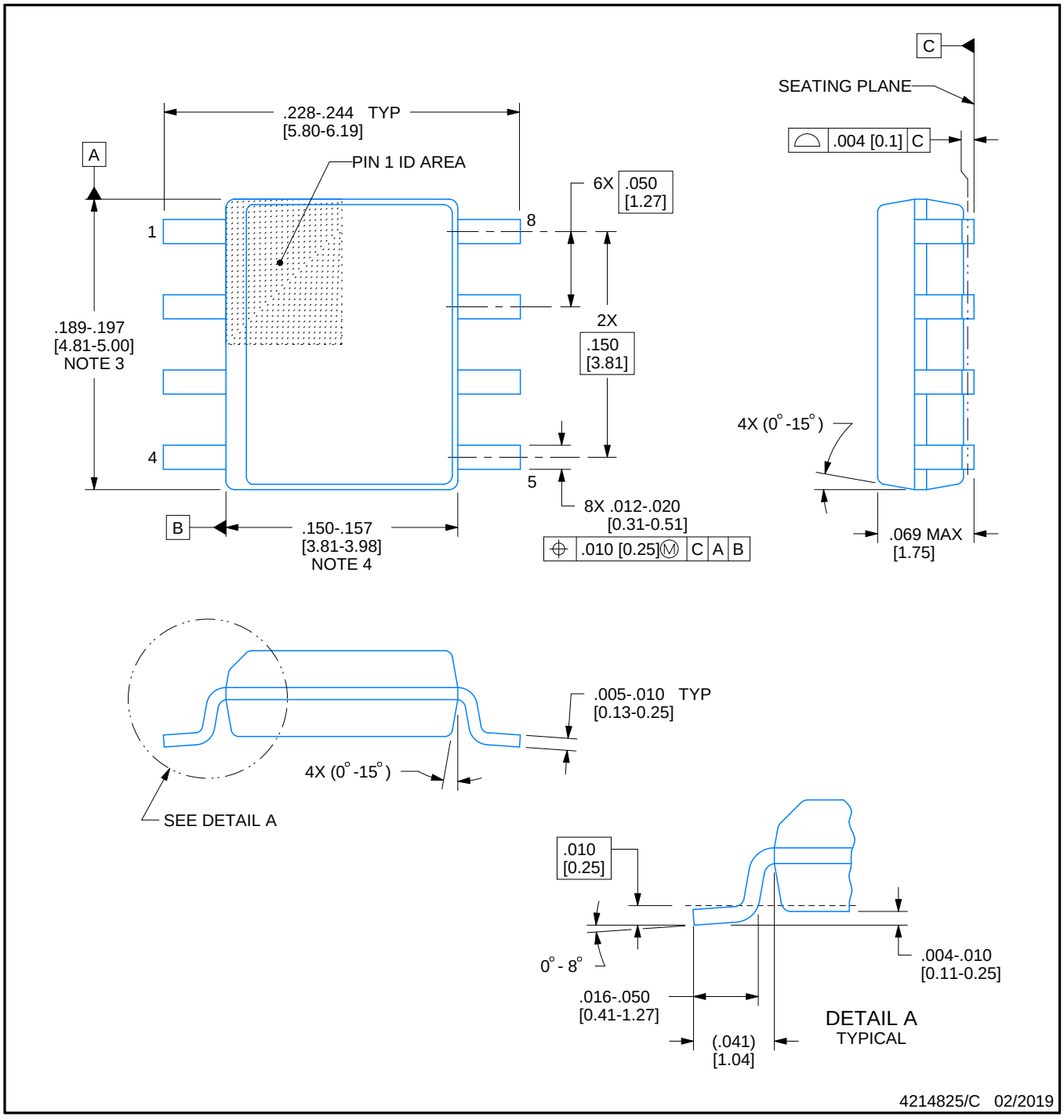


PACKAGE OUTLINE

D0008A

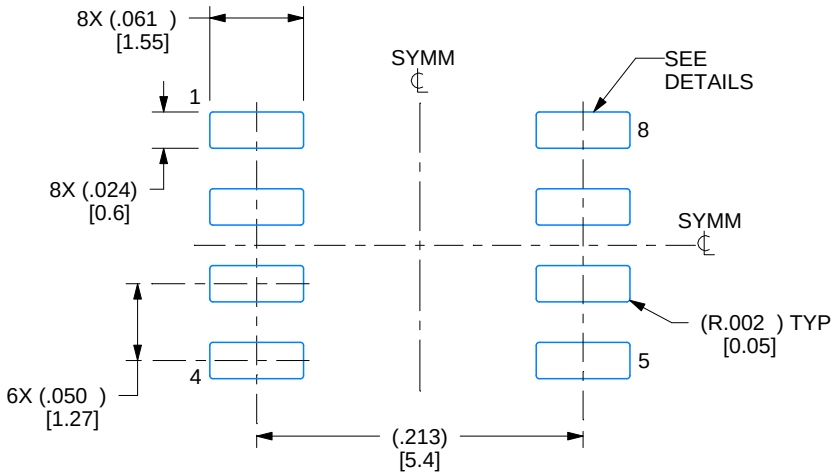
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

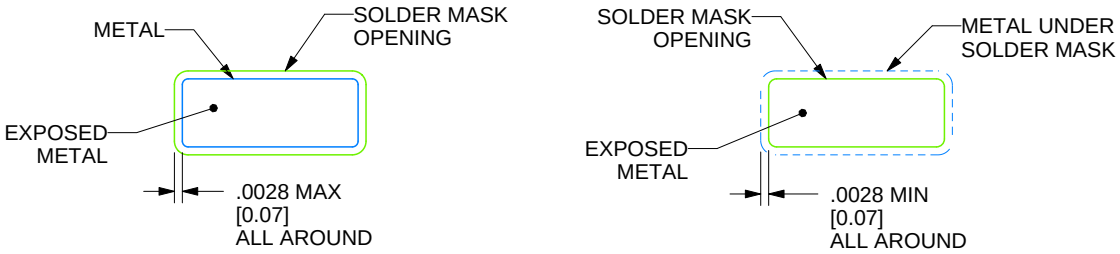


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

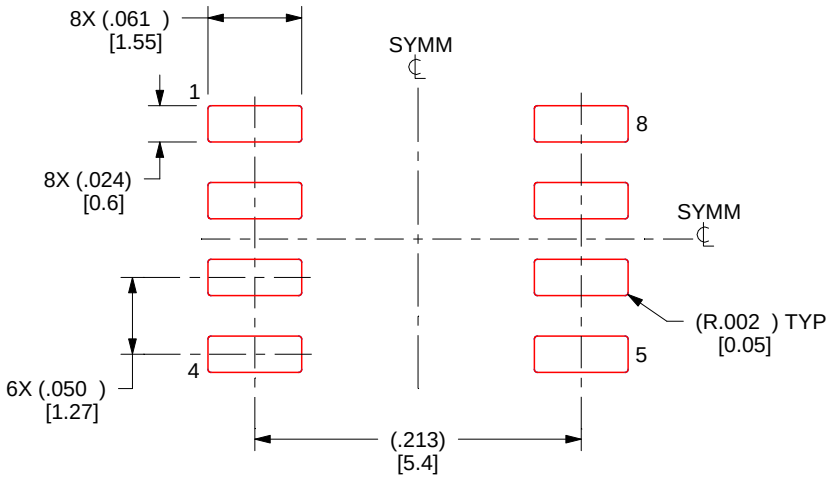
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



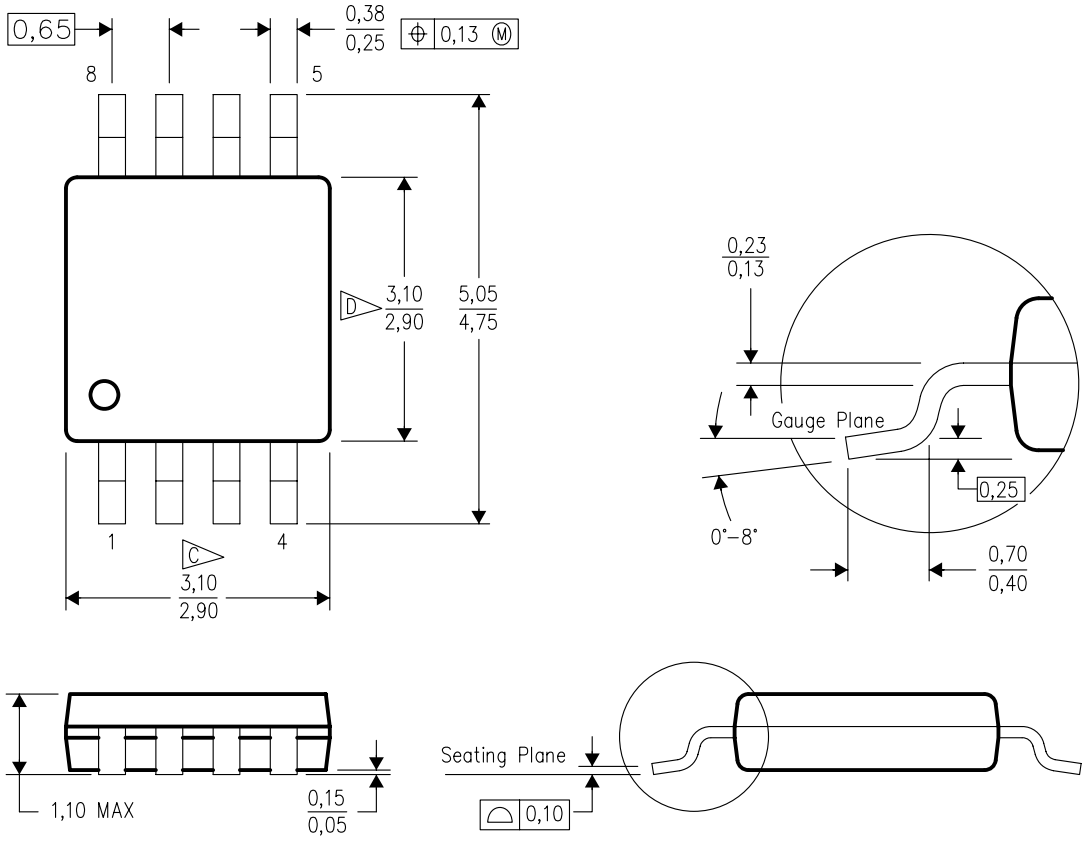
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

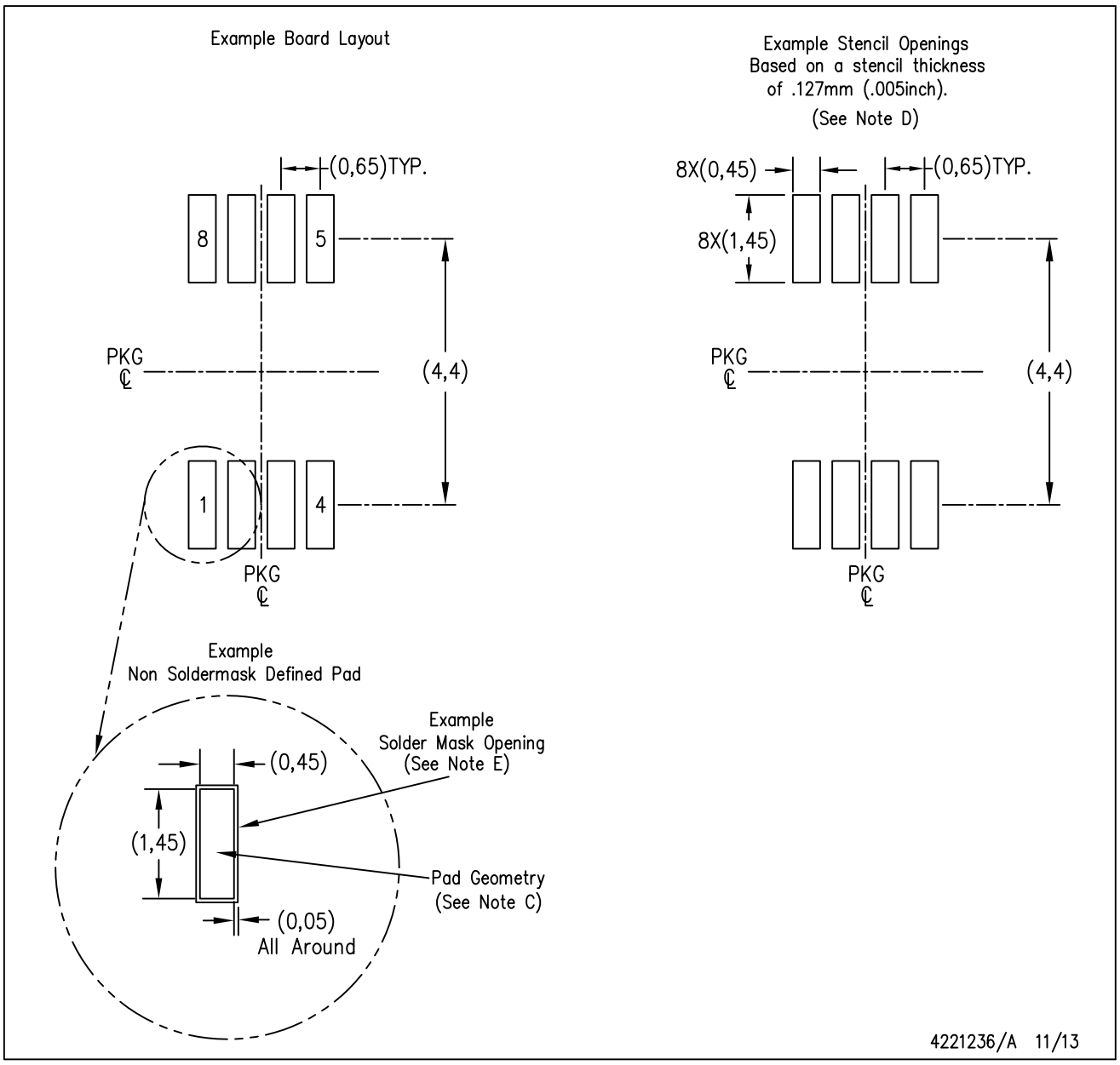
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



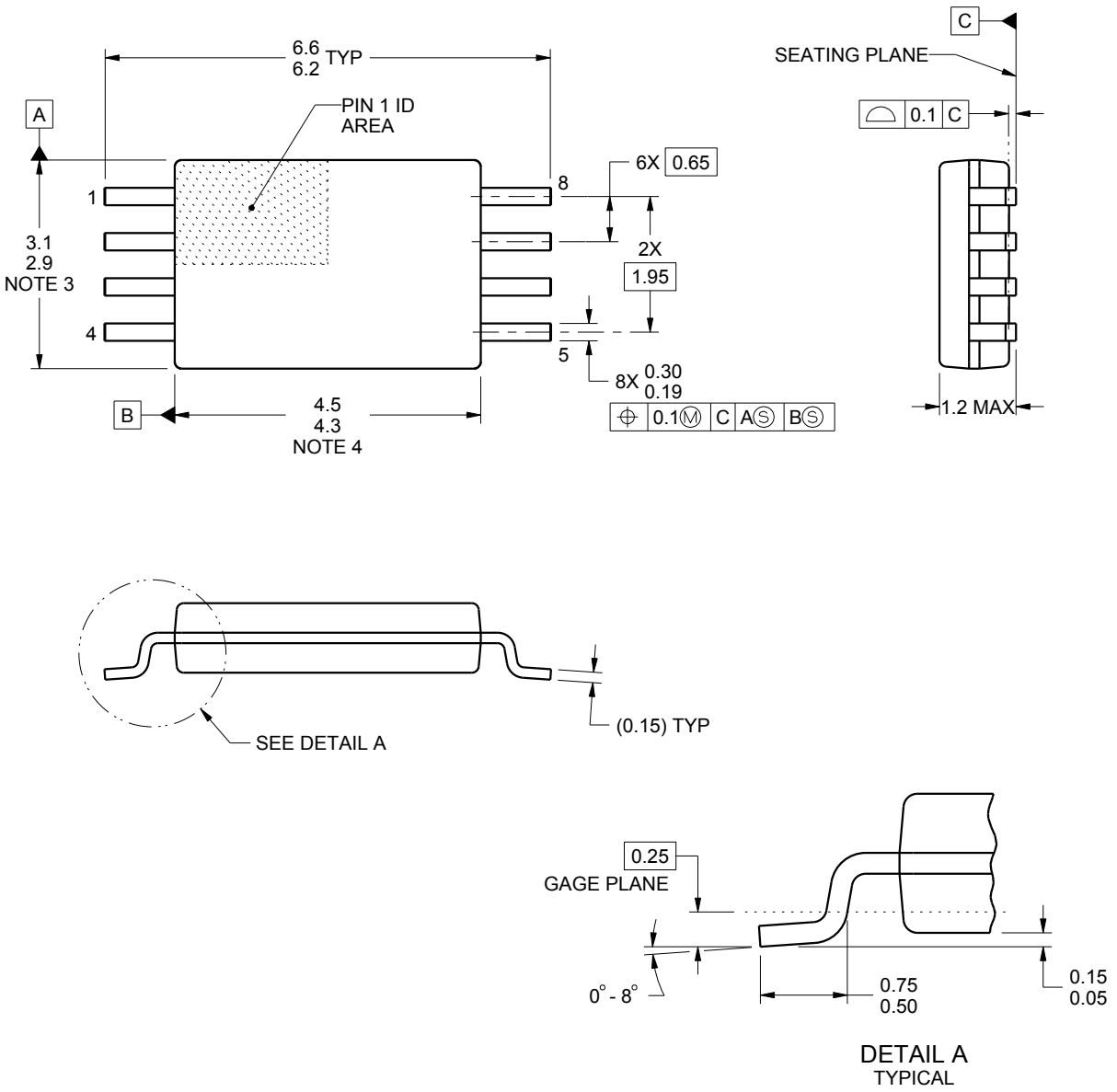
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

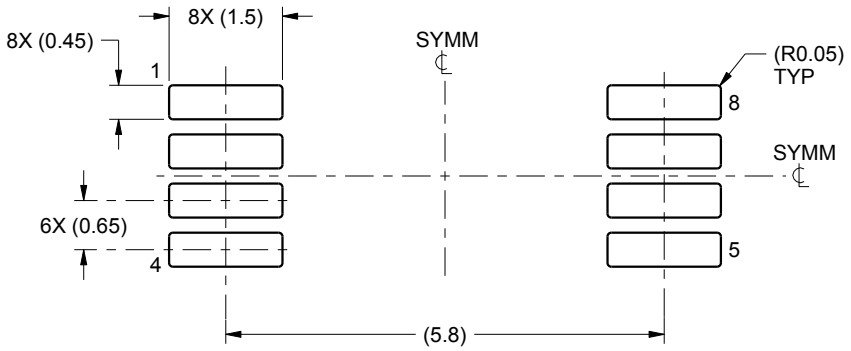
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

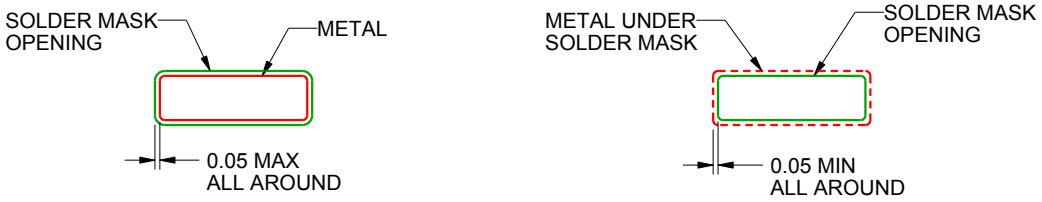


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

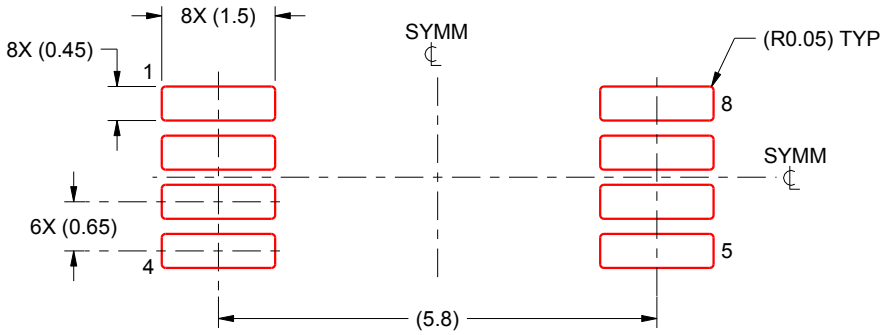


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

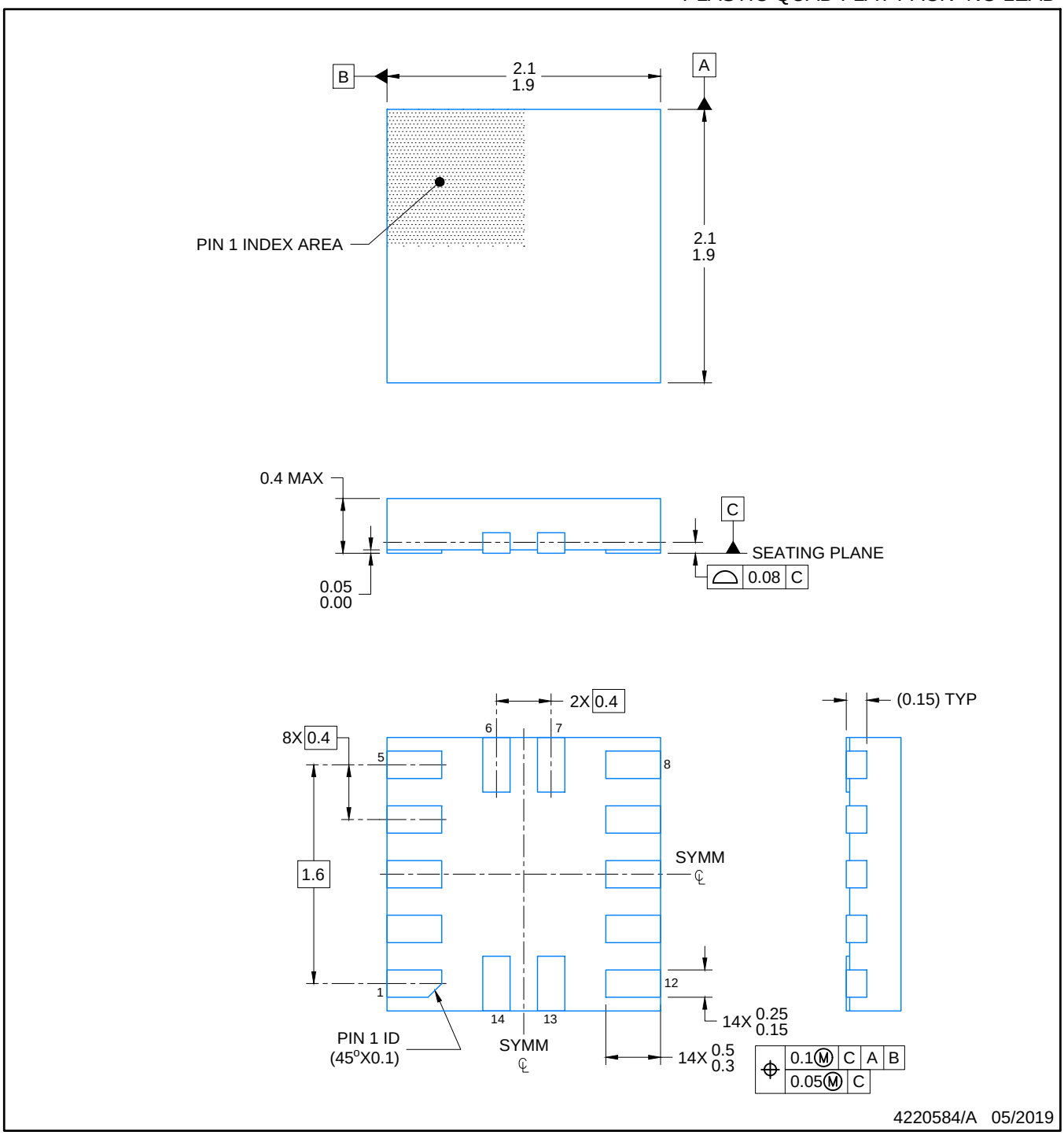
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RUC0014A

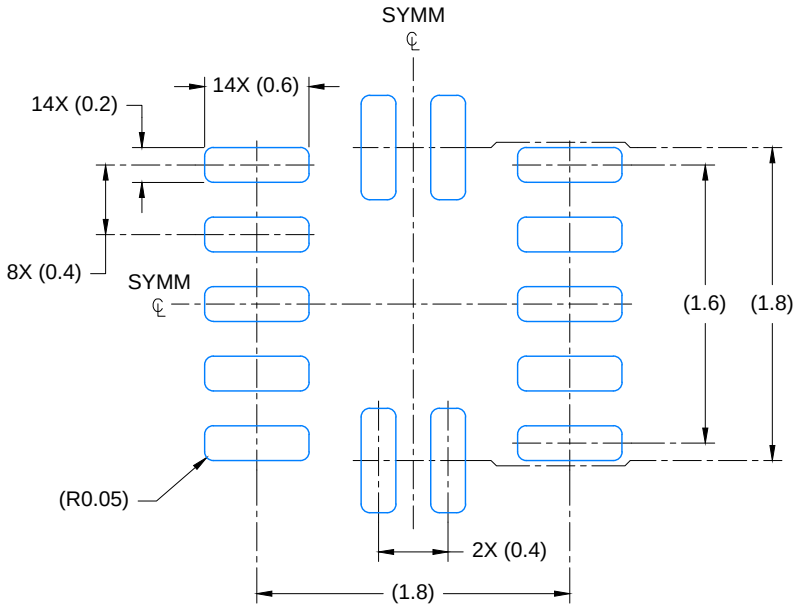
X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

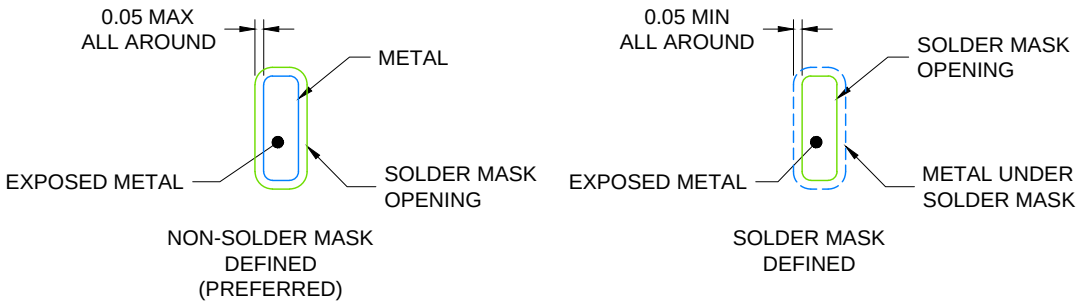


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

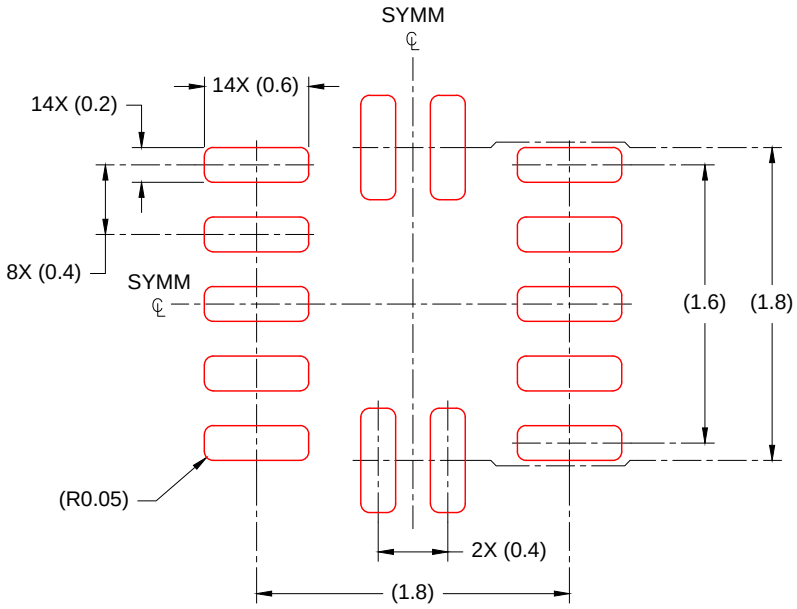


SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



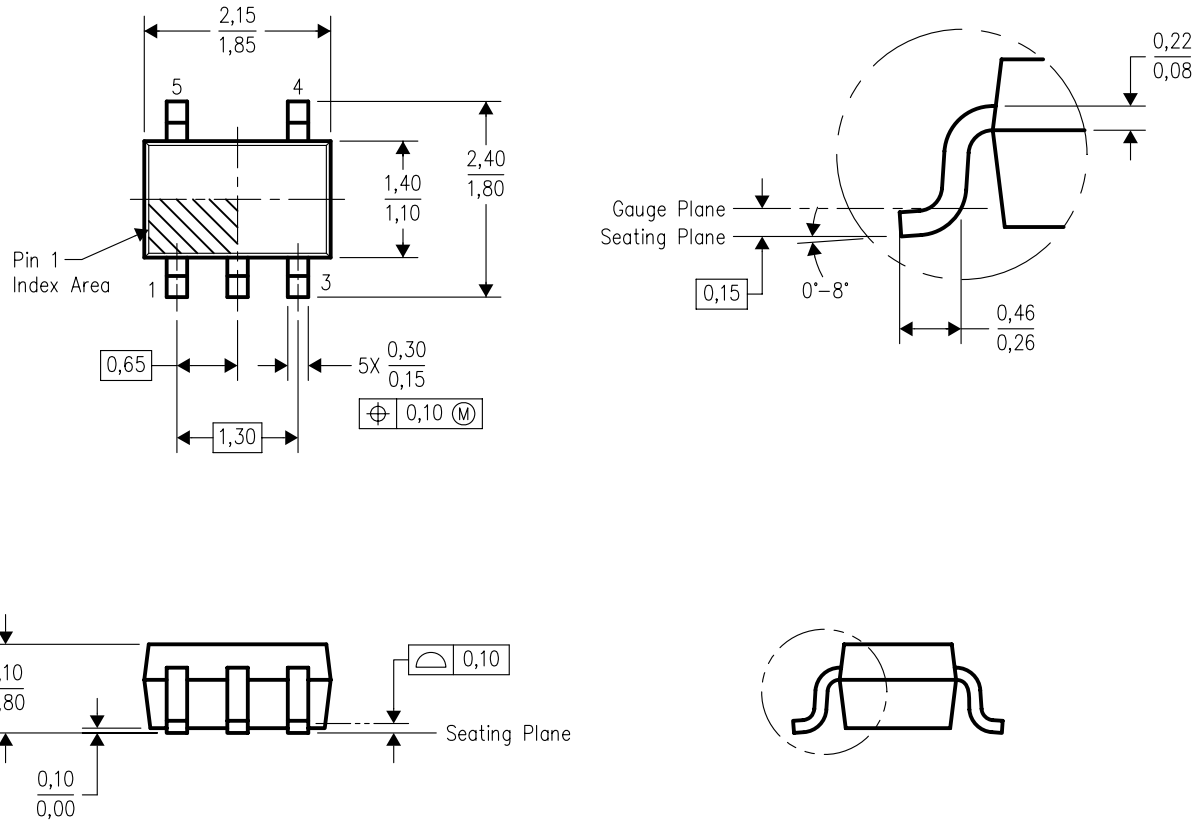
SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

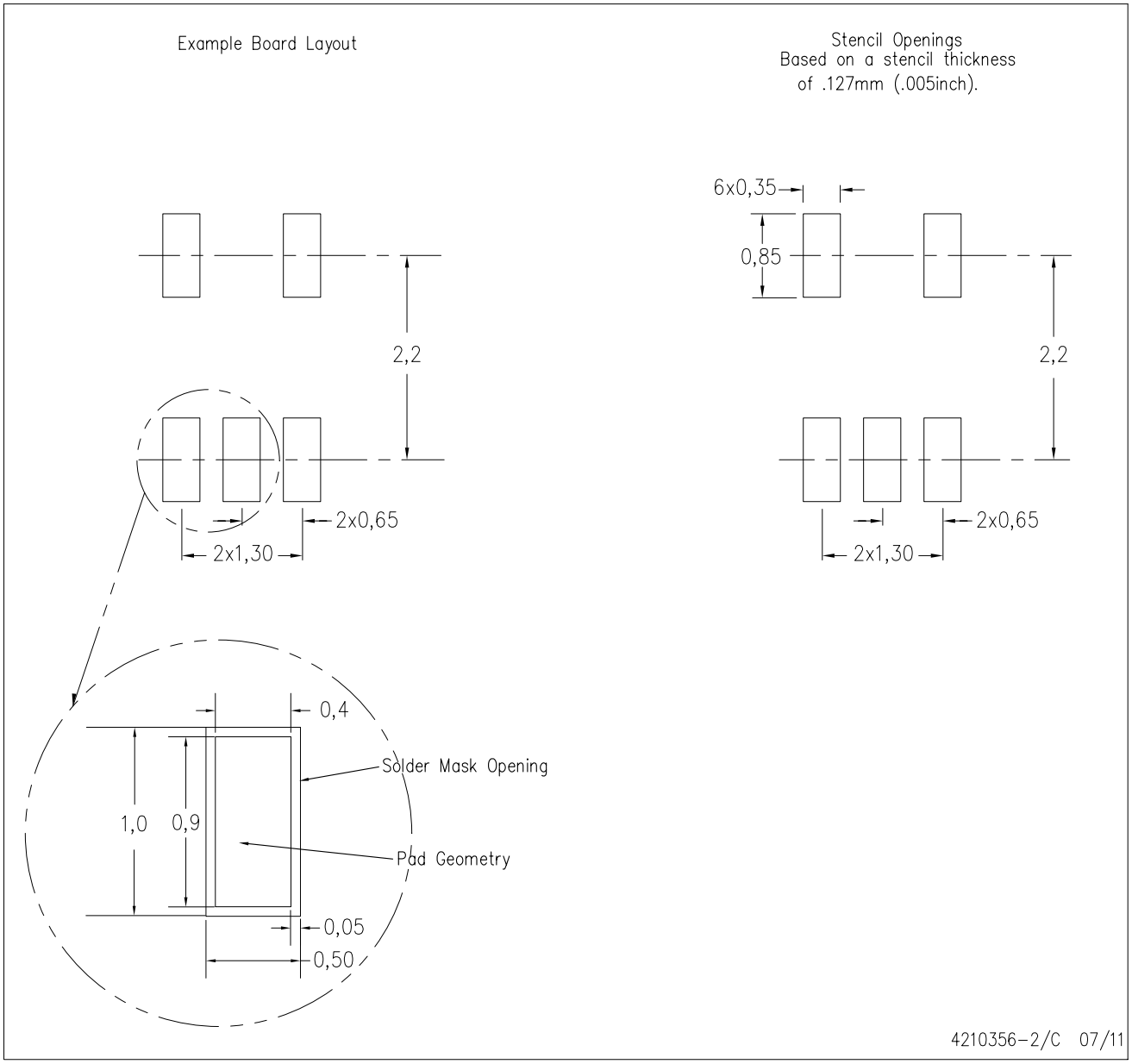
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

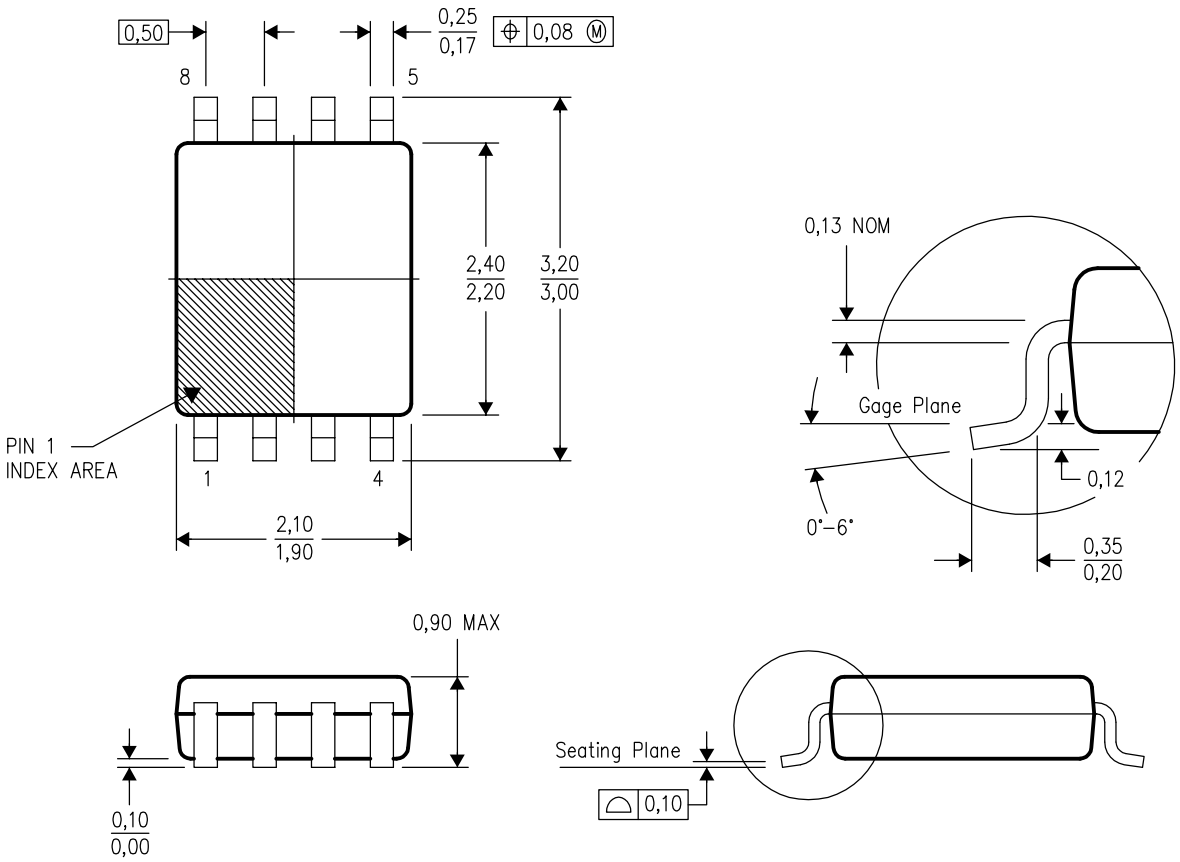
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

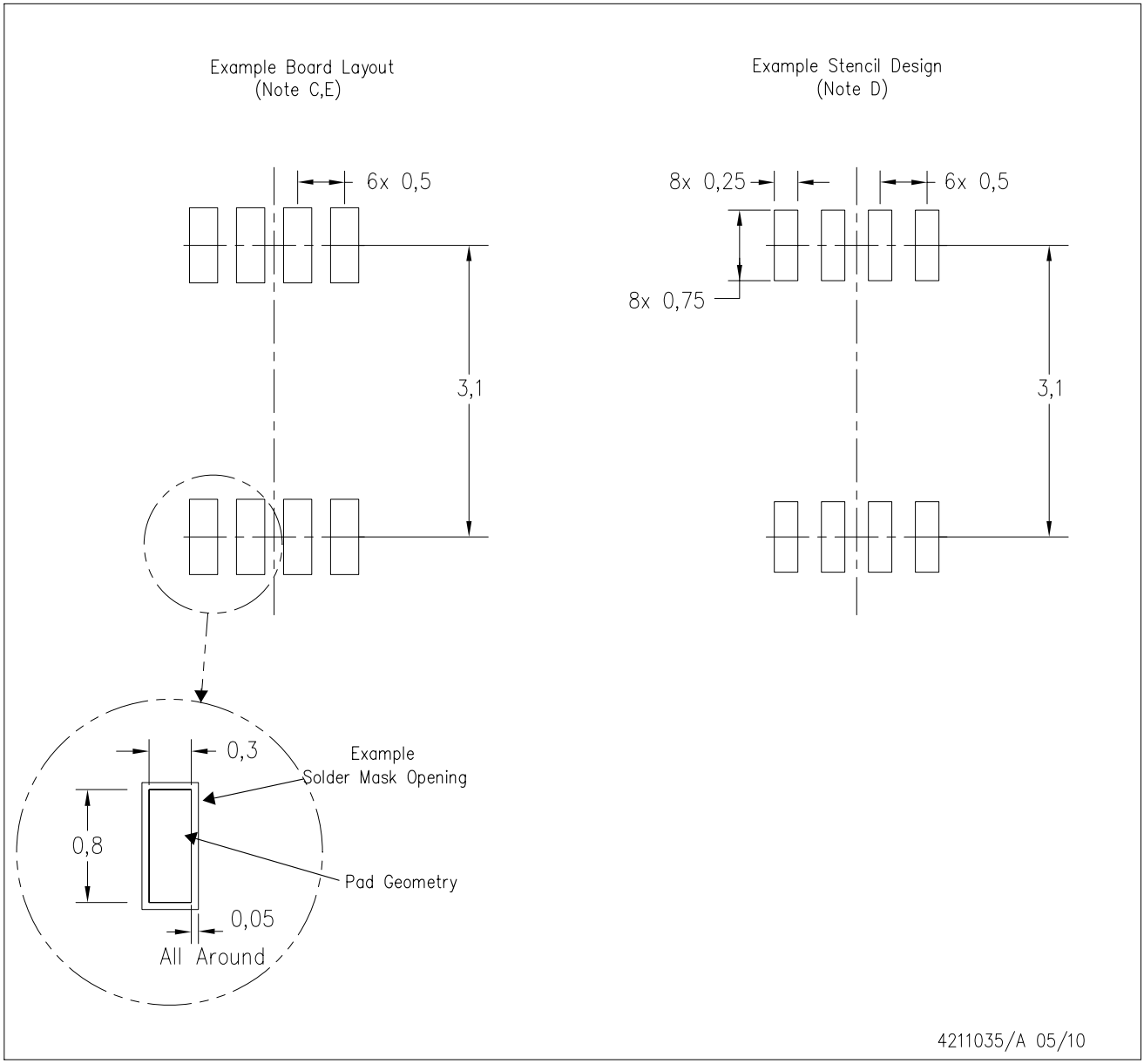
DDU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4205140/A 05/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation CA.

DDU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE UP)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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