TEXAS INSTRUMENTS
LM61495-Q1, LM61480-Q1, LM62460-Q1
ZHCSLY1D – FEBRUARY 2020 – REVISED AUGUST 2021

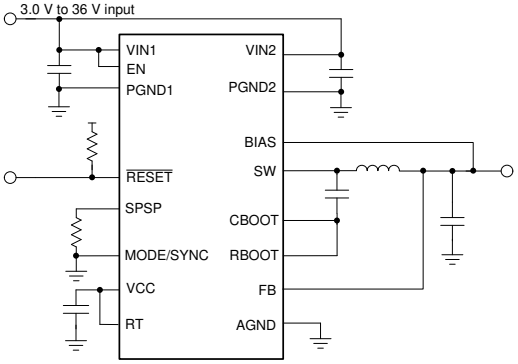
针对功率密度和低 EMI 进行了优化的 LM62460-Q1、LM61480-Q1 和 LM61495-Q1 引脚兼容 6A/8A/10A 汽车类降压转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 输入电压范围：3V 至 36V
- 具有滤波器和延迟释放的 $\overline{\text{RESET}}$ 输出
- 可实现低 EMI：
  - 符合 CISPR 25 5 级要求的 EVM
  - 引脚可配置展频
  - 可调节 SW 节点上升时间
  - 高于和低于 AM 频带运行：引脚可配置为固定 400kHz 和 2.2MHz，或可在 200kHz 至 2.2MHz 之间调节
  - 低 EMI 对称引脚排列
  - 对于恒定频率或脉冲频率调制 (PFM)，轻负载模式下可对引脚进行配置
- 高效解决方案
  - 8A 负载可实现 95% 的效率
  - 在自动模式下空载时具有 5μA 的输入电流
  - <1μA 关断电流（典型值）
- 高功率密度
  - 内置补偿、软启动、电流限制、热关断和 UVLO
  - 4.5mm × 3.5mm 可湿性侧面 QFN 封装
  - Θ_{JA} = 21.6°C/W，在 LM61495RPHEVM 上测量

2 应用

- 汽车信息娱乐系统
- 仪表组
- ADAS



简化版原理图

3 说明

LM6x4xx-Q1 降压稳压器系列是面向汽车的稳压器，可提供固定或可调节输出电压（可设置范围为 1V 至预期输入电压的 95%）。这些稳压器可在宽输入电压范围（3V 至 36V）内工作，可承受高达 42V 的瞬态容差。

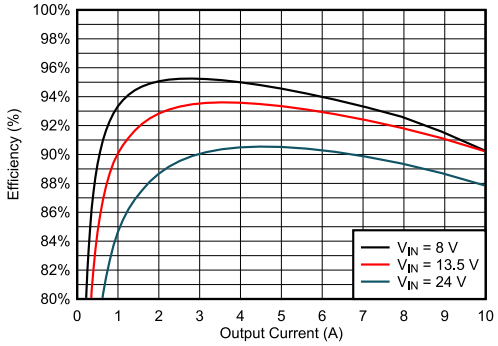
该系列专为低 EMI 设计。该器件具有可选择引脚的展频和可调节的 SW 节点上升时间。双随机展频 (DRSS) 跳频设置为 ±4%（典型值），可通过三角调制与假随机调制的组合大幅降低峰值发射，并采用先进的技术来减少展频调制导致的输出电压纹波。

开漏 $\overline{\text{RESET}}$ 输出具有滤波和延迟释放功能，可提供正确的系统状态指示。在自动模式中，器件自动在固定频率脉宽调制 (FPWM) 和脉冲频率调制 (PFM) 运行模式之间转换，从而实现仅 5μA（典型值）的空载电流消耗。电气特性额定结温范围为 –40°C 至 +150°C。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM61495-Q1	VQFN (16)	4.50mm × 3.50mm
LM61480-Q1		
LM62460-Q1		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



EVM 效率：V_{OUT} = 5V，F_{SW} = 2.2MHz

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (May 2021) to Revision D (August 2021)	Page
• Changed status of 8-A devices to released	3
• Changed status of 4-V options to released	3
• Updated 图 9-29 to 图 9-45	41

Changes from Revision B (March 2021) to Revision C (May 2021)	Page
• Changed status of 6-A devices to released	3
• Added sentence to the SYNC/MODE pin	4

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5 Device Comparison Table

DEVICE	VARIANT	LIGHT LOAD	SPREAD SPECTRUM	OUTPUT VOLTAGE	TYPICAL FREQUENCY	CURRENT
LM61495-Q1 (10-A rating)	LM61495QRPHRQ1	Pin selectable	Pin selectable	Adjustable	Pin selectable	10 A
	LM61495Q3RPHRQ1			3.3 V		
	LM61495Q4RPHRQ1			4.0 V		
	LM61495Q5RPHRQ1			5.0 V		
LM61480-Q1 (8-A rating)	LM61480QRPHRQ1	Pin selectable	Pin selectable	Adjustable	Pin selectable	8 A
	LM61480Q3RPHRQ1			3.3 V		
	LM61480Q4RPHRQ1			4.0 V		
	LM61480Q5RPHRQ1			5.0 V		
LM62460-Q1 (6-A rating)	LM62460QRPHRQ1	Pin selectable	Pin selectable	Adjustable	Pin selectable	6 A
	LM62460Q3RPHRQ1			3.3 V		
	LM62460Q4RPHRQ1			4.0 V		
	LM62460Q5RPHRQ1			5.0 V		

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6 Pin Configuration and Functions

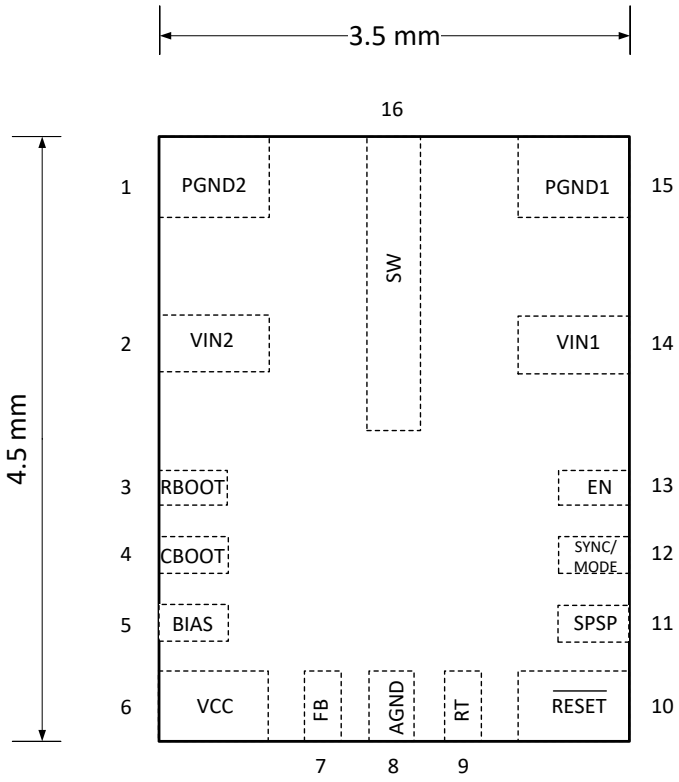


图 6-1. 16-Pin VQFN RPH Package (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND2	1	G	Power ground to internal low-side MOSFET. Connect to system ground. Low-impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
VIN2	2	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Provide a low-impedance connection to VIN1.
RBOOT	3	P	Connect to CBOOT through a resistor. A resistance, typically between 0 Ω and 100 Ω, is used to adjust the slew rate of the SW node rise time. See 图 8-10.
CBOOT	4	P	High-side driver upper supply rail. Connect a 100-nF capacitor between the SW pin and CBOOT. An internal diode charges the capacitor while SW node is low.
BIAS	5	P	Input to internal voltage regulator. Connect the pin to an output voltage point or an external bias supply from 3.3 V to 12 V. Connect an optional high-quality 0.1-µF capacitor from this pin to GND for the best performance. If output voltage is above 12 V and no external supply is used, tie the pin to ground.
VCC	6	O	Internal regulator output. Used as supply to internal control circuits. Do not connect this pin to any external loads. Connect a high-quality 1-µF capacitor from this pin to AGND.
FB	7	I	Feedback input to regulator. Connect this pin to an output voltage sense point for fixed output versions (for example, 3.3 V and 5 V). Connect this pin to a feedback divider tap point for adjustable output options. Do not float or ground.
AGND	8	G	Analog ground for regulator and system. All electrical parameters are measured with respect to this pin. Connect this pin to PGND1 and PGND2 on PCB.
RT	9	I/O	Connect this pin to ground through a resistor with a value between 6.8 kΩ and 80 kΩ to set the switching frequency between 200 kHz and 2200 kHz. Connect to VCC for 400 kHz. Connect to GND for 2.2 MHz. Do not float.

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表 6-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RESET	10	O	Open-drain RESET output. Connect to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. RESET goes low when EN = low.
SPSP	11	I	Connect to VCC or through a resistor to ground to enable spread spectrum. Connect to GND to disable spread spectrum. If using spread spectrum, a VCC connection turns off the spread spectrum tone correction while a resistor to ground adjusts the tone correction to lower the output voltage ripple. Do not float this pin. See 节 8.3.10.
SYNC/MODE	12	I	This pin controls the mode of operation of the LM6x4xx. Modes include Auto mode (automatic PFM/PWM operation), forced pulse width modulation (FPWM), and synchronized to an external clock. The clock triggers on the rising edge of an applied external clock. Pull low to enable PFM operation, pull high to enable FPWM, or connect to a clock to synchronize to an external frequency in FPWM mode. Do not float this pin. When synchronized to an external clock, use the RT pin to set the internal frequency close to the synchronized frequency to avoid disturbances if the external clock is turned on and off.
EN	13	I	Precision enable input to regulator. High = on, low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Do not float. See 节 8.3.2.
VIN1	14	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low-impedance connection must be provided to VIN2.
PGND1	15	G	Power ground to internal low-side MOSFET. Connect to system ground. Low-impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
SW	16	P	Switch node of the regulator. Connect to the output inductor.

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Voltages	Transient VIN to AGND, PGND(2)	–0.3	42	V
	Continuous VIN to AGND, PGND(2)	–0.3	36	
	SW to AGND, PGND(3)	–0.3	V_{IN} + 0.3	
	RBOOT, CBOOT to SW	–0.3	5.5	
	Transient EN or SYNC/MODE to AGND, PGND(2)	–0.3	42	
	Continuous EN or SYNC/MODE to AGND, PGND(2)	–0.3	36	
	BIAS to AGND, PGND	–0.3	16	
	FB to AGND, PGND: Fixed Versions	–0.3	16	
	FB to AGND, PGND: Adjustable Versions	–0.3	5.5	
	$\overline{\text{RESET}}$ to AGND, PGND	0	20	
Current	$\overline{\text{RESET}}$ sink current(5)	0	10	mA
Voltages	RT to AGND, PGND	-0.3	5.5	V
	VCC to AGND, PGND	–0.3	5.5	
	PGND to AGND(4)	–1	2	
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A maximum of 42V can be sustained at this pin for duration of ⩽100ms at a duty cycle of ⩽0.01%. 36 V can be sustained for the life of this device.
(3) A voltage of 2V below GND and 2V above VIN can appear on this pin for ⩽200ns with a duty cycle of ⩽ 0.01%.
(4) This specification applies to voltage durations of 100 ns or less. The maximum D.C. voltage should not exceed +/- 0.3V.
(5) Do not exceed pin 's voltage rating.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Clasification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD clasiffication Level C5	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	Input Voltage Range(1)	3	36	V
Output voltage	Output Adjustment Range for adjustable output versions (2)	1	0.95 × VIN	V
Frequency	Frequency adjustment range	200	2200	kHz
Sync Frequency	Synchronization frequency range	200	2200	kHz
Output current	I_{OUT}, LM62460	0	6	A
Output current	I_{OUT}, LM61480	0	8	A
Output current	I_{OUT}, LM61495	0	10	A

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Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Temperature	Operating junction temperature, T_J	–40	150	°C

(1) 3.7 V is required at VIN for start up, an extended input voltage range down to 3.0 V is possible after start up; See the minimum input voltage for startup conditions.
(2) Under no conditions should the output voltage be allowed to fall below zero volts.

7.4 Thermal Information

THERMAL METRIC (1)		LM6X4XX RPH 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (LM61495RPHEVM) (3)	21.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7) (2)	51.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, the EVM $R_{\Theta JA}$ = 21.6 °C/W. For design information please see the Maximum Ambient Temperature section.
(3) Refer to the EVM User's Guide for board layout and additional information. For thermal design information please see the Maximum Ambient Temperature section.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is output set point.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	Minimum operating input voltage	Needed to start up			3.7	V
		Once Operating			3	V
$V_{IN_OP_H}$	Minimum voltage hysteresis			1		V
I_Q	Non-switching input current; measured at VIN pin (3)	V_{IN} =13.5 V, V_{FB} = +5%, V_{BIAS} = 5 V		0.662	10	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0 V, V_{IN} = 13.5V		0.662	7.5	µA
I_B	Current into BIAS pin (not switching)	V_{IN} = 13.5 V, V_{FB} = +5%, V_{BIAS} = 5 V, Auto Mode Enabled		18.5	26	µA
ENABLE (EN PIN)						
V_{EN}	Enable input-threshold voltage - rising	V_{EN} rising	1.161	1.263	1.365	V
V_{EN_HYST}	Enable threshold hysteresis		0.25		0.5	V
V_{EN_WAKE}	Enable Wake-up threshold		0.4			V
I_{EN}	Enable pin input current	V_{IN} = V_{EN} = 13.5 V		0.3	50	nA
INTERNAL LDO (VCC PIN)						
V_{CC}	Internal VCC voltage	V_{IN} = 13.5 V, V_{BIAS} = 0V		3.4		V
		V_{IN} = 13.5 V, V_{BIAS} = 3.3 V, 20 mA		3.2		

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC_UVLO}	V_{IN} voltage at which Internal VCC under voltage lock-out is released	I_{VCC} = 0A			3.7	V
$V_{CC_UVLO_HYST}$	Internal VCC under voltage lock-out hysteresis	Hysteresis below V_{CC_UVLO}		1.2		V
VOLTAGE REFERENCE (FB PIN)						
$V_{FB_3.3V}$	Initial reference voltage accuracy for 3.3 V option	V_{IN} = 5 V to 36 V, FPWM Mode	3.24	3.3	3.34	V
V_{FB_4V}	Initial reference voltage accuracy for 4 V option	VIN = 5 V to 36 V, FPWM Mode	3.9	4	4.04	
V_{FB_5V}	Initial reference voltage accuracy for 5 V option	V_{IN} = 6 V to 36 V, FPWM Mode	4.91	5	5.06	V
V_{FB}	Initial reference voltage accuracy for adjustable (1 V FB) versions	V_{IN} = 3.0 V to 36 V, FPWM Mode	0.99	1	1.01	V
R_{FB}	Resistance from FB to AGND	5 V Fixed Option		1.8		MΩ
		4 V Fixed Option		2.1		
		3.3 V Fixed Option		2.2		
I_{FB}	Input current from FB to AGND	Adjustable versions only, V_{FB} = 1 V			50	nA
CURRENT LIMITS						
I_{SC_6}	Short circuit high-side current Limit	6 A Variant, Duty cycle approaches 0%	8	10.35	12.6	A
$I_{LS\text{-}LIMIT_6}$	Low-side current limit		5.7	6.9	8.1	A
$I_{PEAK\text{-}MIN_6}$	Minimum Peak Inductor Current			1.2		A
$I_{L\text{-}NEG_6}$	Negative current limit		-4.9	-3.8	-2.4	A
I_{SC_8}	Short circuit high-side current Limit	8 A Variant, Duty cycle approaches 0%	11.5	13.8	15.6	A
$I_{LS\text{-}LIMIT_8}$	Low-side current limit		8	9.2	10.4	A
$I_{PEAK\text{-}MIN_8}$	Minimum Peak Inductor Current			1.6		A
$I_{L\text{-}NEG_8}$	Negative current limit		-6.4	-5.3	-3.9	A
I_{SC_10}	Short circuit high-side current Limit	10 A Variant, Duty cycle approaches 0%	14	17.3	20	A
$I_{LS\text{-}LIMIT_10}$	Low-side current limit		9.8	11.5	12.9	A
$I_{PEAK\text{-}MIN_10}$	Minimum Peak Inductor Current			1.8		A
$I_{L\text{-}NEG_10}$	Negative current limit		-6.6	-5.3	-4	A
$I_{L\text{-}ZC}$	Zero-cross current limit. Positive current direction is out of SW pin.	Auto Mode, static measurement	10		200	mA
V_{HICCUP}	Hiccup threshold on FB pin		0.36	0.4	0.44	V
POWER GOOD (/RESET PIN)						
$V_{\overline{RESET}\text{-}OV}$	$\overline{RESET}$ upper threshold - Rising	% of FB voltage	110	112	114	%
$V_{\overline{RESET}\text{-}UV}$	$\overline{RESET}$ lower threshold - Falling	% of FB voltage	92	94	96.5	%
$V_{\overline{RESET}_GUARD}$	$\overline{RESET}$ UV threshold as percentage of steady state output voltage with output voltage and UV threshold, falling, read at the same T_J, and V_{IN}.	Falling			97	%
$V_{\overline{RESET}\text{-}HYS\text{-}FALLING}$	$\overline{RESET}$ fallling threshold hysteresis	% of FB voltage	0.5	1.3	2.5	%
$V_{\overline{RESET}\text{-}HYS\text{-}RISING}$	$\overline{RESET}$ rising threshold hysteresis	% of FB voltage	0.5	1.3	2.5	%
$V_{\overline{RESET}_VALID}$	Minimum input voltage for proper $\overline{RESET}$ function	Measured when $V_{\overline{RESET}}$ < 0.4 V with 10 kOhm pullup to external 5 V			1.2	V

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Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is output set point.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	$\overline{RESET}$ Low-level function output voltage	46.0 µA pull up to $\overline{RESET}$ pin, V_{IN} = 1.0 V, V_{EN} = 0 V			0.4	V
		1 mA pull up to $\overline{RESET}$ pin, V_{IN} = 13.5 V, V_{EN} = 0 V			0.4	
		2 mA pull up to $\overline{RESET}$ pin, V_{IN} = 13.5 V, V_{EN} = 3.3 V			0.4	
$R_{\overline{RESET}}$	$\overline{RESET}$ ON resistance,	V_{EN} = 5 V, 1mA pull up current		44	125	Ω
$R_{\overline{RESET}}$	$\overline{RESET}$ ON resistance,	V_{EN} = 0 V, 1mA pull up current		18	40	Ω
OSCILLATOR (SYNC/MODE PIN)						
V_{SYNCDL}	SYNC/MODE input voltage low		0.4			V
V_{SYNCDH}	SYNC/MODE input voltage high				1.7	V
V_{SYNCD_HYST}	SYNC/MODE input voltage hysteresis		0.185		1	V
R_{SYNC}	Internal pulldown resistor to ensure SYNC/MODE doesn't float			100		kΩ
HIGH SIDE DRIVE (CBOOT PIN)						
V_{CBOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turnoff high-side switch			1.9		V
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET on-resistance	Load = 1 A, $C_{BOOT-SW}$ = 3.2 V		21	39	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET on-resistance	Load = 1 A, $C_{BOOT-SW}$ = 3.2 V		13	25	mΩ

7.6 Timing Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LIMITS (SW PIN)						
t_{ON-MIN}	Minimum HS switch on-time	V_{IN} =18 V, $V_{SYNC/MODE}$ = 5 V, I_{OUT} = 2A, R_{BOOT} = 0 Ω		62	81	ns
$t_{OFF-MIN}$	Minimum HS switch off-time	V_{IN} = 5 V		70	103	ns
t_{ON-MAX}	Maximum switch on-time	HS timeout in dropout	6.9	8.9	11	µs
START UP						
t_{EN}	Turn-on delay	V_{IN} = 13.5 v, C_{VCC} = 1 µF, time from EN high to first SW pulse if output starts at 0 V		0.82	1.2	ms
t_{SS}	Time from first SW pulse to V_{REF} at 90%, of set point.		1.7	2.2	2.7	ms
t_W	Short circuit wait time ("hiccup" time)			40		ms
POWER GOOD (/RESET PIN) and OVERVOLTAGE PROTECTION						
t_{RESET_FILTER}	$\overline{RESET}$ edge deglitch delay		10	26	45	µs
t_{RESET_ACT}	$\overline{RESET}$ active time	Time FB must be valid before $\overline{RESET}$ is released.	1.2	2.1	3.75	ms
OSCILLATOR (SYNC/MODE PIN)						
t_{PULSE_H}	High duration needed to be recognized on SYNC/MODE pin		100			ns
t_{PULSE_L}	Low duration needed to be recognized on SYNC/MODE pin		100			ns
t_{MSYNC}	Time at one level needed to indicate FPWM or Auto Mode		7		20	µs

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Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LOCK}	Time needed for clock to lock to a valid synchronization signal	RT = 39.2 kΩ		4.3		ms

7.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR (RT and SYNC PINS)						
f_{OSC}	Internal oscillator frequency	RT = GND	1.90	2.2	2.42	MHz
f_{OSC}	Internal oscillator frequency	RT = VCC	350	400	440	kHz
$f_{FIXED_2.2MHz}$	Oscillator frequency measured using maximum value of RT resistor to select 2.2 MHz	RT = 6.81 kΩ	1.95	2.2	2.42	MHz
$f_{FIXED_0.4MHz}$	Oscillator frequency measured using minimum value of RT resistor to select 0.4 MHz	RT = 40.2 kΩ	352	400	448	kHz
f_{ADJ}	Center Trim oscillator frequency	RT = 22.6 kΩ	630	700	770	kHz
SPREAD SPECTRUM						
Δ Fc+	Frequency increase of internal oscillator from spread spectrum		1	4	7.5	%
Δ Fc-	Frequency decrease of internal oscillator from spread spectrum		-8	-4	-1	%
SWITCH NODE						
D_{MAX}	Maximum switch duty cycle	While in frequency fold-back	98			%
		fsw =1.85 MHz		87		

7.8 System Characteristics

The following specifications apply only to the typical application circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{VIN_MIN1}	Input voltage for full functionality at reduced load, after start-up.				3	V
V_{VIN_MIN2}	Input voltage for full functionality at 100% of maximum rated load, after start-up.	V_{OUT} set to 3.3 V			3.95	V
I_{Q_VIN}	Input current to V_{IN} node of DC/DC for fixed V_{OUT} versions	V_{IN} = 13.5 V, V_{OUT} = 3.3 V fixed, I_{OUT} = 0 A, Auto mode		5		µA
		V_{IN} = 13.5 V, V_{OUT} = 5 V fixed, I_{OUT} = 0 A, Auto mode		8		
VOLTAGE REFERENCE (FB PIN)						
$V_{OUT_5V_ACC}$	V_{OUT} = 5 V, V_{IN} = 6 V to 36 V, I_{OUT} = 1 A to full load (1)	V_{IN} = 6 V to 36 V , PWM Operation	-1.5		1.5	%
	V_{OUT} = 5 V, V_{IN} = 6 V to 36 V, I_{OUT} = 0 A to full load (1)	V_{IN} = 6 V to 36 V, PFM and PWM operation	-1.5		2.5	
$V_{OUT_3r3V_ACC}$	V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 1 A to full load (1)	V_{IN} = 3.8 V to 36 V , PWM Operation	-1.5		1.5	%
	V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 0 A to full load (1)	V_{IN} = 3.8 V to 36 V, PFM and PWM operation	-1.5		2.5	
THERMAL SHUTDOWN						

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The following specifications apply only to the typical application circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_R}	Thermal shutdown tripping threshold		158	168	180	ºC
T_{SD_F}	Thermal shutdown recovery threshold		150	159		ºC
OTHER PARAMATERS						
V_{DROP1}	Input to output voltage differential to maintain regulation accuracy, without inductor DCR drop		0.45			V
V_{DROP2}	Input to output voltage differential to maintain $f_{SW} \geqslant$ 1.85 MHz, without inductor DCR drop		1.2			V
η	Typical 2.2MHz Efficiency	V_{IN} =13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 5 A, R_{RBOOT} = 0 Ω		92.6		%
	Typical 400 kHz Efficiency	V_{IN} = 13.5 V, Vout = 5.0 V, I_{OUT} = 8 A, R_{RBOOT} = 0 Ω		95.1		
	Typical 250 kHz Efficiency	V_{IN} = 13.5 V, Vout = 5.0 V, I_{OUT} = 10 A, R_{RBOOT} = 0 Ω		93.7		

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7.9 Typical Characteristics

Unless otherwise specified, V_{IN} = 13.5 V.

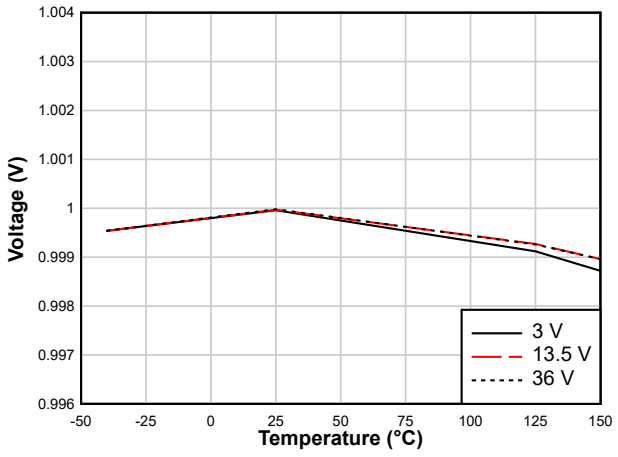


图 7-1. Feedback Voltage

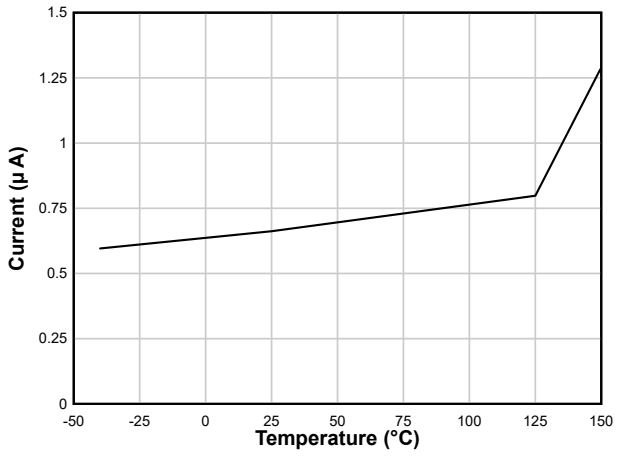


图 7-2. Shutdown Supply Current

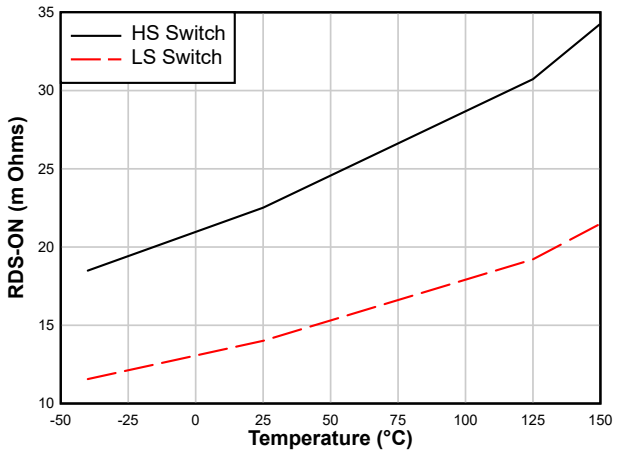


图 7-3. High-side and Low-side Switches R_{DS_ON}

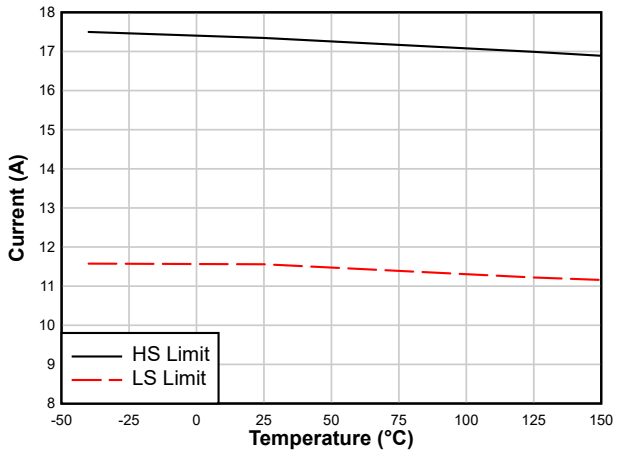


图 7-4. High-side and Low-side Current Limits

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8 Detailed Description

8.1 Overview

The LM6x4xx-Q1 is a wide-input and output-voltage range, low-quiescent current, high-performance regulator that operates over a wide range of frequencies and conversion ratios. If the minimum on-time or minimum off-time does not support the desired conversion ratio, the frequency is reduced. This action automatically allows regulation to be maintained during load dump and with very low dropout during cranking.

This device is designed to minimize end-product cost and size while operating in demanding automotive and high-performance industrial environments. The LM6x4xx-Q1 can be set to operate at fixed 400 kHz, fixed 2.2 MHz, or is adjustable from 200 kHz to 2.2 MHz using the RT pin. Internal compensation and an accurate current limit scheme minimizes BOM cost and component count. In addition, the $\overline{\text{RESET}}$ output feature with built-in delayed release and low-current light-load mode lets the user eliminate a backup LDO and reset chip in many applications.

The LM6x4xx-Q1 has been designed for low EMI. The device includes the following:

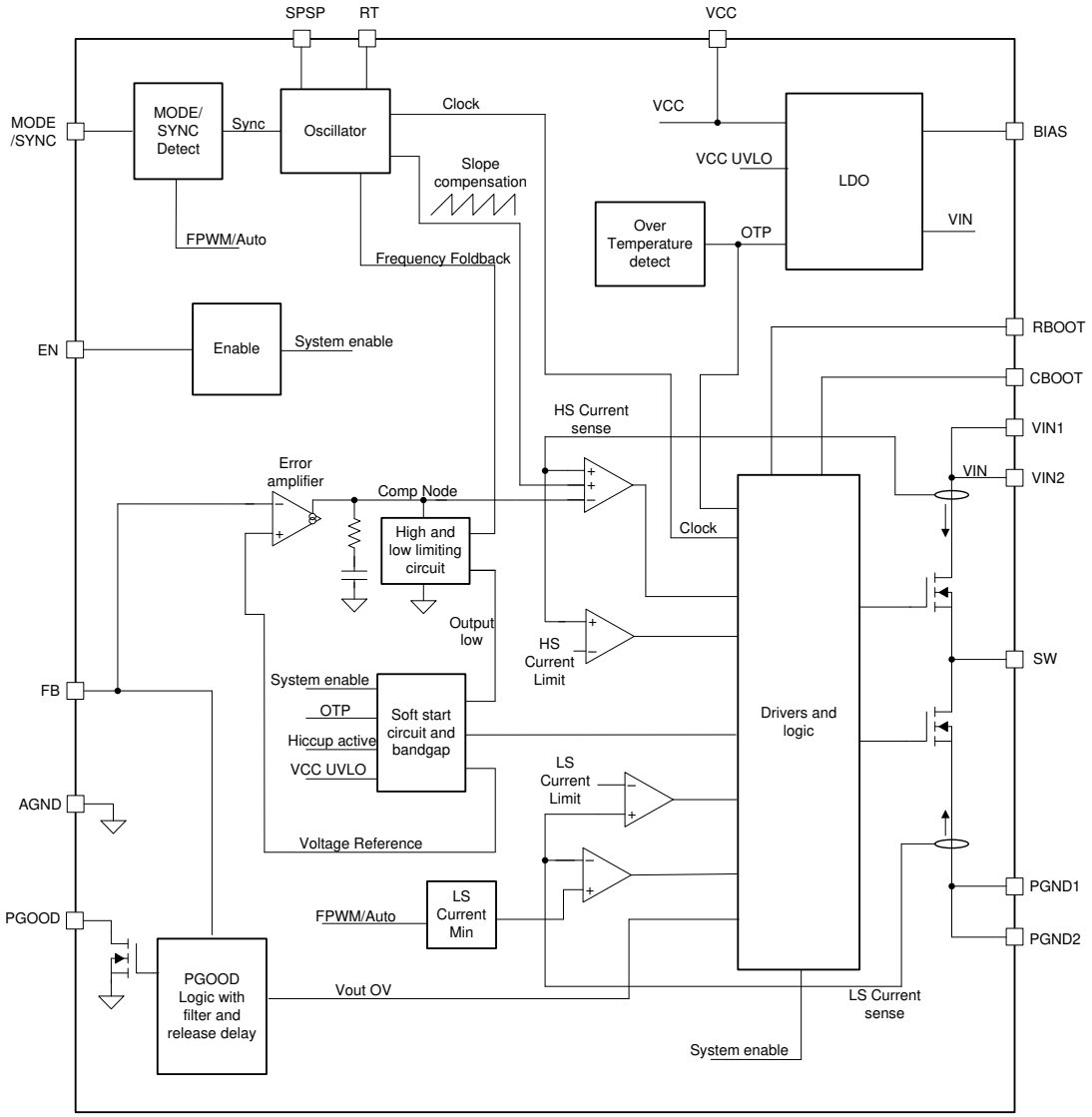
- Adjustable switch node rising slew rate
- Pin-configurable spread spectrum
- Low input inductance package
- Operation over a frequency range above and below AM radio band

Together, these features can eliminate shielding and other expensive EMI mitigation measures.

To use the device in reliability-conscious environments, the LM6x4xx-Q1 has a package with enlarged corner terminals for improved BLR and wettable flanks, allowing optical inspection.

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8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Output Voltage Selection

A voltage divider between output voltage and the FB pin is used to adjust output voltage. See 图 8-1.

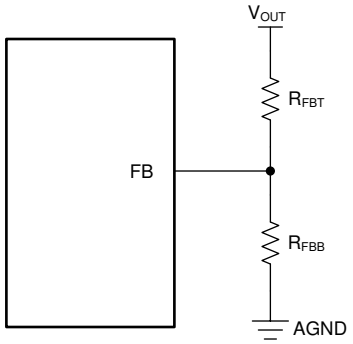


图 8-1. Setting Output Voltage of Adjustable Versions

The LM6x4xx-Q1 uses a 1-V reference for control to derive 方程式 1. This equation can be used to determine R_{FBB} for a desired output voltage and a given R_{FBT}. Usually, R_{FBT} is limited to a maximum value of 100 kΩ to prevent shifting due to PCB leakage under harsh conditions. A larger resistance of up to 1 MΩ can be used to improve light load efficiency in cleaner environments, or the fixed output voltage options under harsher conditions.

$$R_{FBB} = \frac{R_{FBT}}{V_{OUT} - 1} \quad (1)$$

In addition, a feedforward capacitor C_{FF} can be used to optimize the transient response.

8.3.2 Enable EN Pin and Use as V_{IN} UVLO

Apply a voltage less than 0.4 V to the EN pin to put the device into shutdown mode. In shutdown mode, the quiescent current drops to 0.66 µA (typical). Above this voltage but below the LM6x4xx-Q1 lower EN threshold, VCC is active but the SW node remains inactive. Once EN is above V_{EN}, the chip operates normally as long as input voltage is above the minimum operating voltage.

The EN terminal cannot be left floating. The simplest way to enable the operation is to connect the EN pin to VIN. This action allows the self-start-up of the device when VIN drives the internal VCC above its UVLO level. However, many applications benefit from employing an enable divider string, which establishes a precision input undervoltage lockout (UVLO). The precision UVLO can be used for the following:

- Sequencing
- Preventing the device from retriggering when used with long input cables
- Reducing the occurrence of deep discharge of a battery power source

Note that EN thresholds are accurate. The rising enable threshold has 8.1% tolerance. Hysteresis is enough to prevent retriggering upon shutdown of the load (approximately 25%). The external logic output of another IC can also be used to drive the EN terminal, allowing system power sequencing.

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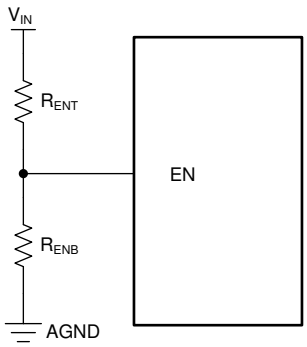


图 8-2. VIN UVLO Using the EN Pin

Resistor values can be calculated using 方程式 2:

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot (1 - V_{EN\text{-}HYST}) \quad (2)$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

8.3.3 SYNC/MODE Uses for Synchronization

The LM6x4xx-Q1 SYNC/MODE pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by coupling a positive edge into the SYNC/MODE pin. The coupled edge voltage at the SYNC/MODE pin must exceed the SYNC amplitude threshold of V_{SYNCDH} to trip the internal synchronization pulse detector. The minimum SYNC rising pulse and falling pulse durations must be longer than t_{PULSE_H} and t_{PULSE_L} respectively. The LM6x4xx-Q1 switching action can be synchronized to an external clock from 200 kHz to 2.2 MHz.

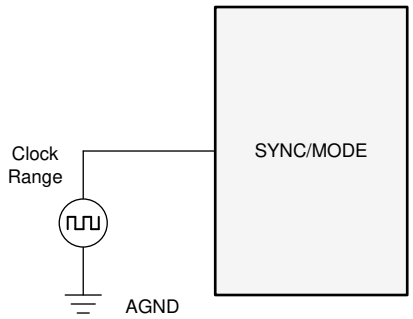
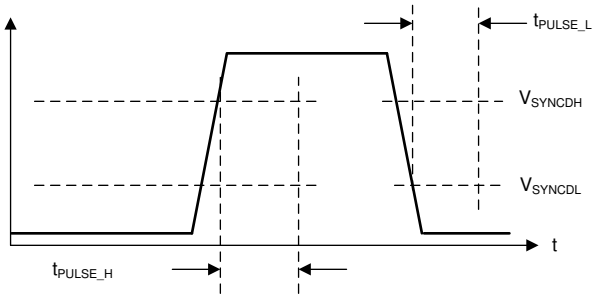


图 8-3. Typical Implementation Allowing Synchronization Using the SYNC/MODE Pin

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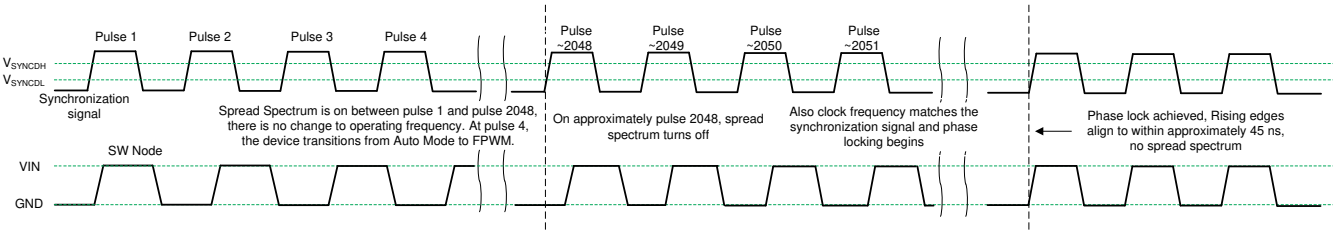


This image shows the conditions needed for detection of a synchronization signal.

图 8-4. Typical SYNC/MODE Waveform

8.3.4 Clock Locking

Once a valid synchronization signal is detected, a clock locking procedure is initiated. After approximately 2048 pulses, the clock frequency abruptly changes to the frequency of the synchronization signal. While the frequency adjusts suddenly, phase is maintained so the clock cycle lying between operation at the default and synchronization frequencies is of intermediate length. There are no very long or very short pulses. Once frequency is adjusted, phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising the SW node pulses. See 图 8-5.



At pulse 4, the synchronization signal is detected. After approximately pulse 2048, it is ready to synchronize and the frequency is adjusted using a glitch-free technique. Later, phase is locked.

图 8-5. Synchronization Process

8.3.5 Adjustable Switching Frequency

The RT pin is configurable. This pin can be tied to VCC for 400-kHz operation, grounded for 2.2-MHz operation, or a resistor to AGND can be used to set an adjustable operating frequency. See 图 8-6 for resistor values. Note that if a resistor value falls outside of the recommended range, it can cause the LM6x4xx-Q1 to revert to 400 kHz or 2.2 MHz. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, see the SYNC/MODE pin in 节 8.3.3.

$$R_T\ (k\Omega) = (16.4 / f_{SW\ (MHz)}) - 0.633 \quad (3)$$

For example, for f_{SW} = 400 kHz, R_T = (16.4 / 0.4) - 0.633 = 40.37, so a 40.2-kΩ resistor is selected as the closest choice.

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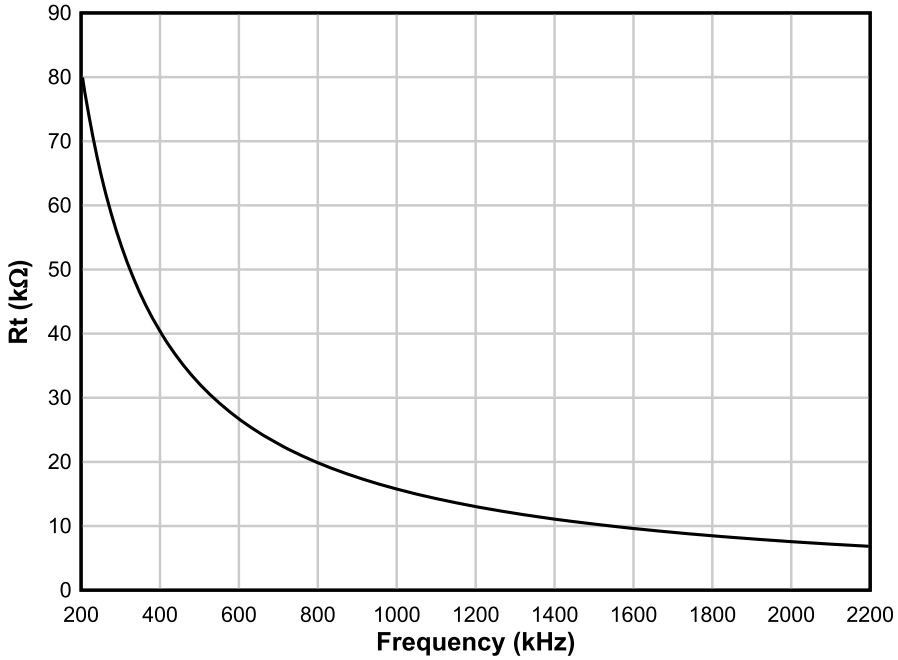


图 8-6. Setting Clock Frequency

8.3.6 $\overline{\text{RESET}}$ Output Operation

While the $\overline{\text{RESET}}$ function of the LM6x4xx-Q1 resembles a standard power-good function, the functionality is designed to replace a discrete reset IC, reducing BOM cost. There are three major differences between the reset function and the normal power-good function seen in most regulators:

- A delay has been added for release of reset. See 表 8-1.
- $\overline{\text{RESET}}$ output signals a fault (pulls its output to ground) while the part is disabled.
- $\overline{\text{RESET}}$ continues to operate with input voltage as low as 1.2 V. Below this input voltage, $\overline{\text{RESET}}$ output can be high impedance.

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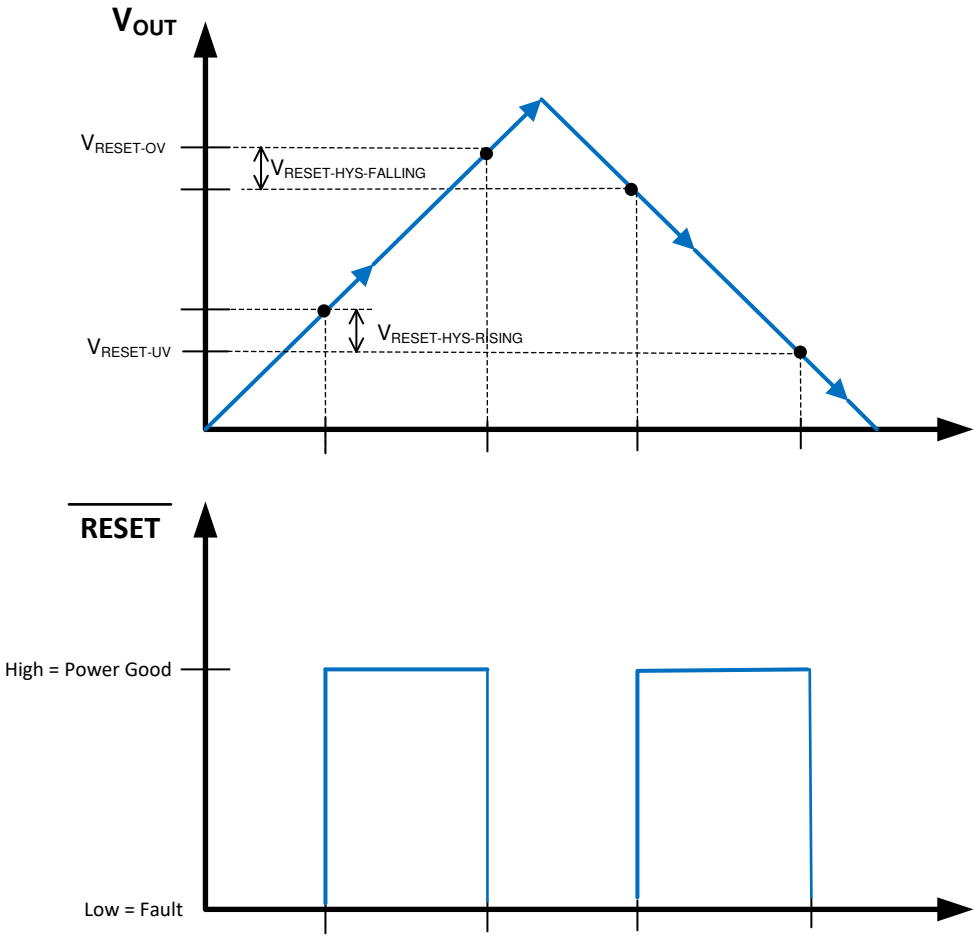


图 8-7. $\overline{\text{RESET}}$ Static Voltage Thresholds

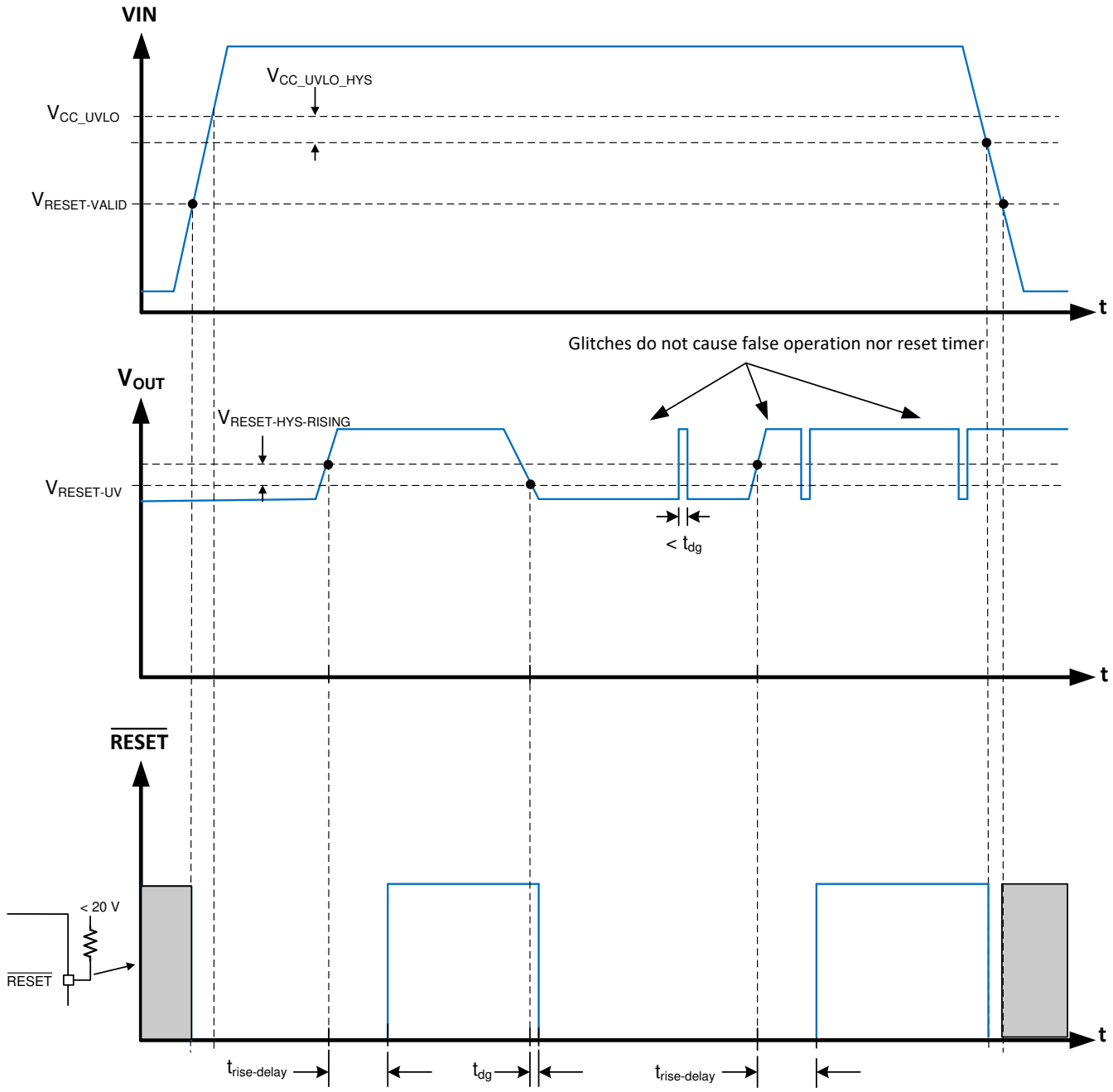


图 8-8. $\overline{\text{RESET}}$ Timing Diagram (Excludes OV Events)

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表 8-1. Conditions that Cause $\overline{\text{RESET}}$ to Signal a Fault (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{RESET_ACT} MUST PASS BEFORE RESET OUTPUT IS RELEASED)
FB below V_{RESET_UV} for longer than t_{RESET_FILTER}	FB above V_{RESET_UV} + V_{RESET_HYST} for longer than t_{RESET_FILTER}
FB above V_{RESET_OV} for longer than t_{RESET_FILTER}	FB below V_{RESET_OV} - V_{RESET_HYST} for longer than t_{RESET_FILTER}
Junction temperature exceeds T_{SD_R}	Junction temperature falls below T_{SD_F} (1)
EN low	t_{EN} passes after EN becomes high(1)
VIN falls low enough so that VCC falls below V_{CC_UVLO} - $V_{CC_UVLO_HYST}$. This value is called $V_{IN_OPERATE}$.	Voltage on VIN is high enough so that VCC pin exceed V_{CC_UVLO} (1)

(1) As an additional operational check, $\overline{\text{RESET}}$ remains low during soft start. It is defined as until the lesser of either full output voltage reached or t_{SS2} has passed since initiation. This is true even if all other conditions in this table are met and t_{RESET_ACT} has passed. Lockout during soft start does not require t_{RESET_ACT} to pass before $\overline{\text{RESET}}$ is released.

The threshold voltage for the $\overline{\text{RESET}}$ function is specified to take advantage of the availability of the LM6x4xx-Q1 internal feedback threshold to the $\overline{\text{RESET}}$ circuit. This allows a maximum threshold of 96.5% of selected output voltage to be specified at the same time as 96% of actual operating point. The net result is a more accurate reset function while expanding the system allowance for transient response. See the output voltage error stack-up comparison in 图 8-9.

In addition to signaling a fault upon overvoltage detection (FB above V_{RESET_OV}), the switch node is shut down and a small, approximately 1-mA pulldown is applied to the SW node.

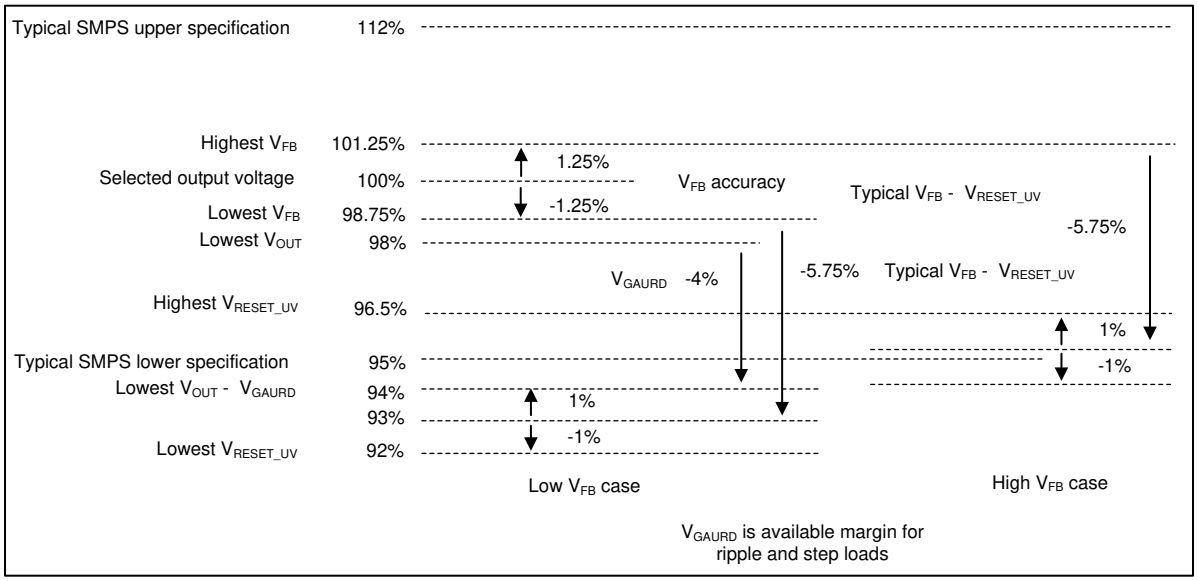


图 8-9. Reset Threshold Voltage Stack-up

8.3.7 Internal LDO, VCC UVLO, and BIAS Input

The LM6x4xx-Q1 uses VCC as its internal power supply. VCC is, in turn, powered from VIN or BIAS. Once the LM6x4xx-Q1 is active, power comes from VIN if BIAS is less than approximately 3.1 V. Power comes from BIAS if BIAS is more than 3.1 V. VCC is typically 3 V to 3.3 V under most conditions, but can be lower if VIN is very low. To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low. See V_{CC_UVLO} and $V_{CC_UVLO_HYST}$ in 节 7.5. During start-up, VCC momentarily exceeds its normal operating voltage until V_{CC_UVLO} is exceeded, then drops to its normal operating voltage. These UVLO values, when combined with the dropout of the LDO when only powering the LM6x4xx-Q1, are used to derive minimum $V_{IN_OPERATE}$ and $V_{IN_OP_H}$.

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8.3.8 Bootstrap Voltage and $V_{CBOOT-UVLO}$ (CBOOT Pin)

The driver of the power switch (HS switch) requires bias higher than VIN when the HS switch is ON. The capacitor connected between CBOOT and SW works as a charge pump to boost voltage on the CBOOT terminal to (SW + VCC). The boot diode is integrated on the LM6x4xx-Q1 die to minimize the physical solution size. TI recommends a 100-nF capacitor rated for 10 V with X7R or better dielectric for the CBOOT capacitor. The boot (CBOOT) rail has a UVLO to protect the chip from operation with too little bias. This UVLO has a threshold of V_{BOOT_UVLO} and is typically 2.1 V. If the CBOOT capacitor voltage drops below V_{BOOT_UVLO}, then the device initiates a charging sequence using the low-side FET before attempting to turn on the high-side device.

8.3.9 Adjustable SW Node Slew Rate

To allow optimization of EMI with respect to efficiency, the LM6x4xx-Q1 is designed to allow a resistor to select the strength of the high-side FET driver during turn-on. See 图 8-10. The current drawn through the RBOOT pin (the dotted loop) is magnified and drawn through from CBOOT (the dashed line). This current is used to turn on the high-side power MOSEFT.

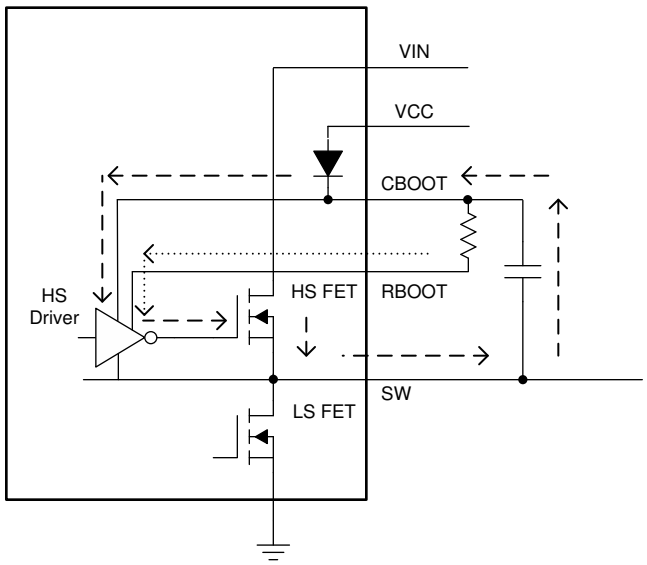


图 8-10. Simplified Circuit Showing How RBOOT Functions

Rise time is rapid with RBOOT short circuited to CBOOT. In this condition SW node harmonics roll off at -20 dBµV per decade until around 150 MHz where the harmonics begin rolling off at -40 dBµV per decade. Slowing the rise time decreases the frequency where this transition occurs which provides more rolloff in the higher frequencies which provides more margin on EMI scans. If CBOOT and RBOOT are connected through 700 Ω, slew time due to high-side turnon is limited to no more than 13 ns. 10 ns is typical when converting 13.5 V to 5 V. This slow rise time allows energy in SW node harmonics to roll off near 50 MHz under most conditions. Rolling off harmonics eliminates the need for shielding and common mode chokes in many applications. Note that rise time increases with increasing input voltage. Noise due to stored charge is also greatly reduced with higher RBOOT resistance. Switching with a slower slew rate decreases efficiency. Take care to optimize the resistance to provide the best EMI while not generating too much heat. If RBOOT is left open, rise time is set to its maximum value.

8.3.10 Spread Spectrum

Spread spectrum is configurable using the SPSP pin. Spread spectrum eliminates peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The LM6x4xx-Q1 implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LM6x4xx-Q1 uses a ±4% (typical)

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spread of frequencies which can spread energy smoothly across the FM and TV bands. The device implements Dual Random Spread Spectrum (DRSS). DRSS is a combination of a triangular frequency spreading pattern and pseudorandom frequency hopping. The combination allows the spread spectrum to be very effective at spreading the energy at the following:

- Fundamental switching harmonic with slow triangular pattern
- High frequency harmonics with additional psuedorandom jumps at the switching frequency

The advantage of DRSS is its equivalent harmonic attenuation in the upper frequencies with a smaller fundamental frequency deviation. This reduces the amount of input current and output voltage ripple that is introduced at the modulating frequency. Additionally, the LM6x4xx-Q1 also allows you to further reduce the output voltage ripple caused by the spread spectrum modulating pattern. With the SPSP pin grounded, the spread spectrum is disabled. With the SPSP pin tied to VCC, the spread spectrum is on. With the SPSP pin tied through a resistor to ground, the spread spectrum is on. Also, a modulating tone correction is applied to the switcher to reduce the output voltage ripple caused by the frequency modulation. The resistor is usually around 20 kΩ, and can be more precisely calculated using 方程式 4.

$$R_{SPSP}\ (k\Omega) = \frac{14.17 \times \frac{V_{IN}}{V_{OUT}}}{\frac{V_{IN} - V_{OUT}}{I_{RATED} \times L \times f_{SW}} + 1.22} \quad (4)$$

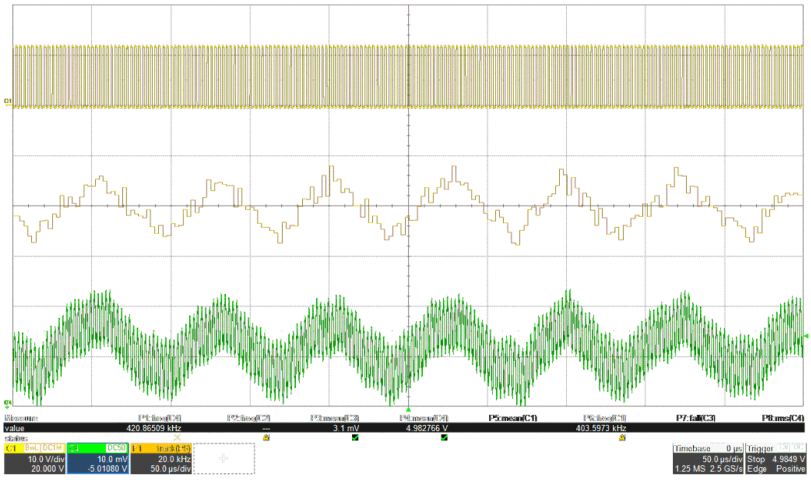


图 8-11. Output Ripple Without Ripple Cancellation Showing V_{SW} (top), F_{SW} (middle), V_{OUT} (bottom)

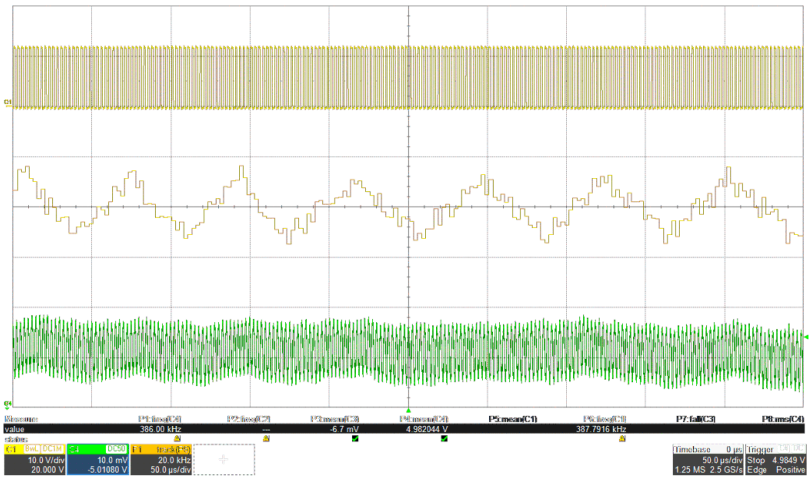


图 8-12. Output Ripple with Ripple Cancellation Showing V_{SW} (top), F_{SW} (middle), V_{OUT} (bottom)

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The spread spectrum is only available while the clock of the LM6x4xx-Q1 are free running at their natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed due to operation at low input voltage. This is operation in dropout.
- The clock is slowed under light load in auto mode. This is normally not seen above 750-mA load. Note that if the device is operating in FPWM mode, spread spectrum is active, even if there is no load.
- The clock is slowed due to high input-to-output voltage ratio. This mode of operation is expected if on-time reaches minimum on-time. See the *Timing Characteristics*.
- The clock is synchronized with an external clock.

8.3.11 Soft Start and Recovery From Dropout

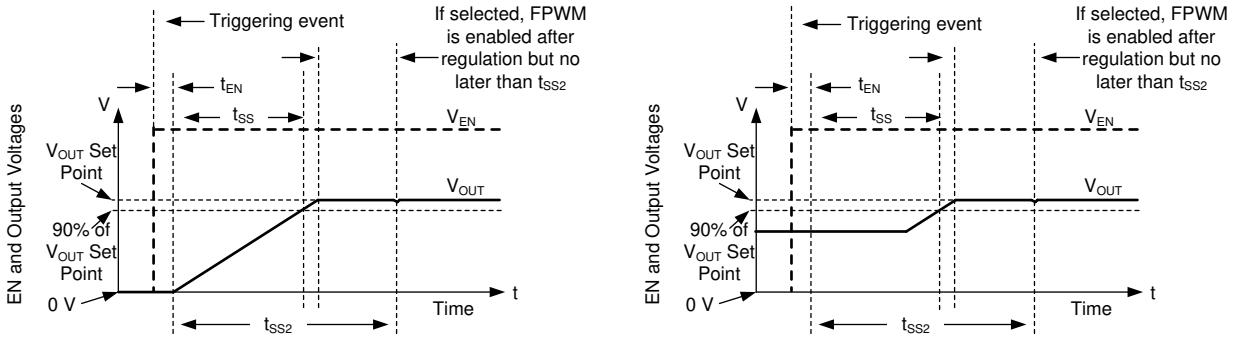
When designing with the LM6x4xx-Q1, slowed rise in output voltage due to recovery from dropout and soft start must be considered separate phenomena. Soft start is triggered by any of the following conditions:

- EN is used to turn on the device.
- Recovery from a hiccup waiting period; see 节 8.3.13.
- Recovery from shutdown due to overtemperature protection
- Power is applied to the VIN of the IC or the VCC UVLO is released.

Once soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped from zero. The net result is that output voltage, if previously 0 V, takes t_{SS} to reach 90% of its desired value.
- Operating mode is set to auto, activating diode emulation. This allows start-up without pulling output low if there is a voltage already present on the output.
- Hiccup is disabled for the duration of soft start; see 节 8.3.13.

All of these actions together provide start-up with limited inrush currents. They also allow the use of output capacitors and loading conditions that cause current to border on current limit during start-up without triggering hiccup. In addition, if output voltage is already present, output is not pulled down. See 图 8-13.



The left curves show soft start from 0 V. The right curves show soft starting behavior from a pre-biased or non-zero voltage. In either case, the output voltage reaches within 10% of the desired setpoint t_{SS} time after soft start is initiated. During soft start, FPWM and hiccup are disabled. Both hiccup and FPWM are enabled once output reaches regulation or t_{SS2}, whichever happens first.

图 8-13. Soft-Start Operation

Any time output voltage is more than a few percent low for any reason, output voltage ramps up slowly. This condition, called recovery from dropout, differs from soft start in three important ways:

- Hiccup is allowed only if output voltage is less than 0.4 times its set point. Note that during dropout regulation itself, hiccup is inhibited. See 节 8.3.13.

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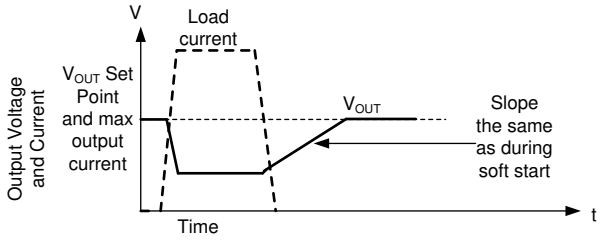
- FPWM mode is allowed during recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the LM6x4xx-Q1 can pull down on the output. Note that all the protections that are present during normal operation are in place, protecting the device if output is shorted to a high voltage or ground.
- The reference voltage is set to approximately 1% above that needed to achieve the current output voltage. It is not started from zero.

Despite the name, recovery from dropout is active whenever output voltage is more than a few percent lower than the setpoint for long enough that:

- Duty factor is controlled by minimum on-time or
- When the part is operating in current limit.

This primarily occurs under the following conditions:

- Dropout: When there is insufficient input voltage for the desired output voltage to be generated. See 节 8.4.3.5.
- Overcurrent that is not severe enough to trigger hiccup or if the duration is too short to trigger hiccup. See 节 8.3.13.



Whether output voltage falls due to high load or low input voltage, once the condition that causes output to fall below its setpoint is removed, output climbs at the same speed as during start-up. Even though hiccup does not trigger due to dropout, it can, in principal, be triggered during recovery if output voltage is below 0.4 times output the setpoint for more than 128 clock cycles during recovery.

图 8-14. Recovery From Dropout

8.3.12 Overcurrent and Short Circuit Protection

The LM6x4xx-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to the minimum of a fixed current setpoint, or the output of the voltage regulation loop minus slope compensation, every switching cycle. Since the voltage loop has a maximum value and slope compensation increases with duty cycle, the HS current limit decreases with increased duty cycle if duty cycle is above 35%. See 图 8-15.

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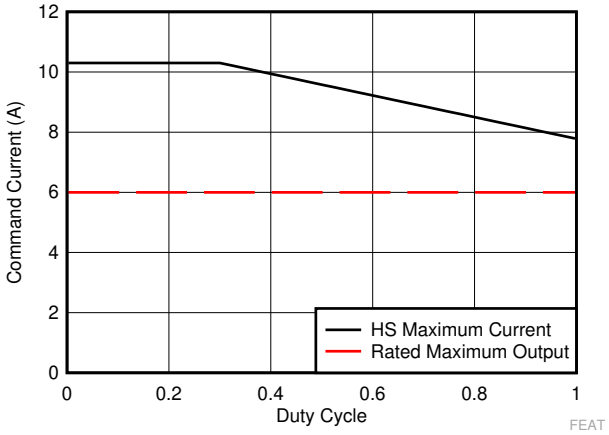


图 8-15. Maximum Current Allowed Through the HS FET - Function of Duty Cycle for LM62460-Q1

When the LS switch is turned on, the current going through it is also sensed and monitored. Like the high-side device, the low-side device turn-off is commanded by the voltage control loop. For a low-side device, turn-off is prevented if current exceeds this value, even if the oscillator normally starts a new switching cycle. See 节 8.4.3.4. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This is called the low-side current limit; see the *Electrical Characteristics* for values. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not turned on. The LS switch is turned off once the LS current falls below its limit. The HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

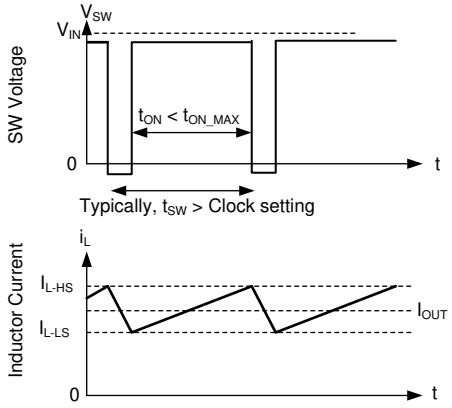
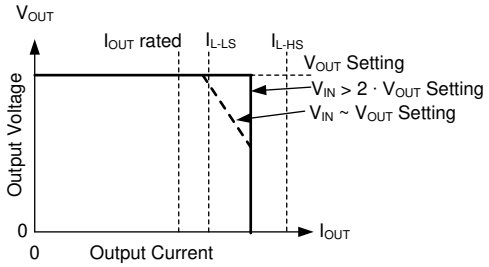


图 8-16. Current Limit Waveforms

The net effect of the operation of high-side and low-side current limit is that the IC operates in hysteretic control. Since the current waveform assumes values between I_{L-HS} and I_{L-LS}, output current is close to the average of these two values unless duty cycle is very high. Once operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If duty cycle is very high, current ripple must be very low to prevent instability; see 节 9.2.2.3. Since current ripple is low, the part is able to deliver full current. The current delivered is very close to I_{L-LS}.

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Under most conditions, current is limited to the average of I_{L-HS} and I_{L-LS}, approximately 1.4 times the rated current. If input voltage is low, current can be limited to approximately I_{L-LS}. Current does not exceed the average of I_{L-HS} and I_{L-LS} as output drops to 0.4 times the output voltage setting. Below 0.4 times the output voltage setting, the peak current does not exceed the average of I_{L-HS} and I_{L-LS} and the hiccup mode activates, preventing excessive heating.

图 8-17. Output Voltage versus Output Current

Once the overload is removed, the device recovers as though in soft start; see 节 8.3.11. Note that hiccup can be triggered if output voltage drops below approximately 0.4 times the intended output voltage.

8.3.13 Hiccup

The LM6x4xx-Q1 employs hiccup overcurrent protection when all of the following conditions are met for 128 consecutive switching cycles:

- A time greater than t_{SS2} has passed since soft start has started; see 节 8.3.11.
- Output voltage is below approximately 0.4 times output setpoint.
- The part is not operating in dropout defined as having minimum off-time controlled by duty factor.

In hiccup mode, the device shuts itself down and attempts to soft start after t_W. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions and short circuits.

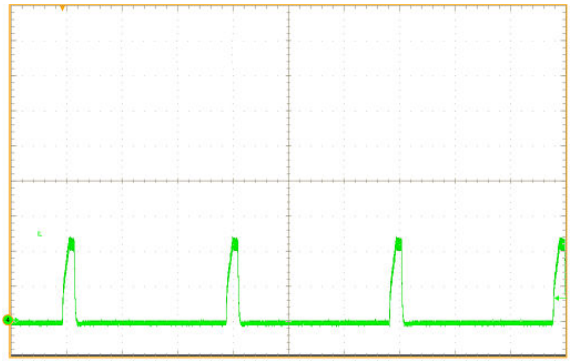


图 8-18. Inductor Current Bursts During Hiccup

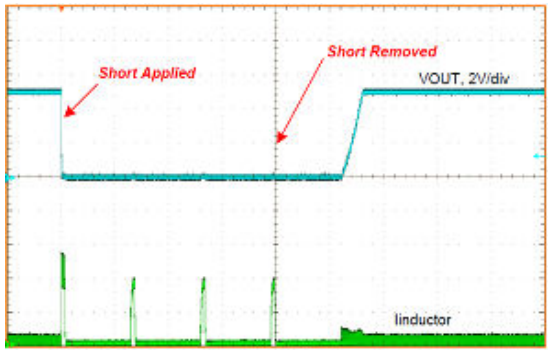


图 8-19. Short-Circuit Transient and Recovery

8.3.14 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the IC junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 159°C. When the junction temperature falls below 159°C (typical), the LM6x4xx-Q1 attempts to soft start.

While the LM6x4xx-Q1 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating from a short circuit applied to VCC, the LDO providing power to VCC has reduced

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current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical on and off control of the device. When the EN pin voltage is below 0.4 V, both the regulator and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 0.66 µA.

8.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the regulator. The internal LDO regulates the VCC voltage at 3.3 V, typically when:

- The EN pin voltage is above 1.1 V (maximum) and
- The EN pin voltage is below the precision enable threshold for the output voltage.

The precision enable circuitry is ON once VCC is above its UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on the EN terminal goes above its precision enable threshold. The LM6x4xx-Q1 also employs UVLO protection. If the VCC voltage is below its UVLO level, the output of the regulator is turned off.

8.4.3 Active Mode

The LM6x4xx-Q1 is in active mode when the following occurs:

- The EN pin is above V_{EN}.
- V_{IN} is above V_{EN}.
- V_{IN} is high enough to satisfy the V_{IN} minimum operating input voltage.
- No other fault conditions are present.

See 节 8.3 for protection features. The simplest way to enable the operation is to connect EN to VIN, allowing self-start-up when the applied input voltage exceeds the minimum $V_{IN_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the LM6x4xx-Q1 is in one of six sub-modes:

- Continuous conduction mode (CCM) with fixed switching frequency and peak current mode operation
- Discontinuous conduction mode (DCM) while in auto mode when the load current is lower than half of the inductor current ripple. If current continues to reduce, the device enters Pulse Frequency Modulation (PFM) which reduces the switch frequency to maintain regulation while reducing switching losses to achieve higher efficiency at light load.
- Minimum on-time operation while the on-time of the device needed for full-frequency operation at the requested low-duty cycle is not supported by T_{ON_MIN}
- Forced pulse width modulation (FPWM) similar to CCM with fixed-switching frequency, but extends the fixed frequency range of operation from full to no load
- Dropout mode when switching frequency is reduced to minimize dropout
- Recovery from dropout similar to other modes of operation except the output voltage setpoint is gradually moved up until the programmed setpoint is reached.

8.4.3.1 Peak Current Mode Operation

The following operating description of the LM6x4xx-Q1 refers to 节 8.2 and the waveforms in 图 8-20. Both supply a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW terminal voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, forcing V_{SW} to swing below ground by the voltage drop across the LS switch. The regulator loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period: $D = T_{ON} / (T_{ON} + T_{OFF})$.

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In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

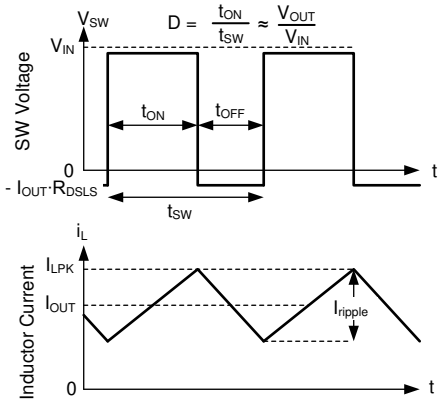


图 8-20. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

To get accurate DC load regulation, a voltage feedback loop is used. Peak and valley inductor currents are sensed for peak current mode control and current protection. The regulator operates with continuous conduction mode with constant switching frequency when load level is above one half of the minimum peak inductor current. The internally-compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

8.4.3.2 Auto Mode Operation

The LM6x4xx-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows a seamless transition between normal current mode operation while heavily loaded and in highly-efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the LM6x4xx-Q1 operates in depends on the SYNC/MODE pin. When SYNC/MODE is high, the part is in FPWM. When SYNC/MODE is low, the part is in PFM.

In auto mode, light-load operation is employed in the LM6x4xx-Q1 at load lower than approximately 1/10th of the rated maximum output current. Light-load operation employs two techniques to improve efficiency:

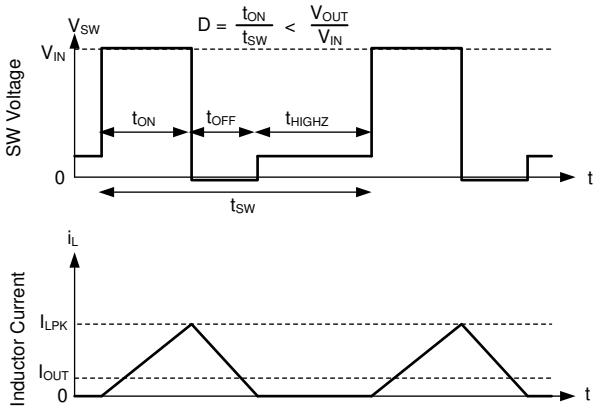
- Diode emulation, which allows DCM operation
- Frequency reduction

Note that while these two features operate together to create excellent light load behavior, they operate independently of each other.

8.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current though the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. Frequency will be reduced when peak inductor current goes below $I_{PEAK-MIN}$. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.

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In auto mode, the low-side device is turned off once inductor current is near zero. As a result, once output current is less than half of inductor ripple in CCM, the part operates in DCM. This is equivalent to saying that diode emulation is active.

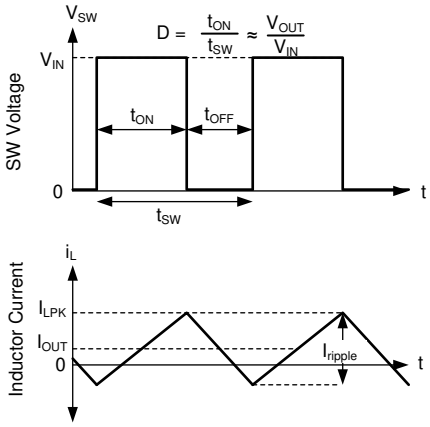
图 8-21. PFM Operation

The LM6x4xx-Q1 has a minimum peak inductor current setting in auto mode. That being said, when current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency . This mode of operation is called PFM mode regulation.

8.4.3.3 FPWM Mode Operation

Like auto mode operation, FPWM mode operation during light-load operation is selected using the SYNC/MODE pin.

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry. See the *Electrical Characteristics* for reverse current limit values.



FPWM mode Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of Iripple.

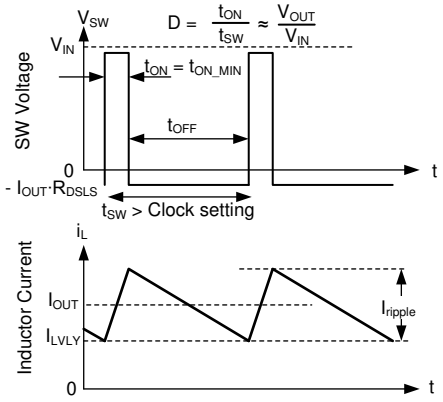
图 8-22. FPWM Mode Operation

In FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time, even while lightly loaded. This allows good behavior during faults which involves the output being pulled up.

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8.4.3.4 Minimum On-time (High Input Voltage) Operation

The LM6x4xx-Q1 continues to regulate output voltage. This is true even if the input-to-output voltage ratio requires an on-time less than the minimum on-time of the chip with a given clock setting. This is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If, for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If it is not operating in current limit, the maximum valley current is set above the peak inductor current. This prevents valley control from being used unless there is a failure to regulate using peak current only. If the input-voltage to output-voltage ratio is too high, even though current exceeds the peak value dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. See t_{ON_MIN} in the *Electrical Characteristics*. As a result, the compensation circuit reduces both peak and valley current. Once a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Since on-time is fixed at its minimum value, this type of operation resembles that of a device using a COT control scheme. See 图 8-23.



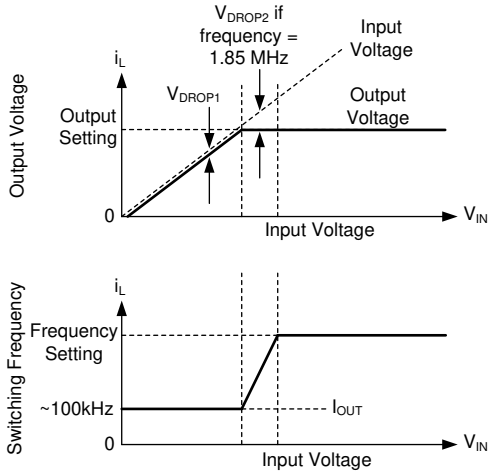
In valley control mode, the minimum inductor current is regulated, not peak inductor current.

图 8-23. Valley Current Mode Operation

8.4.3.5 Dropout

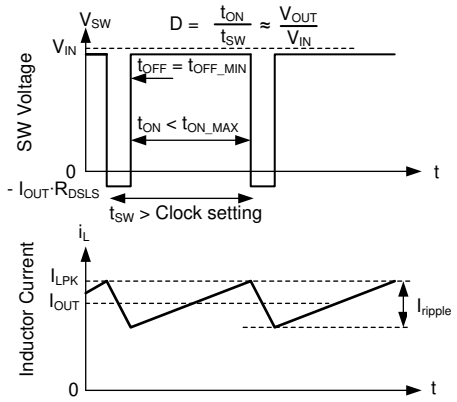
Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the needed duty factor. At a given clock frequency, duty factor is limited by minimum off-time. Once this limit is reached, if clock frequency is maintained, output voltage falls. Instead of allowing the output voltage to drop, the LM6x4xx-Q1 extends on-time past the end of the clock cycle until the required peak inductor current is achieved. The clock can start a new cycle once peak inductor current is achieved or once a pre-determined maximum on-time, t_{ON-MAX}, of approximately 9 µs passes. As a result, once the needed duty factor cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. If input voltage is low enough that the output voltage cannot be regulated even with an on-time of t_{ON_MAX}, output voltage drops to slightly below input voltage, V_{DROP1}. See 节 7.

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Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, output voltage tracks input voltage.

图 8-24. Frequency and Output Voltage in Dropout



This image shows the switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON_MAX}.

图 8-25. Dropout Waveforms

8.4.3.6 Recovery from Dropout

In some applications, input voltage can drop below the desired output voltage then recover to a higher value suddenly. With most regulators, the sudden increase in input voltage results in output voltage rising at a rate limited only by current limit until regulation is achieved. As input voltage reaches the desired output voltage, there is overshoot due to wind up in the control loop. This overshoot can be large in applications that have small output capacitors and light loads. Also, large inrush currents can cause large fluctuations on the input line once the regulator starts regulating the output voltage. This typically requires less current than during this initial inrush.

The LM6x4xx-Q1 greatly reduces inrush current and overshoot. This is done by engaging the soft-start circuit whenever the input voltage suddenly rises, after dipping low enough to cause the output voltage to droop. To prevent this feature from accidently engaging, output voltage must fall more than 1% to engage this feature. Also, this feature engages only if operating in dropout or current limit, preventing interference with normal transient response but allowing several percent overshoot while engaging. If output voltage is very close to its

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desired level, overshoot is reduced by inductor current not having time to rise to a high level before regulation starts.

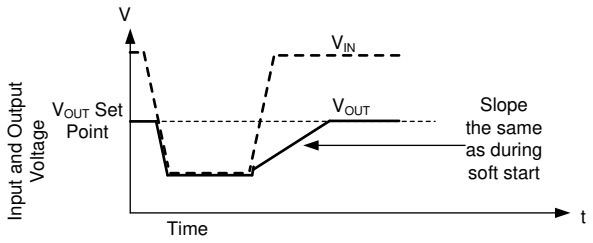


图 8-26. When Output Voltage Falls, It Recovers Slowly Preventing Overshoot and Large Inrush Currents

8.4.3.7 Other Fault Modes

Fault modes and their description can be found in 节 8.3 of this data sheet.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM6x4xx-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 10 A. If run at 400 kHz, 10 A can be sustained continuously. If run at 2.2 MHz, continuous current must be limited to 6 A if ambient temperature is 105°C. The following design procedure can be used to select components for the LM6x4xx-Q1.

9.2 Typical Application

图 9-1 shows a typical application circuit for the LM6x4xx-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, 表 9-2 provides typical component values for some of the most common configurations. The values given in the table are typical. Other values can be used to enhance certain performance criterion as required by the application. Note that for this QFN package, the input capacitors are split and placed on either side of the package. See 节 9.2.2.5 for more details.

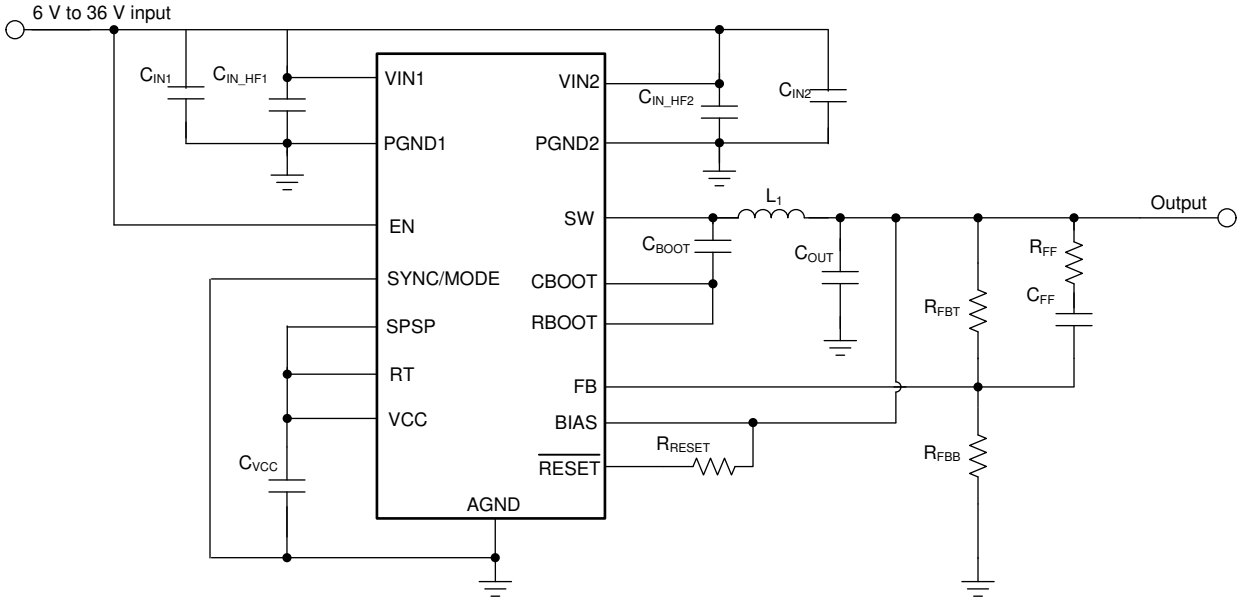


图 9-1. Example Application Circuit - 400-kHz Adjustable Output

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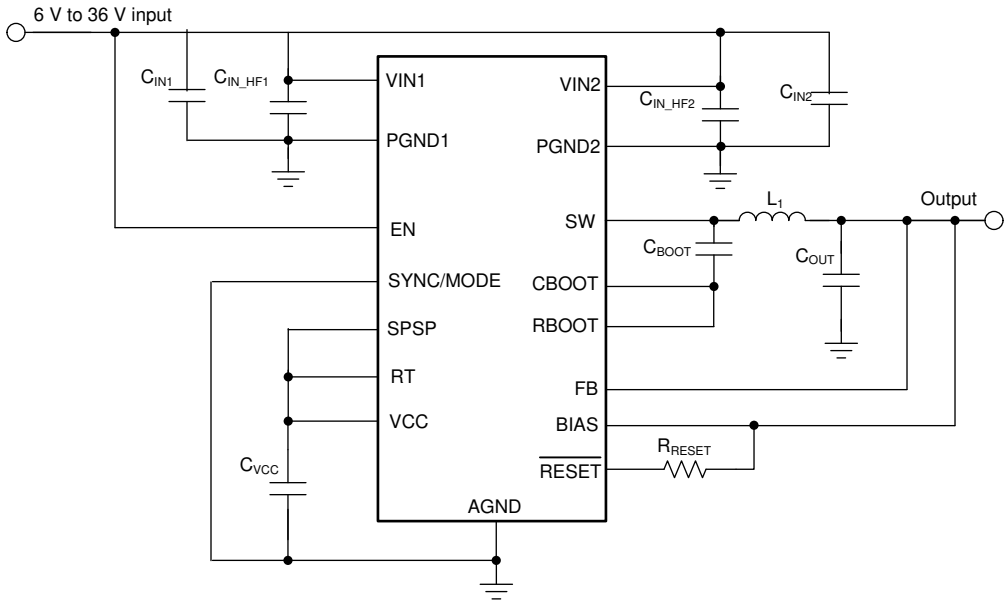


图 9-2. Example Application Circuit - 400-kHz Fixed Output

9.2.1 Design Requirements

表 9-1 provides the parameters for our detailed design procedure example:

表 9-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	13.5 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	10 A continuous
Switching frequency	400 kHz

表 9-2. Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	I_{OUT} (A)	L1 (µH)	C_{OUT} (RATED)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{IN} + C_{HF} (µF)	C_{BOOT} (µF)	R_{BOOT} (Ω)	C_{VCC} (µF)	C_{FF} (pF)	R_{FF} (kΩ)
400	5	10	2.7	5 × 22 µF ceramic or 2 x 22 µF + 15 mΩ 150 µF	100	24.9	2 x 10 + 2 x 0.47	0.1	0	1	10	4.99
400	5 Fixed Min BOM	10	2.7	2 × 47 µF ceramic	Short	Open	1 x 10 + 2 x 0.47	0.1	Short	1	Open	Open
400	3.3	10	2.2	3 × 47 µF ceramic or 3 x 22 µF + 15 mΩ 150 µF	100	43.2	2 x 10 + 2 x 0.47	0.1	0	1	10	4.99
400	3.3 Fixed Min BOM	10	2.2	3 × 47 µF ceramic	Short	Open	1 x 10 + 2 x 0.47	0.1	Short	1	Open	Open
2200	5	6	0.75	3 × 22 µF ceramic or 1 x 22 µF + 15 mΩ 150 µF	100	24.9	2 x 10 + 2 x 0.47	0.1	0	1	10	4.99
2200	5 Fixed Min BOM	6	0.75	2 × 33 µF ceramic	Short	Open	1 x 10 + 2 x 0.47	0.1	Short	1	Open	Open
2200	3.3	6	0.62	3 × 33 µF ceramic or 1 x 33 µF + 15 mΩ 150 µF	100	43.2	2 x 10 + 2 x 0.47	0.1	0	1	10	4.99

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表 9-2. Typical External Component Values (continued)

f_{SW} (kHz)	V_{OUT} (V)	I_{OUT} (A)	L1 (µH)	C_{OUT} (RATED)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{IN} + C_{HF} (µF)	C_{BOOT} (µF)	R_{BOOT} (Ω)	C_{VCC} (µF)	C_{FF} (pF)	R_{FF} (kΩ)
2200	3.3 Fixed Min BOM	6	0.62	2 × 47 µF ceramic	Short	Open	1 x 10 + 2 x 0.47	0.1	Short	1	Open	Open

9.2.2 Detailed Design Procedure

The following design procedure refers to 图 9-1 and 表 9-1.

9.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses, usually resulting in less power dissipated in the IC. Lower power dissipated in the IC results in higher system efficiency and a lower IC temperature. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. Many applications require that the AM band be avoided. These applications tend to operate at either 400 kHz below the AM band, or 2.2 MHz above the AM band. In this example, 400 kHz is chosen.

9.2.2.2 Setting the Output Voltage

The output voltage of the LM6x4xx-Q1 is externally adjustable using a resistor divider network. Two divider networks for two recommended output voltages are found in 表 9-2. The divider network is comprised of the top and bottom feedback resistors, R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{FB} = 1 V. The total resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Lower resistance values reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ with a maximum value of 1 MΩ. If 1 MΩ is selected for R_{FBT}, then a feedforward capacitor C_{FF} must be used across this resistor to provide adequate loop phase margin (see 节 9.2.2.9). Once R_{FBT} is selected, 方程式 1 is used to select R_{FBB}. For this 5-V example, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ.

9.2.2.3 Inductor Selection

The main parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current. It is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current for systems with a fixed input voltage. For systems with a variable input voltage such as the 12-V battery in a car, 25% is commonly used. This example uses V_{IN} = 13.5 V, which is closer to the nominal voltage of a 12-V car battery. When selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must still be used for this calculation. 方程式 5 can be used to determine the value of the inductance. The constant K is the percentage of peak-to-peak inductor current ripple to rated output current. For this 10-A, 400-kHz, 5-V example, K = 0.25 is chosen and an inductance of approximately 3.15 µH is found. The closest standard value of 3.0 µH was selected.

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \cdot K \cdot I_{OUT(MAX)}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{5}$$

Ideally, the saturation current rating of the inductor should be at least as large as the high-side switch current limit, I_{SC}. This ensures that the inductor does not saturate, even during a soft-short condition on the output. A hard short causes the LM6x4xx-Q1 to enter hiccup mode (see 节 8.3.13). A soft short can hold the output current at current limit without triggering hiccup. When the inductor core material saturates, the inductance can fall to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, $I_{LS-LIMIT}$, is

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designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This could lead to component damage, so it is crucial that the inductor does not saturate. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a soft saturation, allowing some relaxation in the saturation current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. To avoid subharmonic oscillation, the inductance value must not be less than that given in 方程式 6. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L > \frac{V_{OUT}}{f_{SW} * 0.6 * I_{RATED}} \quad (6)$$

9.2.2.4 Output Capacitor Selection

The output capacitor value and ESR determine the output voltage ripple and load transient performance. The output capacitor is usually limited by the load transient requirements rather than the output voltage ripple. 表 9-3 can be used to find capacitor values for C_{OUT} and C_{FF} for a few common applications. Note that 4.99-kΩ R_{FF} must be used in series with C_{FF}. In this example, good transient performance is desired, giving 4 x 47-µF ceramic + 220-µF electrolytic as the output capacitor and 15 pF as C_{FF}.

表 9-3. Selected Output Capacitor and C_{FF} Values

FREQUENCY	I_{OUT}	TRANSIENT PERFORMANCE	3.3-V OUTPUT		5-V OUTPUT	
			C_{OUT}	C_{FF}	C_{OUT}	C_{FF}
400 kHz	10 A	Minimum	6 x 22-µF ceramic	15 pF	5 x 22-µF ceramic	15 pF
400 kHz	10 A	Better Transient	6 x 22-µF ceramic + 220-µF electrolytic	15 pF	5 x 22-µF ceramic + 220-µF electrolytic	15 pF
2.2 MHz	6 A	Minimum	5 x 22-µF ceramic	15 pF	3 x 22-µF ceramic	15 pF
2.2 MHz	6 A	Better Transient	5 x 22-µF ceramic + 220-µF electrolytic	15 pF	3 x 22-µF ceramic + 220-µF electrolytic	15 pF

9.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10-µF ceramic capacitance is required on the input of the LM6x4xx-Q1. Use 2 x 10-µF ceramic capacitance or more for better EMI performance. This must be rated for at least the maximum input voltage that the application requires. It is preferable to have twice the maximum input voltage to reduce DC bias derating. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size (0603 or 0402) ceramic capacitor must be used at each input/ground pin pair, VIN1/PGND1 and VIN2/PGND2, immediately adjacent to the regulator. The capacitor should have a voltage rating of at least double the maximum input voltage to minimize derating. The capacitor must also have an X7R or better dielectric. Choose the highest capacitor value with these parameters. This provides a high frequency bypass to reduce switch-node ring and electromagnetic interference emissions. The QFN (RJR) package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. This example places two 10-µF, 50-V, 1206, X7R ceramic capacitors and two 0.47-µF, 50-V, 0603, X7R ceramic capacitors at each VIN/PGND pin pair.

Often, it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help dampen ringing on the input supply caused by the inductance of the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

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Most of the input switching current passes through the ceramic input capacitors. The approximate worst case RMS value of this current can be calculated with 方程式 7. This value must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \approx \frac{I_{OUT}}{2} \tag{7}$$

9.2.2.6 BOOT Capacitor

The LM6x4xx-Q1 requires a bootstrap capacitor connected between the CBOOT pin and the SW pin. This capacitor stores energy which is used to supply the gate drivers for the power MOSFETs. A high-quality 100-nF ceramic capacitor with a rating of at least 10 V is required. The package provides space between the VIN2 and RBOOT pins to route SW to the boot capacitor without needing long traces or multi-layer routing.

9.2.2.7 BOOT Resistor

A BOOT resistor can be connected between the CBOOT and RBOOT pins to slow the rise-time of the SW node. If EMI performance is not critical, these two pins can be shorted. If EMI is critical, use a 0-Ω placeholder. The value can be increased if additional EMI margin is required. Increase to 200 Ω as a first step. This slows the rise-time of the SW node, reducing EMI at hundreds of MHz by a few dBµV. This is at the expense of about 0.3% efficiency at 400 kHz at 10 A. Use 50 Ω for a similar efficiency drop at 2.2 MHz at 6 A. In this example, 0 Ω is chosen to maximize efficiency. Continue to increase the value of RBOOT to further improve high-frequency EMI emissions at the expense of more efficiency. RBOOT connected to pins RBOOT and CBOOT can be any value between a short and an open without triggering BOOT UVLO.

9.2.2.8 VCC

The VCC pin is the output of the internal LDO used as a supply to the internal control circuits of the regulator. This output requires a 1-µF, 16-V, X7R or similar, 0603 or similar ceramic capacitor connected from VCC to AGND for proper operation. Generally avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the $\overline{\text{RESET}}$ (power-good) function (see 节 8.3.6). A pullup resistor with value of 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3 V. Do not short this output to ground or any other external voltage.

9.2.2.9 C_{FF} and R_{FF} Selection

A feedforward capacitor, C_{FF} on the order of tens of picofarads, is used to improve phase margin and transient response of circuits which have output capacitors with low ESR. Since this C_{FF} capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, a 4.99-kΩ resistor, R_{FF}, must be placed in series with C_{FF}. If the ESR zero of the output capacitor is below 200 kHz, no C_{FF} must be used.

If output voltage is less than 2.5 V, C_{FF} has little effect, so it can be omitted. If output voltage is greater than 14 V, C_{FF} must be used cautiously since it can easily introduce too much gain at higher frequencies.

If 1 MΩ is selected for R_{FBT}, then a feedforward capacitor C_{FF} must be used.

9.2.2.10 R_{SPSP} Selection

The SPSP pin can be connected to GND to disable spread spectrum. The pin can be connected to VCC to enable spread spectrum. The pin can also be connected to GND through a resistor to enable spread spectrum with ripple cancellation. This actively reduces the output ripple associated with spread spectrum which arises from the inductor current ripple amplitude modulation caused by the spread spectrum frequency modulation. The value is typically approximately 20 kΩ and can be more precisely calculated using 方程式 4.

9.2.2.11 R_T Selection

The R_T resistor sets the switching frequency of the converter. See 节 8.3.5 for more details. A resistor value of 40.2 kΩ corresponds to 400 kHz. The pin is also configured to set the switching frequency at 400 kHz when the

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RT pin is connected to VCC. Connecting the RT pin to VCC allows you to save cost and space, but placing a 40.2-k resistor allows for more flexibility if a different frequency is desired at a later time.

9.2.2.12 R_{MODE} Selection

The SYNC/MODE pin allows you to synchronize the converter to an external clock voltage (SYNC). The pin also allows the selection between two modes (MODE). The following are the selectable modes:

- Forced pulse width modulation (FPWM) operation, which operates at a fixed frequency at all loads in typical operation
- Auto mode which automatically switches to pulse-frequency modulation (PFM) at light loads to improve light-load efficiency

Connect the SYNC/MODE pin to VCC for FPWM. Connect to GND for auto. You can also apply a clock signal to synchronize the switching frequency to an external clock. See 节 8.3.3 for more information.

9.2.2.13 External UVLO

In some cases, the user may need an input undervoltage lockout (UVLO) level different than that provided internal to the device. This can be accomplished by using the circuit shown in 图 8-2. The input voltage at which the device turns on is designated V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then 方程式 2 is used to calculate R_{ENT} and V_{OFF}.

9.2.2.14 Maximum Ambient Temperature

As with any power conversion device, the LM6x4xx-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient temperature. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$ of the device
- PCB layout

The maximum internal die temperature for the LM6x4xx-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 方程式 8 shows the relationships between the important parameters. Larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in the *Application Curves* section. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in the 节 7.4 is not valid for design purposes and must not be used to estimate the thermal performance of the device in a real application. The values reported in the 节 7.4 table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}\big|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \tag{8}$$

where

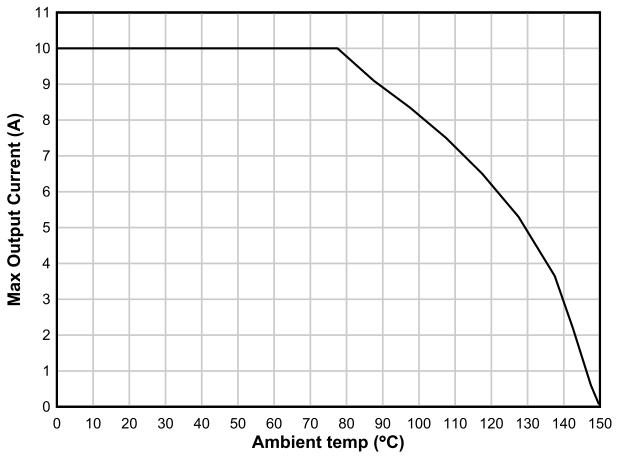
- η = efficiency
- T_A = ambient temperature
- T_J = junction temperature
- $R_{\theta JA}$ = the effective thermal resistance of the IC junction to the air, mainly through the PCB

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors (just to mention a few of the most critical parameters:

- Power dissipation
- Air temperature

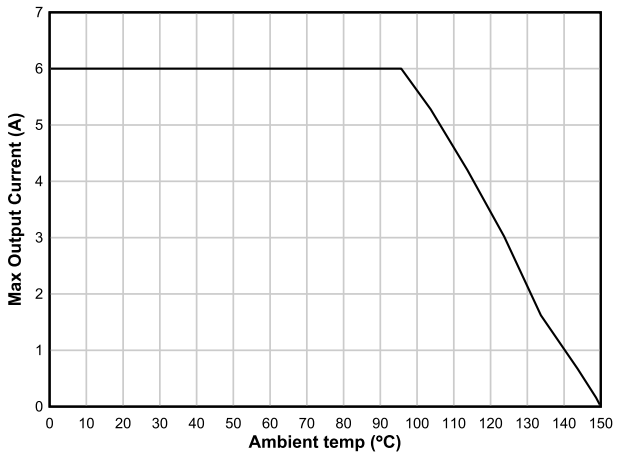
- Airflow
- PCB area
- Copper heat-sink area
- Number of thermal vias under or near the package
- Adjacent component placement

Due to the ultra-miniature size of the VQFN (RNX) package, a die-attach pad is not available, requiring most of the heat to flow from the pins to the board. This means that this package exhibits a somewhat large $R_{\theta JA}$ value when the layout does not allow for heat to flow from the pins. A typical curve of maximum output current versus ambient temperature is shown in 图 9-3 and 图 9-4 for a good thermal layout. This data was taken on the LM61495RPHEVM evaluation board with a device and PCB combination, giving an $R_{\theta JA}$ of about 21.6°C/W. It must be remembered that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.



V_{IN} = 13.5 V　　V_{OUT} = 5 V
f_{SW} = 400 kHz　　$R_{\theta JA}$ = 22°C/W

图 9-3. Maximum Output Current versus Ambient Temperature



V_{IN} = 13.5 V　　V_{OUT} = 5 V
f_{SW} = 2.2 MHz　　$R_{\theta JA}$ = 22°C/W

图 9-4. Maximum Output Current versus Ambient Temperature

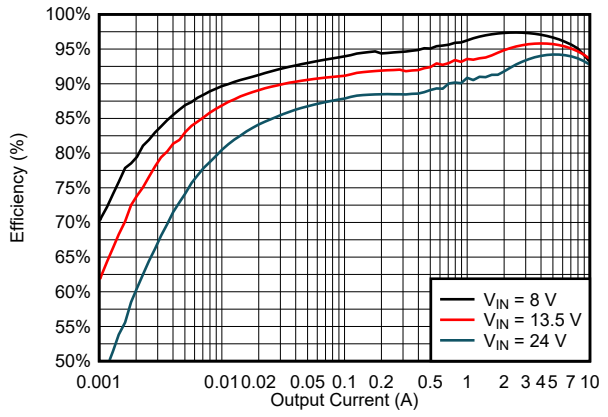
Use the following resources as a guide to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
- *Semiconductor and IC Package Thermal Metrics*
- *Thermal Design Made Simple with LM43603 and LM43602*
- *PowerPAD™ Thermally Enhanced Package*
- *PowerPAD™ Made Easy*
- *Using New Thermal Metrics*

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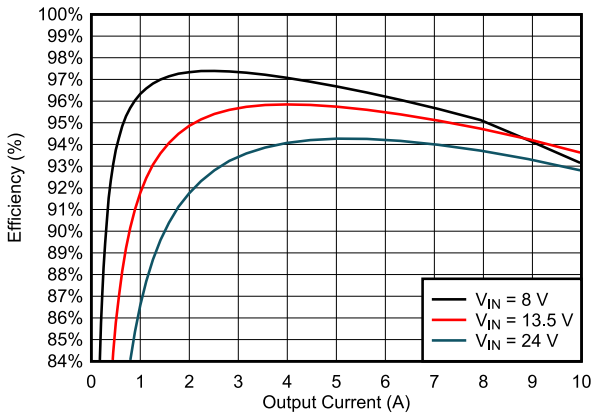
9.2.3 Application Curves

Unless otherwise specified, the following conditions apply: Device: LM61495-Q1, V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



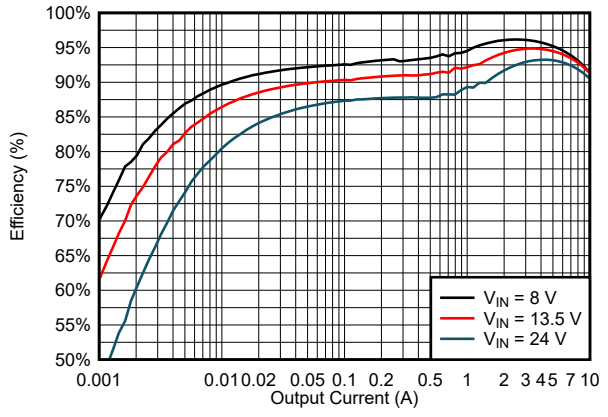
V_{OUT} = 5 V F_{SW} = 400 kHz Auto mode

图 9-5. Efficiency



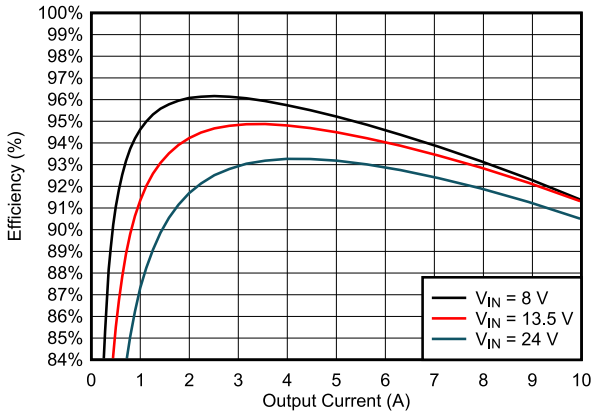
V_{OUT} = 5 V F_{SW} = 400 kHz FPWM mode

图 9-6. Efficiency



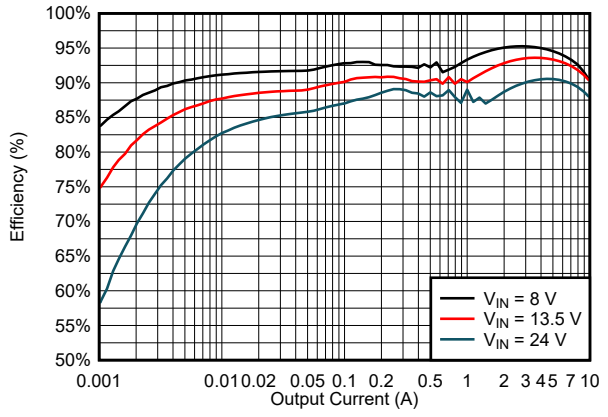
V_{OUT} = 3.3 V F_{SW} = 400 kHz Auto mode

图 9-7. Efficiency



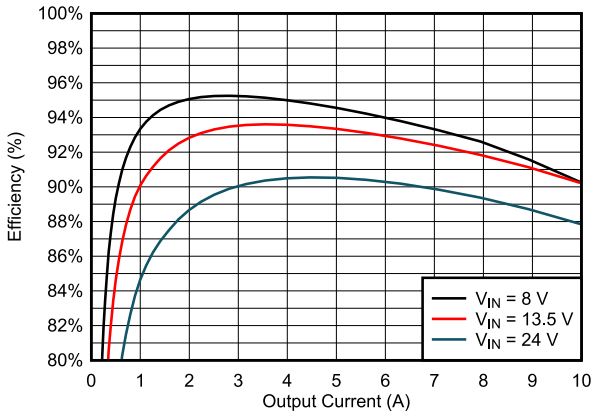
V_{OUT} = 3.3 V F_{SW} = 400 kHz FPWM mode

图 9-8. Efficiency



V_{OUT} = 5 V F_{SW} = 2.2 MHz Auto mode

图 9-9. Efficiency

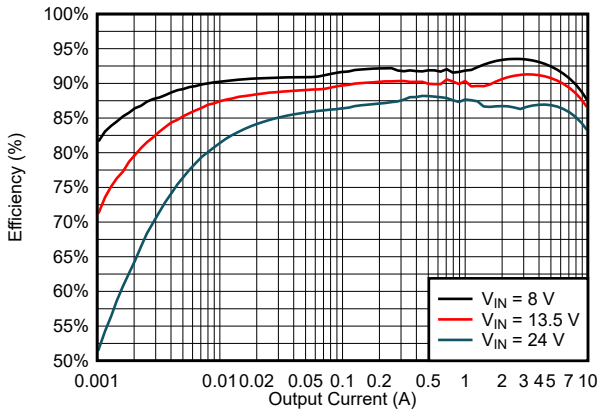


V_{OUT} = 5 V F_{SW} = 2.2 MHz FPWM mode

图 9-10. Efficiency

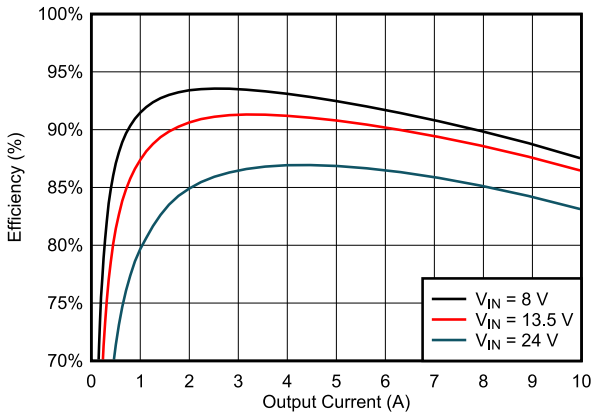
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9.2.3 Application Curves (continued)



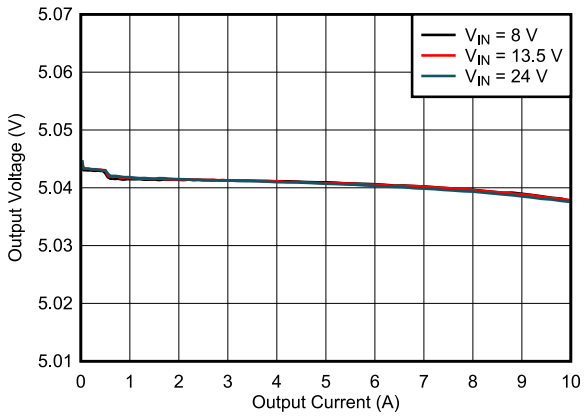
V_{OUT} = 3.3 V F_{SW} = 2.2 MHz Auto mode

图 9-11. Efficiency



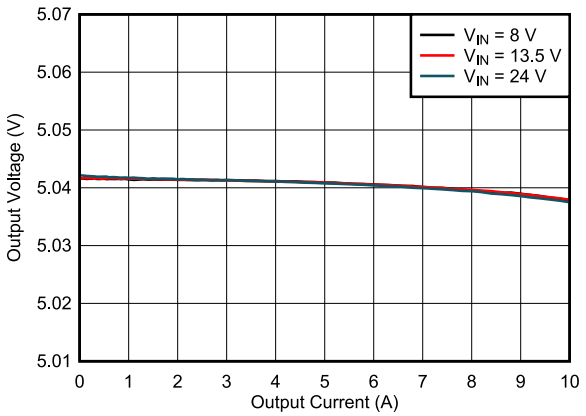
V_{OUT} = 3.3 V F_{SW} = 2.2 MHz FPWM mode

图 9-12. Efficiency



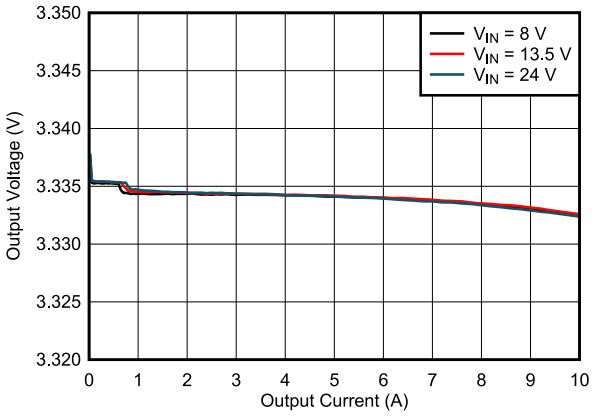
V_{OUT} = 5 V F_{SW} = 400 kHz Auto mode

图 9-13. Load and Line Regulation



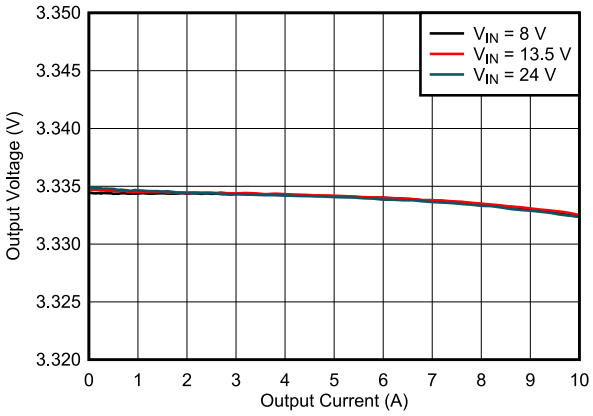
V_{OUT} = 5 V F_{SW} = 400 kHz FPWM mode

图 9-14. Load and Line Regulation



V_{OUT} = 3.3 V F_{SW} = 400 kHz Auto mode

图 9-15. Load and Line Regulation

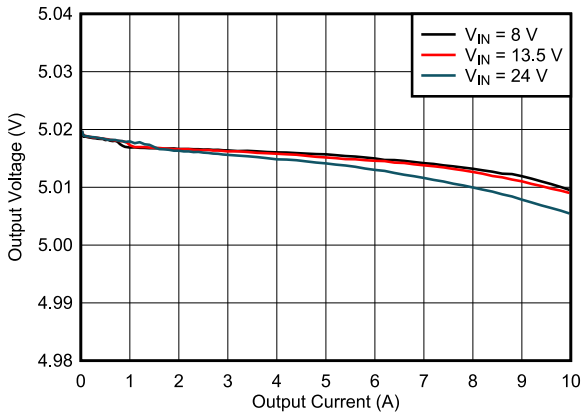


V_{OUT} = 3.3 V F_{SW} = 400 kHz FPWM mode

图 9-16. Load and Line Regulation

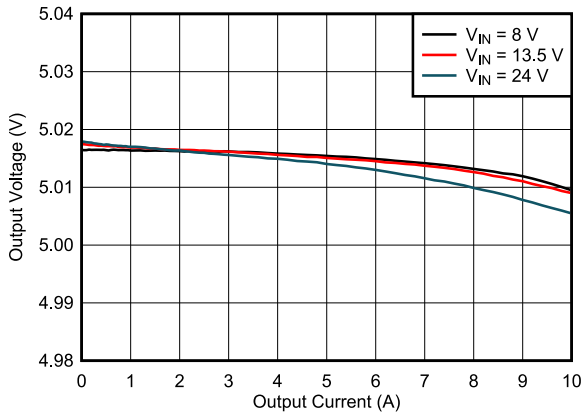
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9.2.3 Application Curves (continued)



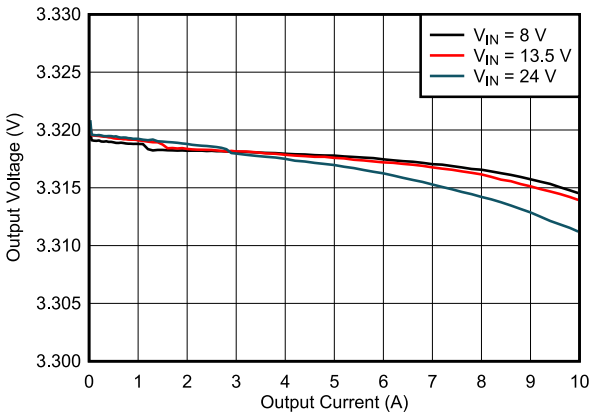
V_{OUT} = 5 V F_{SW} = 2.2 MHz Auto mode

图 9-17. Load and Line Regulation



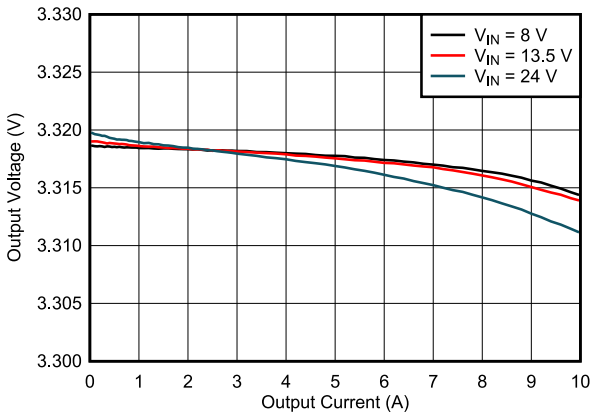
V_{OUT} = 5 V F_{SW} = 2.2 MHz FPWM mode

图 9-18. Load and Line Regulation



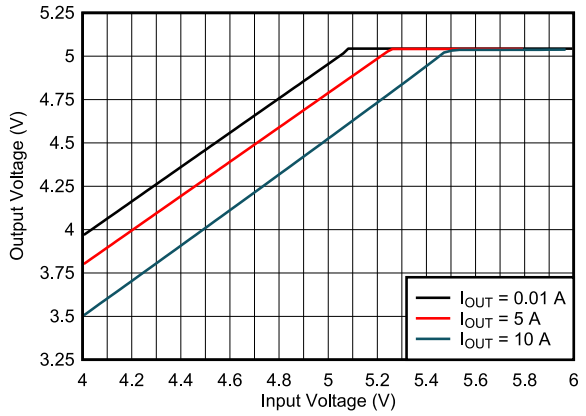
V_{OUT} = 3.3 V F_{SW} = 2.2 MHz Auto mode

图 9-19. Load and Line Regulation



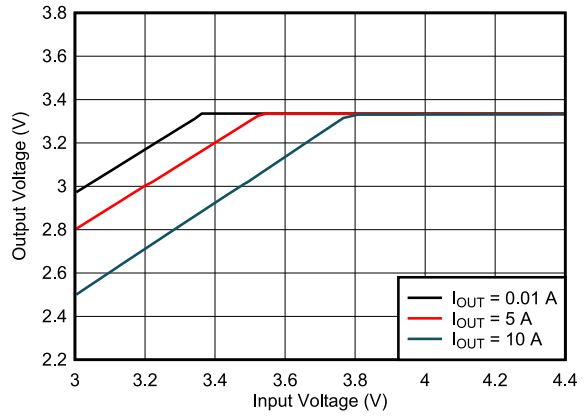
V_{OUT} = 3.3 V F_{SW} = 2.2 MHz FPWM mode

图 9-20. Load and Line Regulation



V_{OUT} = 5 V F_{SW} = 400 kHz Auto mode

图 9-21. Dropout

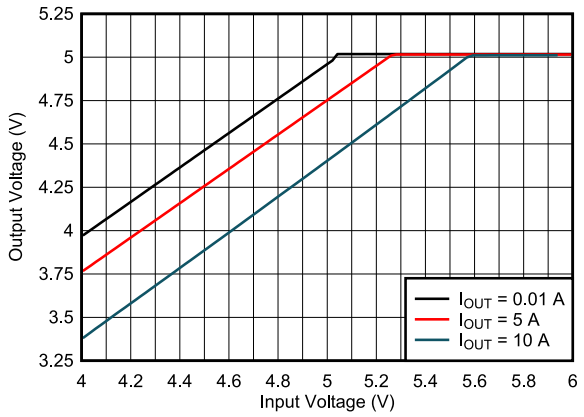


V_{OUT} = 3.3 V F_{SW} = 400 kHz Auto mode

图 9-22. Dropout

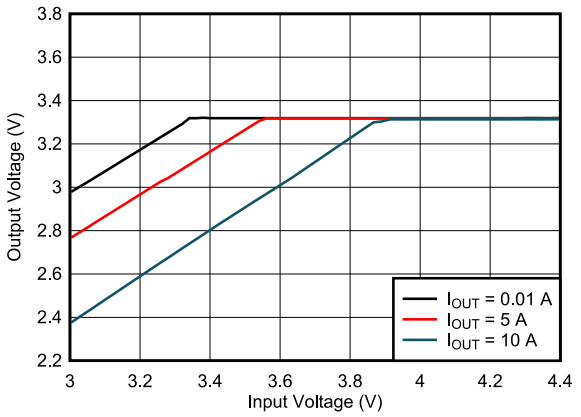
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9.2.3 Application Curves (continued)



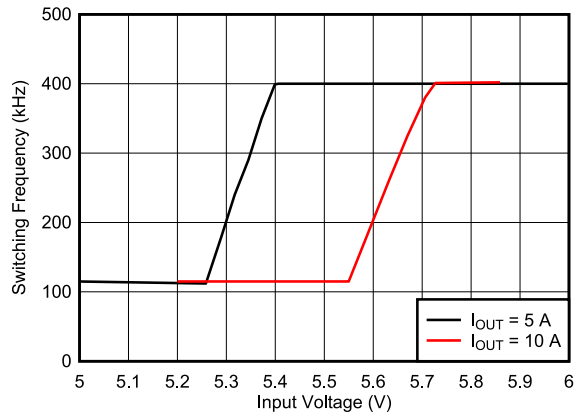
V_{OUT} = 5 V F_{SW} = 2.2 MHz Auto mode

图 9-23. Dropout



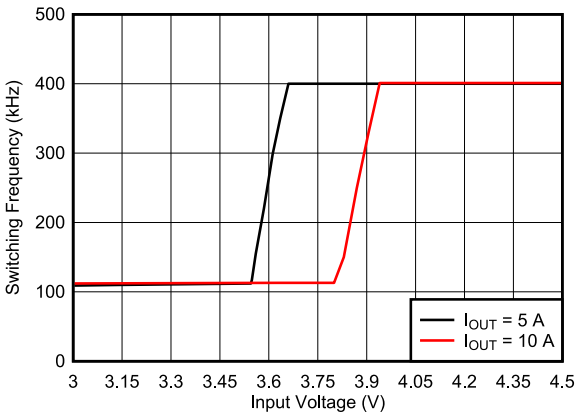
V_{OUT} = 3.3 V F_{SW} = 2.2 MHz Auto mode

图 9-24. Dropout



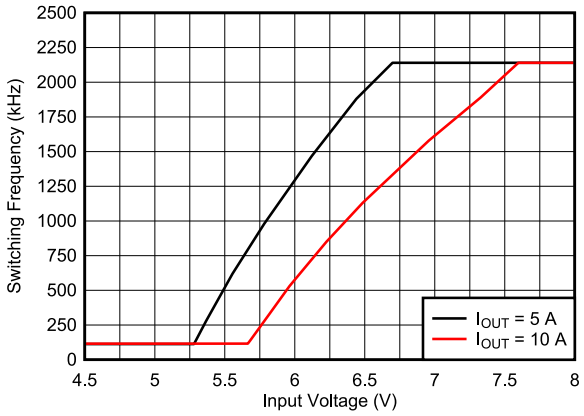
V_{OUT} = 5 V F_{SW} = 400 kHz Auto mode

图 9-25. Frequency Dropout



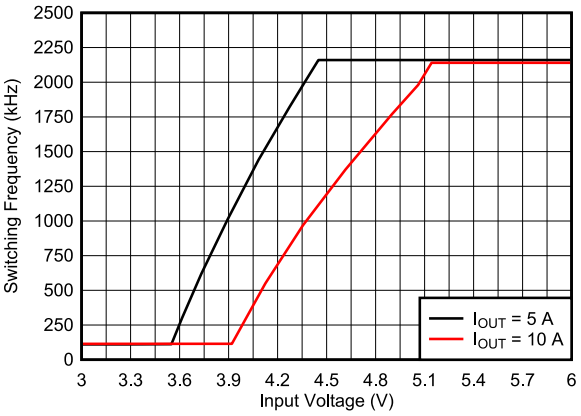
V_{OUT} = 3.3 V F_{SW} = 400 kHz Auto mode

图 9-26. Frequency Dropout



V_{OUT} = 5 V F_{SW} = 2.2 MHz Auto mode

图 9-27. Frequency Dropout

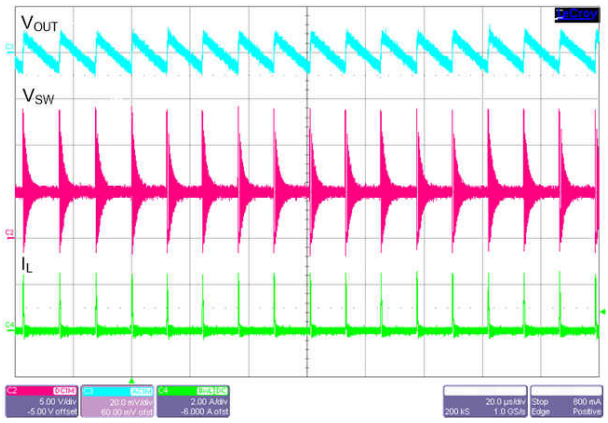


V_{OUT} = 3.3 V F_{SW} = 2.2 MHz Auto mode

图 9-28. Frequency Dropout

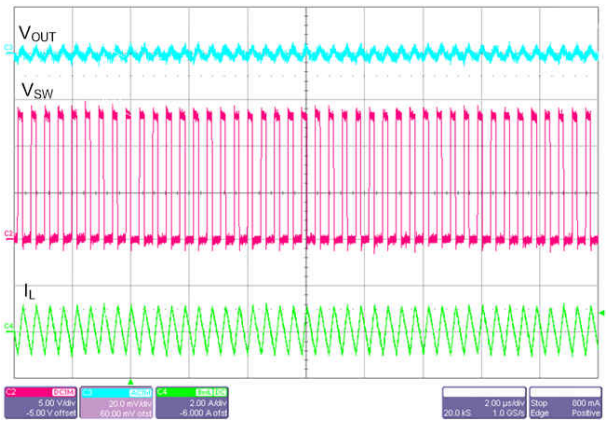
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9.2.3 Application Curves (continued)



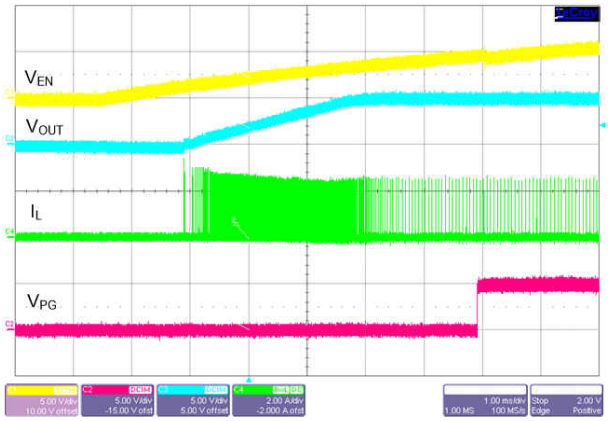
V_{OUT} = 5 V　F_{SW} = 2100 kHz　Auto mode
I_{OUT} = 50 mA　V_{IN} = 13.5 V

图 9-29. Switching Waveform and V_{OUT} Ripple



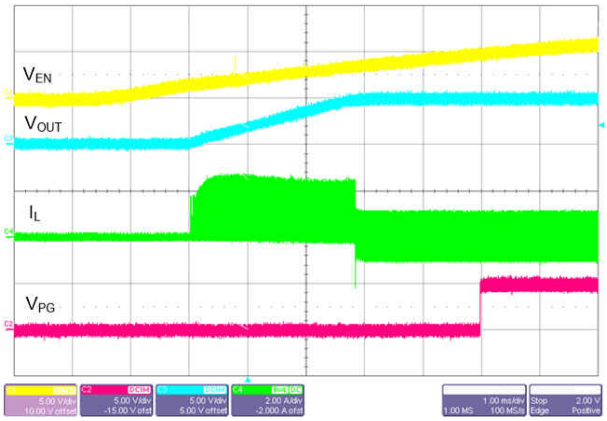
V_{OUT} = 5 V　F_{SW} = 2100 kHz　FPWM mode
I_{OUT} = 50 mA　V_{IN} = 13.5 V

图 9-30. Switching Waveform and V_{OUT} Ripple



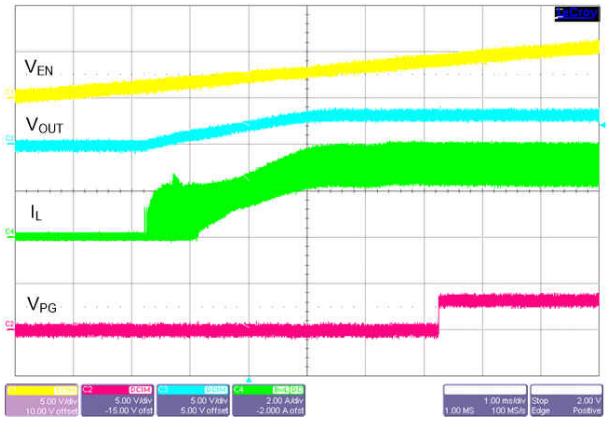
V_{OUT} = 5 V　F_{SW} = 2100 kHz　Auto mode
I_{OUT} = 50 mA　V_{IN} = 13.5 V

图 9-31. Start-up with 50-mA Load



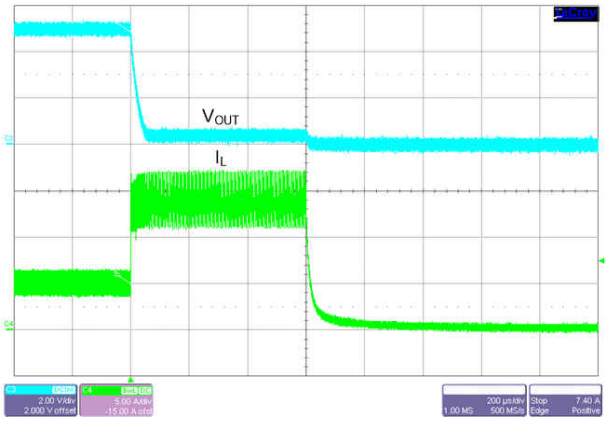
V_{OUT} = 5 V　F_{SW} = 2100 kHz　FPWM mode
I_{OUT} = 50 mA　V_{IN} = 13.5 V

图 9-32. Start-up with 50-mA Load



V_{OUT} = 3.3 V　F_{SW} = 2100 kHz　FPWM mode
I_{OUT} = 3.25 A　V_{IN} = 13.5 V

图 9-33. Start-up with 3.25-A Load

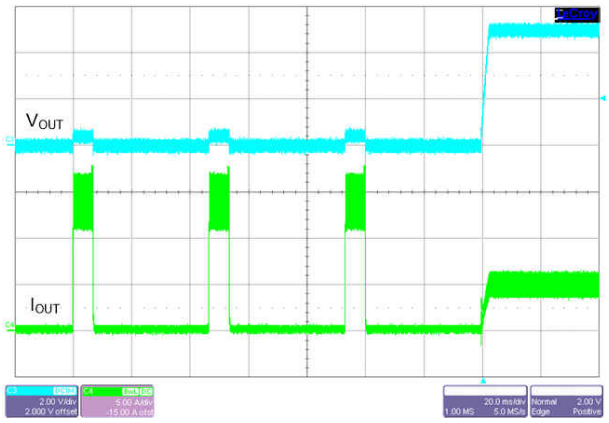


V_{OUT} = 5 V　F_{SW} = 2100 kHz　FPWM mode
I_{OUT} = 5 A to Short Circuit　V_{IN} = 13.5 V

图 9-34. Short Circuit Protection

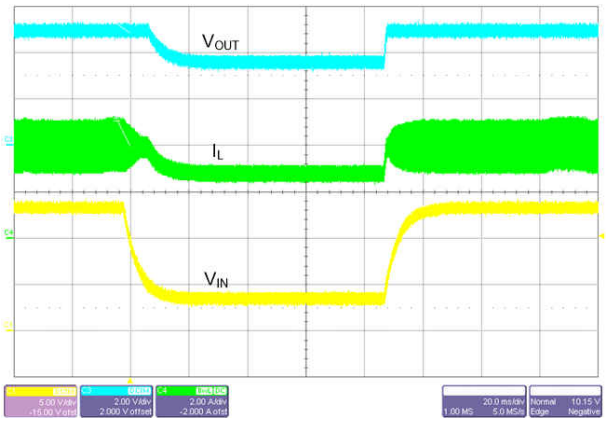
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9.2.3 Application Curves (continued)



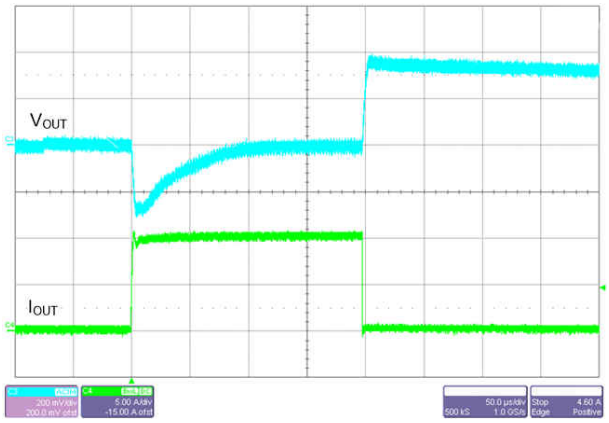
V_{OUT} = 5 V　　F_{SW} = 2100 kHz　　FPWM mode
I_{OUT} = Short Circuit to 5 A　　V_{IN} = 13.5 V

图 9-35. Short Circuit Recovery



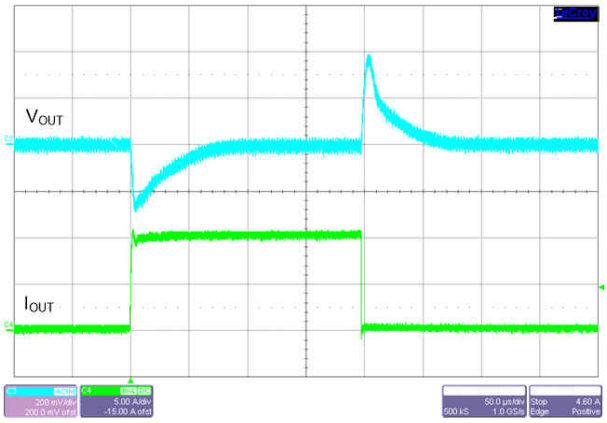
V_{OUT} = 5 V　　F_{SW} = 2100 kHz　　FPWM mode
I_{OUT} = 4 A　　V_{IN} = 13.5 V to 4 V to 13.5 V

图 9-36. Recovery from Dropout



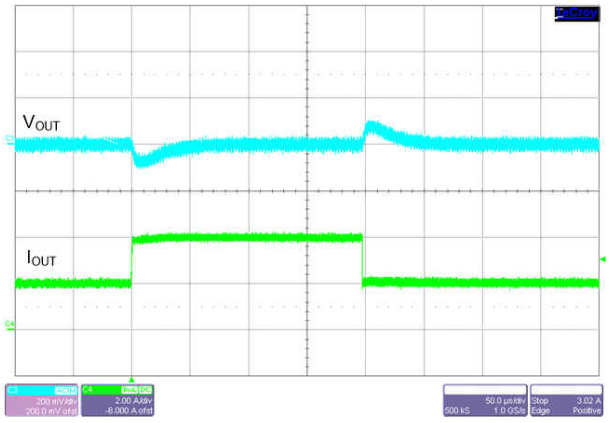
V_{OUT} = 5 V　　F_{SW} = 400 kHz　　Auto mode
I_{OUT} = 10 mA to 10 A to 10 mA　　V_{IN} = 13.5 V　　$T_R = T_F$ = 1 µs

图 9-37. Load Transient



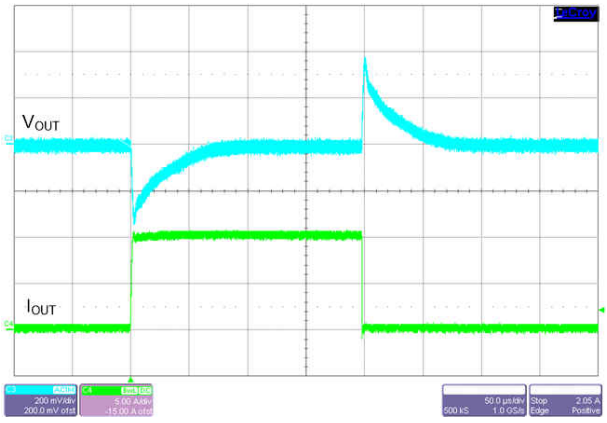
V_{OUT} = 5 V　　F_{SW} = 400 kHz　　FPWM mode
I_{OUT} = 10 mA to 10 A to 10 mA　　V_{IN} = 13.5 V　　$T_R = T_F$ = 1 µs

图 9-38. Load Transient



V_{OUT} = 5 V　　F_{SW} = 400 kHz　　Auto mode
I_{OUT} = 2 A to 4 A to 2 A　　V_{IN} = 13.5 V　　$T_R = T_F$ = 1 µs

图 9-39. Load Transient

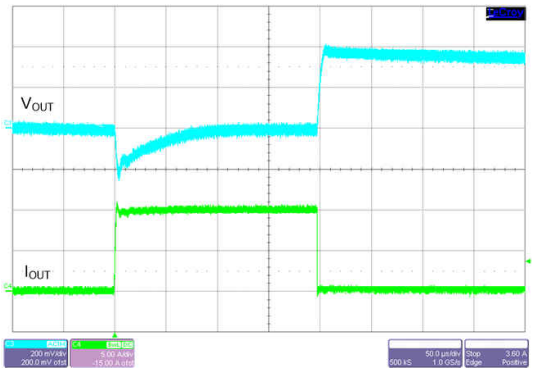


V_{OUT} = 5 V　　F_{SW} = 400 kHz　　Auto mode
I_{OUT} = 5 A to 10 A to 5 A　　V_{IN} = 13.5 V　　$T_R = T_F$ = 1 µs

图 9-40. Load Transient

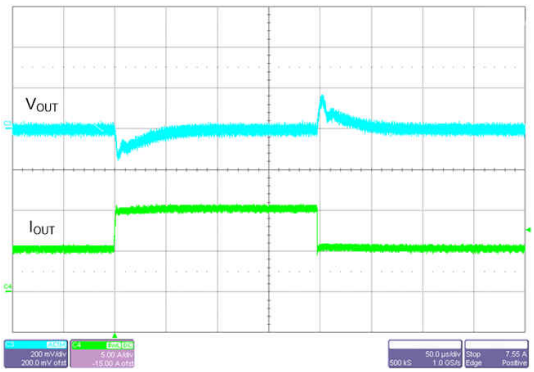
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9.2.3 Application Curves (continued)



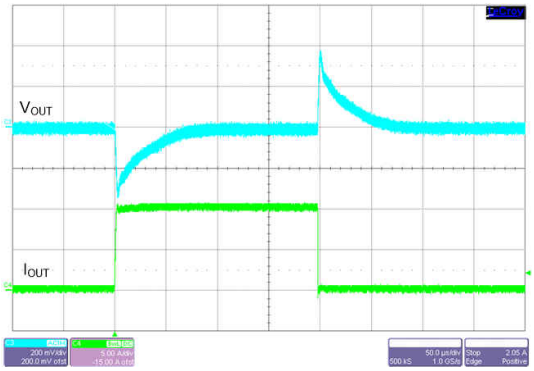
V_{OUT} = 3.3 V
I_{OUT} = 10 mA to 10 A to 10 mA
F_{SW} = 400 kHz
V_{IN} = 13.5 V
Auto mode
$T_R = T_F$ = 1 µs

图 9-41. Load Transient



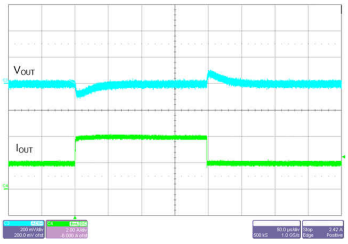
V_{OUT} = 3.3 V
I_{OUT} = 5 A to 10 A to 5 A
F_{SW} = 400 kHz
V_{IN} = 13.5 V
Auto mode
$T_R = T_F$ = 1 µs

图 9-42. Load Transient



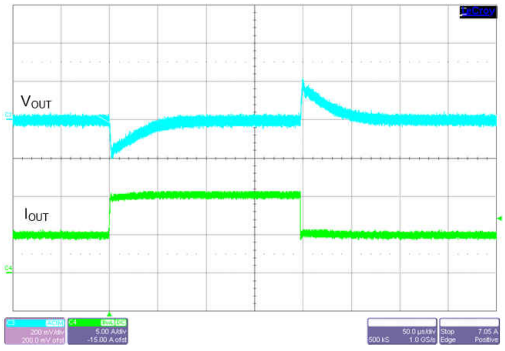
V_{OUT} = 5 V
I_{OUT} = 10 mA to 10 A to 10 mA
F_{SW} = 2200 kHz
V_{IN} = 13.5 V
FPWM mode
$T_R = T_F$ = 1 µs

图 9-43. Load Transient



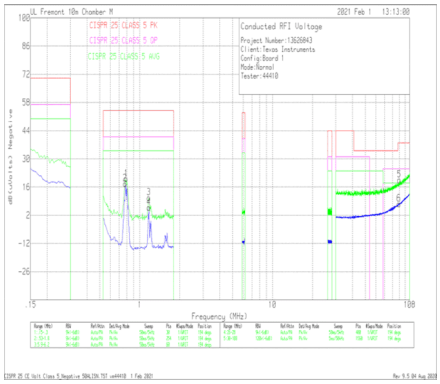
V_{OUT} = 5 V
I_{OUT} = 2 A to 4 A to 2 A
F_{SW} = 2200 kHz
V_{IN} = 13.5 V
Auto mode
$T_R = T_F$ = 1 µs

图 9-44. Load Transient



V_{OUT} = 5 V
I_{OUT} = 5 A to 10 A to 5 A
F_{SW} = 2200 kHz
V_{IN} = 13.5 V
Auto mode
$T_R = T_F$ = 1 µs

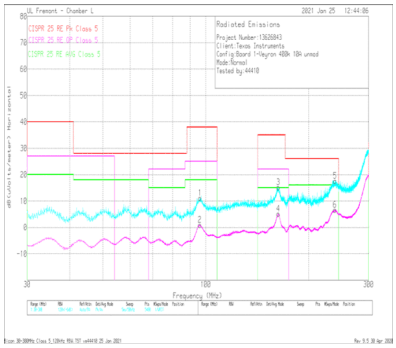
图 9-45. Load Transient



V_{OUT} = 5 V
F_{SW} = 400 kHz
I_{OUT} = 10 A
Frequency Tested: 150 kHz to 30 MHz

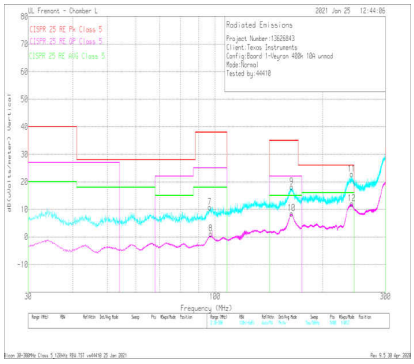
图 9-46. Conducted EMI versus CISPR25 Class 5 Limits (Green: Peak Signal, Blue: Average Signal)

9.2.3 Application Curves (continued)



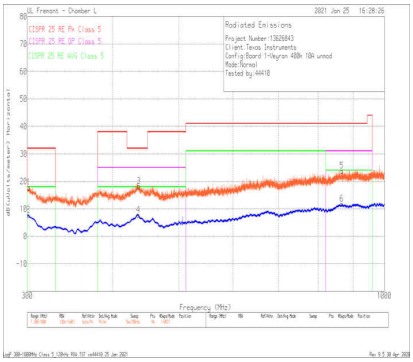
V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A
Frequency Tested: 30 MHz to 300 MHz

图 9-47. Radiated EMI Bicon Horizontal versus CISPR25 Class 5 Limits



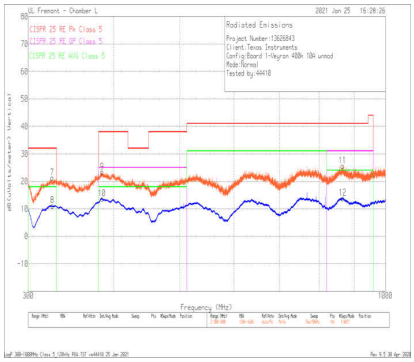
V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A
Frequency Tested: 30 MHz to 300 MHz

图 9-48. Radiated EMI Bicon Vertical versus CISPR25 Class 5 Limits



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A
Frequency Tested: 300 MHz to 1 GHz

图 9-49. Radiated EMI Log Horizontal versus CISPR25 Class 5 Limits



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A
Frequency Tested: 300 MHz to 1 GHz

图 9-50. Radiated EMI Log Vertical versus CISPR25 Class 5 Limits

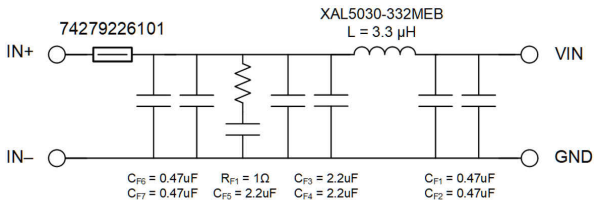
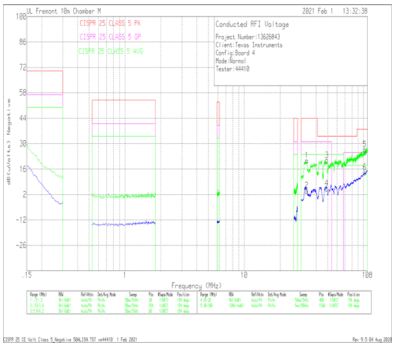


图 9-51. Recommended Input EMI Filter

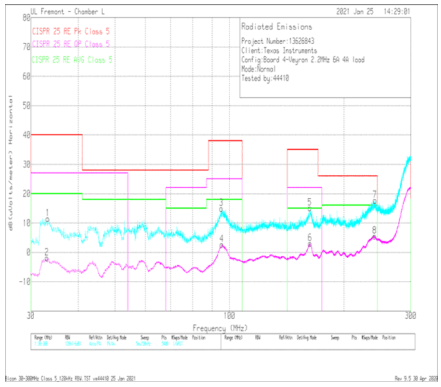


V_{OUT} = 5 V F_{SW} = 2.2 MHz I_{OUT} = 4 A
Frequency Tested: 150 kHz to 30 MHz

图 9-52. Conducted EMI versus CISPR25 Class 5 Limits (Green: Peak Signal, Blue: Average Signal)

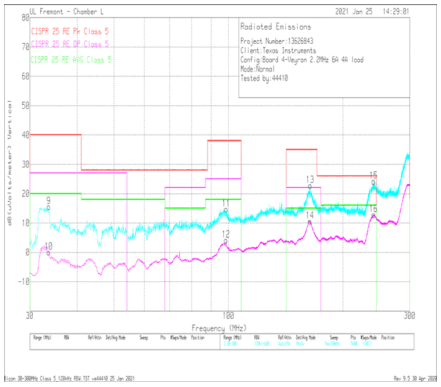
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9.2.3 Application Curves (continued)



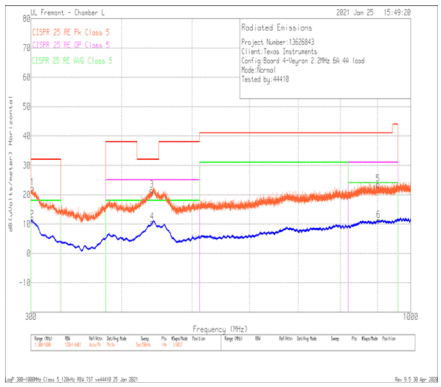
V_{OUT} = 5 V F_{SW} = 2.2 MHz I_{OUT} = 4 A
Frequency Tested: 30 MHz to 300 MHz

图 9-53. Radiated EMI Bicon Horizontal versus CISPR25 Class 5 Limits



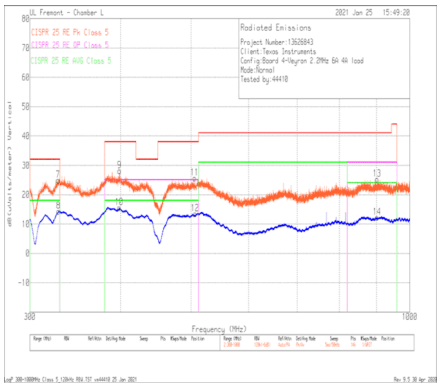
V_{OUT} = 5 V F_{SW} = 2.2 MHz I_{OUT} = 4 A
Frequency Tested: 30 MHz to 300 MHz

图 9-54. Radiated EMI Bicon Vertical versus CISPR25 Class 5 Limits



V_{OUT} = 5 V F_{SW} = 2.2 MHz I_{OUT} = 4 A
Frequency Tested: 300 MHz to 1 GHz

图 9-55. Radiated EMI Log Horizontal versus CISPR25 Class 5 Limits



V_{OUT} = 5 V F_{SW} = 2.2 MHz I_{OUT} = 4 A
Frequency Tested: 300 MHz to 1 GHz

图 9-56. Radiated EMI Log Vertical versus CISPR25 Class 5 Limits

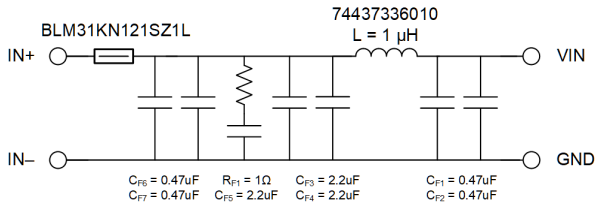


图 9-57. Recommended Input EMI Filter

9.2.3 Application Curves (continued)

表 9-4. BOM for Typical Application Curves

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	C_{IN} + C_{HF}	L	C_{FF}
3.3 V	400 kHz	43.2 kΩ	4 x 47 µF + 100 µF electrolytic + 2 x 2.2 µF	4 × 10 µF + 2 × 470 nF + 100 µF electrolytic	2.4 µH (744325240)	22 pF
3.3 V	2200 kHz	43.2 kΩ	2 x 47 µF + 100 µF electrolytic + 2 x 2.2 µF	2 × 10 µF + 2 × 470 nF + 100 µF electrolytic	0.68 µH (744373460068)	10 pF
5 V	400 kHz	24.9 kΩ	4 x 47 µF + 100 µF electrolytic + 2 x 2.2 µF	4 × 10 µF + 2 × 470 nF + 100 µF electrolytic	2.4 µH (744325240)	22 pF
5 V	2200 kHz	24.9 kΩ	2 x 47 µF + 100 µF electrolytic + 2 x 2.2 µF	2 × 10 µF + 2 × 470 nF + 100 µF electrolytic	0.68 µH (744373460068)	10 pF

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10 Power Supply Recommendations

The characteristics of the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 方程式 9.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{9}$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can form an underdamped resonant circuit. This can result in overvoltage transients at the input to the regulator or tripping UVLO. Consider that the supply voltage can dip when a load transient is applied to the output depending on the parasitic resistance and inductance of the harness and characteristics of the supply. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator. Additionally, use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoots or undershoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a snap-back characteristic (thyristor type). It is not recommended to use a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the input supply and the output.

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11 Layout

11.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout to a great extent. In a buck converter, the most EMI-critical PCB feature is the loop formed by the input capacitor or capacitors and power ground. This is shown in 图 11-1. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. Excessive transient voltages can disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short while keeping the loop area as small as possible to reduce the parasitic inductance. 图 11-2 shows a recommended layout for the critical components of the LM6x4xx-Q1 circuit.

- ***Place the input capacitor or capacitors as close as possible to the input pin pairs***: VIN1 to PGND1 and VIN2 to PGND2. Place the small capacitors closest. Each pair of pins are adjacent, simplifying the input capacitor placement. With the QFN package, there are two VIN/PGND pairs on either side of the package. This provides a symmetrical layout and helps minimize switching noise and EMI generation. Use a wide VIN plane on a mid-layer to connect both of the VIN pairs together to the input supply. It is best to route symmetrically from the supply to each VIN pin to best utilize the benefits of the symmetric pinout.
- ***Place the bypass capacitor for VCC close to the VCC pin and AGND pin:*** This capacitor must be routed with short, wide traces to the VCC and AGND pins.
- ***Place the CBOOT capacitor as close as possible to the device with short, wide traces to the CBOOT and SW pins:*** It is important to route the SW connection under the device through the gap between VIN2 and RBOOT pins, reducing exposed SW node area. If an RBOOT resistor is used, place it as close as possible to the CBOOT and RBOOT pins. If high efficiency is desired, RBOOT and CBOOT pins can be shorted. This short must be placed as close as possible to the RBOOT and CBOOT pins.
- ***Place the feedback divider as close as possible to the FB pin of the device***: Place R_{FBB}, R_{FBT}, C_{FF} if used, and R_{FF} if used, physically close to the device. The connections to FB and AGND through R_{FBB} must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- ***Layer 2 of the PCB must be a ground plane***: This plane acts as a noise shield and as a heat dissipation path. Using layer 2 reduces the inclosed area in the input circulating current in the input loop, reducing inductance.
- ***Provide wide paths for V_{IN}, V_{OUT}, and GND***: These paths must be as wide and direct as possible to reduce any voltage drops on the input or output paths of the converter to maximize efficiency.
- ***Provide enough PCB area for proper heat sinking***: Enough copper area must be used to ensure a low $R_{\theta JA}$, considering maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces can be used for all pins except where noise considerations dictate minimization of area.
- ***Keep switch area small***: Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

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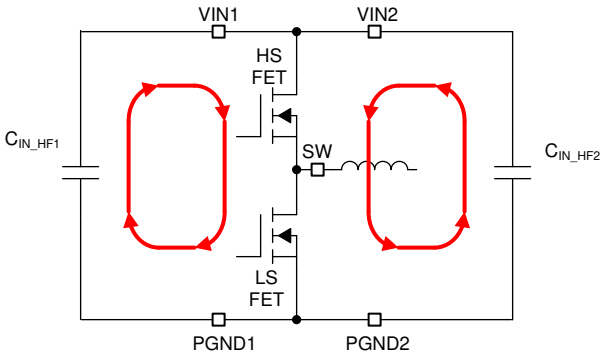


图 11-1. Input Current Loop

11.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET, and connect directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and must be used for sensitive traces.

TI recommends providing adequate device heat sinking by using vias near PGND and VIN pins to connect to the system ground plane or V_{IN} strap, both of which dissipate heat. Use as much copper as possible for the system ground plane on the top and bottom layers and avoid plane cuts and bottlenecks for the heat flow for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness and proper layout provides low current conduction impedance, proper shielding, and low thermal resistance.

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11.2 Layout Example

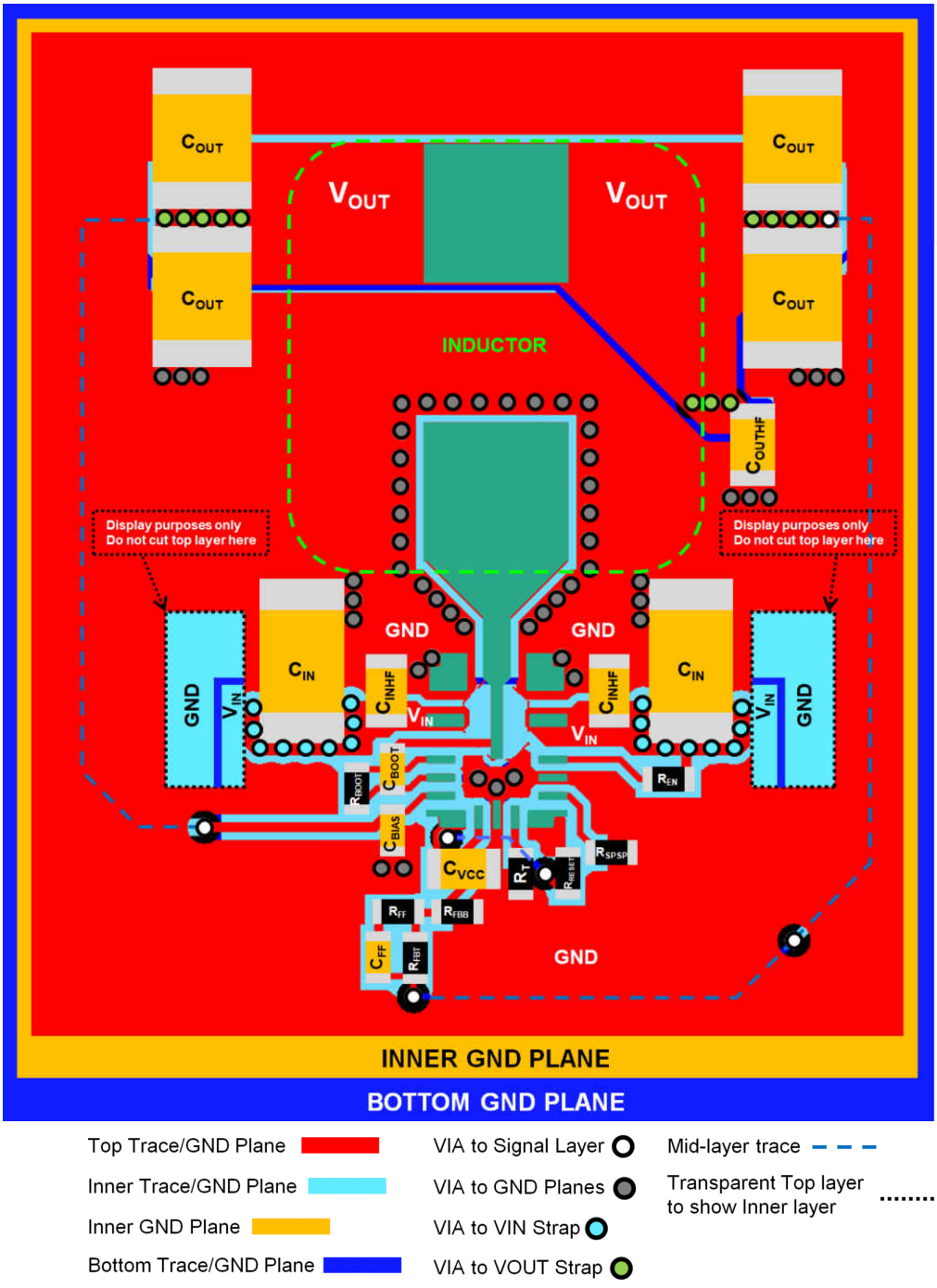


图 11-2. Layout Example

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12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

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12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM61480Q3RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	6148Q3	Samples
LM61480Q4RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	6148Q4	Samples
LM61480Q5RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	6148Q5	Samples
LM61480QRPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	61480Q	Samples
LM61495Q3RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	1495Q3	Samples
LM61495Q4RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	1495Q4	Samples
LM61495Q5RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	1495Q5	Samples
LM61495QRPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	61495Q	Samples
LM62460Q3RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	6246Q3	Samples
LM62460Q4RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	6246Q4	Samples
LM62460Q5RPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	6246Q5	Samples
LM62460QRPHRQ1	ACTIVE	VQFN-HR	RPH	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	62460Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM61480-Q1, LM61495-Q1, LM62460-Q1 :

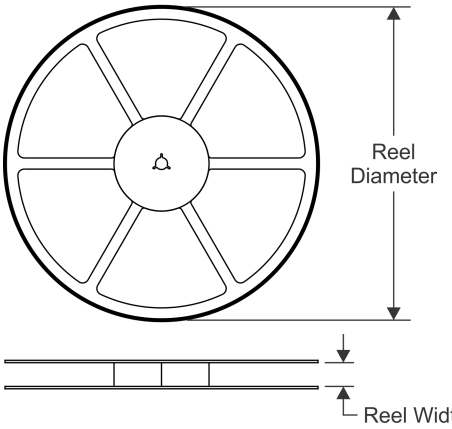
- Catalog : LM61480, LM61495, LM62460

NOTE: Qualified Version Definitions:

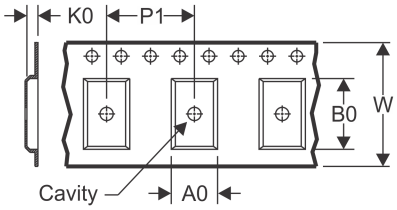
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

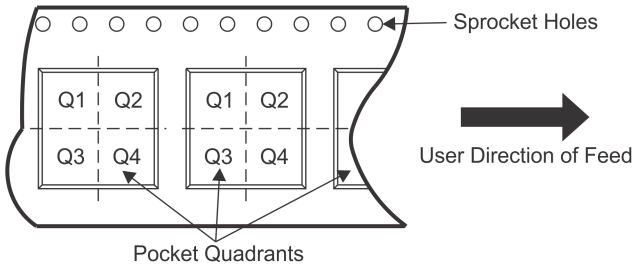


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

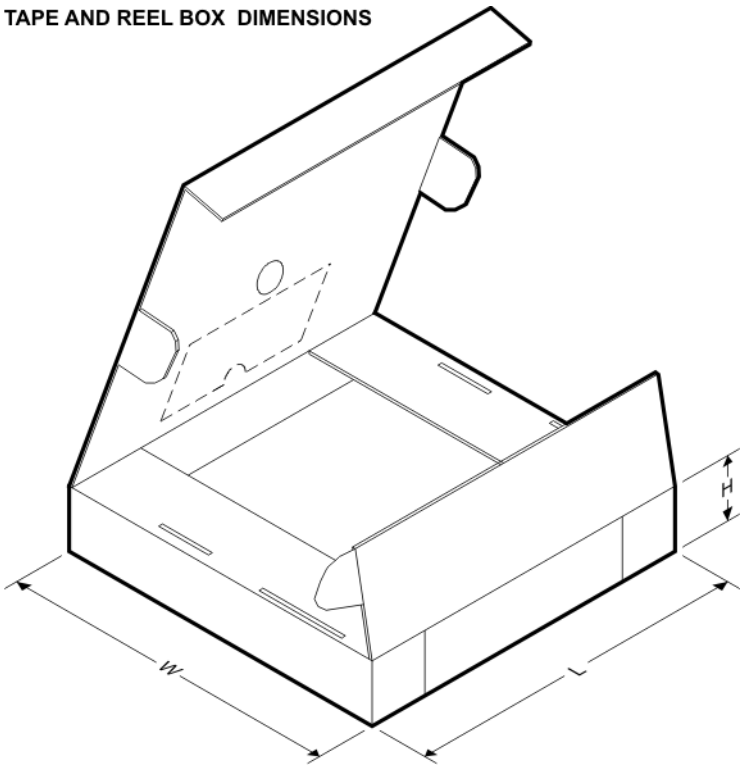


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM61480Q3RPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM61480Q4RPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM61480Q5RPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM61480QRPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM61495Q3RPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM61495Q4RPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM61495Q5RPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM61495QRPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM62460Q3RPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM62460Q4RPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM62460Q5RPHRQ1	VQFN-	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	HR											
LM62460QRPHRQ1	VQFN-HR	RPH	16	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM61480Q3RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM61480Q4RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM61480Q5RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM61480QRPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM61495Q3RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM61495Q4RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM61495Q5RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM61495QRPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM62460Q3RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM62460Q4RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM62460Q5RPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0
LM62460QRPHRQ1	VQFN-HR	RPH	16	3000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

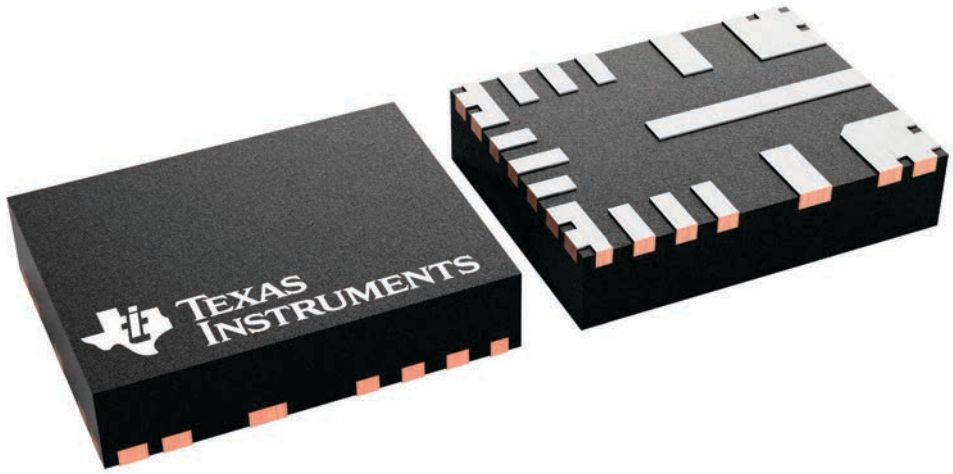
RPH 16

VQFN-HR - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



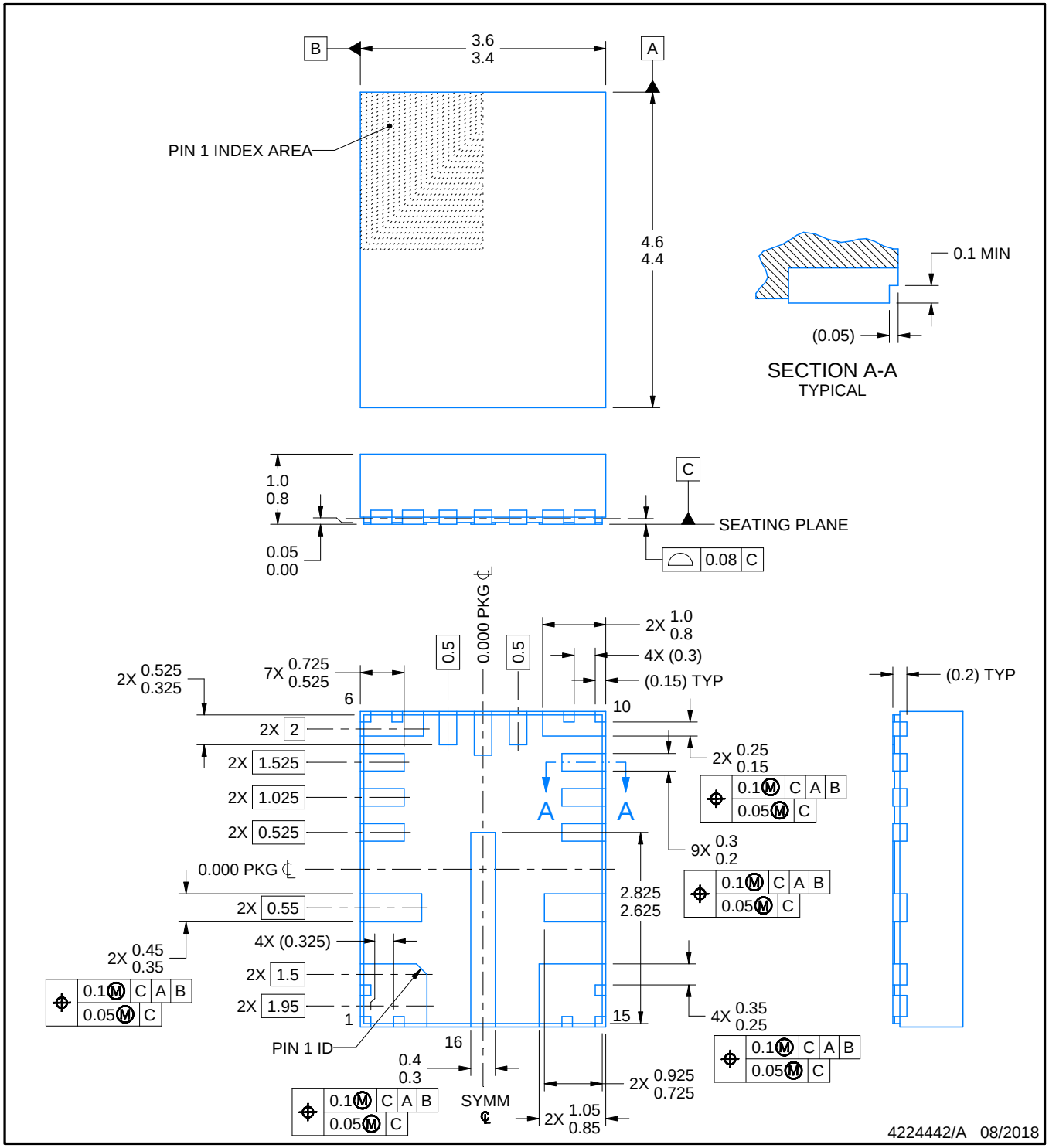
4227133/A

PACKAGE OUTLINE

RPH0016A

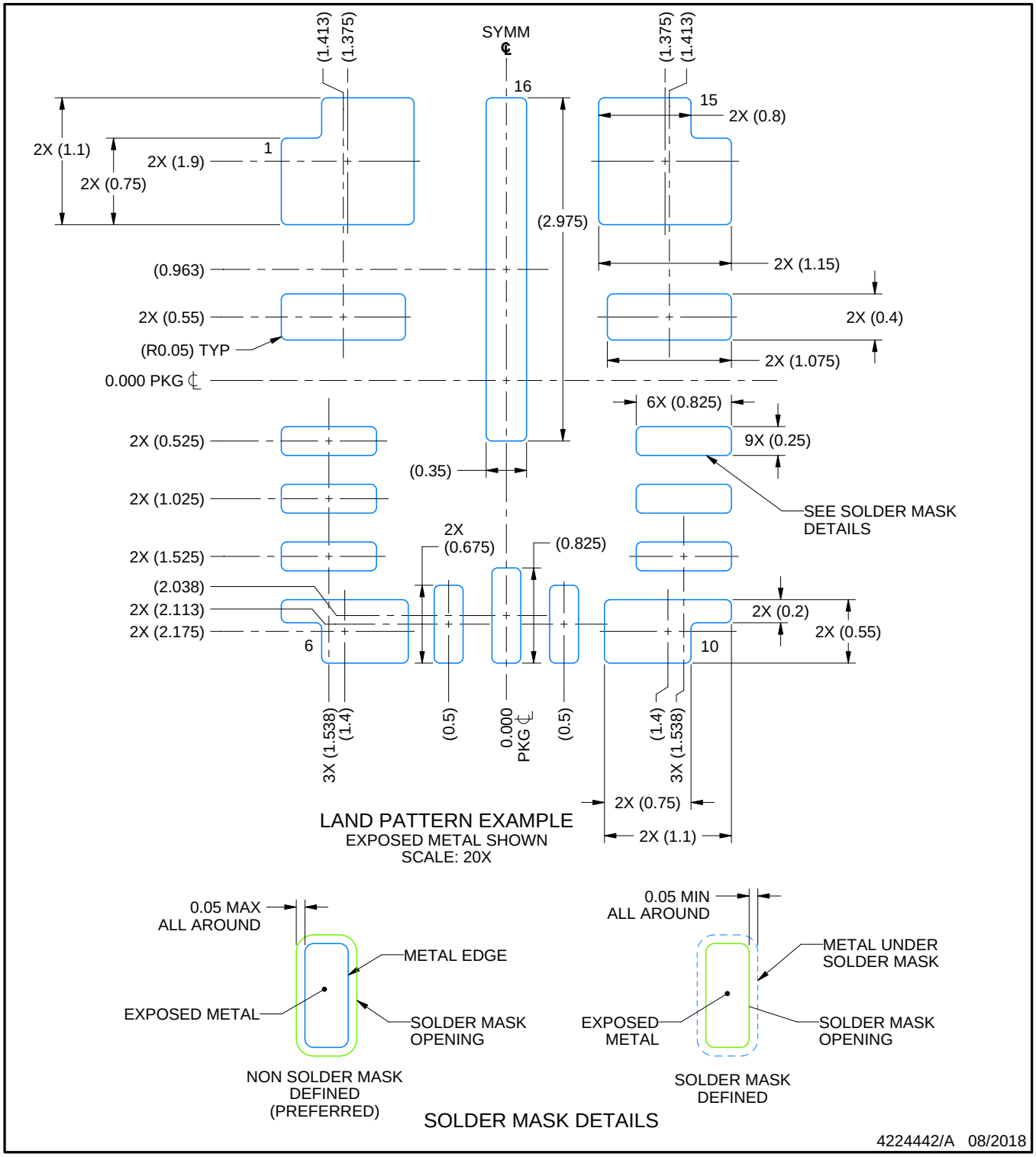
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



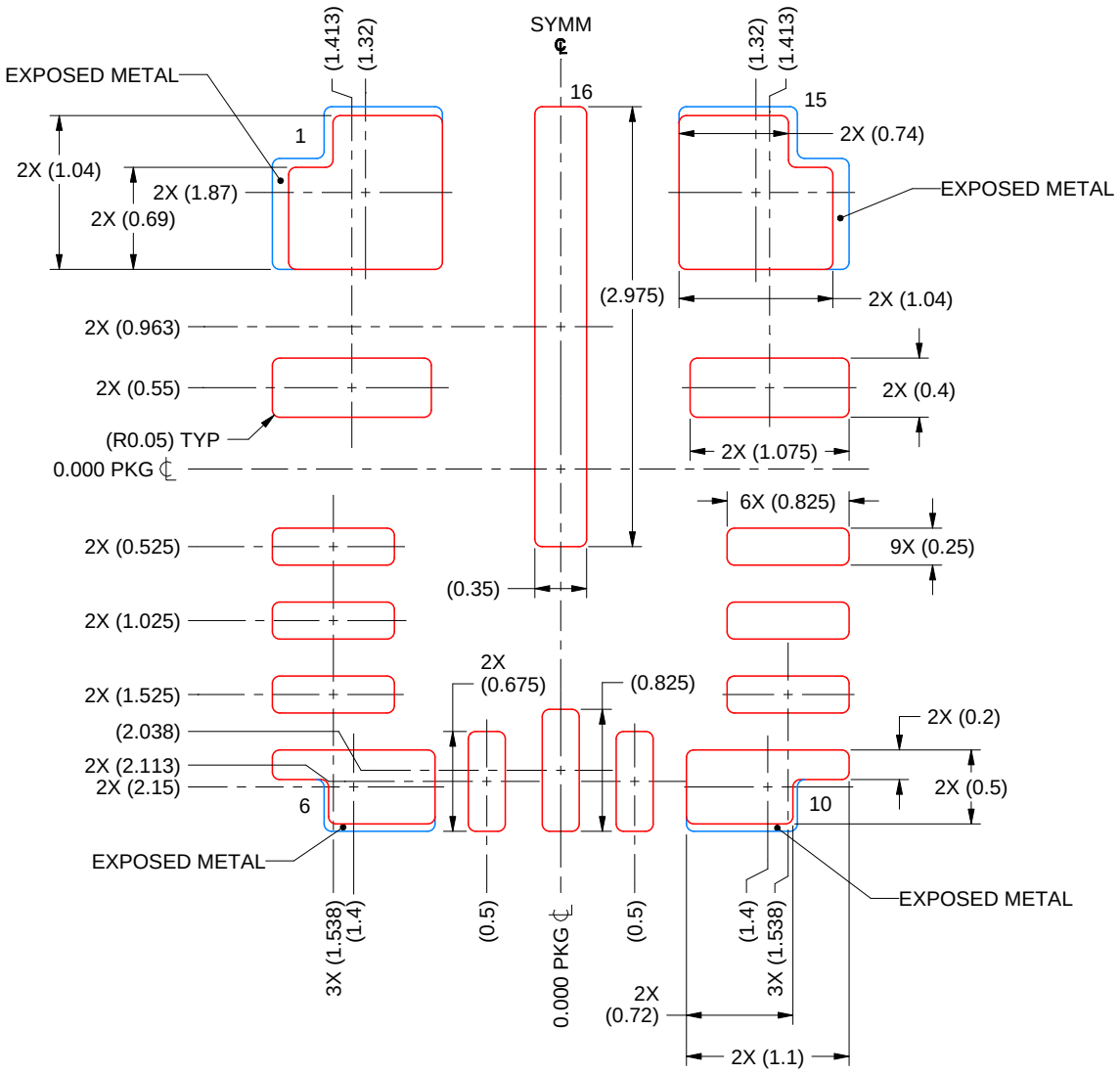
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

PADS 1 & 15:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 10:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224442/A 08/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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