LMV771/LMV772/LMV772Q/LMV774 Single/Dual/Quad, Low Offset, Low Noise, RRO Operational Amplifiers

Check for Samples: LMV771, LMV772, LMV774

FEATURES

- **(Unless otherwise noted, typical values at V_S = 2.7V)**
- **Guaranteed 2.7V and 5V specifications**
- **Maximum V_{OS} (LMV771) 850µV (limit)**
- **Voltage noise**
- **f = 100 Hz 12.5nV/√Hz**
- **f = 10 kHz 7.5nV/√Hz**
- **Rail-to-Rail output swing**
- **R_L = 600Ω 100mV from rail**
- **R_L = 2kΩ 50mV from rail**
- **Open loop gain with R_L = 2kΩ 100dB**
- **V_{CM} 0 to V^+ −0.9V**
- **Supply current (per amplifier) 550µA**
- **Gain bandwidth product 3.5MHz**
- **Temperature range −40°C to 125°C**
- **LMV772Q is AEC-Q100 Grade 1 qualified and is manufactured on Automotive grade flow**

APPLICATIONS

- **Transducer amplifier**
- **Instrumentation amplifier**
- **Precision current sensing**
- **Data acquisition systems**
- **Active filters and buffers**
- **Sample and hold**
- **Portable/battery powered electronics**
- **Automotive**

DESCRIPTION

The LMV771/LMV772/LMV772Q/LMV774 are Single, Dual, and Quad low noise precision operational amplifiers intended for use in a wide range of applications. Other important characteristics of the family include: an extended operating temperature range of −40°C to 125°C, the tiny SC70-5 package for the LMV771, and low input bias current.

The extended temperature range of −40°C to 125°C allows the LMV771/LMV772/LMV772Q/LMV774 to accommodate a broad range of applications. The LMV771 expands National Semiconductor's Silicon Dust™ amplifier portfolio offering enhancements in size, speed, and power savings. The LMV771/LMV772/LMV772Q/LMV774 are guaranteed to operate over the voltage range of 2.7V to 5.0V and all have rail-to-rail output.

The LMV771/LMV772/LMV772Q/LMV774 family is designed for precision, low noise, low voltage, and miniature systems. These amplifiers provide rail-to-rail output swing into heavy loads. The maximum input offset voltage for the LMV771 is 850 µV at room temperature and the input common mode voltage range includes ground.

The LMV771 is offered in the tiny SC70-5 package, LMV772/LMV772Q in the space saving MSOP-8 and SOIC-8, and the LMV774 in TSSOP-14.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Silicon Dust is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2010, Texas Instruments Incorporated

Connection Diagram

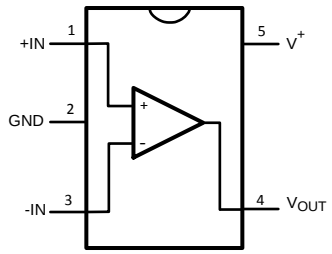
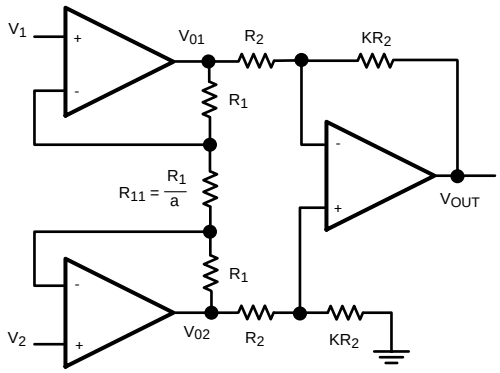


Figure 1. SC70-5 (Top View)

Instrumentation Amplifier



$$V_O = -K\,(2a + 1)\,(V_1 - V_2) \quad (1)$$

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2004–2010, Texas Instruments Incorporated

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Machine Model	200V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Voltage at Input Pins	(V^+) + 0.3V, (V^-) – 0.3V
Current at Input Pins	±10 mA
Supply Voltage $(V^+–V^-)$	5.75V
Output Short Circuit to V^+	(3)
Output Short Circuit to V^-	(4)
Mounting Temperture	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp (10 sec)	260°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature (5)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 20 pF.
(3) Shorting output to V^+ will adversely affect reliability.
(4) Shorting output to V^- will adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}–T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings (1)

Supply Voltage	2.7V to 5.5V
Temperature Range	−40°C to 125°C
Thermal Resistance (θ_{JA})	
SC70-5 Package	440 °C/W
8-Pin MSOP	235°C/W
8-Pin SOIC	190°C/W
14-Pin TSSOP	155°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Copyright © 2004–2010, Texas Instruments Incorporated

2.7V DC Electrical Characteristics (1)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMV771		0.3	0.85 **1.0**	mV
		LMV772/LMV772Q/LMV774		0.3	1.0 **1.2**	
TCV_{OS}	Input Offset Voltage Average Drift			−0.45		µV/°C
I_B	Input Bias Current (4)	V_{CM} = 1V		−0.1	100 **250**	pA
I_{OS}	Input Offset Current (4)			0.004	100	pA
I_S	Supply Current (Per Amplifier)			550	900 **910**	µA
CMRR	Common Mode Rejection Ratio	0.5 ≤ V_{CM} ≤ 1.2V	74 **72**	80		dB
PSSR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V	82 **76**	90		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	0		1.8	V
A_V	Large Signal Voltage Gain (5)	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V, (6)	92 **80**	100		dB
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V, (7)	98 **86**	100		
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ± 100mV, (6)	0.11 **0.14**	0.084 to 2.62	2.59 **2.56**	V
		R_L = 2kΩ to 1.35V V_{IN} = ± 100mV, (7)	0.05 **0.06**	0.026 to 2.68	2.65 **2.64**	
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	18 **11**	24		mA
		Sinking, V_O = 2.7V V_{IN} = −100mV	18 **11**	22		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Limits guaranteed by design.
(5) R_L is connected to mid-supply. The output voltage is set at 200mV from the rails. V_O = GND + 0.2V and V_O = V^+ −0.2V
(6) For LMV772/LMV772Q/LMV774, temperature limits apply to −40°C to 85°C.
(7) For LMV772/LMV772Q/LMV774, temperature limits apply to −40°C to 85°C. If R_L is relaxed to 10 kΩ, then for LMV772/LMV772Q/LMV774 temperature limits apply to −40°C to 125°C.

Copyright © 2004–2010, Texas Instruments Incorporated

2.7V AC Electrical Characteristics [1]

Unless otherwise specified, all limits are guaranteed for T_A = 25°C. V^+ = 5.0V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
SR	Slew Rate [4]	A_V = +1, R_L = 10 kΩ		1.4		V/µs
GBW	Gain-Bandwidth Product			3.5		MHz
Φ_m	Phase Margin			79		Deg
G_m	Gain Margin			−15		dB
e_n	Input-Referred Voltage Noise (Flatband)	f = 10kHz		7.5		nV/√Hz
e_n	Input-Referred Voltage Noise (l/f)	f = 100Hz		12.5		nV/√Hz
i_n	Input-Referred Current Noise	f = 1kHz		0.001		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1 V_{PP}		0.007		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) The number specified is the slower of positive and negative slew rates.

Copyright © 2004–2010, Texas Instruments Incorporated

5.0V DC Electrical Characteristics (1)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C. V^+ = 5.0V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMV771		0.25	0.85 **1.0**	mV
		LMV772/LMV772Q/LMV774		0.25	1.0 **1.2**	
TCV_{OS}	Input Offset Voltage Average Drift			−0.35		µV/°C
I_B	Input Bias Current (4)	V_{CM} = 1V		−0.23	100 **250**	pA
I_{OS}	Input Offset Current (4)			0.017	100	pA
I_S	Supply Current (Per Amplifier)			600	950 **960**	µA
CMRR	Common Mode Rejection Ratio	0.5 ≤ V_{CM} ≤ 3.5V	80 **79**	90		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V	82 **76**	90		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	0		4.1	V
A_V	Large Signal Voltage Gain (5)	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V, (6)	92 **89**	100		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V, (7)	98 **95**	100		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ± 100mV, (6)	0.15 **0.23**	0.112 to 4.9	4.85 **4.77**	V
		R_L = 2kΩ to 2.5V V_{IN} = ± 100mV, (7)	0.06 **0.07**	0.035 to 4.97	4.94 **4.93**	
I_O	Output Short Circuit Current (4) (8)	Sourcing, V_O = 0V V_{IN} = 100mV	35 **35**	75		mA
		Sinking, V_O = 2.7V V_{IN} = −100mV	35 **35**	66		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Limits guaranteed by design.
(5) R_L is connected to mid-supply. The output voltage is set at 200mV from the rails. V_O = GND + 0.2V and V_O = V^+ −0.2V
(6) For LMV772/LMV772Q/LMV774, temperature limits apply to −40°C to 85°C.
(7) For LMV772/LMV772Q/LMV774, temperature limits apply to −40°C to 85°C. If R_L is relaxed to 10 kΩ, then for LMV772/LMV772Q/LMV774 temperature limits apply to −40°C to 125°C.
(8) Continuous operation of the device with an output short circuit current larger than 35mA may cause permanent damage to the device.

Copyright © 2004–2010, Texas Instruments Incorporated

5.0V AC Electrical Characteristics [1]

Unless otherwise specified, all limits are guaranteed for T_A = 25°C. V^+ = 5.0V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
SR	Slew Rate [4]	A_V = +1, R_L = 10 kΩ		1.4		V/µs
GBW	Gain-Bandwidth Product			3.5		MHz
Φ_m	Phase Margin			79		Deg
G_m	Gain Margin			−15		dB
e_n	Input-Referred Voltage Noise (Flatband)	f = 10kHz		6.5		nV/√Hz
e_n	Input-Referred Voltage Noise (l/f)	f = 100Hz		12		nV/√Hz
i_n	Input-Referred Current Noise	f = 1kHz		0.001		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1 V_{PP}		0.007		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) The number specified is the slower of positive and negative slew rates.

Connection Diagrams

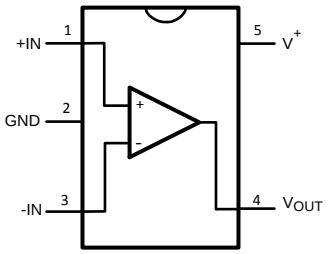


Figure 2. SC70-5 (Top View)

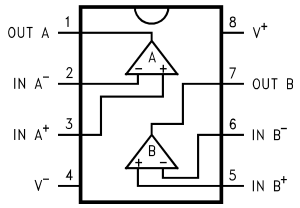


Figure 3. 8-Pin MSOP/SOIC (Top View)

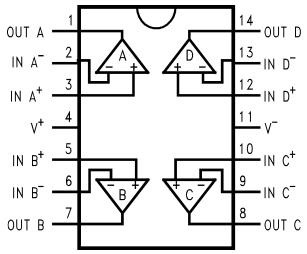
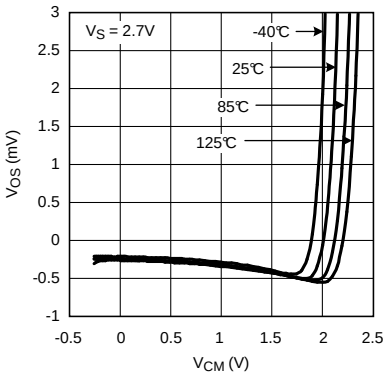


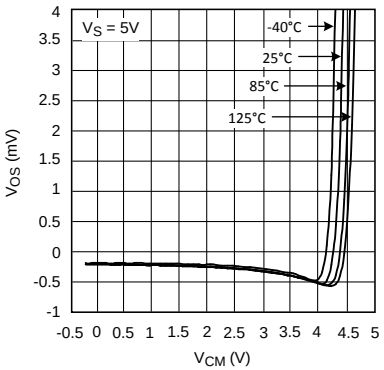
Figure 4. 14-Pin TSSOP (Top View)

Typical Performance Characteristics

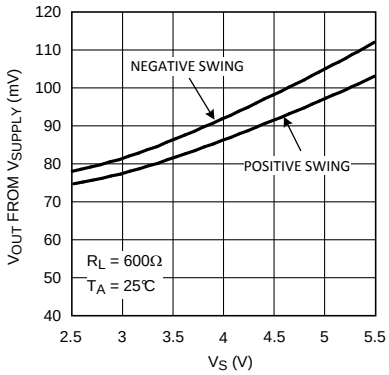
V_{OS} vs. V_{CM} Over Temperature



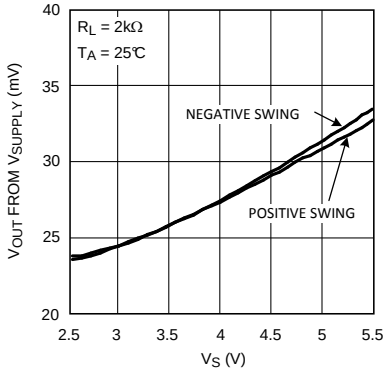
V_{OS} vs. V_{CM} Over Temperature



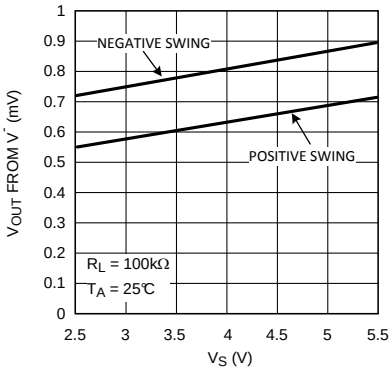
Output Swing vs. V_S



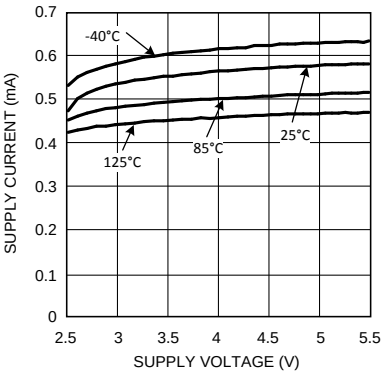
Output Swing vs. V_S



Output Swing vs. V_S



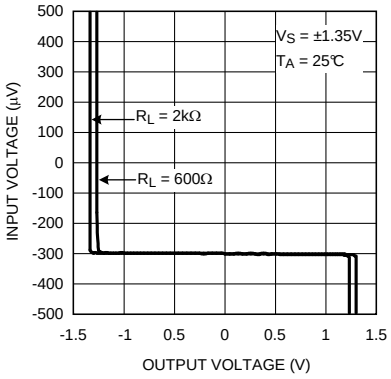
I_S vs. V_S Over Temperature



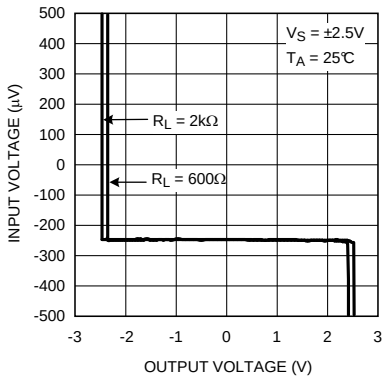
Copyright © 2004–2010, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

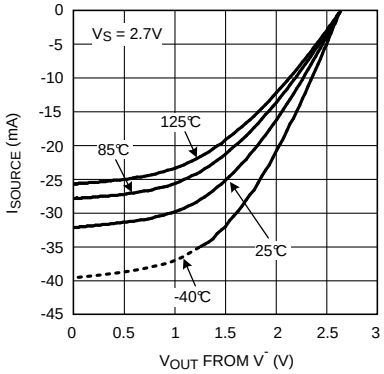
V_{IN} vs. V_{OUT}



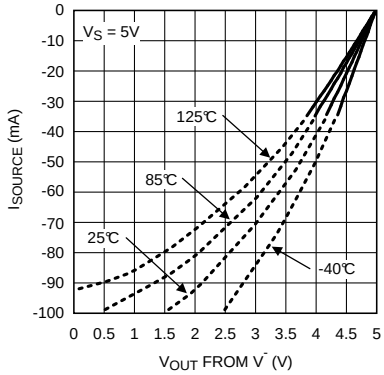
V_{IN} vs. V_{OUT}



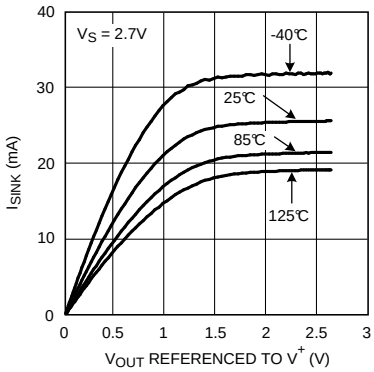
Sourcing Current vs. V_{OUT} (1)



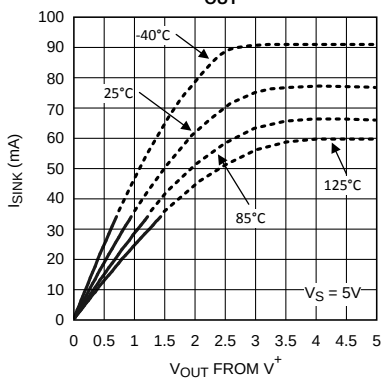
Sourcing Current vs. V_{OUT} (1)



Sinking Current vs. V_{OUT} (2)



Sinking Current vs. V_{OUT} (2)

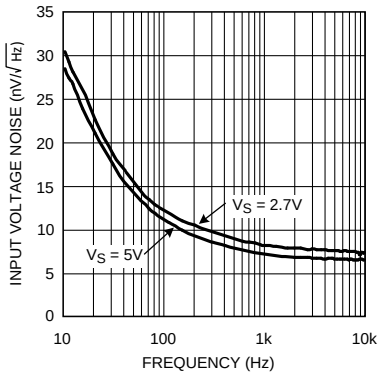


(1) Continuous operation of the device with an output short circuit current larger than 35mA may cause permanent damage to the device.
(2) Continuous operation of the device with an output short circuit current larger than 35mA may cause permanent damage to the device.

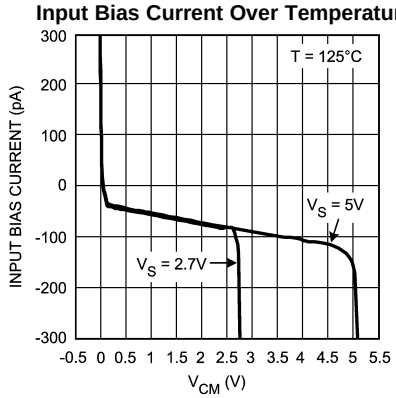
Copyright © 2004–2010, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

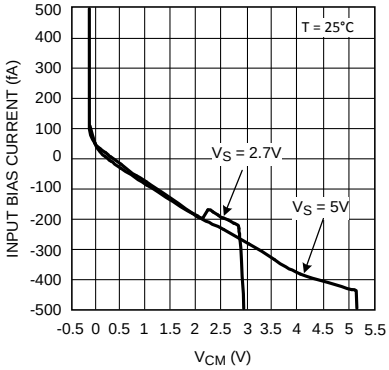
Input Voltage Noise vs. Frequency



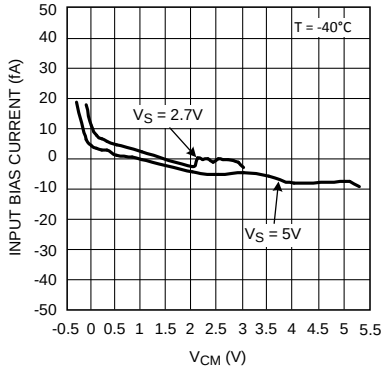
Input Bias Current Over Temperature



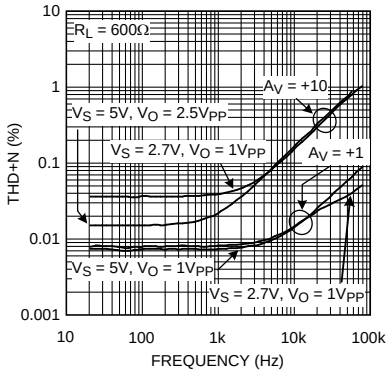
Input Bias Current Over Temperature



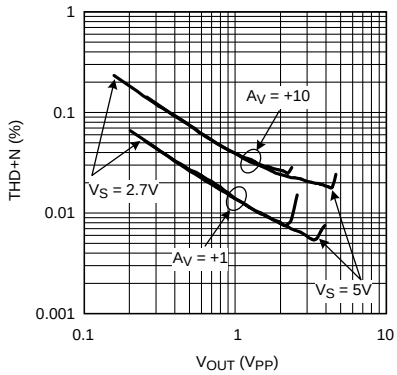
Input Bias Current Over Temperature



THD+N vs. Frequency



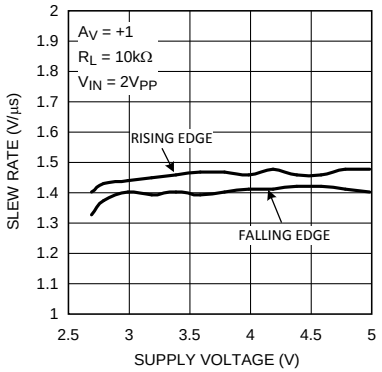
THD+N vs. V_{OUT}



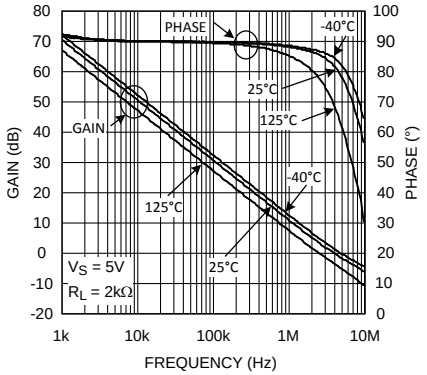
Copyright © 2004–2010, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

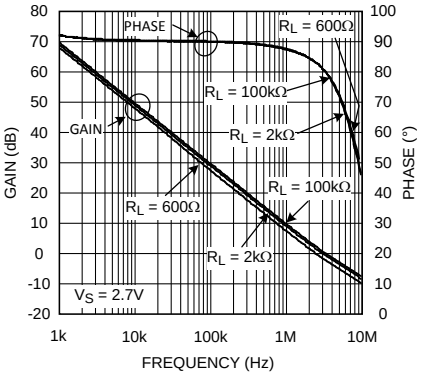
Slew Rate vs. Supply Voltage



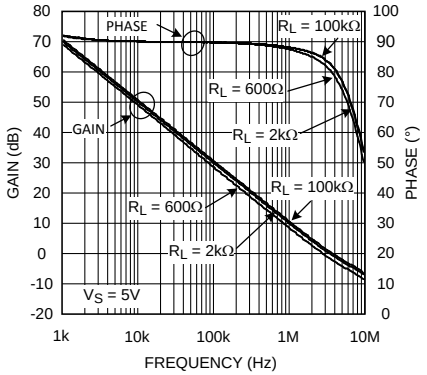
Open Loop Frequency Response Over Temperature



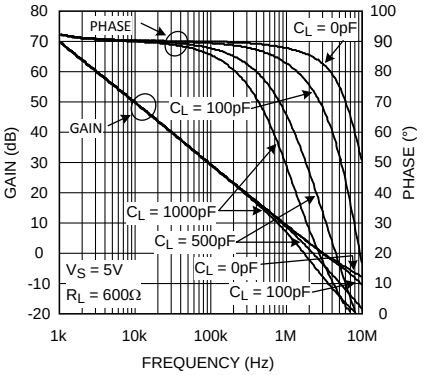
Open Loop Frequency Response



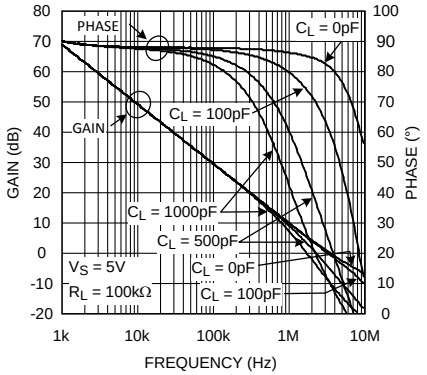
Open Loop Frequency Response



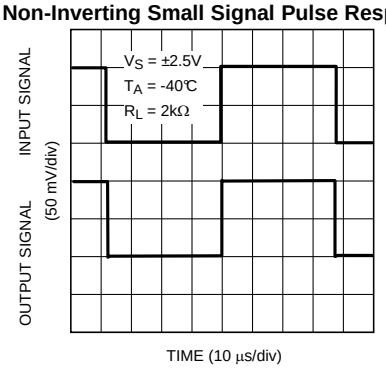
Open Loop Gain & Phase with Cap. Loading



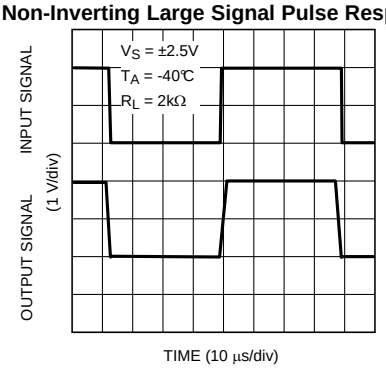
Open Loop Gain & Phase with Cap. Loading



Non-Inverting Small Signal Pulse Response



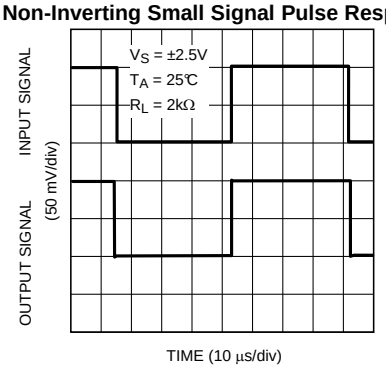
Non-Inverting Large Signal Pulse Response



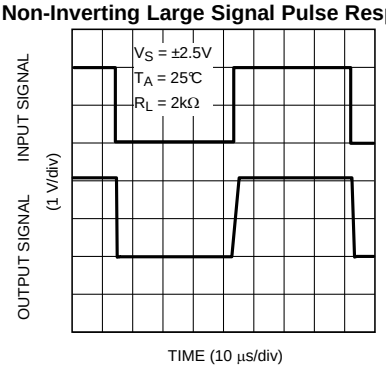
Copyright © 2004–2010, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

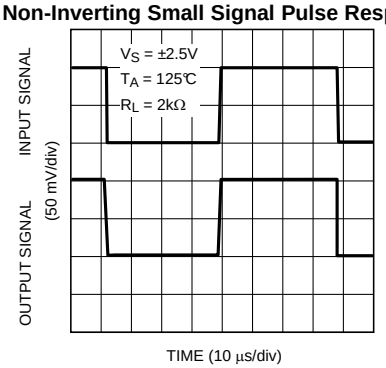
Non-Inverting Small Signal Pulse Response



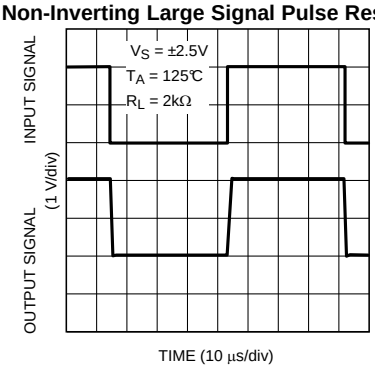
Non-Inverting Large Signal Pulse Response



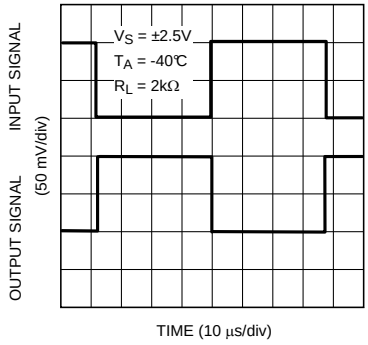
Non-Inverting Small Signal Pulse Response



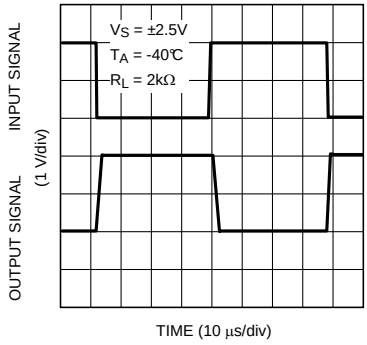
Non-Inverting Large Signal Pulse Response



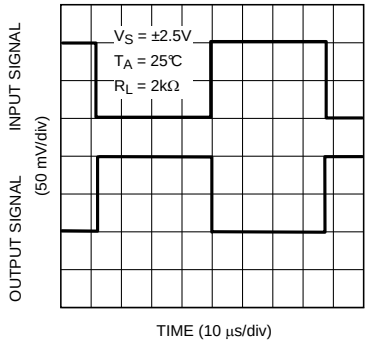
Inverting Small Signal Pulse Response



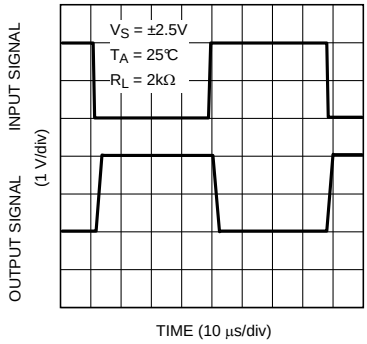
Inverting Large Signal Pulse Response



Inverting Small Signal Pulse Response



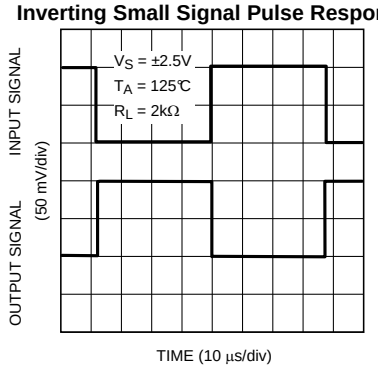
Inverting Large Signal Pulse Response



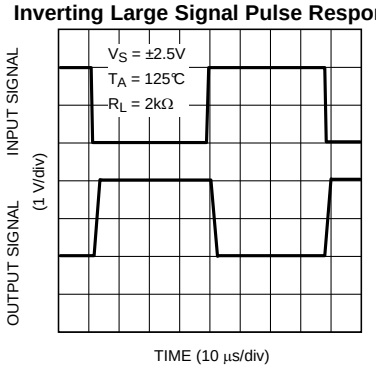
Copyright © 2004–2010, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

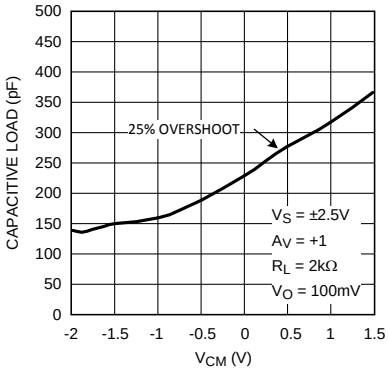
Inverting Small Signal Pulse Response



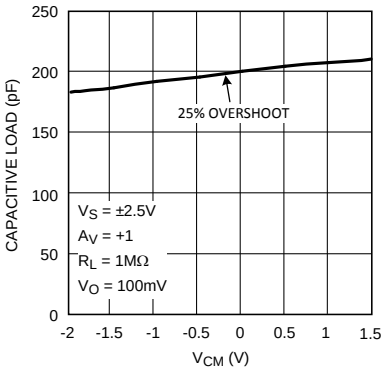
Inverting Large Signal Pulse Response



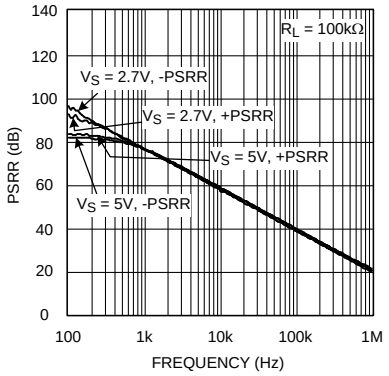
Stability vs. V_{CM}



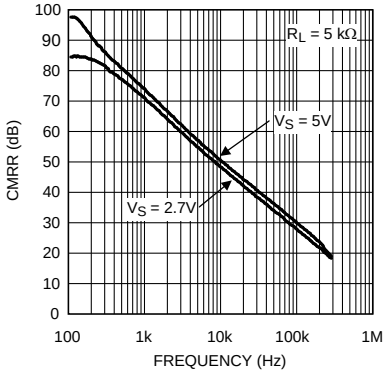
Stability vs. V_{CM}



PSRR vs. Frequency

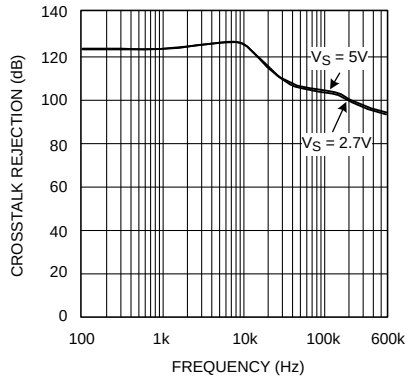


CMRR vs. Frequency



Typical Performance Characteristics (continued)

Crosstalk Rejection vs. Frequency (LMV772/LMV772Q/LMV774)



Application Note

LMV771/LMV772/LMV772Q/LMV774

The LMV771/LMV772LMV772Q/LMV774 are a family of precision amplifiers with very low noise and ultra low offset voltage. LMV771/LMV772/LMV772Q/LMV774's extended temperature range of −40°C to 125°C enables the user to design this family of products into a variety of applications including automotive.

The LMV771 has a maximum offset voltage of 1mV over the extended temperature range. This makes the LMV771 ideal for applications where precision is important.

The LMV772/LMV772Q/LMV774 have a maximum offset voltage of 1mV at room temperature and 1.2mV over the extended temperature range of −40°C to 125°C. Care must be taken when the LMV772/LMV772Q/LMV774 are designed into applications with heavy loads under extreme temperature conditions. As indicated in the DC tables, the LMV772/LMV772Q/LMV774's gain and output swing may be reduced at temperatures between 85°C and 125°C with loads heavier than 2kΩ.

INSTRUMENTATION AMPLIFIER

Measurement of very small signals with an amplifier requires close attention to the input impedance of the amplifier, gain of the overall signal on the inputs, and the gain on each input since we are only interested in the difference of the two inputs and the common signal is considered noise. A classic solution is an instrumentation amplifier. Instrumentation amplifiers have a finite, accurate, and stable gain. Also they have extremely high input impedances and very low output impedances. Finally they have an extremely high CMRR so that the amplifier can only respond to the differential signal. A typical instrumentation amplifier is shown in Figure 5.

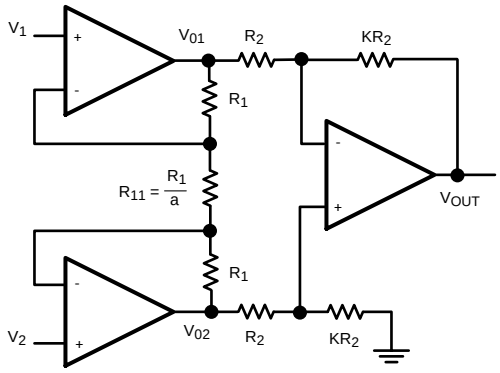


Figure 5. Instrumentation Amplifier

Copyright © 2004–2010, Texas Instruments Incorporated

There are two stages in this amplifier. The last stage, output stage, is a differential amplifier. In an ideal case the two amplifiers of the first stage, input stage, would be set up as buffers to isolate the inputs. However they cannot be connected as followers because of real amplifier's mismatch. That is why there is a balancing resistor between the two. The product of the two stages of gain will give the gain of the instrumentation amplifier. Ideally, the CMRR should be infinite. However the output stage has a small non-zero common mode gain which results from resistor mismatch.

In the input stage of the circuit, current is the same across all resistors. This is due to the high input impedance and low input bias current of the LMV771. With the node equations we have:

$$\text{GIVEN: } I_{R_1} = I_{R_{11}} \tag{2}$$

By Ohm's Law:

$$\begin{aligned} V_{O1} - V_{O2} &= (2R_1 + R_{11})\, I_{R_{11}} \\ &= (2a + 1)\, R_{11} \bullet I_{R_{11}} \\ &= (2a + 1)\, V_{R_{11}} \end{aligned} \tag{3}$$

However:

$$V_{R_{11}} = V_1 - V_2 \tag{4}$$

So we have:

$$V_{O1} - V_{O2} = (2a + 1)\,(V_1 - V_2) \tag{5}$$

Now looking at the output of the instrumentation amplifier:

$$\begin{aligned} V_O &= \frac{KR_2}{R_2}\,(V_{O2} - V_{O1}) \\ &= -K\,(V_{O1} - V_{O2}) \end{aligned} \tag{6}$$

Substituting from Equation 5:

$$V_O = -K\,(2a + 1)\,(V_1 - V_2) \tag{7}$$

This shows the gain of the instrumentation amplifier to be:

$$-K(2a+1) \tag{8}$$

Typical values for this circuit can be obtained by setting: a = 12 and K= 4. This results in an overall gain of −100.

Figure 6 shows typical CMRR characteristics of this Instrumentation amplifier over frequency. Three LMV771 amplifiers are used along with 1% resistors to minimize resistor mismatch. Resistors used to build the circuit are: R_1 = 21.6kΩ, R_{11} = 1.8kΩ, R_2 = 2.5kΩ with K = 40 and a = 12. This results in an overall gain of −1000, −K(2a+1) = −1000.

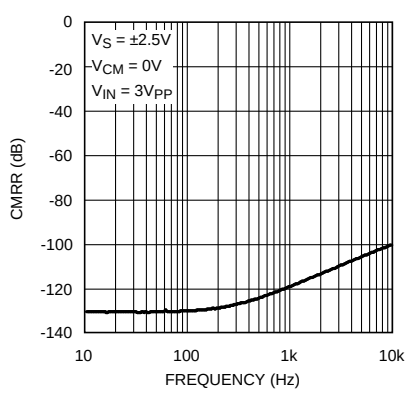


Figure 6. CMRR vs. Frequency

ACTIVE FILTER

Active filters are circuits with amplifiers, resistors, and capacitors. The use of amplifiers instead of inductors, which are used in passive filters, enhances the circuit performance while reducing the size and complexity of the filter.

The simplest active filters are designed using an inverting op amp configuration where at least one reactive element has been added to the configuration. This means that the op amp will provide "frequency-dependent" amplification, since reactive elements are frequency dependent devices.

LOW PASS FILTER

The following shows a very simple low pass filter.

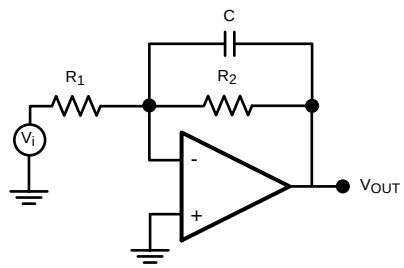


Figure 7. Lowpass Filter

The transfer function can be expressed as follows:

By KCL:

$$\frac{-V_i}{R_1} - \frac{V_O}{\left[\frac{1}{jwc}\right]} - \frac{V_O}{R_2} = O \tag{9}$$

Simplifying this further results in:

$$V_O = \frac{-R_2}{R_1}\left[\frac{1}{jwcR_2 + 1}\right] V_i \tag{10}$$

or

$$\frac{V_O}{V_i} = \frac{-R_2}{R_1}\left[\frac{1}{jwcR_2 + 1}\right] \tag{11}$$

Now, substituting ω=2πf, so that the calculations are in f(Hz) and not ω(rad/s), and setting the DC gain $H_O = -R_2/R_1$ and $H = V_O/V_i$

$$H = H_O\left[\frac{1}{j2\pi fcR_2 + 1}\right] \tag{12}$$

Set: $f_o = 1/(2\pi R_1 C)$

$$H = H_O\left[\frac{1}{1 + j\,(f/f_o)}\right] \tag{13}$$

Low pass filters are known as lossy integrators because they only behave as an integrator at higher frequencies. Just by looking at the transfer function one can predict the general form of the bode plot. When the f/f_O ratio is small, the capacitor is in effect an open circuit and the amplifier behaves at a set DC gain. Starting at f_O, −3dB corner, the capacitor will have the dominant impedance and hence the circuit will behave as an integrator and the signal will be attenuated and eventually cut. The bode plot for this filter is shown in the following picture:

Copyright © 2004–2010, Texas Instruments Incorporated

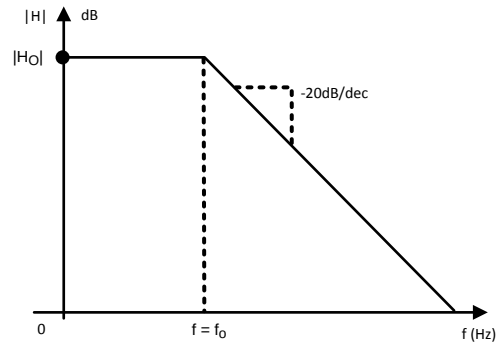


Figure 8. Lowpass Filter Transfer Function

HIGH PASS FILTER

In a similar approach, one can derive the transfer function of a high pass filter. A typical first order high pass filter is shown below:

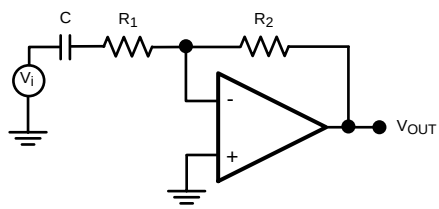


Figure 9. Highpass FIlter

Writing the KCL for this circuit :

(V_1 denotes the voltage between C and R_1)

$$\frac{V_1 - V_i}{\frac{1}{jwC}} = \frac{V_1 - V^-}{R_1} \tag{14}$$

$$\frac{V^- + V_1}{R_1} = \frac{V^- + V_O}{R_2} \tag{15}$$

Solving these two equations to find the transfer function and using:

$$f_O = \frac{1}{2\pi R_1 C} \tag{16}$$

(high frequency gain) $H_O = \frac{-R_2}{R_1}$ and $H = \frac{V_O}{V_i}$

Which results:

$$H = H_O \frac{j\,(f/f_O)}{1 + j\,(f/f_O)} \tag{17}$$

Looking at the transfer function, it is clear that when f/f_O is small, the capacitor is open and hence no signal is getting in to the amplifier. As the frequency increases the amplifier starts operating. At $f = f_O$ the capacitor behaves like a short circuit and the amplifier will have a constant, high frequency, gain of H_O. Figure 10 shows the transfer function of this high pass filter:

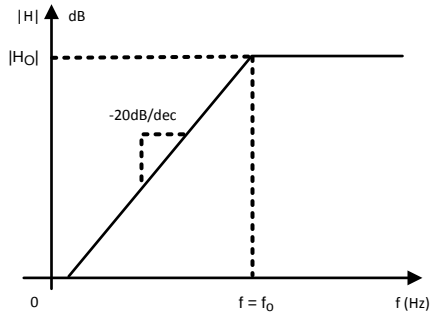


Figure 10. Highpass Filter Transfer Function

BAND PASS FILTER

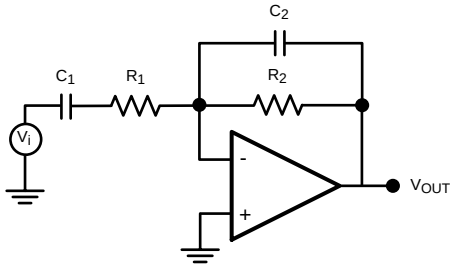


Figure 11. Bandpass Filter

Combining a low pass filter and a high pass filter will generate a band pass filter. In this network the input impedance forms the high pass filter while the feedback impedance forms the low pass filter. Choosing the corner frequencies so that $f_1 < f_2$, then all the frequencies in between, $f_1 \le f \le f_2$, will pass through the filter while frequencies below f_1 and above f_2 will be cut off.

The transfer function can be easily calculated using the same methodology as before.

$$H = H_O \frac{j\,(f/f_1)}{[1 + j\,(f/f_1)]\;[1 + j\,(f/f_2)]} \tag{18}$$

Where

$$f_1 = \frac{1}{2\pi R_1 C_1}$$

$$f_2 = \frac{1}{2\pi R_2 C_2}$$

$$H_O = \frac{-R_2}{R_1} \tag{19}$$

The transfer function is presented in the following figure.

Copyright © 2004–2010, Texas Instruments Incorporated

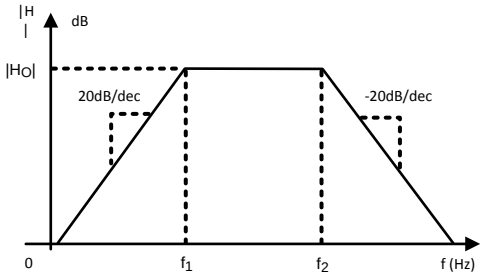


Figure 12. Bandpass filter Transfer Function

STATE VARIABLE ACTIVE FILTER

State variable active filters are circuits that can simultaneously represent high pass, band pass, and low pass filters. The state variable active filter uses three separate amplifiers to achieve this task. A typical state variable active filter is shown in Figure 13. The first amplifier in the circuit is connected as a gain stage. The second and third amplifiers are connected as integrators, which means they behave as low pass filters. The feedback path from the output of the third amplifier to the first amplifier enables this low frequency signal to be fed back with a finite and fairly low closed loop gain. This is while the high frequency signal on the input is still gained up by the open loop gain of the 1st amplifier. This makes the first amplifier a high pass filter. The high pass signal is then fed into a low pass filter. The outcome is a band pass signal, meaning the second amplifier is a band pass filter. This signal is then fed into the third amplifiers input and so, the third amplifier behaves as a simple low pass filter.

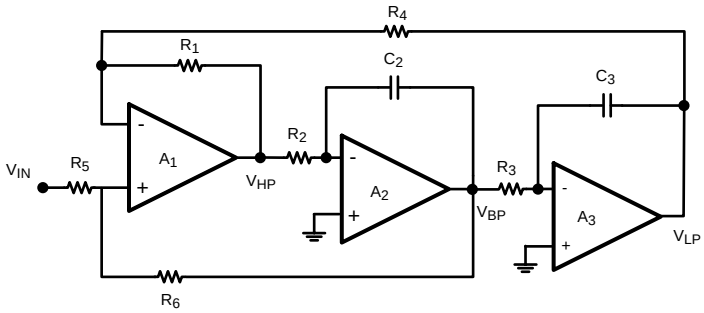
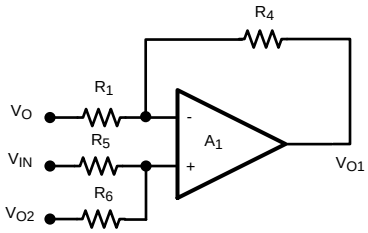
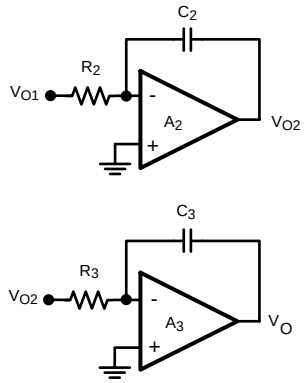


Figure 13. State Variable Active Filter

The transfer function of each filter needs to be calculated. The derivations will be more trivial if each stage of the filter is shown on its own.

The three components are:





For A_1 the relationship between input and output is:

$$V_{O1} = \frac{-R_4}{R_1} V_0 + \left[\frac{R_6}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] V_{IN} + \left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] V_{O2} \tag{20}$$

This relationship depends on the output of all the filters. The input-output relationship for A_2 can be expressed as:

$$V_{O2} = \frac{-1}{s\, C_2 R_2} V_{O1} \tag{21}$$

And finally this relationship for A_3 is as follows:

$$V_O = \frac{-1}{s\, C_3 R_3} V_{O2} \tag{22}$$

Re-arranging these equations, one can find the relationship between V_O and V_{IN} (transfer function of the lowpass filter), V_{O1} and V_{IN} (transfer function of the highpass filter), and V_{O2} and V_{IN} (transfer function of the bandpass filter) These relationships are as follows:

Lowpass Filter

$$\frac{V_O}{V_{IN}} = \frac{\left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right]\left[\frac{1}{C_2C_3R_2R_3}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \tag{23}$$

Highpass Filter

$$\frac{V_{O1}}{V_{IN}} = \frac{s^2\left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \tag{24}$$

Bandpass Filter

$$\frac{V_{O2}}{V_{IN}} = \frac{s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \tag{25}$$

The center frequency and Quality Factor for all of these filters is the same. The values can be calculated in the following manner:

Copyright © 2004–2010, Texas Instruments Incorporated

$$\omega_c = \sqrt{\frac{1}{C_2C_3R_2R_3}}$$

and

$$Q = \sqrt{\frac{C_2R_2}{C_3R_3}}\left[\frac{R_5 + R_6}{R_6}\right]\left[\frac{R_1}{R_1 + R_4}\right] \tag{26}$$

A design example is shown here:

Designing a bandpass filter with center frequency of 10kHz and Quality Factor of 5.5

To do this, first consider the Quality Factor. It is best to pick convenient values for the capacitors. $C_2 = C_3 =$ 1000pF. Also, choose $R_1 = R_4 = 30k\Omega$. Now values of R_5 and R_6 need to be calculated. With the chosen values for the capacitors and resistors, Q reduces to:

$$Q = \frac{11}{2} = \frac{1}{2}\left[\frac{R_5 + R_6}{R_6}\right] \tag{27}$$

or

$$R_5 = 10R_6 \quad R_6 = 1.5k\Omega \quad R_5 = 15k\Omega \tag{28}$$

Also, for f = 10kHz, the center frequency is $\omega_c = 2\pi f = 62.8kHz$.

Using the expressions above, the appropriate resistor values will be $R_2 = R_3 = 16k\Omega$.

The following graphs show the transfer function of each of the filters. The DC gain of this circuit is:

$$\text{DC GAIN} = \left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right] = -14.8\ \text{dB}$$

The frequency responses of each stage of the state variable active filter when implemented with the LMV774 are shown in the following figures:

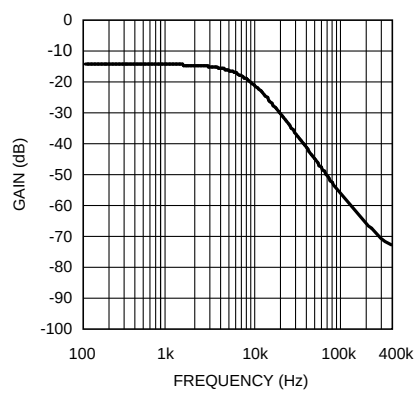


Figure 14. Lowpass Filter Frequency Response

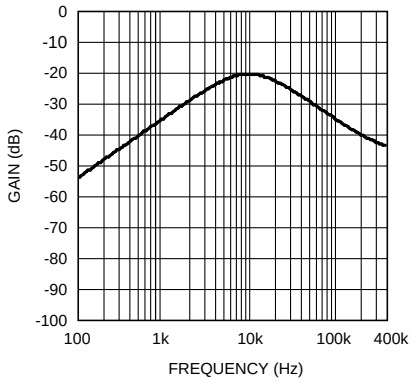


Figure 15. Bandpass Filter Frequency Response

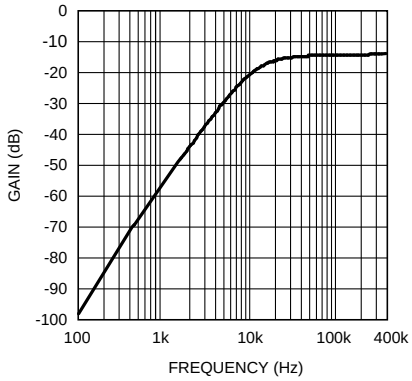


Figure 16. Highpass Filter Frequency Response

Copyright © 2004–2010, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV771MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A75	Samples
LMV771MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A75	Samples
LMV772MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 72MA	Samples
LMV772MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 72MA	Samples
LMV772MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A91A	Samples
LMV772MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A91A	Samples
LMV772QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AJ7A	Samples
LMV772QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AJ7A	Samples
LMV774MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV77 4MT	Samples
LMV774MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV77 4MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV772, LMV772-Q1 :

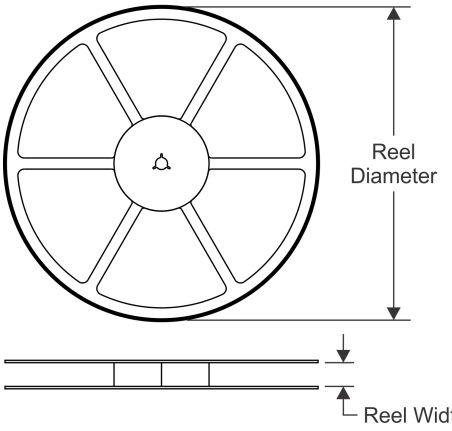
- Catalog: LMV772
- Automotive: LMV772-Q1

NOTE: Qualified Version Definitions:

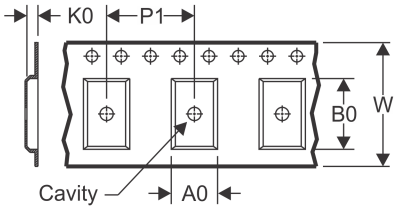
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

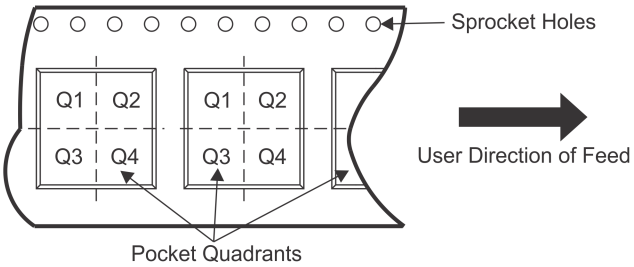


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

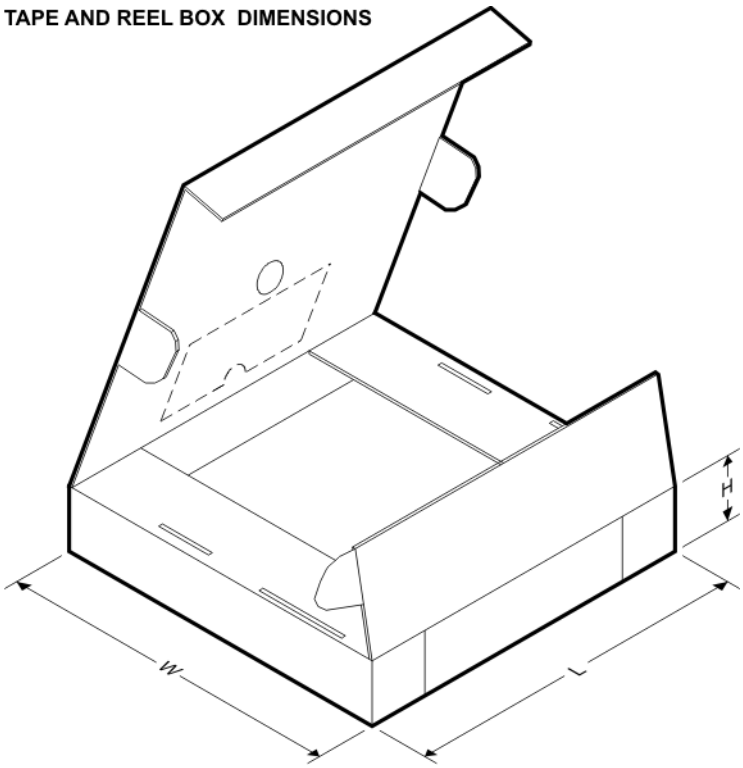
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV771MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV771MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV772MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV772MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV772MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV772QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV772QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV774MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV774MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

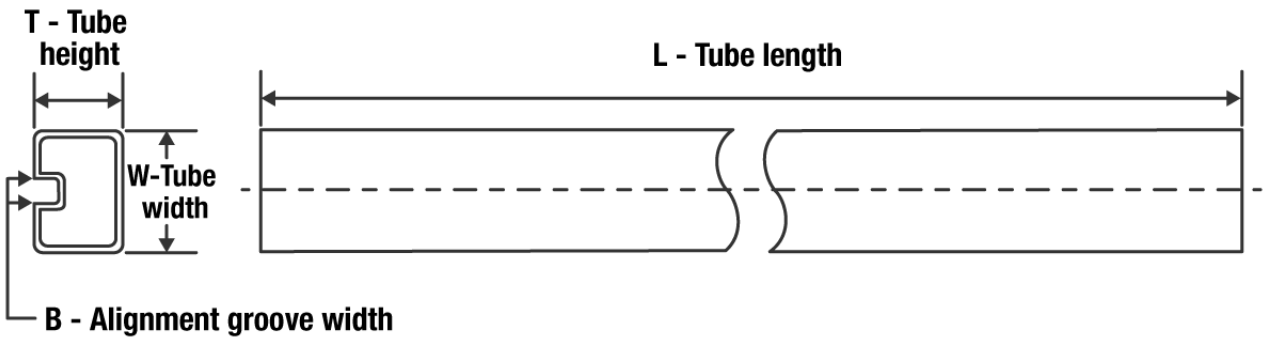
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV771MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV771MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV772MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV772MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV772MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV772QMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV772QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV774MTX/NOPB	TSSOP	PW	14	2500	853.0	449.0	35.0
LMV774MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

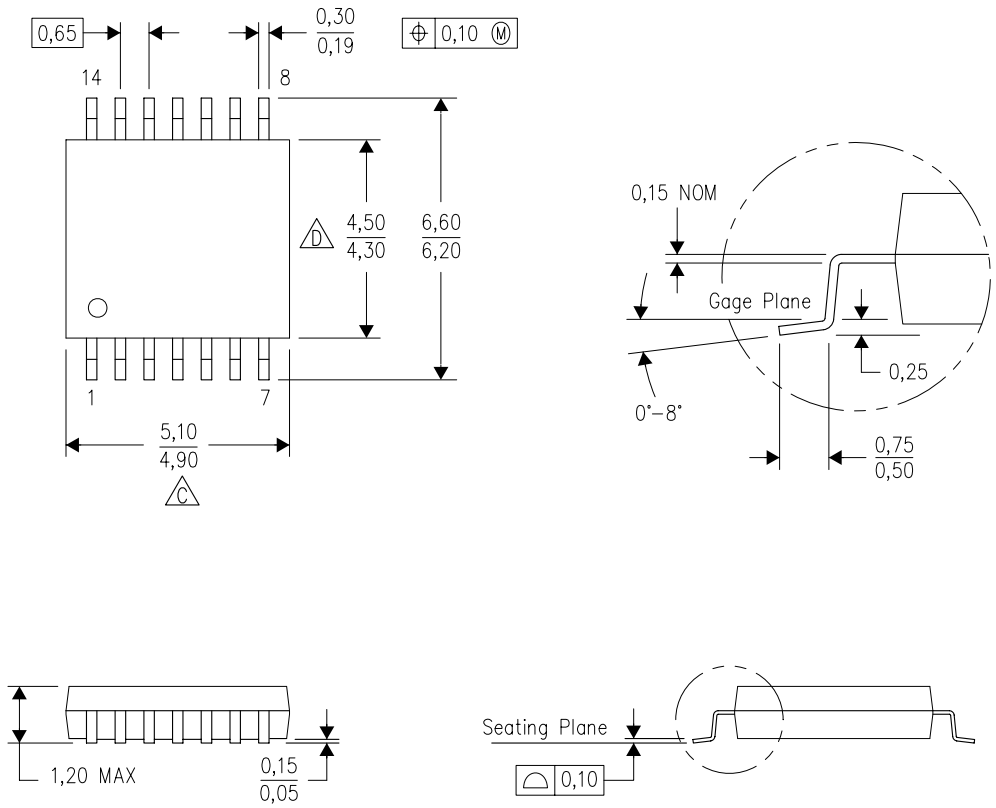
TUBE



*All dimensions are nominal

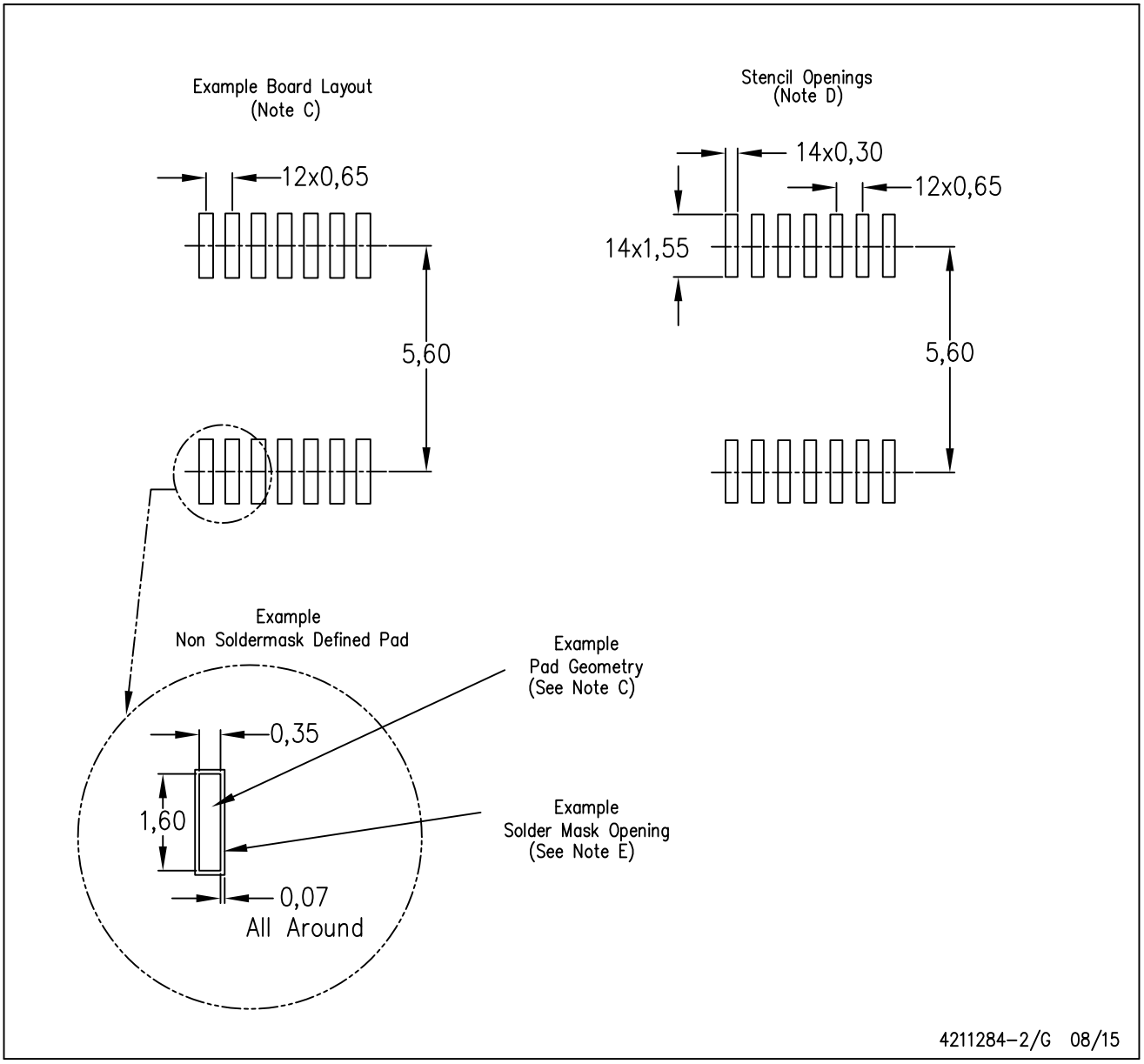
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV772MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV774MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV774MT/NOPB	PW	TSSOP	14	94	530	10.2	3600	3.5

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

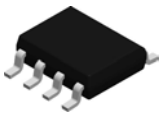


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

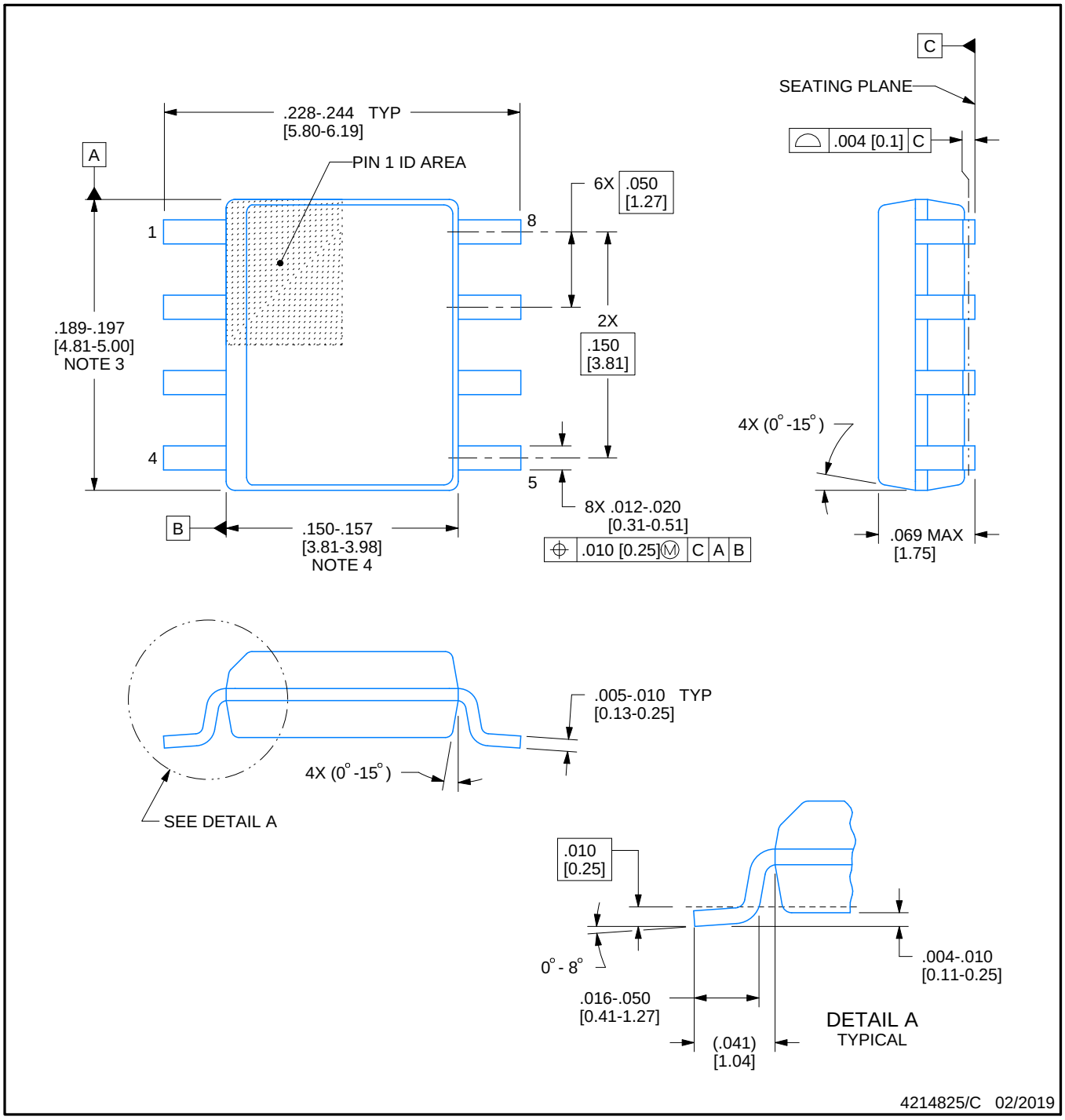


PACKAGE OUTLINE

D0008A

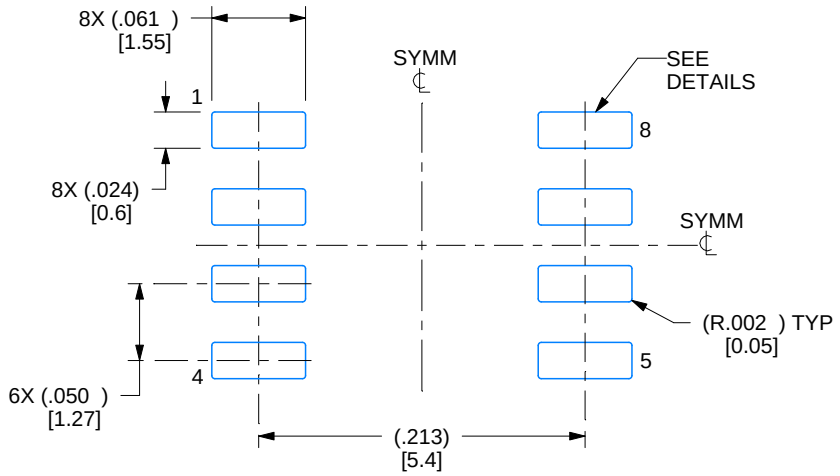
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

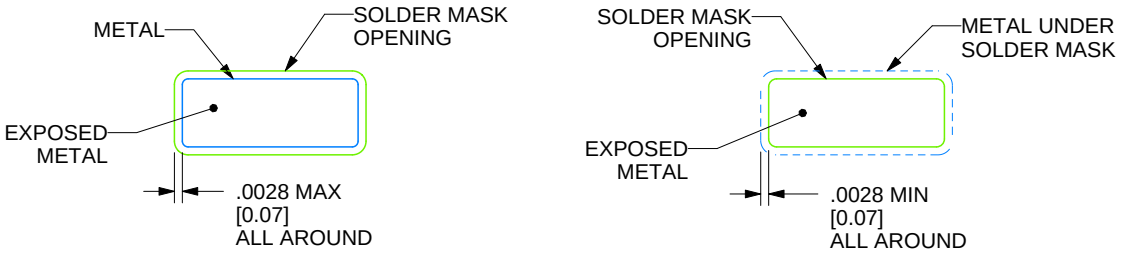


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

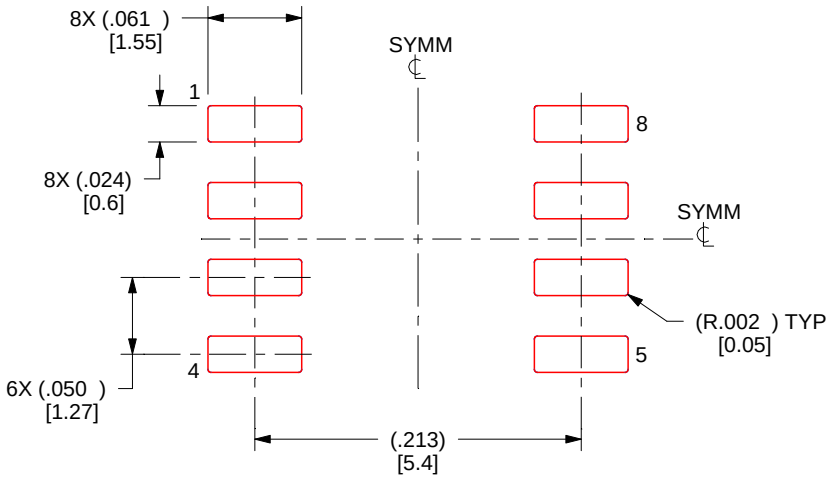


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



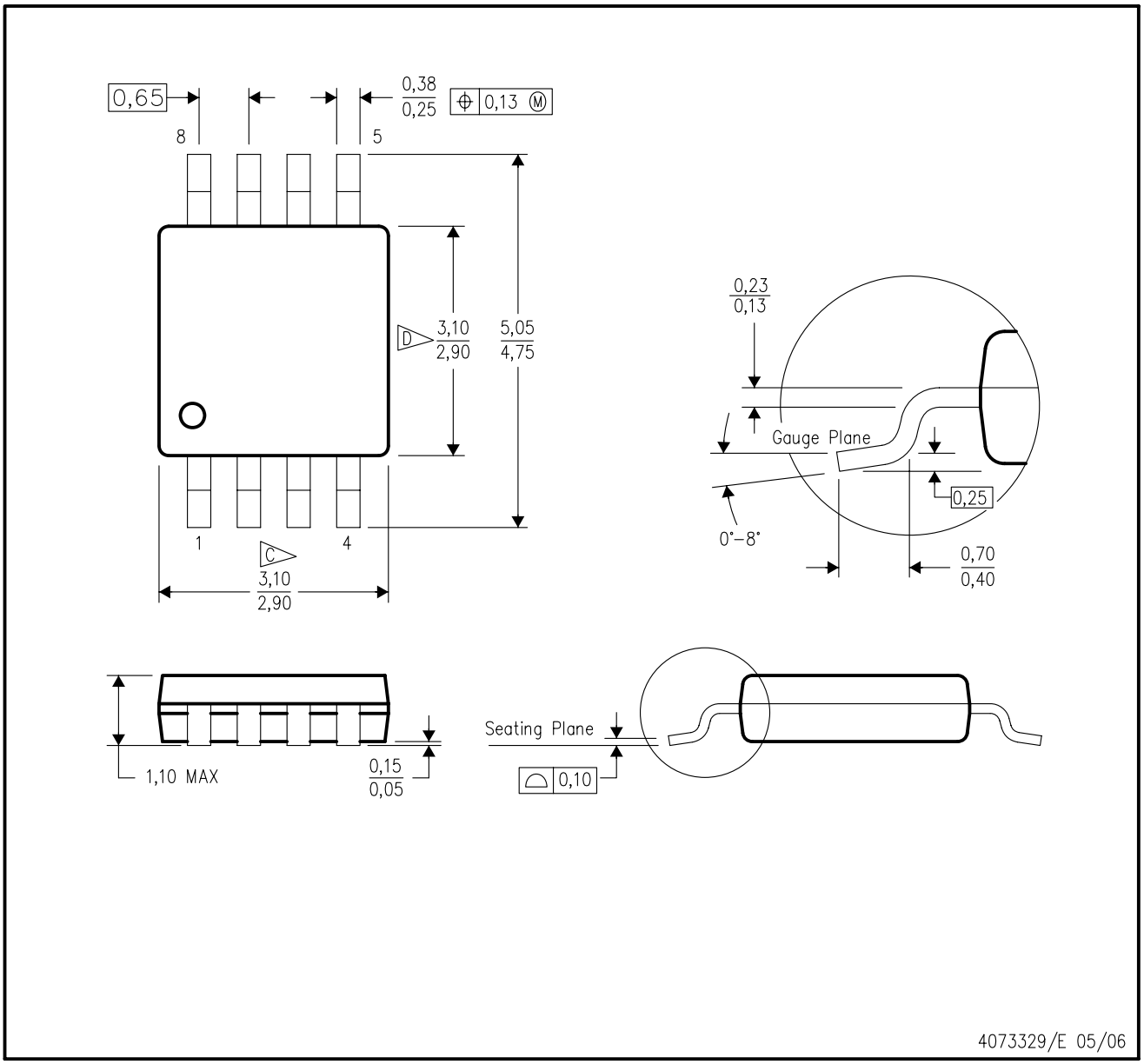
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

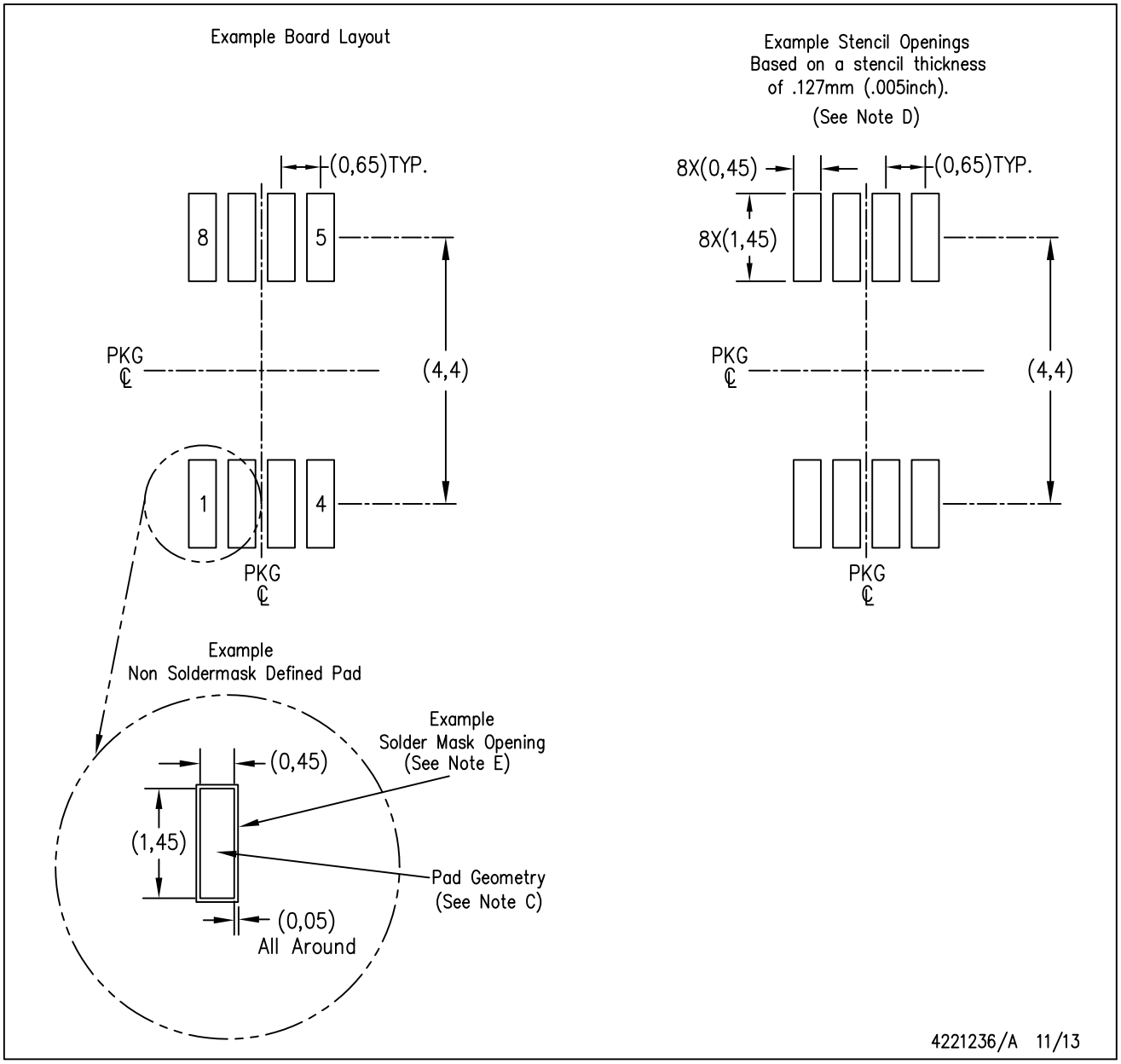
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



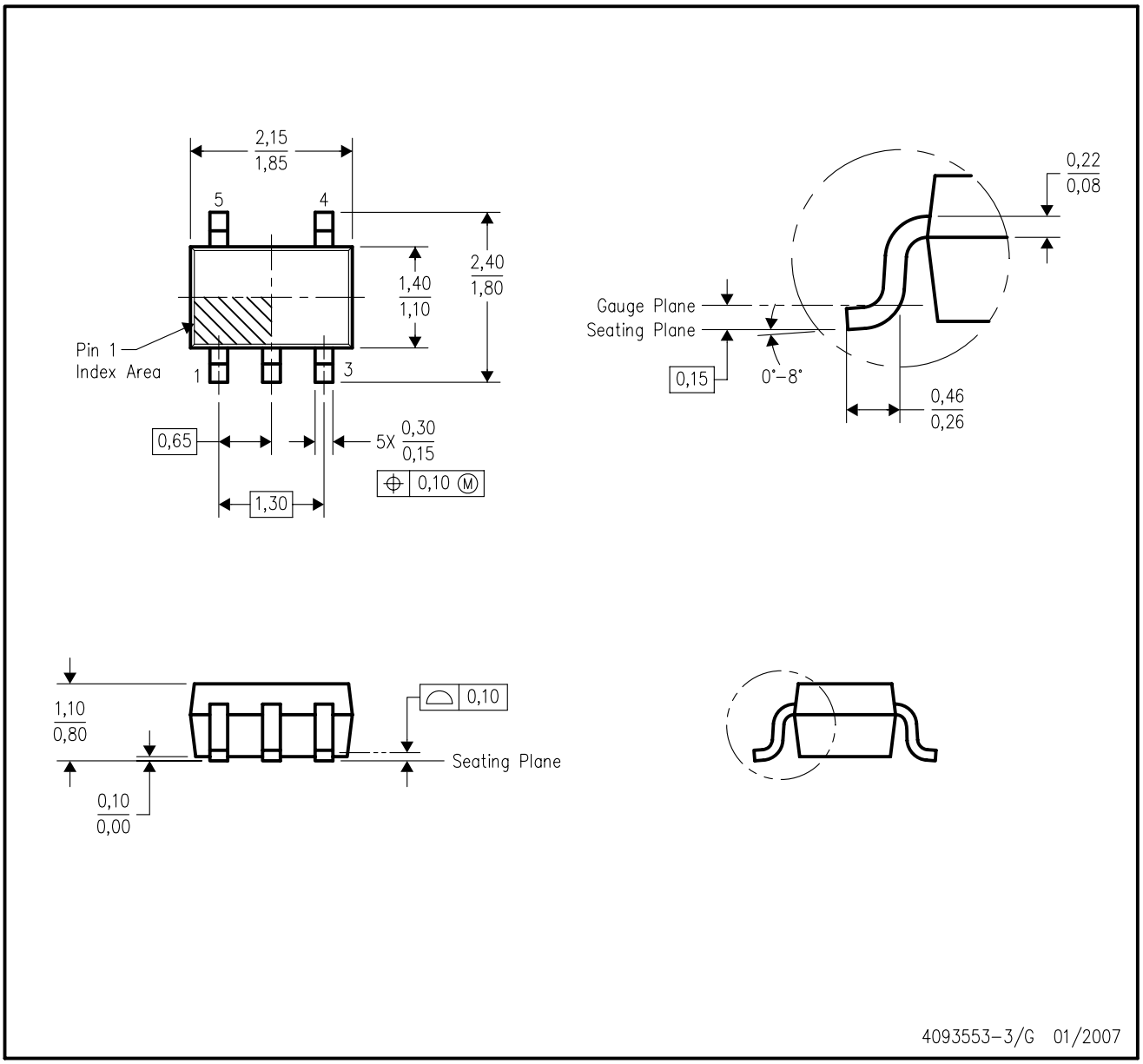
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



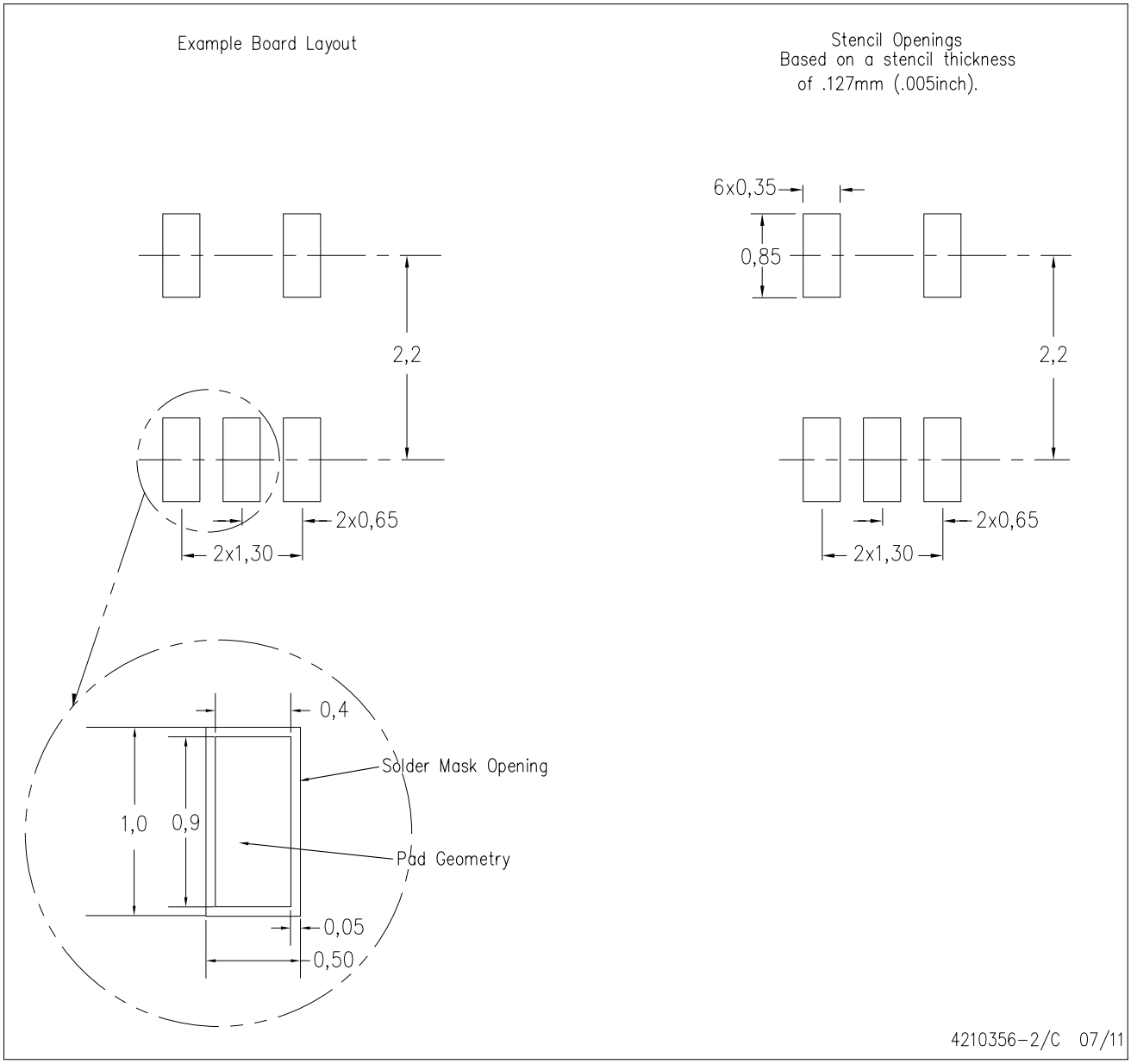
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated