TPD1E6B06 采用 0201 封装的单通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
  - ±15kV 接触放电
  - ±15kV 气隙放电
- IEC 61000-4-5 浪涌：3.8A (8/20μs)
- I/O 电容：6pF（典型值）
- R_{DYN}：0.55Ω（典型值）
- 直流击穿电压：±6V（最小值）
- 低泄漏电流 10nA（典型值）
- 低 ESD 钳位电压
- 工业温度范围：-40°C 至 125°C
- 节省空间的 0201 封装 (0.6mm × 0.3mm × 0.3mm)

2 应用

- 终端设备
  - 移动电话
  - 平板电脑
  - 可穿戴产品
  - 远程控制器
  - 电子销售点 (EPOS)
- 接口
  - 音频线路
  - 通用输入/输出 (GPIO)
  - 按钮

3 说明

TPD1E6B06 器件是一款用于静电放电 (ESD) 保护的单通道瞬态电压抑制器 (TVS) 二极管，采用小型 0201 封装。TPD1E6B06 的额定 ESD 冲击消散值高于 IEC 61000-4-2 4 级国际标准中规定的最高水平，并且具有 ±15kV 接触放电和 ±15kV 气隙 ESD 保护。该器件提供背靠背 TVS 二极管配置以支持双极或双向信号。6pF 线路电容适合为多种应用提供瞬态电压抑制电路保护，支持的数据速率高达 800Mbps。

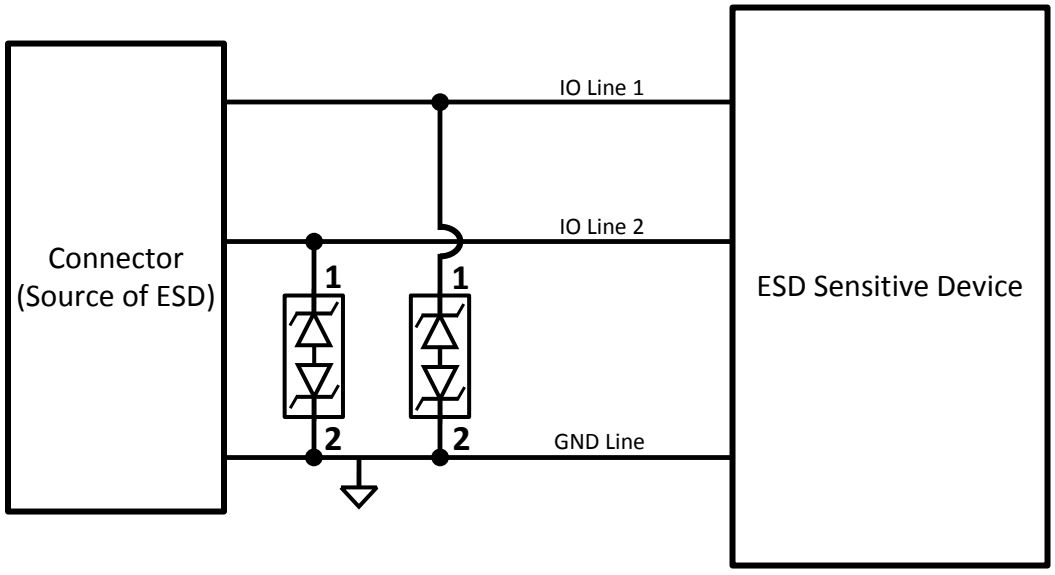
TPD1E6B06 的典型应用接口包括音频线路（麦克风、耳机和扬声器）、SD 接口、键盘或其他按钮以及 USB 端口的 VBUS 和 ID 引脚。TPD1E6B06 采用行业标准 0201 封装，因此体积超小，非常适合手机、平板电脑和可穿戴设备等空间受限类终端设备。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD1E6B06	X2SON (2)	0.60mm x 0.30mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (April 2015) to Revision E — **Page**

- Added test condition frequency to capacitance ... 4
- 已添加 *社区资源* ... 11

Changes from Revision C (February 2013) to Revision D — **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 描述* 部分，*器件功能模式*部分，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision B (August 2012) to Revision C — **Page**

- 更新了订购信息表中的顶部标记。 ... 1

Changes from Revision A (April 2012) to Revision B — **Page**

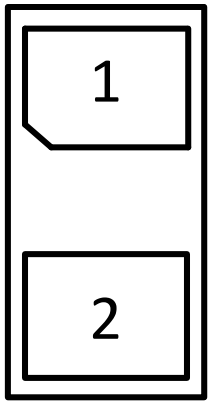
- 已更新 “特性”中的 IEC 61000-4-5（浪涌）值。 ... 1
- 已更新“特性”中的 R_{DYN} 值。 ... 1
- Updated *Absolute Maximum Ratings*. ... 3
- Updated TYPICAL CHARACTERISTICS section. ... 4

Changes from Original (February 2012) to Revision A — **Page**

- 已更改 标题中的 0402 封装至 0201 封装。 ... 1
- 已添加 R_{DYN} 至 特性。 ... 1
- 已更改 支持的数据速率，从 150Mbps 改为 800Mbps （说明 部分） ... 1
- Added I_{LEAK} parameter to the *Electrical Characteristics* table. ... 4
- Changed supporting data rates from 150Mbps to 800Mbps in the DESCRIPTION section.. ... 7

5 Pin Configuration and Functions

DPL Package
2-Pin X2SON
(Top View)



Pin Functions

PIN	I/O	DESCRIPTION
1	I/O	ESD-Protected I/O
2		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{RWM}	Maximum voltage allowed from pin 1 to pin 2, or pin 2 to pin 1	–5	5	V
I_{PP}	Peak pulse current (tp = 8/20 μs)		3.8	A
P_{PP}	Peak pulse power (tp = 8/20 μs)		50	W
T_A	Operating temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		IEC 61000-4-2 contact discharge	±15000	
		IEC 61000-4-2 air-gap discharge	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2500 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A		–40		125	°C
Operating Voltage	Pin 1 to 2 or Pin 2 to 1	–5		5	V

6.4 Thermal Information

THERMAL METRIC(1)		TPD1E6B06 DPL (X2SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	567.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	253.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	379.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{LEAK} = 100 nA			±5	V
I_{LEAK}	Leakage current	Pin 1 = 5 V, Pin 2 = 0 V			100	nA
$V_{Clamp1,2}$	Clamp voltage with ESD strike on pin 1, pin 2 grounded.	I_{PP} = 1 A, tp = 8/20 µs			10	V
		I_{PP} = 5 A, tp = 8/20 µs			14	
$V_{Clamp2,1}$	Clamp voltage with ESD strike on pin 2, pin 1 grounded.	I_{PP} = 1 A, tp = 8/20 µs			10	V
		I_{PP} = 5 A, tp = 8/20 µs			14	
R_{DYN}	Dynamic resistance	Pin 1 to Pin 2(1)		0.55		Ω
		Pin 2 to Pin 1(1)		0.55		
C_{IO}	I/O capacitance	V_{IO} = 2.5 V; f = 1 MHz		6		pF
$V_{BR1,2}$	Breakdown voltage, pin 1 to pin 2	I_{IO} = 1 mA	6			V
$V_{BR2,1}$	Breakdown voltage, pin 2 to pin 1	I_{IO} = 1 mA	6			V

(1) Extraction of R_{DYN} using least squares fit of TLP characteristics between I_{PP} = 10 A and I_{PP} = 20 A.

6.6 Typical Characteristics

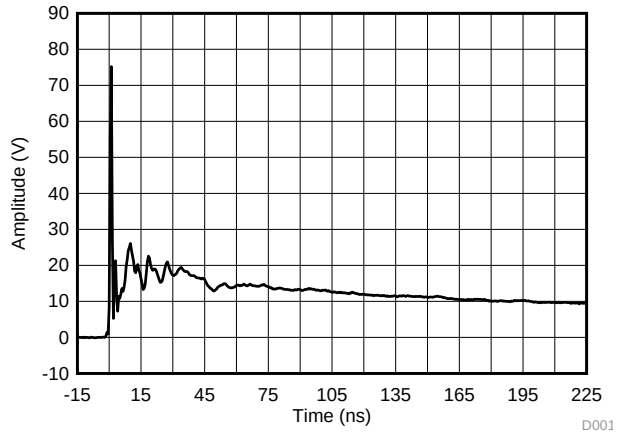


Figure 1. ESD Clamp Voltage +8-kV Contact ESD

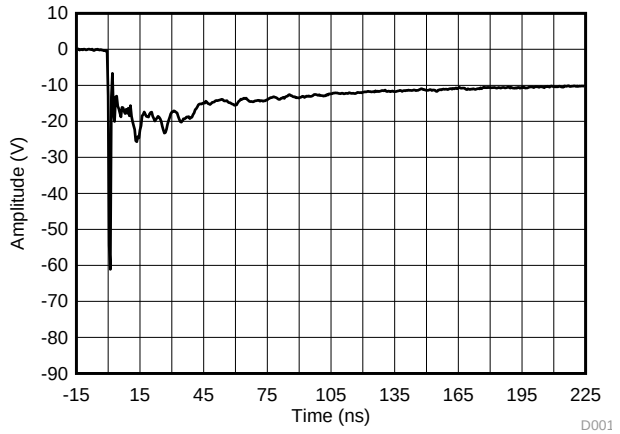


Figure 2. ESD Clamp Voltage –8-kV Contact ESD

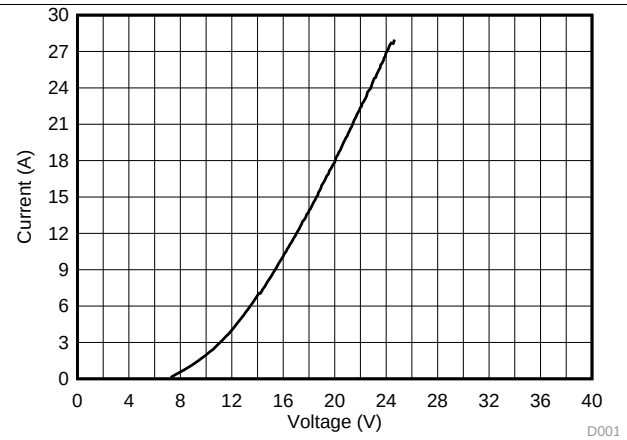


Figure 3. Clamping Voltage V_{TLP} = F(I_{TLP}), PIN1 to PIN2

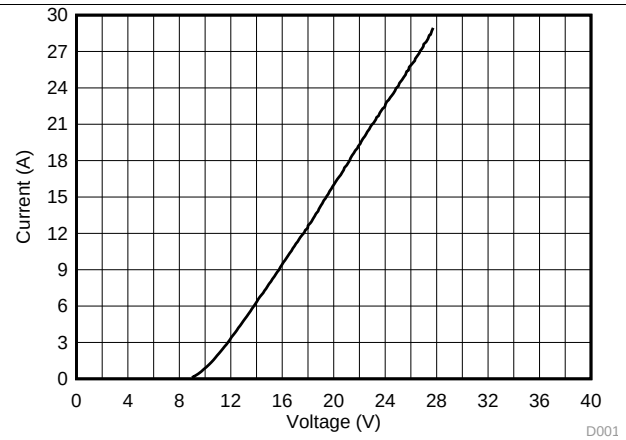


Figure 4. Clamping Voltage V_{TLP} = F(I_{TLP}), PIN2 to PIN1

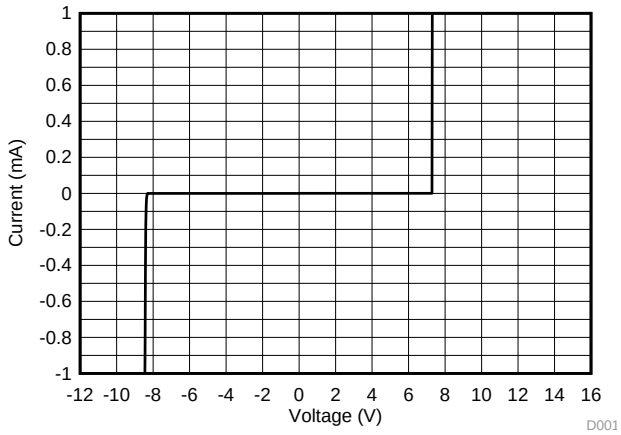


Figure 5. IV Curve

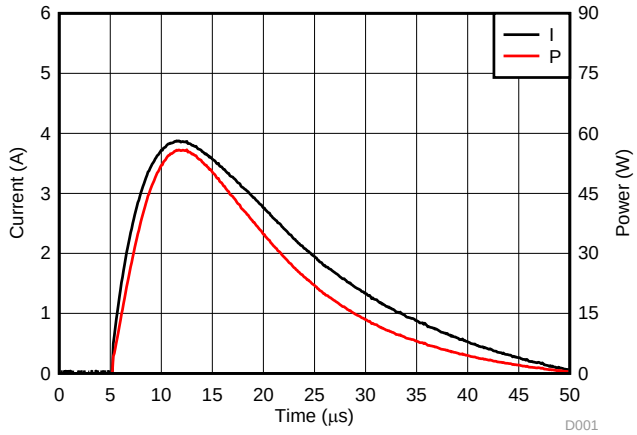


Figure 6. Surge Graph, Pin 1 to Pin 2

Typical Characteristics (continued)

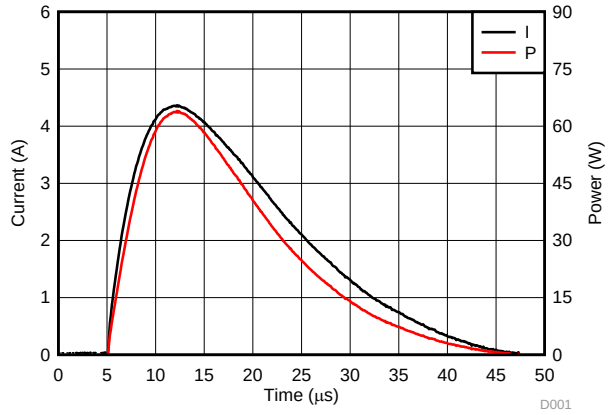


Figure 7. Surge Graph, Pin 2 to Pin 1

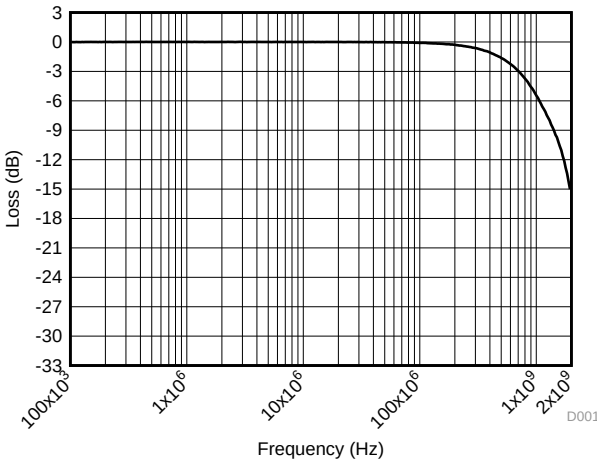


Figure 8. Insertion Loss, Pin 1 to Pin 2

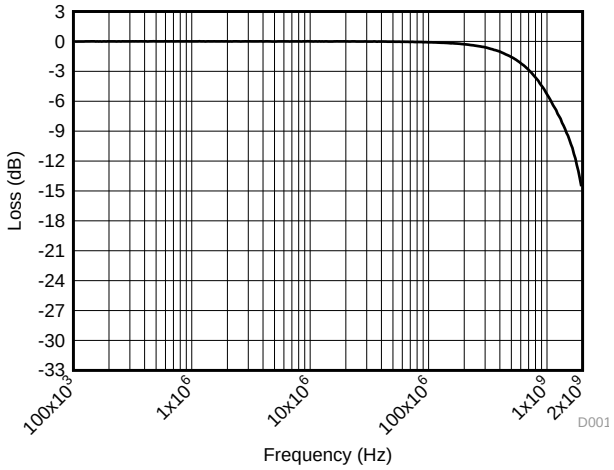


Figure 9. Insertion Loss, Pin 2 to Pin 1

7 Detailed Description

7.1 Overview

The TPD1E6B06 is a single-channel TVS diode for ESD protection in a small 0201 package. The TPD1E6B06 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4), with ±15-kV contact discharge and ±15-kV air-gap ESD protection. The device has a back-to-back TVS diode configuration for bipolar or bidirectional signal support. The 6-pF line capacitance is suitable to provide transient voltage suppression circuit protection for a wide range of applications, supporting data rates up to 800 Mbps. Typical application interfaces for the TPD1E6B06 are audio lines (microphone, earphone, and speakerphone), SD interfacing, keypad or other buttons, as well as the VBUS and ID pins of USB ports.

7.2 Functional Block Diagram

7.3 Feature Description

The TPD1E6B06 is a single-channel TVS diode for ESD protection. This device provides circuit protection from ESD strikes up to ±15-kV contact and ±15-kV air-gap as specified in the IEC 61000-4-2 international standard. The device can also handle up to 3.8 A of surge current (IEC61000-4-5 8/20 μs). The TPD1E6B06 has 6 pF (typical) of capacitance which allows this device to support data rates up to 800 Mbps. Additionally, this low capacitance can even be necessary for an audio signal (for example, if a Class D amplifier is used). The TPD1E6B06 also has a small dynamic resistance of 0.55Ω (typical). This makes the clamping voltage low when it is protecting other circuits, which is crucial for protecting ICs during ESD events. The breakdown is bidirectional so that this protection device is a good fit for GPIO and especially audio lines which carry bidirectional signals. Low leakage current allows the diode to conserve power when working below the V_{RWM}. The industrial temperature range of –40°C to 125°C makes this ESD device to work well at extensive temperatures in most environments. The space-saving 0201 package is designed for small electronic devices like mobile phones and wearables.

7.4 Device Functional Modes

The TPD1E6B06 is a passive clamp that has low leakage during normal operation and activates whenever the voltage between pin 1 and pin 2 goes above V_{RWM} or below $-V_{RWM}$. During IEC ESD events, transient voltages as high as ±15 kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When a system contains a human interface connector, it becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. TPD1E6B06 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from an ESD event passes through the TVS diode, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

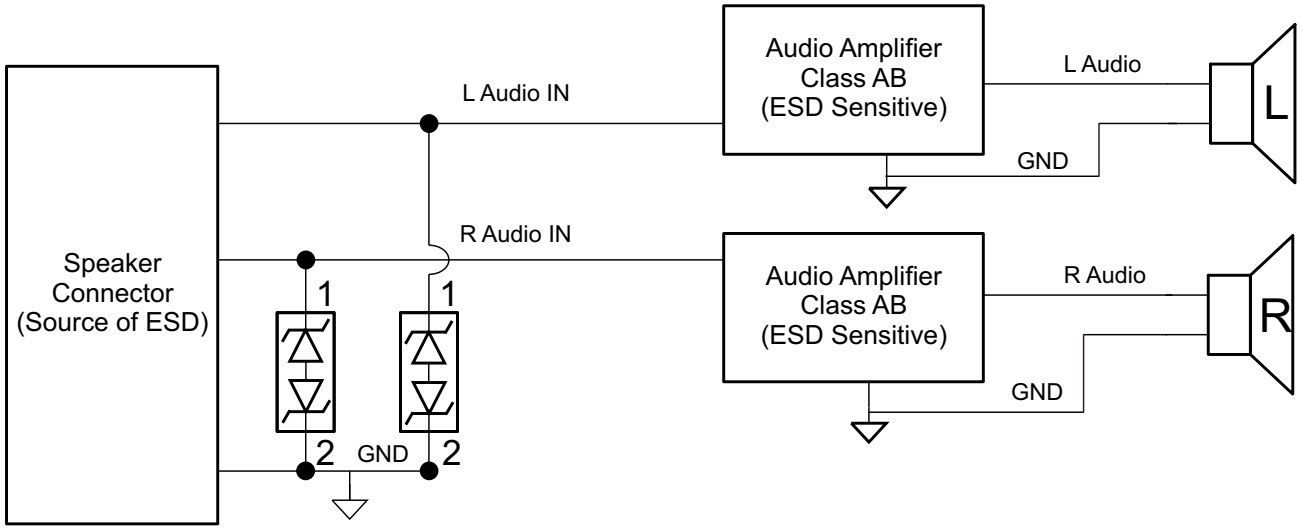


Figure 10. Audio Application Schematic

8.2.1 Design Requirements

For this design example, two TPD1E6B06s will be used to protect left and right audio channels. For this audio application, the following system parameters are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Audio amplifier class	AB
Audio signal voltage range	–3 V to 3 V
Audio frequency content	20 Hz to 20 kHz
Required IEC 61000-4-2 ESD protection	±8 kV Contact and ±15kV Air-Gap

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

- Voltage range on the protected line must not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM}).
- Operating frequency is supported by the I/O capacitance C_{IO} of the TVS diode.

- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the audio signal voltage range is –3 V to 3 V. The V_{RWM} for our TVS is –5 V to 5 V; therefore, our bidirectional TVS will not break down during normal operation, and therefore normal operation of our audio signal will not be effected due to the signal voltage range. Note that in this application, a bidirectional TVS like TPD1E6B06 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz; ensure that the TVS I/O capacitance will not distort this signal by filtering it. With TPD1E6B06 typical capacitance of 6 pF, which leads to a typical 3-dB bandwidth of 700 MHz, this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires standard Level 4 IEC 61000-4-2 system-level ESD protection (±8-kV Contact/ ±15-kV Air-Gap). TPD1E6B06 can survive ±15-kV Contact/ ±15-kV Air-Gap, which indicates that our device can provide sufficient protection for the interface. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will undergo during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. For instructions on properly laying out TPD1E6B06, see *Layout*.

8.2.3 Application Curves

Figure 11 and Figure 12 are captures of the voltage clamping waveforms of TPD1E6B06 during a +8-kV Contact IEC 61000-4-2 ESD strike and a -8-kV Contact IEC 61000-4-2 ESD strike, respectively, in a typical application with proper board layout.

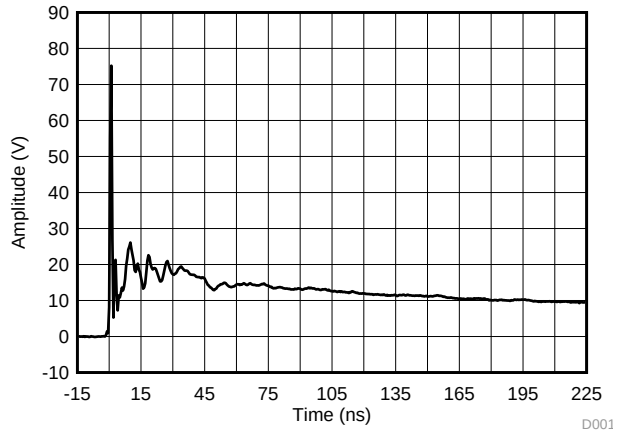


Figure 11. IEC 61000-4-2 ESD Clamp Voltage +8-kV Contact ESD

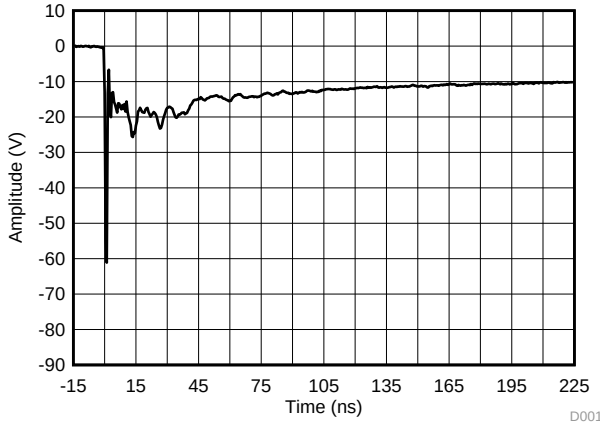


Figure 12. IEC 61000-4-2 ESD Clamp Voltage -8-kV Contact ESD

9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device so there is no need to power it. Take care to make sure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path

10.2 Layout Example

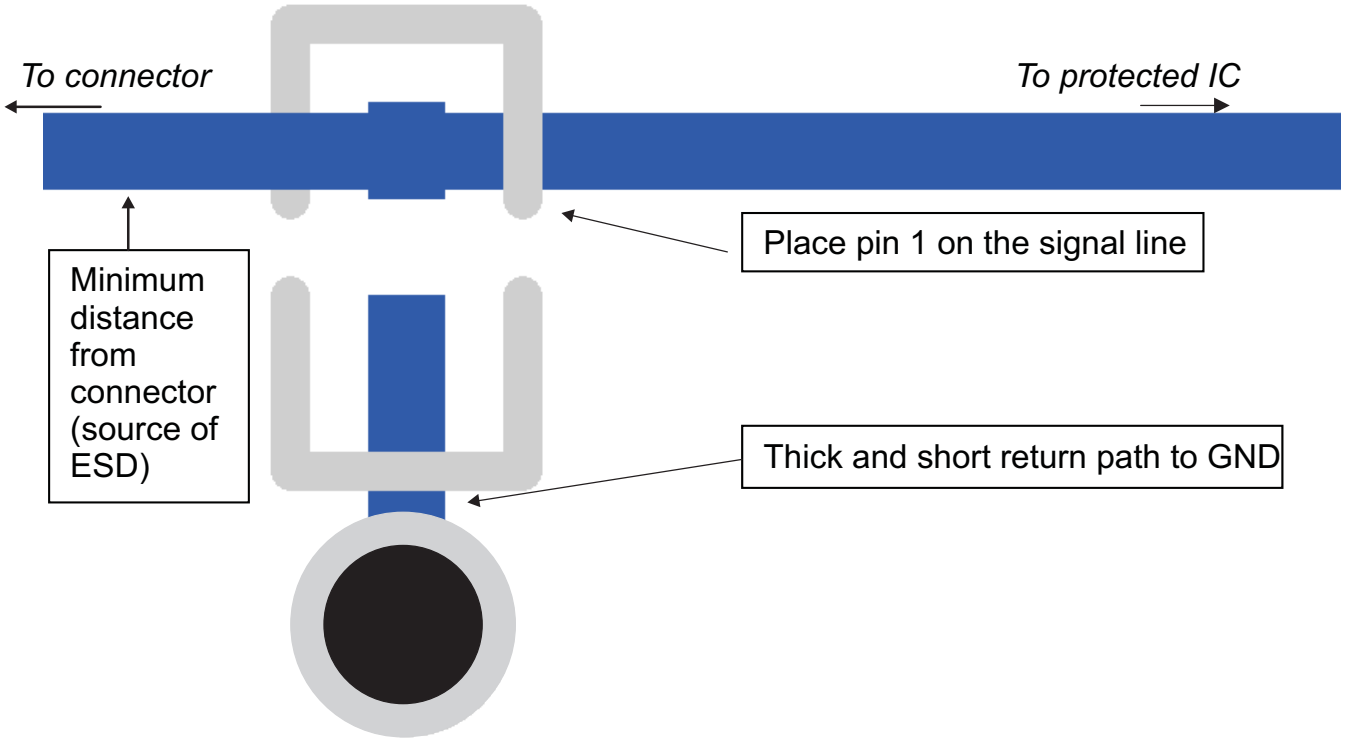


Figure 13. Layout Recommendation

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E6B06DPLR	ACTIVE	X2SON	DPL	2	15000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H	Samples
TPD1E6B06DPLT	ACTIVE	X2SON	DPL	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

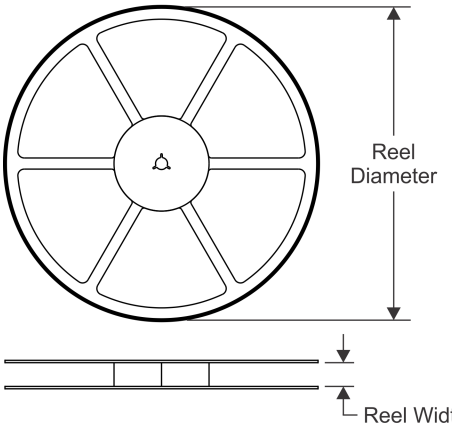
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

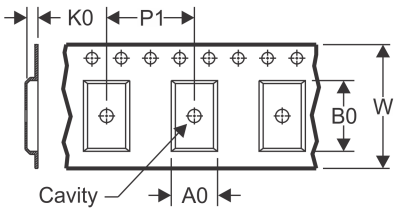
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

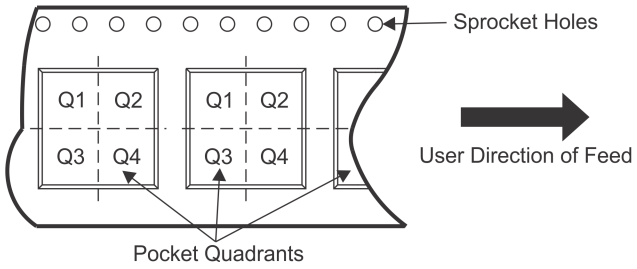


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

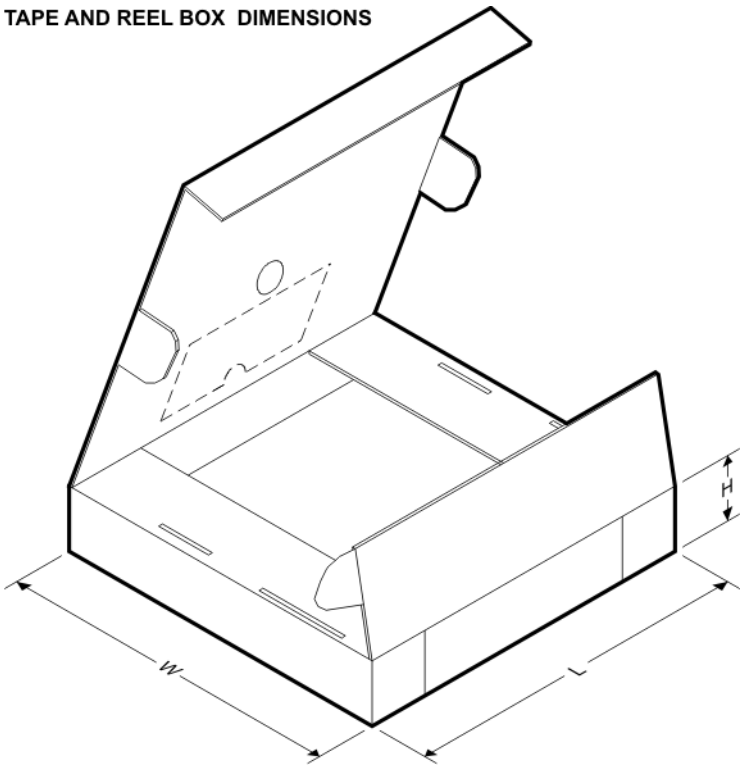
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E6B06DPLR	X2SON	DPL	2	15000	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q3
TPD1E6B06DPLT	X2SON	DPL	2	250	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q3

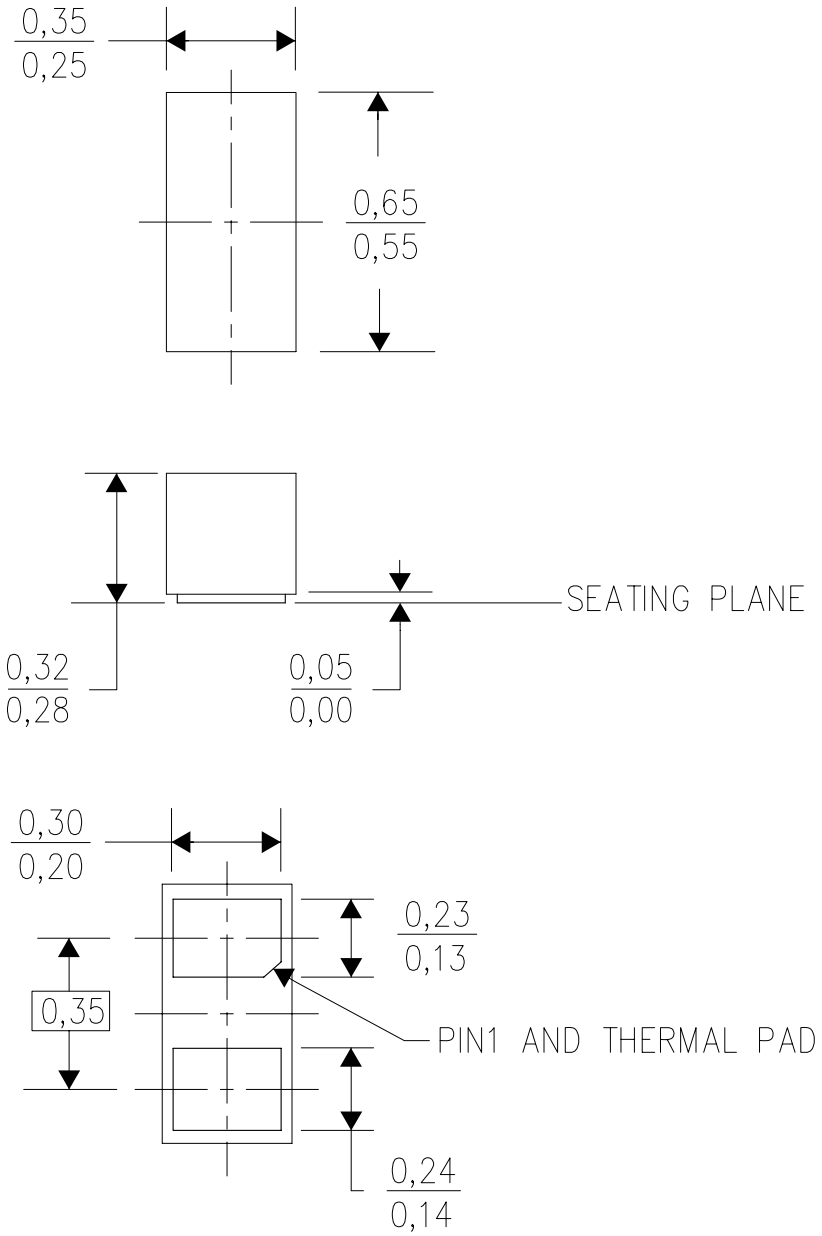
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E6B06DPLR	X2SON	DPL	2	15000	205.0	200.0	33.0
TPD1E6B06DPLT	X2SON	DPL	2	250	205.0	200.0	33.0

DPL (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



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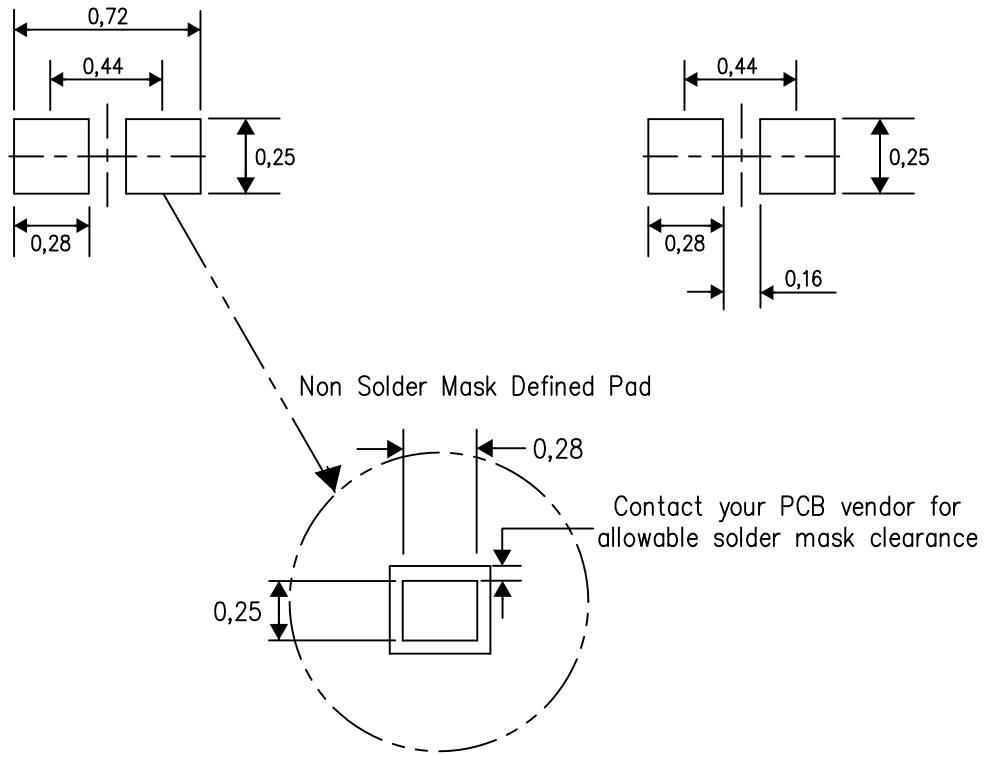
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

DPL (R–PX2SON–N2) SMALL PACKAGE OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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