

Quadruple 2-Input Positive-NAND Gates

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model

2 Applications

- Power Infrastructure
- Network Switch
- Automotive Infotainment
- Servers

3 Description

These quadruple 2-input positive-NAND gates are designed for 2-V to 5.5-V V_{CC} operation.

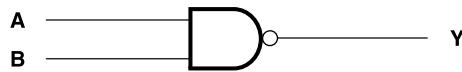
The SNx4LV00A devices perform the boolean function $Y = A \bullet B$ or $Y = \bar{A} + \bar{B}$ in positive logic.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| SNx4LV00A | VQFN (14) | 3.50 mm x 3.50 mm |
| | SOIC (14) | 8.65 mm x 3.91 mm |
| | SOP (14) | 10.30 mm x 5.30 mm |
| | SSOP (14) | 6.20 mm x 5.30 mm |
| | TSSOP (14) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

| | | | | |
|----------|---|----------|-----------|--|
| 1 | Features | 1 | 9 | Detailed Description |
| 2 | Applications | 1 | 9 | 9.1 Overview |
| 3 | Description | 1 | 9 | 9.2 Functional Block Diagram |
| 4 | Simplified Schematic | 1 | 9 | 9.3 Feature Description |
| 5 | Revision History | 2 | 9 | 9.4 Device Functional Modes |
| 6 | Pin Configuration and Functions | 3 | 10 | 10 Application and Implementation |
| 7 | Specifications | 4 | 10 | 10.1 Application Information |
| 7.1 | Absolute Maximum Ratings | 4 | 10 | 10.2 Typical Application |
| 7.2 | ESD Ratings | 4 | 11 | 11 Power Supply Recommendations |
| 7.3 | Recommended Operating Conditions | 5 | 11 | 12 Layout |
| 7.4 | Thermal Information | 5 | 11 | 12.1 Layout Guidelines |
| 7.5 | Electrical Characteristics | 6 | 11 | 12.2 Layout Example |
| 7.6 | Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | 6 | 12 | 13 Device and Documentation Support |
| 7.7 | Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 6 | 12 | 13.1 Related Links |
| 7.8 | Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | 6 | 12 | 13.2 Trademarks |
| 7.9 | Noise Characteristics | 7 | 12 | 13.3 Electrostatic Discharge Caution |
| 7.10 | Operating Characteristics | 7 | 12 | 13.4 Glossary |
| 7.11 | Typical Characteristics | 7 | 12 | |
| 8 | Parameter Measurement Information | 8 | 12 | 14 Mechanical, Packaging, and Orderable Information |

5 Revision History

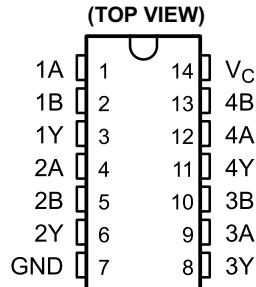
Changes from Revision J (April 2005) to Revision K

Page

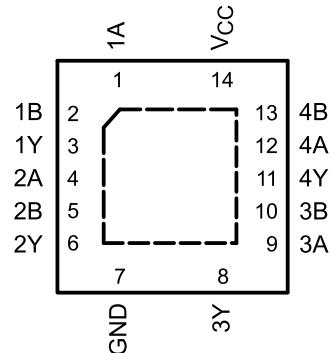
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

6 Pin Configuration and Functions

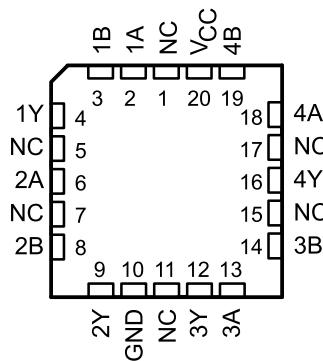
**SN54LV00A . . . J OR W PACKAGE
SN74LV00A . . . D, DB, DGV, NS,
OR PW PACKAGE**



**SN74LV00A . . . RGY PACKAGE
(TOP VIEW)**



**SN54LV00A . . . FK PACKAGE
(TOP VIEW)**



NC - No internal connection

Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----|-----------------|------|-------------|
| NO. | NAME | | |
| 1 | 1A | I | 1A Input |
| 2 | 1B | I | 1B Input |
| 3 | 1Y | O | 1Y Output |
| 4 | 2A | I | 2A Input |
| 5 | 2B | I | 2B Input |
| 6 | 2Y | O | 2Y Output |
| 7 | GND | — | GND |
| 8 | 3Y | O | 3Y Output |
| 9 | 3A | I | 3A Input |
| 10 | 3B | I | 3B Input |
| 11 | 4Y | O | 4Y Output |
| 12 | 4A | I | 4A Input |
| 13 | 4B | I | 4B Input |
| 14 | V _{CC} | — | Power Pin |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------|---|-----------------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 7 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 7 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 7 | V |
| V_O | Output voltage range ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -20 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | ± 25 | mA |
| | Continuous current through V_{CC} or GND | | ± 50 | mA |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

7.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|--|-------|------|
| $V_{(ESD)}$ | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | +2000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | +1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54LV00A ⁽²⁾ | | SN74LV00A | | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | 1.5 | | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | 0.5 | 0.5 | | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2 V | -50 | -50 | | µA |
| | | V _{CC} = 2.3 V to 2.7 V | -2 | -2 | | |
| | | V _{CC} = 3 V to 3.6 V | -6 | -6 | | mA |
| | | V _{CC} = 4.5 V to 5.5 V | -12 | -12 | | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | 50 | 50 | | µA |
| | | V _{CC} = 2.3 V to 2.7 V | 2 | 2 | | |
| | | V _{CC} = 3 V to 3.6 V | 6 | 6 | | mA |
| | | V _{CC} = 4.5 V to 5.5 V | 12 | 12 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 2.3 V to 2.7 V | 200 | 200 | | |
| | | V _{CC} = 3 V to 3.6 V | 100 | 100 | | ns/V |
| | | V _{CC} = 4.5 V to 5.5 V | 20 | 20 | | |
| T _A | Operating free-air temperature | -40 | 125 | -40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* ([SCBA004](#)).

(2) Product Preview.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SNx4LV00A | | | | | | UNIT |
|-------------------------------|--|---------|---------|---------|---------|---------|------|
| | D | DB | DGV | NS | PW | RGY | |
| | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 90.6 | 107.1 | 129.0 | 90.7 | 122.6 | 57.5 |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 50.9 | 59.6 | 521 | 48.3 | 51.4 | 70.8 |
| R _{θJB} | Junction-to-board thermal resistance | 44.8 | 54.4 | 62.0 | 49.4 | 64.4 | 33.6 |
| Ψ _{JT} | Junction-to-top characterization parameter | 14.7 | 20.5 | 6.5 | 14.6 | 6.7 | 34 |
| Ψ _{JB} | Junction-to-board characterization parameter | 44.5 | 53.8 | 61.3 | 49.1 | 63.8 | 33.7 |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | — | — | — | — | — | 13.9 |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN54LV00A ⁽¹⁾ | | | −40°C to 85°C SN74LV00A | | −40°C to 125°C SN74LV00A | | UNIT |
|------------------|---|-----------------|--------------------------|------|-----|----------------------------|------|-----------------------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = −50 µA | 2 V to 5.5 V | V _{CC} − 0.1 | | | V _{CC} − 0.1 | | V _{CC} − 0.1 | | V |
| | I _{OH} = −2 mA | 2.3 V | 2 | | | 2 | | 2 | | |
| | I _{OH} = −6 mA | 3 V | 2.48 | | | 2.48 | | 2.48 | | |
| | I _{OH} = −12 mA | 4.5 V | 3.8 | | | 3.8 | | 3.8 | | |
| V _{OL} | I _{OL} = 50 µA | 2 V to 5.5 V | | 0.1 | | | 0.1 | | 0.1 | V |
| | I _{OL} = 2 mA | 2.3 V | | 0.4 | | | 0.4 | | 0.4 | |
| | I _{OL} = 6 mA | 3 V | | 0.44 | | | 0.44 | | 0.44 | |
| | I _{OL} = 12 mA | 4.5 V | | 0.55 | | | 0.55 | | 0.55 | |
| I _I | V _I = 5.5 V or GND | 0 to 5.5 V | | ±1 | | | ±1 | | ±1 | µA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | 20 | | | 20 | | 20 | µA |
| I _{off} | V _I or V _O = 0 to 5.5 V | 0 | | 5 | | | 5 | | 5 | µA |
| C _I | V _I = V _{CC} or GND | 3.3 V | | 3.3 | | | | 3.3 | | pF |
| | | 5 V | | 3.3 | | | | 3.3 | | |

(1) Product Preview.

7.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54LV00A ⁽¹⁾ | | −40°C to 85°C SN74LV00A | | −40°C to 125°C SN74LV00A | | UNIT |
|-----------------|-----------------|----------------|------------------------|-----------------------|---------------------|------------------|--------------------------|-----|----------------------------|-----|-----------------------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | C _L = 15 pF | 7.1 ⁽²⁾ | 12.9 ⁽²⁾ | 1 ⁽²⁾ | 16 ⁽²⁾ | 1 | 15 | 1 | 16 | ns | |
| | | | C _L = 50 pF | 9.6 | 16.6 | 1 | 21 | 1 | 20 | 1 | 21 | | |

(1) Product Preview.

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54LV00A ⁽¹⁾ | | −40°C to 85°C SN74LV00A | | −40°C to 125°C SN74LV00A | | UNIT |
|-----------------|-----------------|----------------|------------------------|-----------------------|--------------------|------------------|--------------------------|-----|----------------------------|-----|-----------------------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | C _L = 15 pF | 5 ⁽²⁾ | 7.9 ⁽²⁾ | 1 ⁽²⁾ | 10.5 ⁽²⁾ | 1 | 9.5 | 1 | 10.5 | ns | |
| | | | C _L = 50 pF | 6.9 | 11.4 | 1 | 14 | 1 | 13 | 1 | 14 | | |

(1) Product Preview.

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54LV00A ⁽¹⁾ | | −40°C to 85°C SN74LV00A | | −40°C to 125°C SN74LV00A | | UNIT |
|-----------------|-----------------|----------------|------------------------|-----------------------|--------------------|------------------|--------------------------|-----|----------------------------|-----|-----------------------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | C _L = 15 pF | 3.6 ⁽²⁾ | 5.5 ⁽²⁾ | 1 ⁽³⁾ | 7.5 ⁽³⁾ | 1 | 6.5 | 1 | 7 | ns | |
| | | | C _L = 50 pF | 4.9 | 7.5 | 1 | 9.5 | 1 | 8.5 | 1 | 9 | | |

(1) Product Preview.

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.9 Noise Characteristics⁽¹⁾

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

| PARAMETER | SN74LV04A | | | UNIT |
|--|-----------|------|------|------|
| | MIN | TYP | MAX | |
| $V_{OL(P)}$ Quiet output, maximum dynamic V_{OL} | | 0.2 | 0.8 | V |
| $V_{OL(V)}$ Quiet output, minimum dynamic V_{OL} | | -0.1 | -0.8 | V |
| $V_{OH(V)}$ Quiet output, minimum dynamic V_{OH} | | 3.1 | | V |
| $V_{IH(D)}$ High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ Low-level dynamic input voltage | | 0.99 | | V |

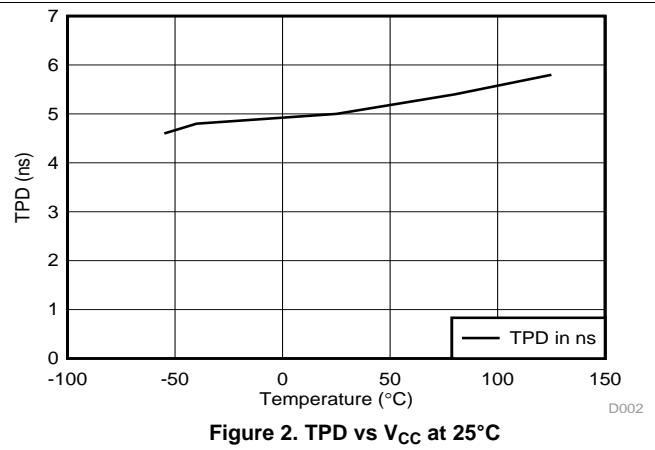
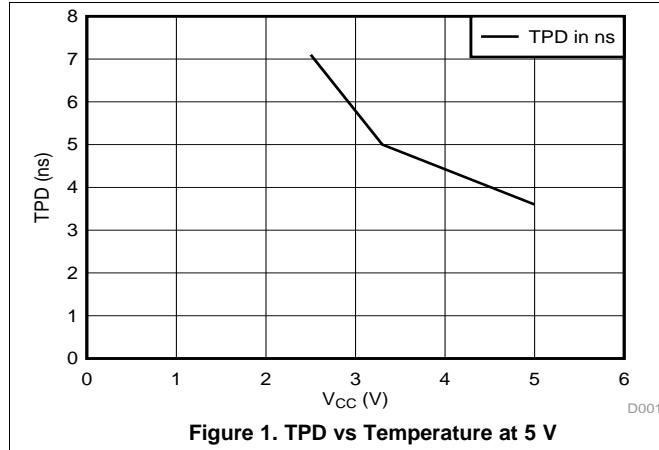
(1) Characteristics are for surface-mount packages only.

7.10 Operating Characteristics

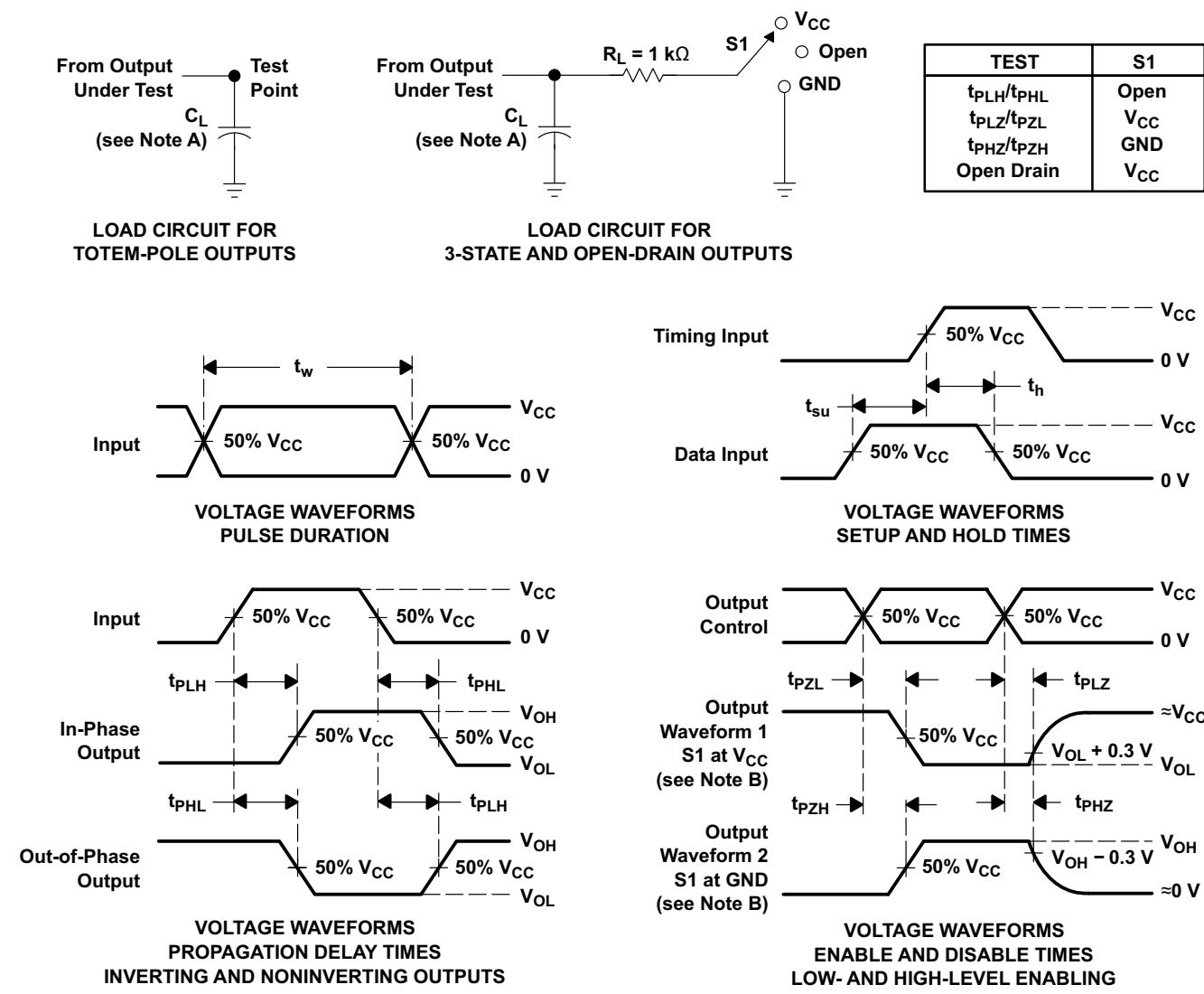
$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|--|--|----------|-----|------|
| C_{pd} Power dissipation capacitance | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 3.3 V | 9.5 | pF |
| | | 5 V | 11 | |

7.11 Typical Characteristics



8 Parameter Measurement Information



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PHL} and t_{PLH} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

These quadruple 2-input positive-NAND gates are designed for 2-V to 5.5-V V_{CC} operation.

The SNx4LV00A devices perform the boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic

These devices are fully specified for partial-power-down application using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the input or output when V_{CC} is 0 V.

9.4 Device Functional Modes

**Table 1. Function Table
(Each Gate)**

| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LV00A is a Low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it Ideal for down translation.

10.2 Typical Application

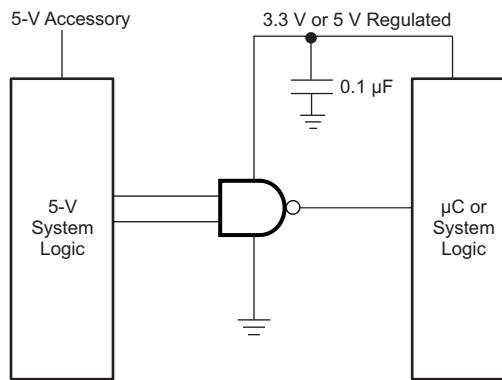


Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Condition
 - Specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves

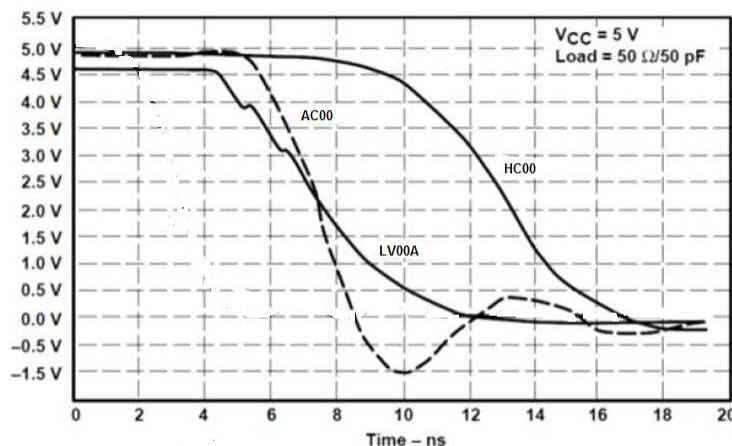


Figure 5. Typical Application Curve

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μ F capacitor is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F capacitors are recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μ F and 1 μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

12.2 Layout Example

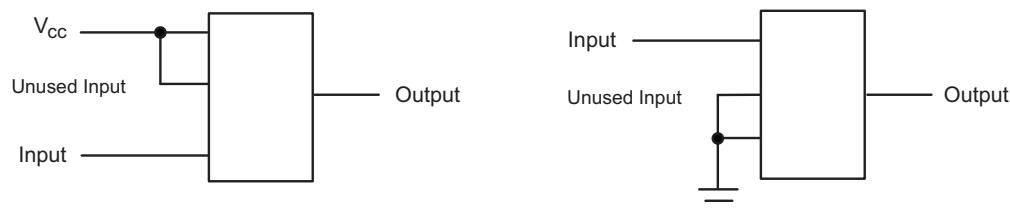


Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74LV04A | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SN74LV00AD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00ADBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00ANSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV00A | Samples |
| SN74LV00APW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00APWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00APWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV00A | Samples |
| SN74LV00ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV00A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

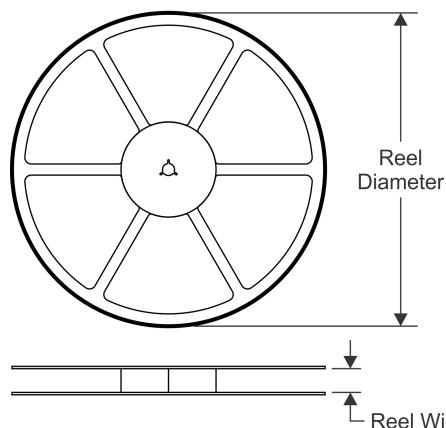
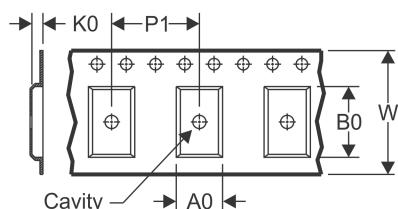
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

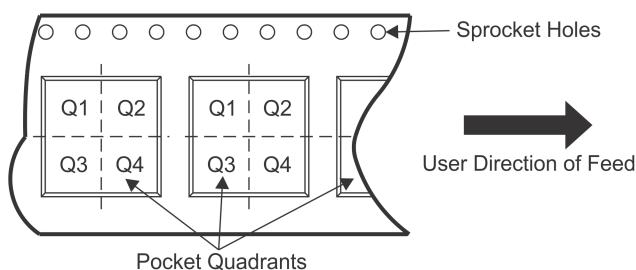
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

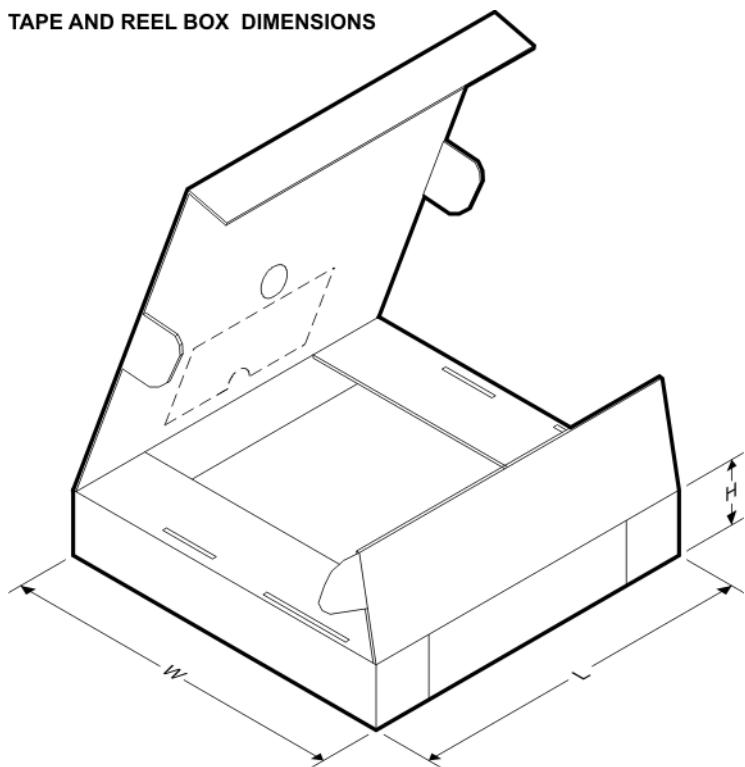
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


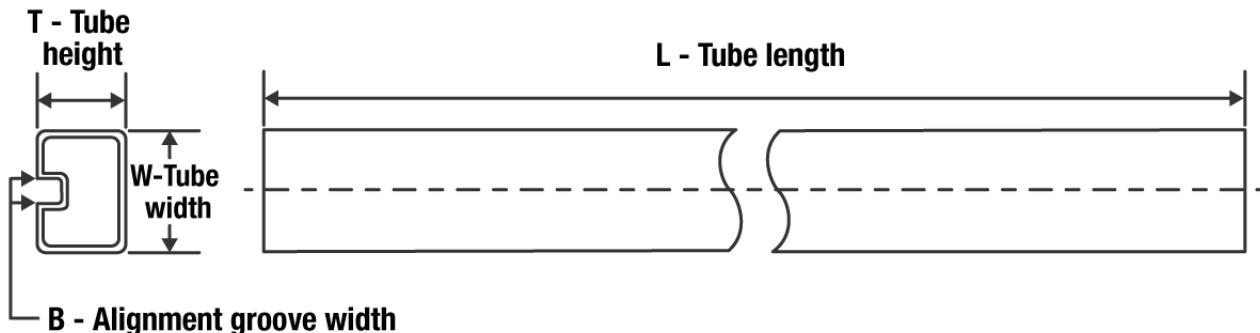
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV00ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV00ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV00ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV00ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV00APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV00APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV00ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV00ADBR | SSOP | DB | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV00ADGVR | TVSOP | DGV | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV00ADR | SOIC | D | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| SN74LV00ANSR | SO | NS | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV00APWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV00APWT | TSSOP | PW | 14 | 250 | 853.0 | 449.0 | 35.0 |
| SN74LV00ARGYR | VQFN | RGY | 14 | 3000 | 853.0 | 449.0 | 35.0 |

TUBE


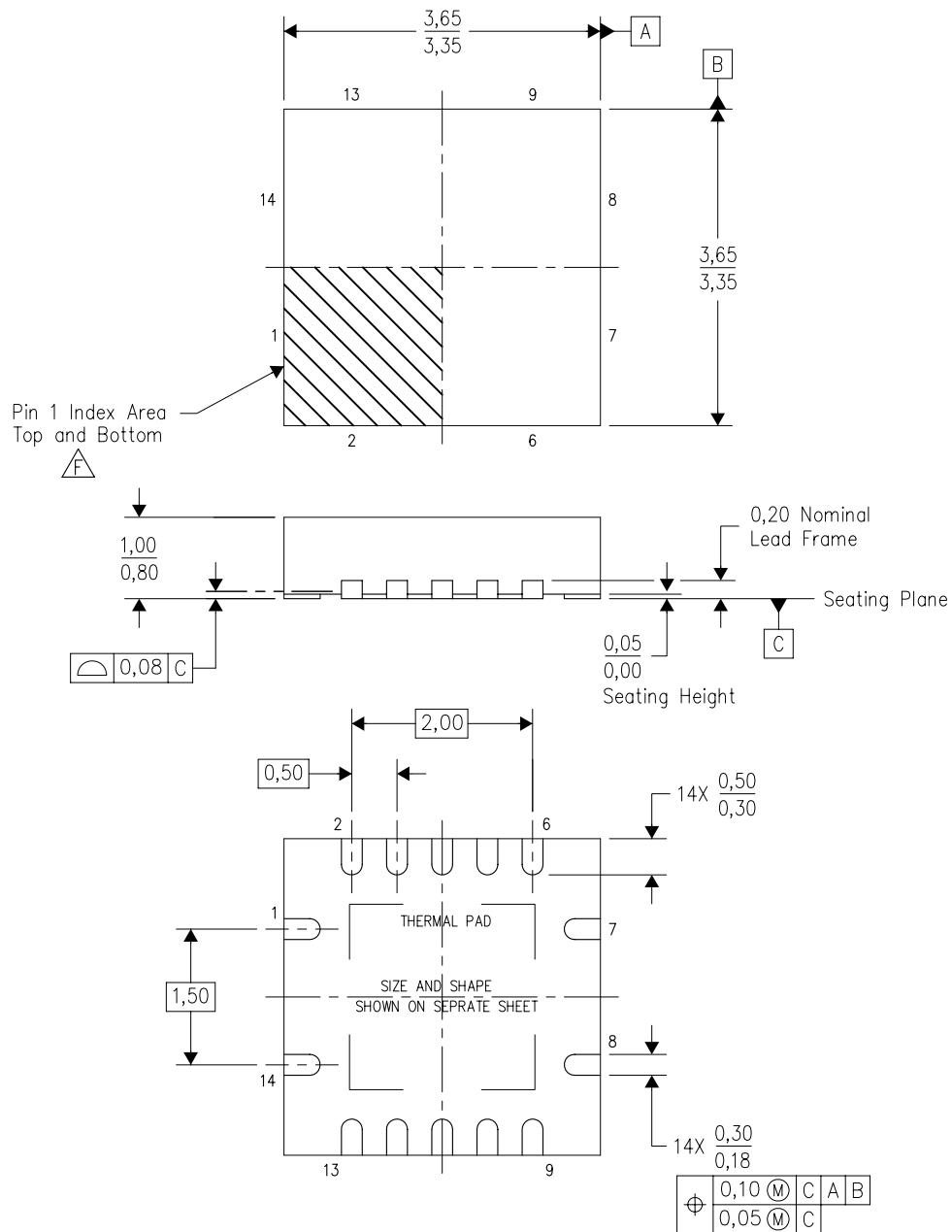
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LV00AD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LV00APW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74LV00APWG4 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

MECHANICAL DATA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-2/l 06/2011

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

THERMAL PAD MECHANICAL DATA

RGY (S-PVQFN-N14)

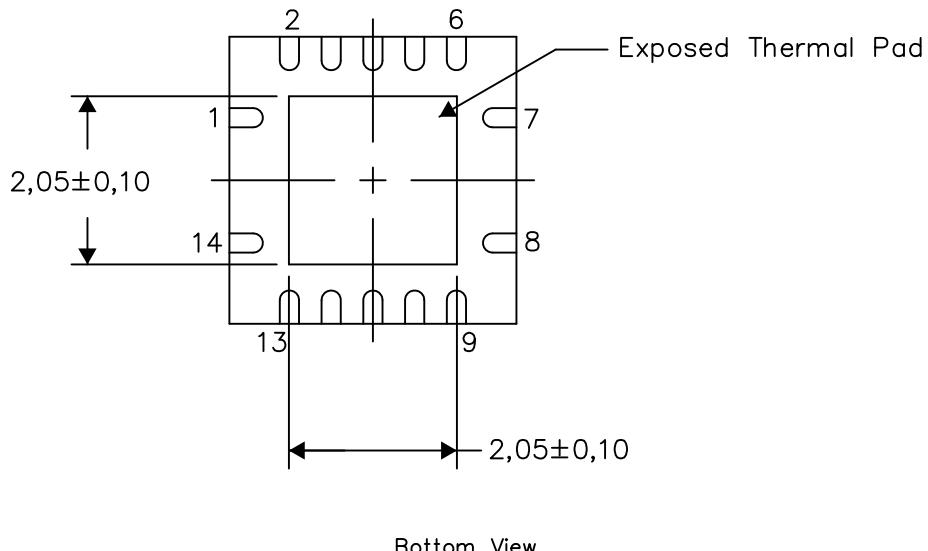
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

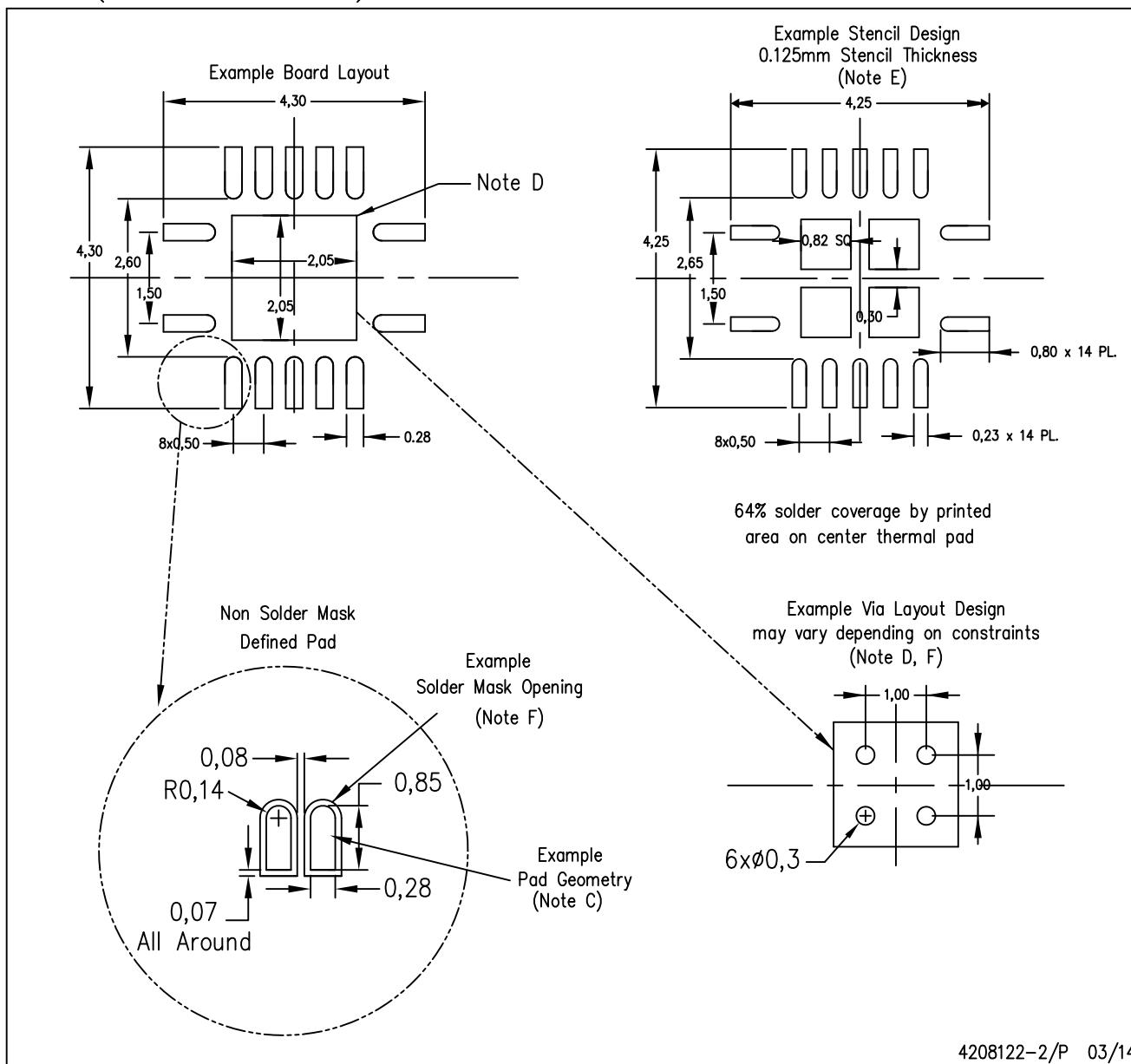
4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

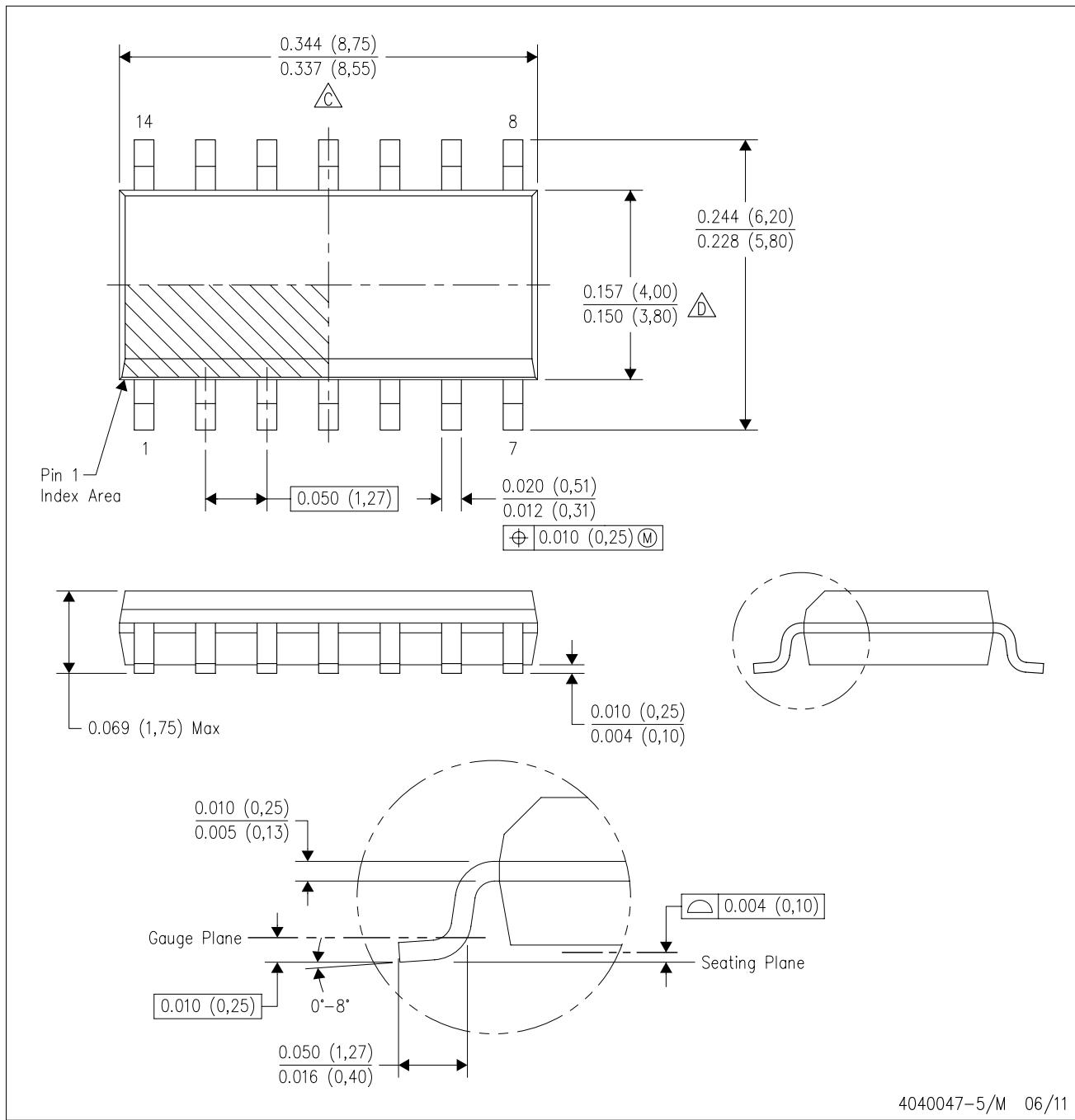


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

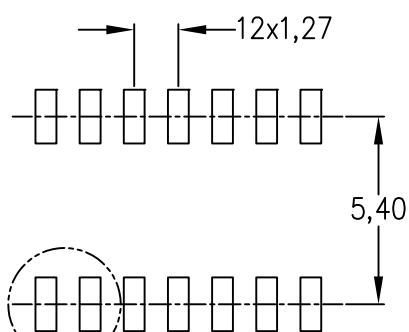
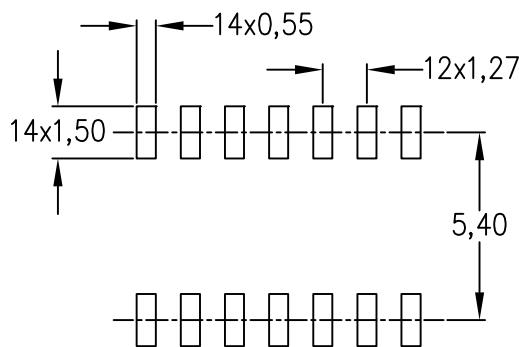
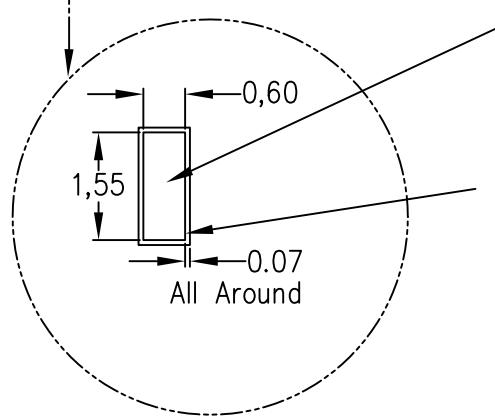
(C) Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

(D) Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

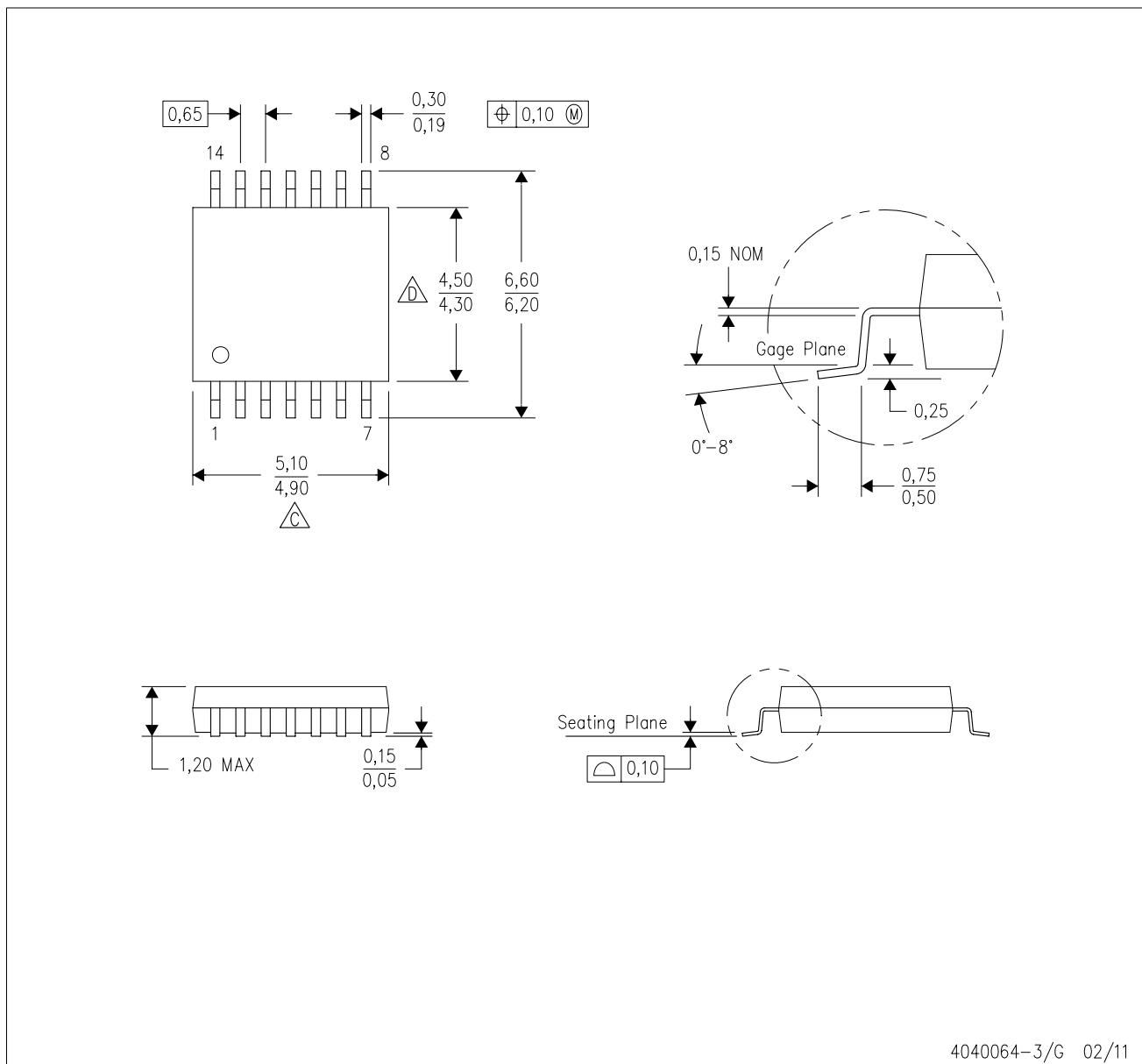
4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

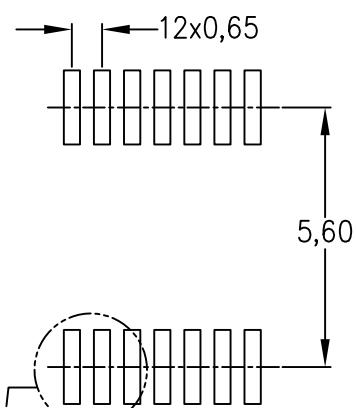
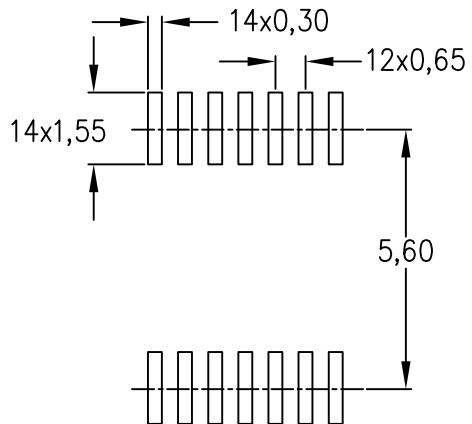
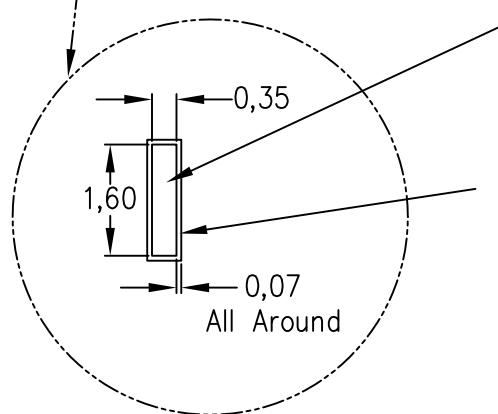
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

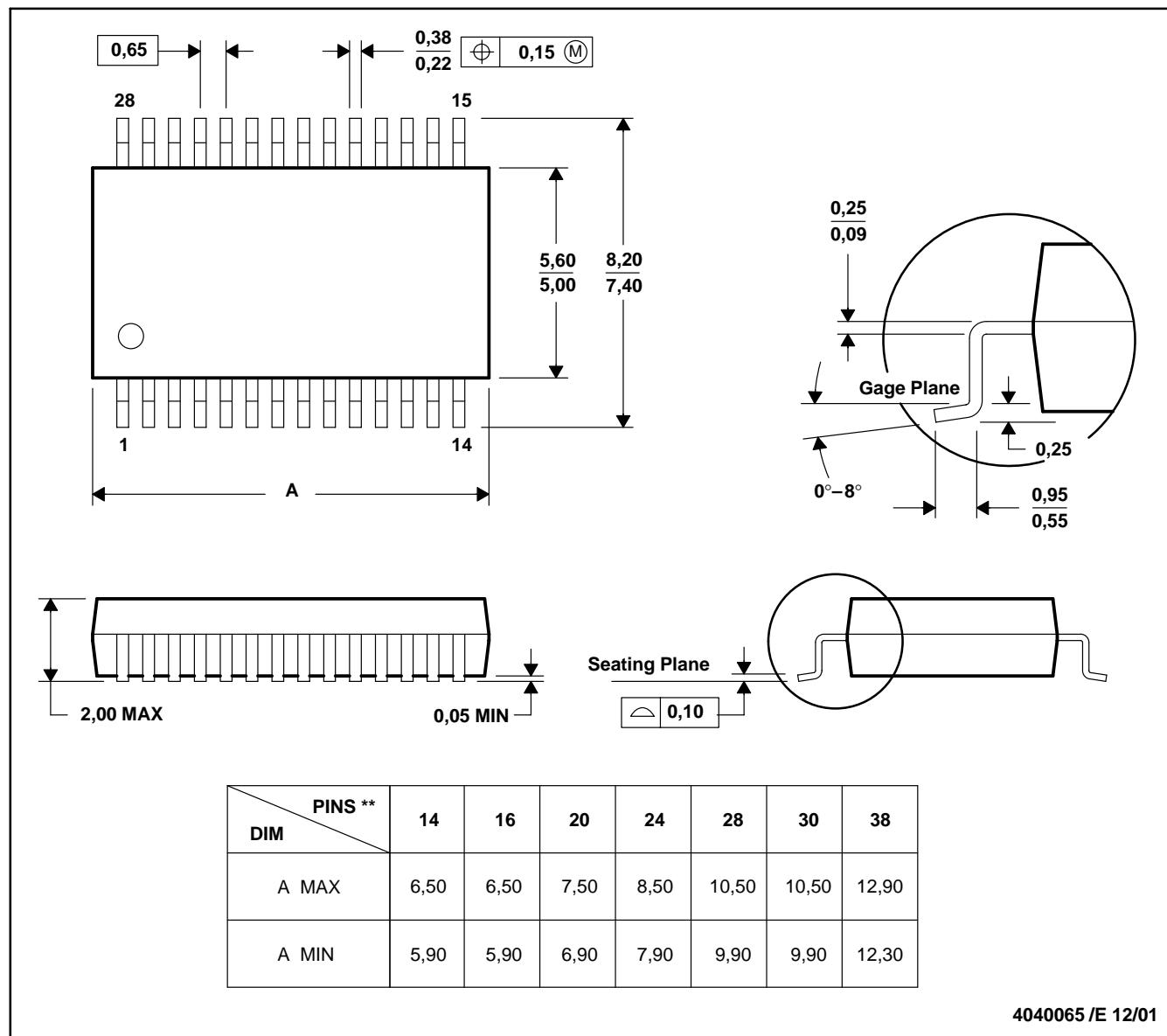
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

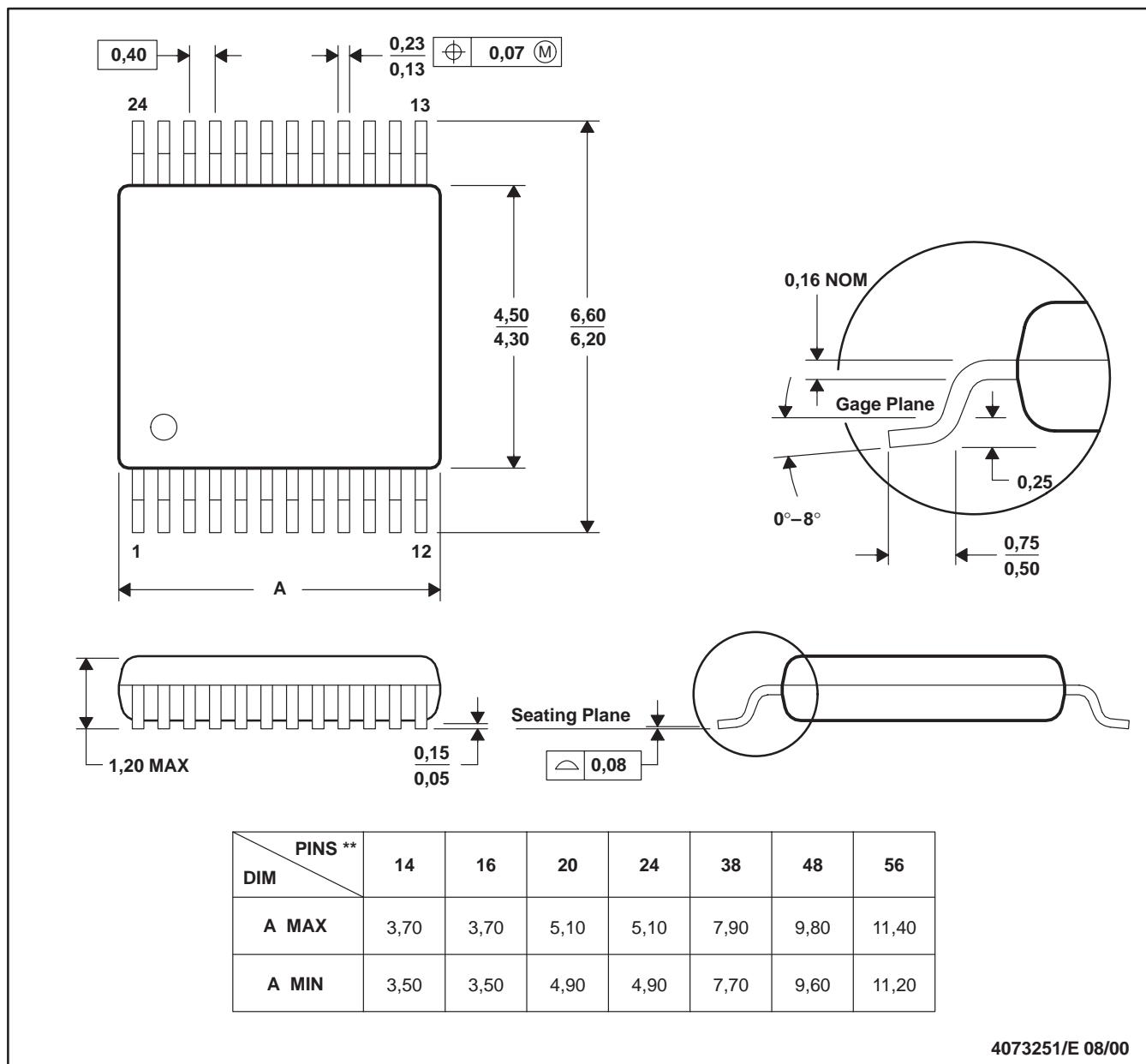


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated