TEXAS INSTRUMENTS

TLV703x 和 TLV704x 小尺寸、毫微功耗、低电压比较器

1 特性

- 超小型 X2SON 封装
  (0.8mm × 0.8mm × 0.4mm)
- 微型 5 引脚 SOT-23、SC70 和 VSSOP 封装
- 1.6V 至 6.5V 的宽电源电压范围
- 335nA 静态电源电流
- 3μs 低传播延迟
- 轨至轨共模输入电压
- 5mV 内部迟滞
- 推挽式输出 (TLV703x)
- 开漏输出 (TLV704x)
- 过驱动输入无相位反转
- –40°C 至 125°C 工作温度

2 应用

- 手机和平板电脑
- 便携式电池供电器件
- 红外接收器
- 电平转换器
- 阈值检测器与鉴别器
- 窗口比较器
- 过零检测器

3 说明

TLV7031/TLV7041（单通道）和 TLV7032/42（双通道）是低电压、毫微功耗的比较器。这些器件采用 0.8mm × 0.8mm 的超小型无引线封装以及标准的 5 引脚 SC70 和 SOT-23 封装，因此适用于空间受限的设计，例如智能手机、智能仪表和其他便携式或电池供电类 应用中的方向终端。

TLV703x 和 TLV704x 提供出色的速度与功耗综合性能，其传播延迟为 3μs，静态电源电流为 335nA。得益于毫微功耗下的快速响应优势，功耗敏感型系统能够监测故障状况并快速做出响应。这些比较器的工作电压范围为 1.6V 至 6.5V，因此可与 3V 和 5V 系统兼容。

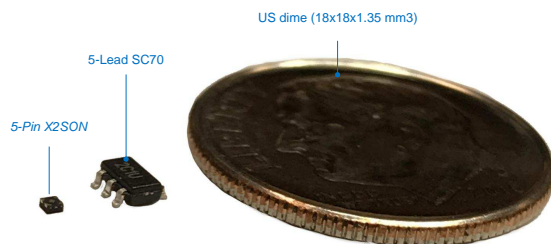TLV703x 和 TLV704x 还凭借过驱输入和内部迟滞来确保不会出现输出相位反转，因此工程师可以将此系列的比较器用在必须将慢速输入信号转换为纯净数字输出的严苛、嘈杂环境中进行精密电压监测。

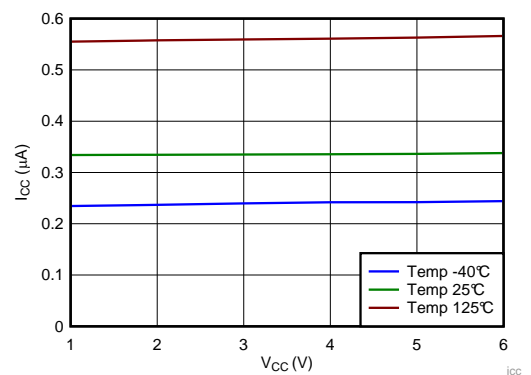TLV703x 具有推挽式输出级，能够灌/拉毫安级电流，同时可对 LED 进行控制或驱动容性负载。TLV704x 具有可上拉到 V_{CC} 之上的漏极开路输出级，因此适用于电平转换器和双极至单端转换器。

器件信息[(1)]

器件型号	封装（引脚）	封装尺寸（标称值）
TLV7031、TLV7041	X2SON (5)	0.80mm × 0.80mm
	SC70 (5)	2.00mm × 1.25mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV7032、TLV7042	VSSOP (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

X2SON 封装与 SC70 和美元硬币对比

US dime (18x18x1.35 mm3)
5-Lead SC70
5-Pin X2SON

I_{CC} 与电源电压间的关系

English Data Sheet: SLVSE13

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4 修订历史记录

Changes from Revision B (May 2018) to Revision C   **Page**

Changes from Revision A (January 2018) to Revision B   **Page**

Changes from Original (September 2017) to Revision A   **Page**

- Changed text 'the TLV7041 features an open-drain output stage enabling the output logic levels to be pulled up to

5 Pin Configuration and Functions

DPW Package
5-Pin X2SON
Top View

Not to scale
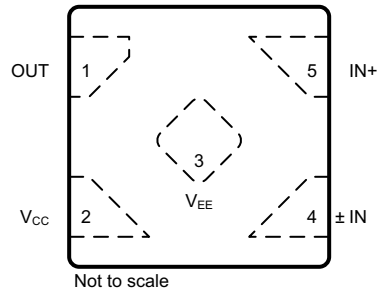
DBV and DCK Package
5-Pin SOT-23 and SC70
Top View
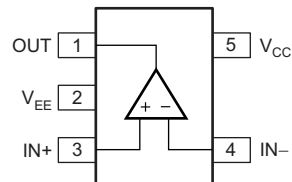
Pin Functions

PIN			I/O[1]	DESCRIPTION
X2SON[2]	SOT-23, SC70	NAME		
1	1	OUT	O	Output
2	5	V_{CC}	P	Positive (highest) power supply
3	2	V_{EE}	P	Negative (lowest) power supply
4	4	IN–	I	Inverting input
5	3	IN+	I	Noninverting input

(1) I = Input, O = Output, P = Power
(2) The application report *Designing and Manufacturing With TI's X2SON Packages* (SCEA055) provides more details on the optimal PCB designs.

DGK Package
8-Pin VSSOP
Top View

OUT A	1	8 V+
–IN A	2	7 OUT B
+IN A	3	6 –IN B
V–	4	5 +IN B
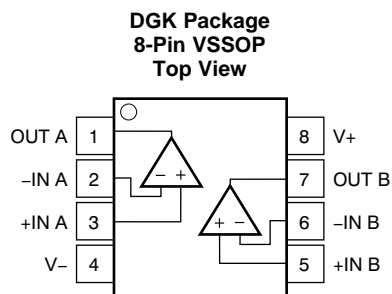
Pin Functions: TLV7032/42

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC}$ - V_{EE}	−0.3	7	V
Input pins (IN+, IN-)[2]	V_{EE} − 0.3	7	V
Current into Input pins (IN+, IN-)		±10	mA
Output (OUT) (TLV703x)[3]	V_{EE} − 0.3	V_{CC} + 0.3	V
Output (OUT) (TLV704x)	V_{EE} − 0.3	7	V
Output short-circuit duration[4]		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to V_{EE}. Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less
(3) Output maximum is (V_{CC} + 0.3 V) or 7 V, whichever is less.
(4) Short-circuit to ground, one comparator per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} − V_{EE}$	1.6	6.5	V
Input voltage range	V_{CC} − 0.1	V_{EE} + 0.1	V
Ambient temperature, T_A	−40	125	°C

6.4 Thermal Information (Dual)

	THERMAL METRIC[1]	TLV7032/TLV7042 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	131.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information (Single)

THERMAL METRIC[1]		TLV7031/TLV7041			UNIT
		DPW (X2SON)	DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	533.2	297.2	278.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	302.7	224.7	186.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	408.3	200.1	113.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	71.5	141.2	82.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	405.9	198.9	112.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	188.3	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics (Dual)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted).
Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2, T_A = 25°C	5	10	20	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7032 only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7042 only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing (for TLV7032 only)		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		300	750	nA

6.7 Switching Characteristics (Dual)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ TLV7042 only) [1]	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ TLV7042 only) [1]	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (TLV7032 only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output is in correct state.		200		µs

(1) The lower limit for RP is 650 Ω

6.8 Electrical Characteristics (Single)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted).
Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2, T_A = 25°C	2	7	17	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7031 only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.7	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	300	mV
I_{LKG}	Open-drain output leakage current (TLV7041 only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		335	900	nA

6.9 Switching Characteristics (Single)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 2.5 kΩ TLV7041 only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 2.5 kΩ TLV7041 only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (TLV7031 only)	Measured from 10% to 90%		4.5		ns
t_F	Fall time	Measured from 10% to 90%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output is in correct state.		200		µs

6.10 Timing Diagrams
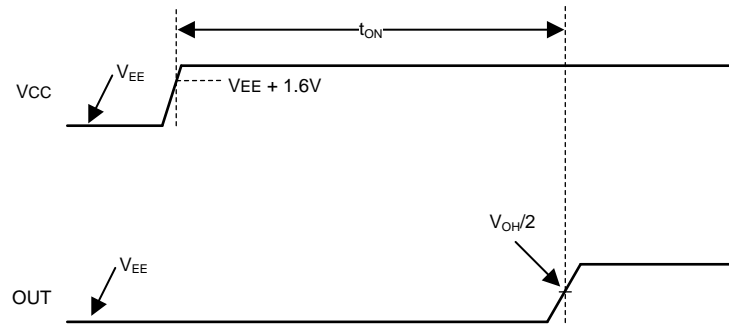
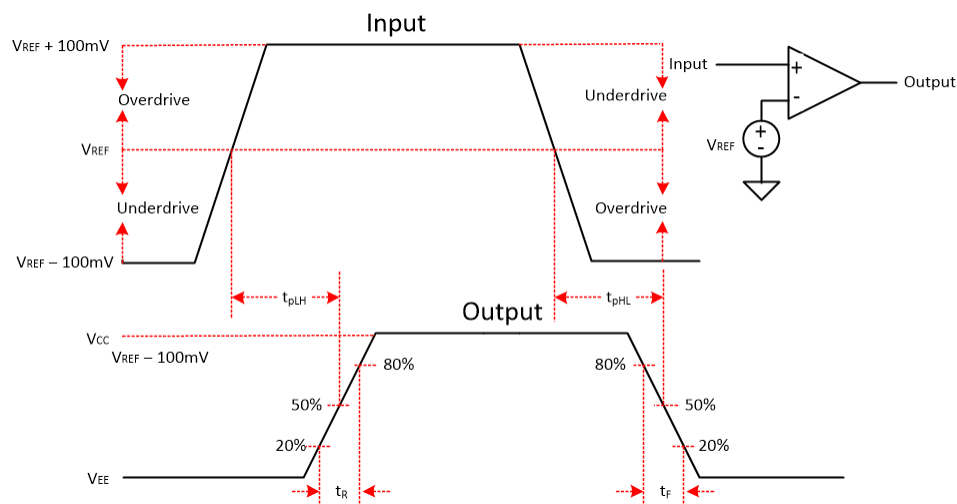图 1. **Start-Up Time Timing Diagram (IN+ > IN–)**

图 2. **Propagation Delay Timing Diagram**

注
The propagation delays t_{pLH} and t_{pHL} include the contribution of input offset and hysteresis.

6.11 Typical Characteristics

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF

V_{CC} = 3.3 V
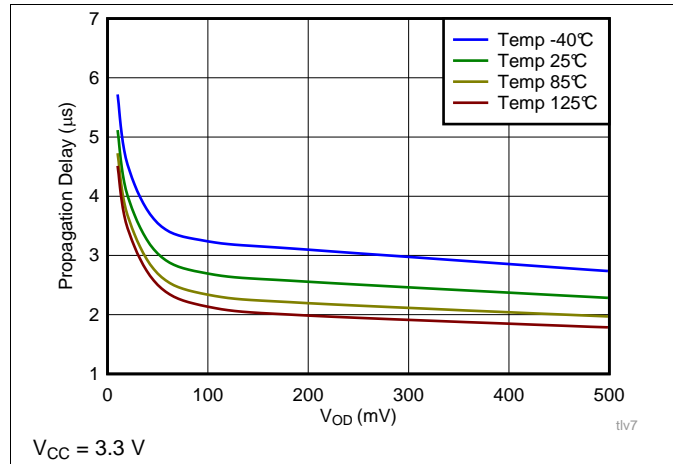
图 3. TLV7031 Propagation Delay (L-H) vs Input Overdrive

V_{CC} = 3.3 V
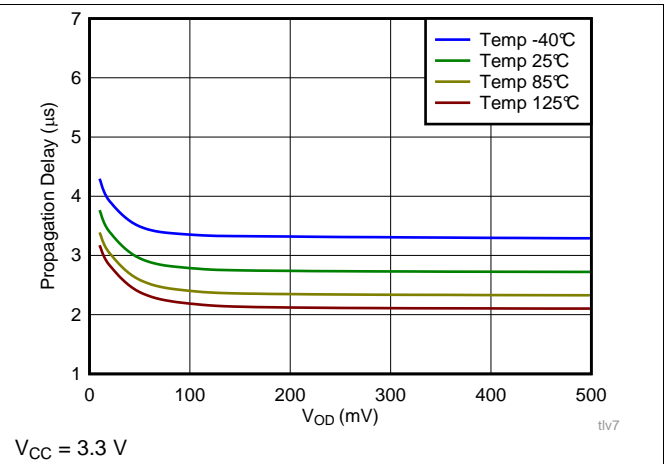
图 4. TLV7031 Propagation Delay (H-L) vs Input Overdrive

V_{CC} = 5 V

图 5. TLV7031 Propagation Delay (L-H) vs Input Overdrive

V_{CC} = 5 V
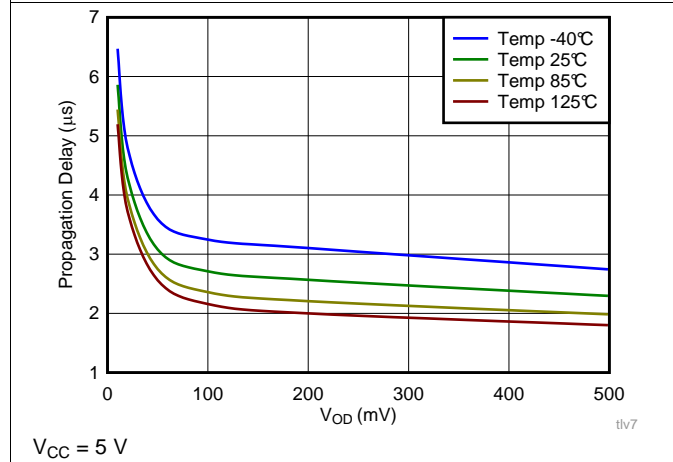
图 6. TLV7031 Propagation Delay (H-L) vs Input Overdrive

R_{pullup} = 2.5 k, V_{CC} = 3.3 V
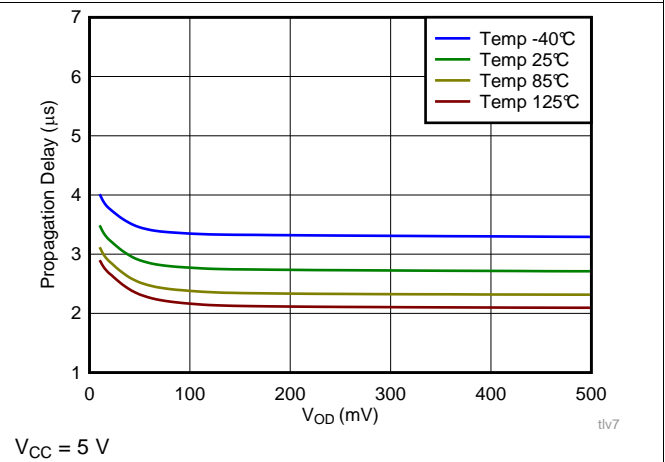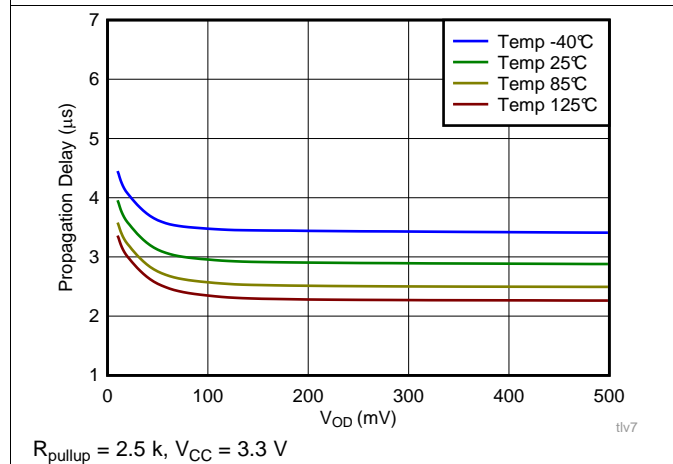
图 7. TLV7041 Propagation Delay (H-L) vs Input Overdrive

R_{pullup} = 2.5 k, V_{CC} = 5 V
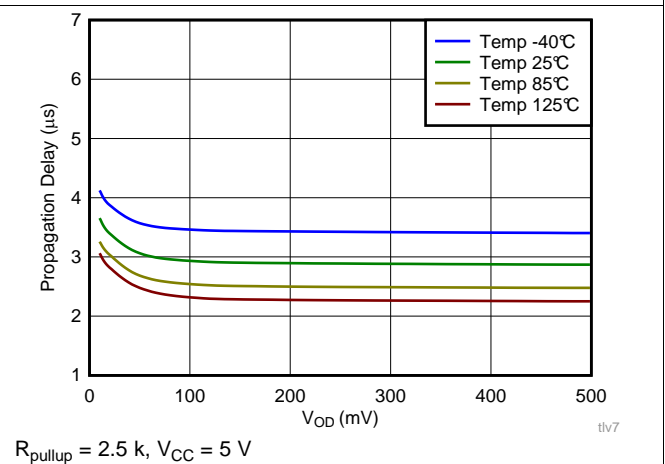
图 8. TLV7041 Propagation Delay (H-L) vs Input Overdrive

Typical Characteristics (接下页)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF
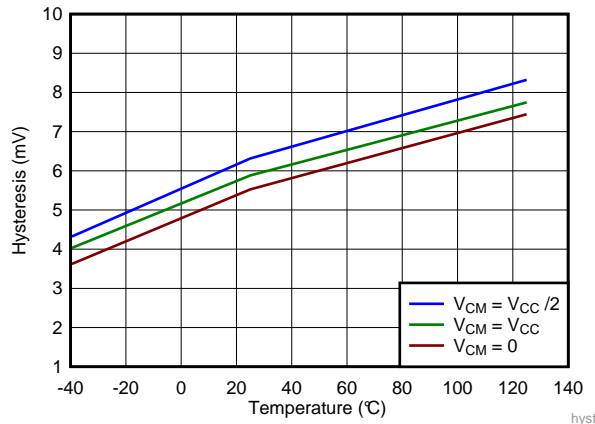
V_{CC} = 1.8 V

图 9. Hysteresis vs Temperature
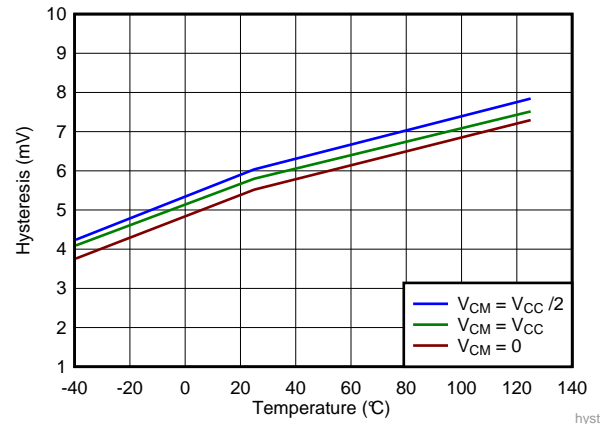
V_{CC} = 3.3 V

图 10. Hysteresis vs Temperature
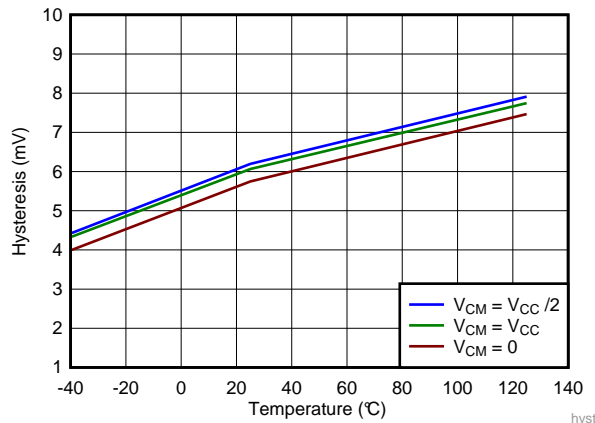
V_{CC} = 5 V

图 11. Hysteresis vs Temperature
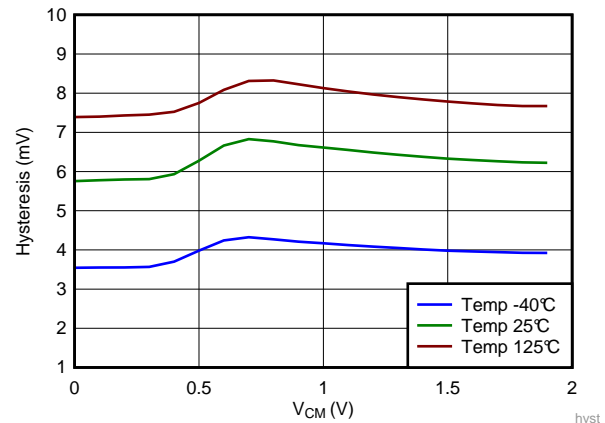
V_{CC} = 1.8 V

图 12. Hysteresis vs V_{CM}
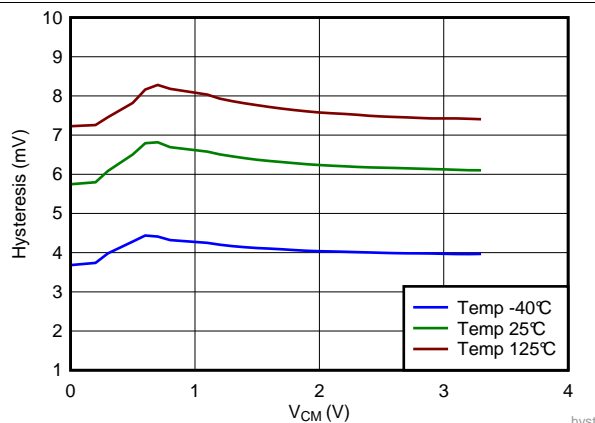
V_{CC} = 3.3 V

图 13. Hysteresis vs V_{CM}
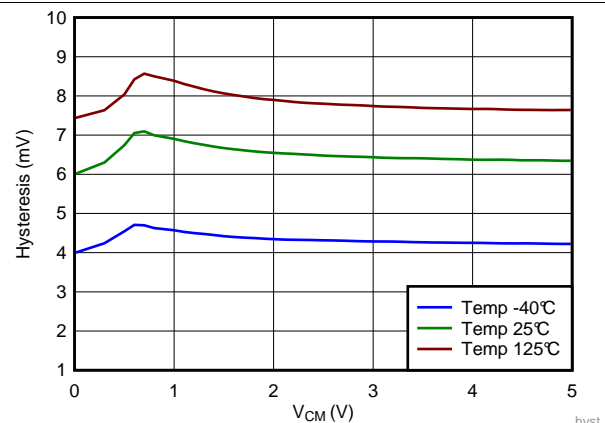
V_{CC} = 5 V

图 14. Hysteresis vs V_{CM}

Typical Characteristics (接下页)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF
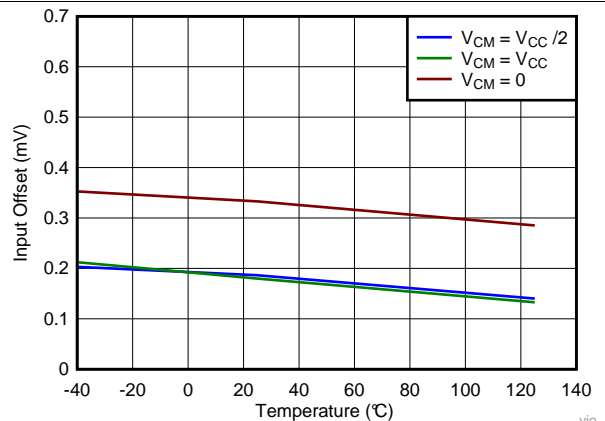
V_{CC} = 1.8 V

图 15. Input Offset vs Temperature
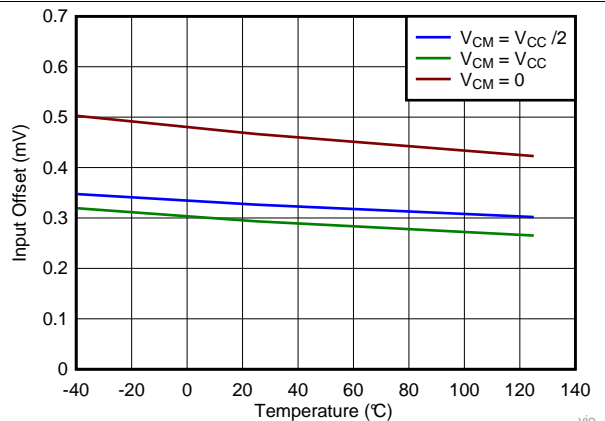
V_{CC} = 3.3 V

图 16. Input Offset vs Temperature
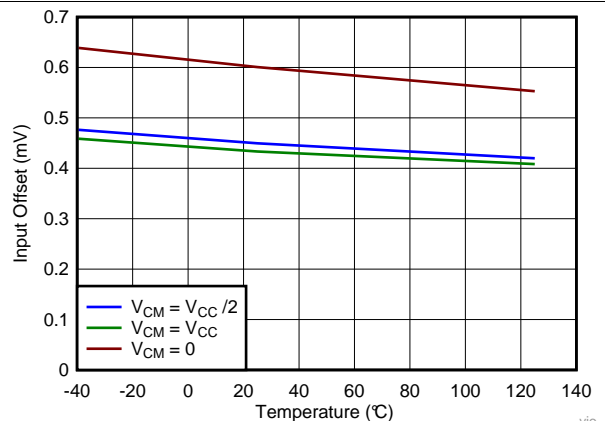
V_{CC} = 5 V

图 17. Input Offset vs Temperature
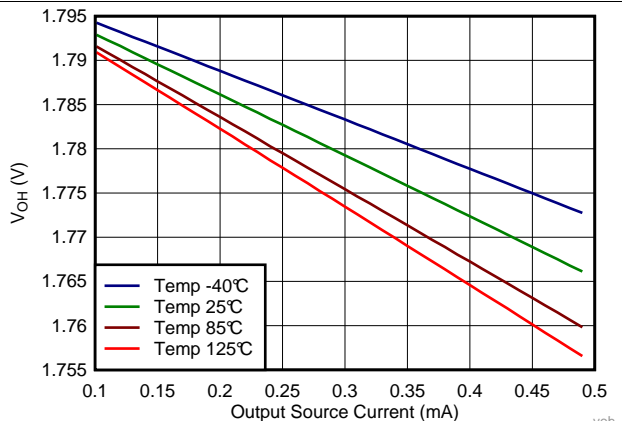
V_{CC} = 1.8 V

图 18. TLV7031 Output Voltage High vs Output Source Current
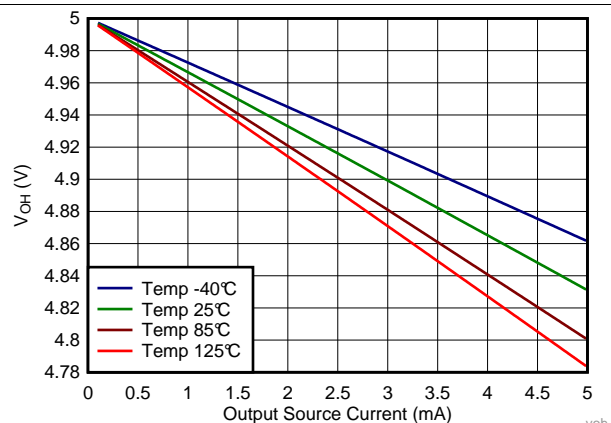
V_{CC} = 5 V

图 19. TLV7031 Output Voltage High vs Output Source Current
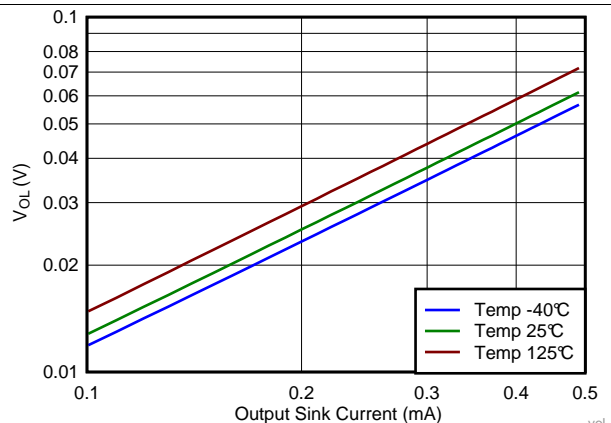
V_{CC} = 1.8 V

图 20. Output Voltage Low vs Output Sink Current

Typical Characteristics (接下页)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF

V_{CC} = 5 V
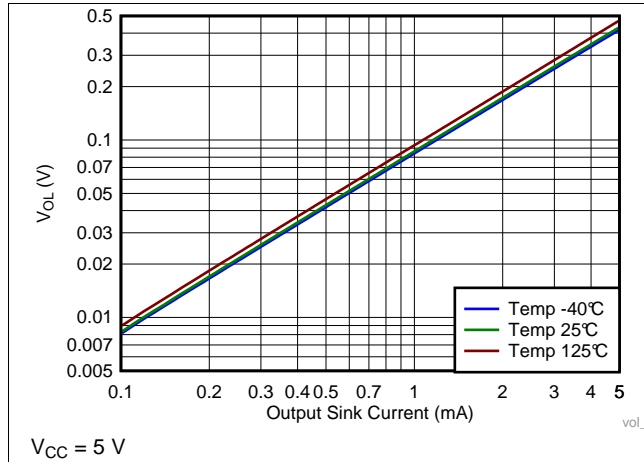
图 21. Output Voltage Low vs Output Sink Current

V_{CM} = V_{CC} / 2
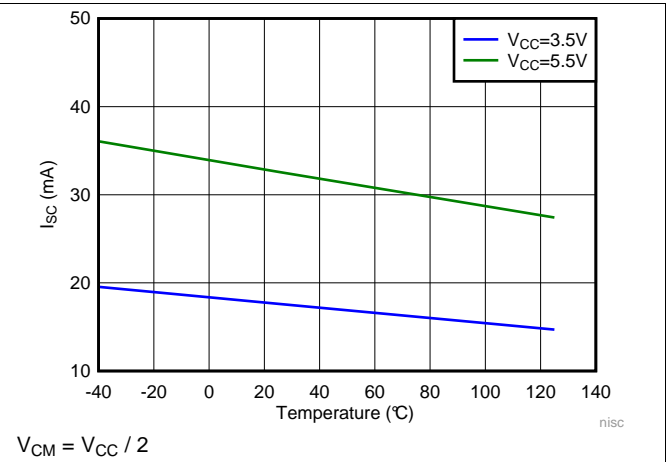
图 22. Output Short-Circuit (Sink) Current vs Temperature
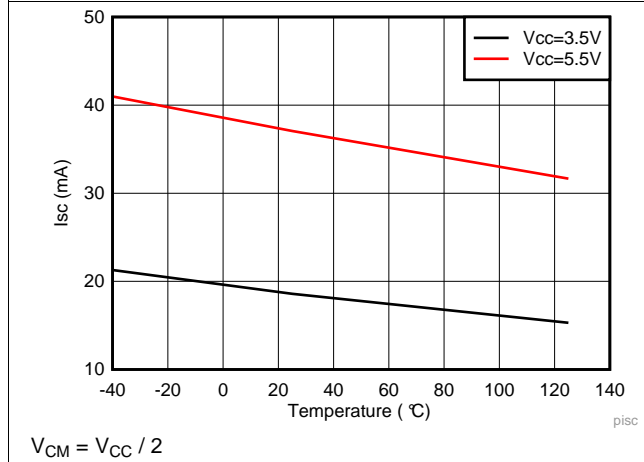
V_{CM} = V_{CC} / 2

图 23. TLV7031 Output Short-Circuit (Source) Current vs Temperature
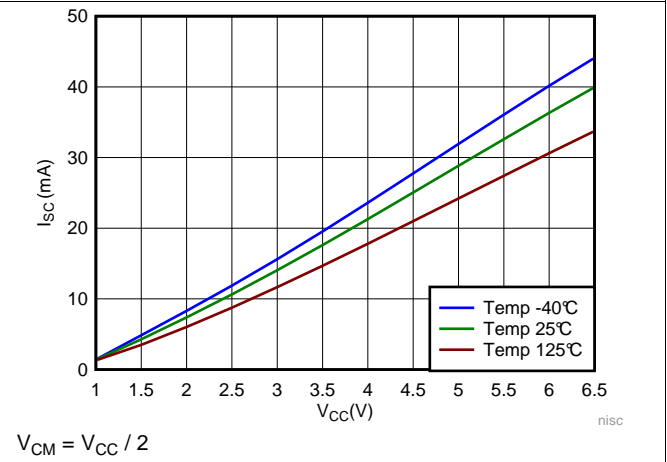
V_{CM} = V_{CC} / 2

图 24. Output Short Circuit (Sink) vs V_{CC}
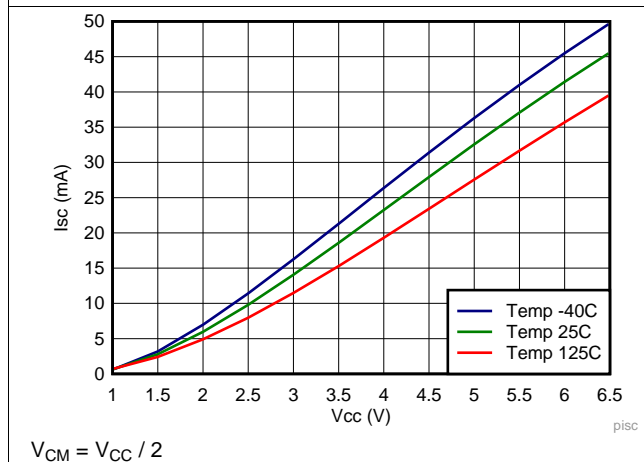
V_{CM} = V_{CC} / 2

图 25. TLV7031 Output Short Circuit (Source) vs V_{CC}
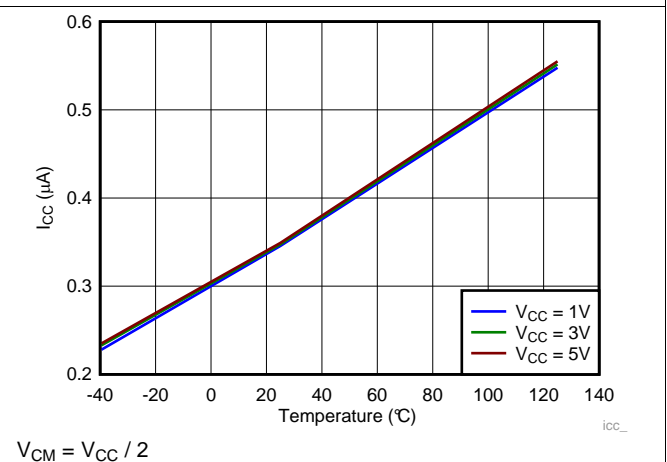
V_{CM} = V_{CC} / 2

图 26. I_{CC} vs Temperature

Typical Characteristics (接下页)

$T_A = 25°C$, $V_{CC} = 5$ V, $V_{EE} = 0$ V, $V_{CM} = V_{CC}/2$, $C_L = 15$ pF
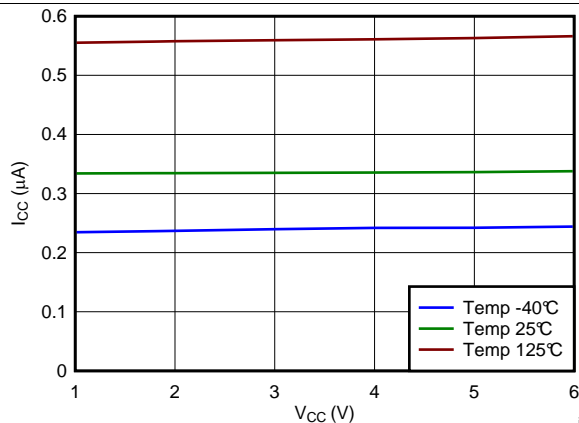
$V_{CM} = V_{CC} / 2$

图 27. I_{CC} vs V_{CC}
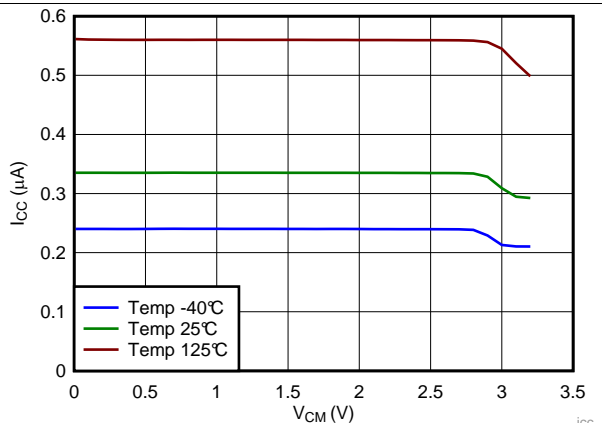
$V_{CC} = 3.3$ V

图 28. I_{CC} vs V_{CM}
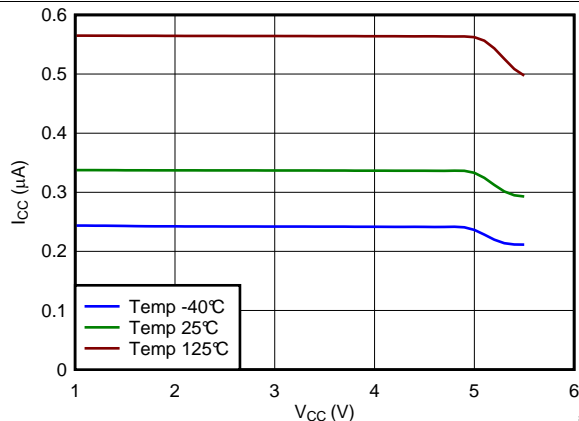
$V_{CC} = 5.5$ V

图 29. I_{CC} vs V_{CM}
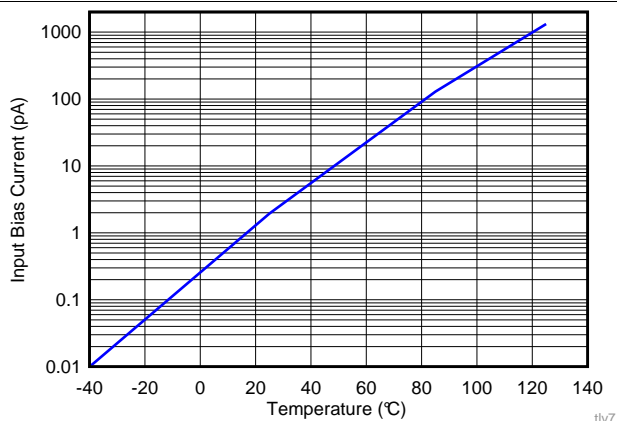
$V_{CC} = 5$ V

图 30. Input Bias Current vs Temperature
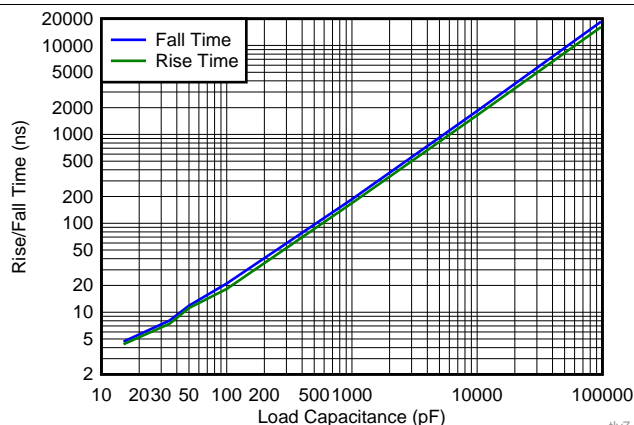
$V_{OD} = 100$ mV

图 31. Rise (TLV7031)/Fall Time vs Load Capacitance
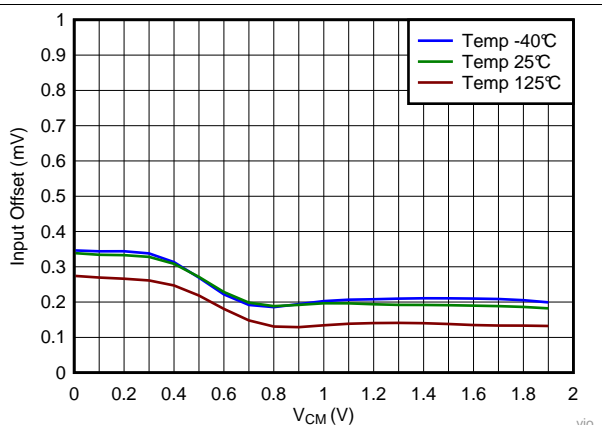
$V_{CC} = 1.8$ V

图 32. Input Offset Voltage vs V_{CM}

Typical Characteristics (接下页)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF

V_{CC} = 3.3 V, 50 devices

图 33. Input Offset Voltage vs V_{CM}

V_{CC} = 5 V, 50 devices

图 34. Input Offset Voltage vs V_{CM}
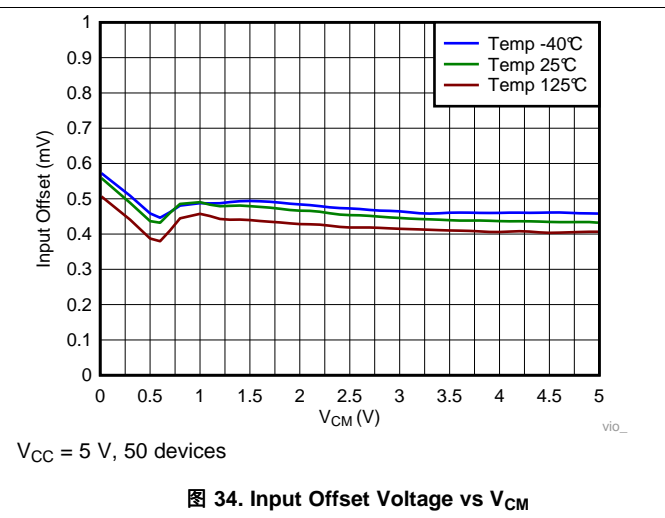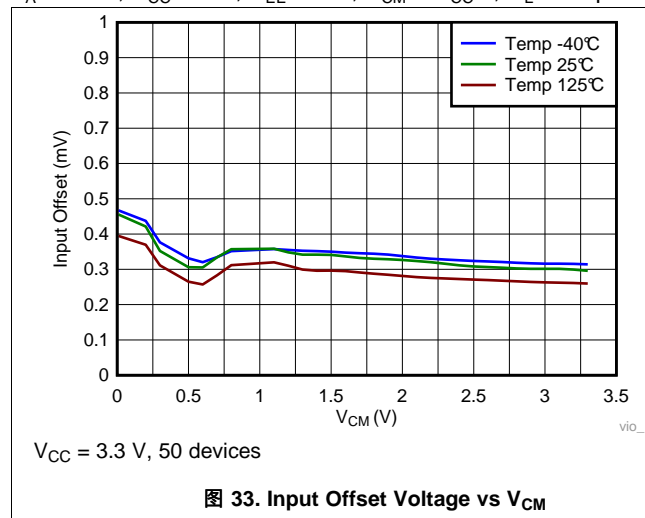
7 Detailed Description

7.1 Overview

The TLV703x and TLV704x devices are single-channel, nano-power comparators with push-pull and open-drain outputs. Operating from 1.6 V to 6.5 V and consuming only 335 nA, the TLV703x and TLV704x are designed for portable and industrial applications. The TLV703x and TLV704x are available in an ultra-small X2SON package (0.8 × 0.8 mm) to offer significant board space saving in space-challenged designs.

7.2 Functional Block Diagram
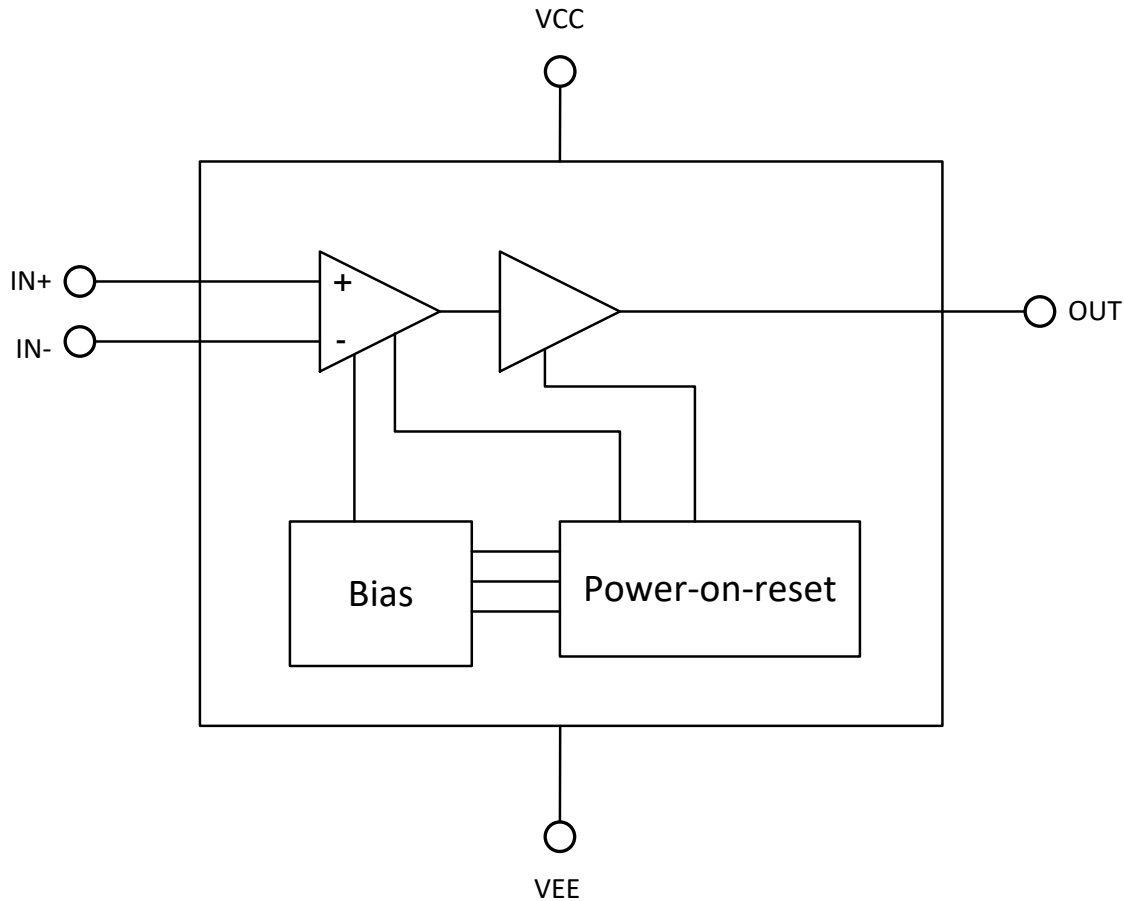
7.3 Feature Description

The TLV703x and TLV704x devices are nanoPower comparators that are capable of operating at low voltages. The TLV703x and TLV704x feature a rail-to-rail input stage capable of operating up to 100 mV beyond the VCC power supply rail. The TLV703x (push-pull) and TLV704x (open-drain) also feature internal hysteresis.

7.4 Device Functional Modes

The TLV703x and TLV704x have a power-on-reset (POR) circuit. While the power supply (V_S) is less than the minimum supply voltage, either upon ramp-up or ramp-down, the POR circuitry is activated.

For the TLV703x, the POR circuit holds the output low (at V_{EE}) while activated.

For the TLV704x, the POR circuit keeps the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

Device Functional Modes (接下页)

7.4.1 Inputs

The TLV703x and TLV704x input common-mode extends from V_{EE} to 100 mV above V_{CC}. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase inversion of the comparator output occurs when the input pins exceed V_{CC} and V_{EE}.

The input of TLV703x and TLV704x is fault tolerant. It maintains the same high input impedance when V_{CC} is unpowered or ramping up. The input can be safely driven up to the specified maximum voltage (7 V) with V_{CC} = 0 V or any value up to the maximum specified. The V_{CC} is isolated from the input such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between V_{CC} and V_{EE}. The comparator inputs are protected from voltages below V_{EE} by internal diodes connected to V_{EE}. As the input voltage goes under V_{EE}, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles every 10°C temperature increases.

7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in 图 35. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (7 mV for both TLV703x and TLV704x).

$V_{TH} + V_{OS} − (V_{HYST} / 2)$ $V_{TH} + V_{OS}$ $V_{TH} + V_{OS} + (V_{HYST} / 2)$
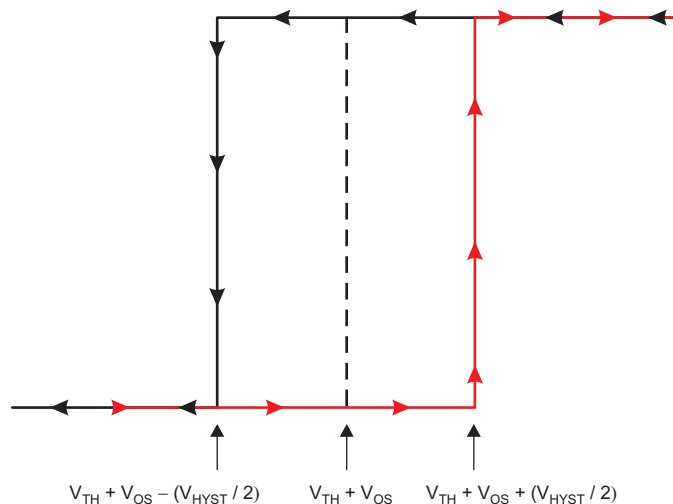
图 35. Hysteresis Transfer Curve

7.4.3 Output

The TLV703x features a push-pull output stage eliminating the need for an external pullup resistor. On the other hand, the TLV704x features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6.5 V independent of the supply voltage.

8 Application and Implementation

> 注
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV703x and TLV704x are nano-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV703x is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV704x with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and small size of the TLV703x and TLV704x make these comparators excellent candidates for battery-operated and portable, handheld designs.

8.1.1 Inverting Comparator With Hysteresis for TLV703x

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 图 36. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. 公式 1 defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2}$$

(1)

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use 公式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)}$$

(2)

公式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2}$$

(3)

Copyright © 2016, Texas Instruments Incorporated
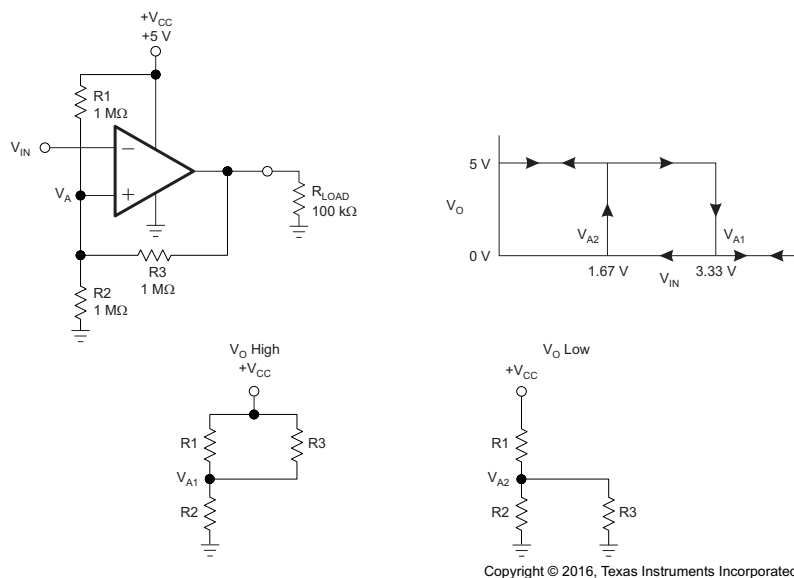
图 36. TLV703x in an Inverting Configuration With Hysteresis

Application Information (接下页)

8.1.2 Noninverting Comparator With Hysteresis for TLV703x

A noninverting comparator with hysteresis requires a two-resistor network, as shown in 图 37, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. Use 公式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF}$$

(4)

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF}. Use 公式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}(R1 + R2) - V_{CC} \times R1}{R2}$$

(5)

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 公式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2}$$

(6)
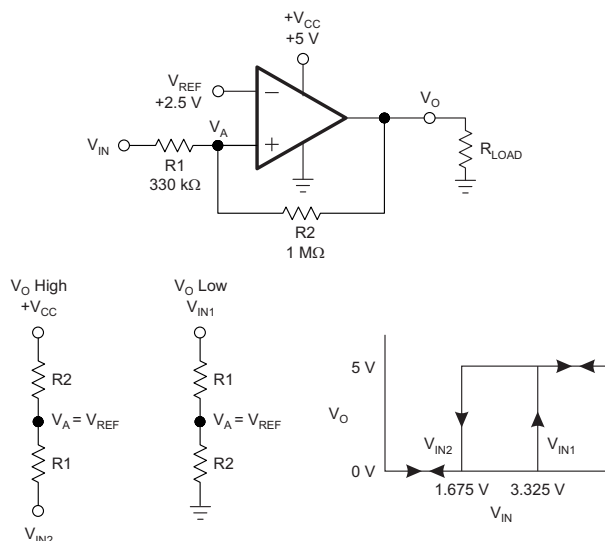
Copyright © 2016, Texas Instruments Incorporated

图 37. TLV703x in a Noninverting Configuration With Hysteresis

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 图 38 shows a simple window comparator circuit.
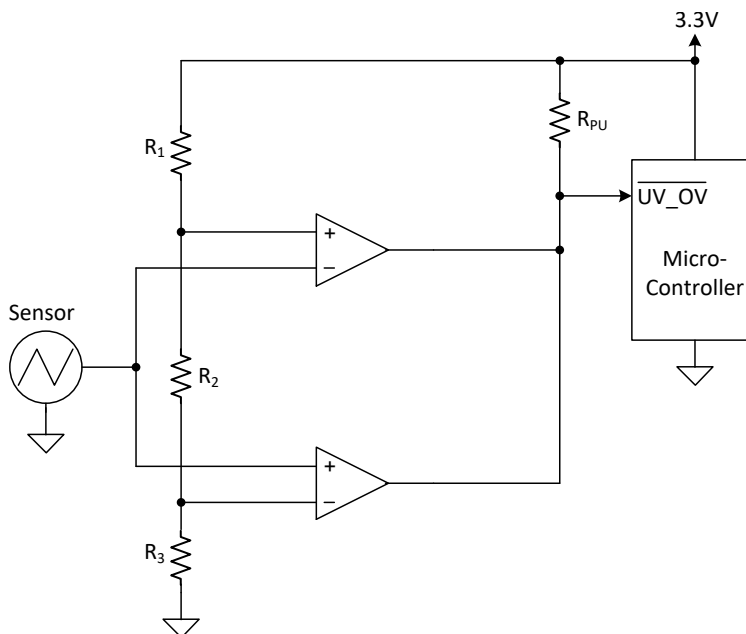
图 38. TLV704x-Based Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:
- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 图 38. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2, and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10 MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV704x devices. The TLV704x is used for its open-drain output configuration. Using the TLV704x allows the two comparator outputs to be wire-ored together. The respective comparator outputs are low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} is high when the sensor is in the range of 1.1 V to 2.2 V.

Typical Applications (接下页)

8.2.1.3 Application Curve
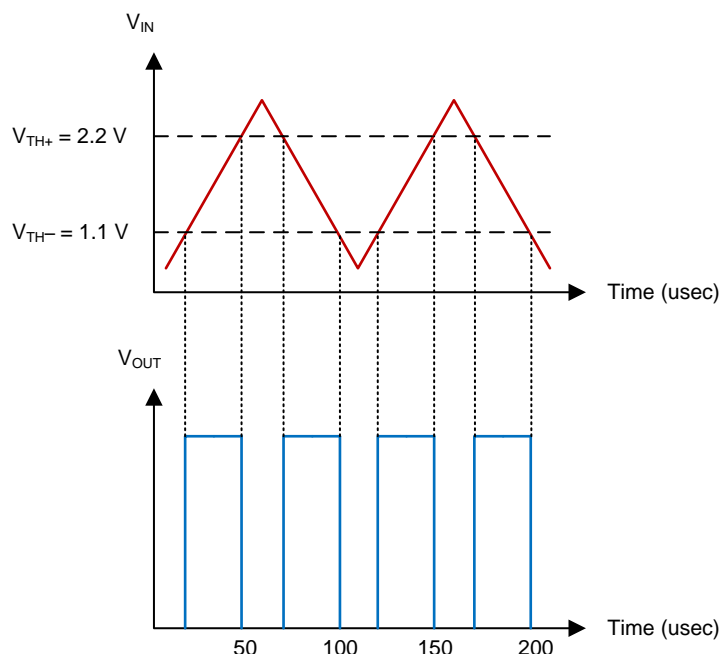
图 **39. Window Comparator Results**

8.2.2 IR Receiver Analog Front End

A single TLV703x device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.
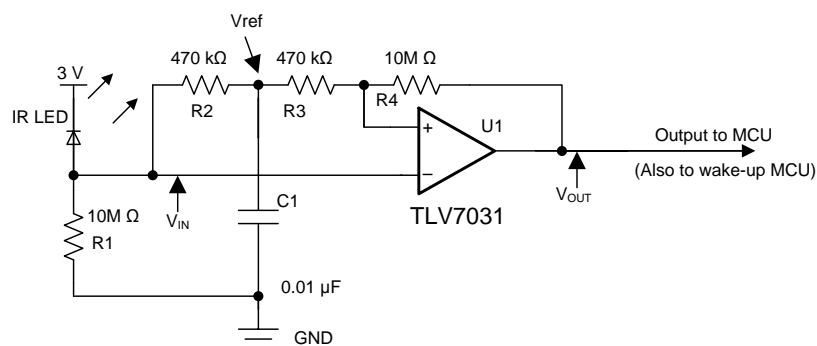
Copyright © 2017, Texas Instruments Incorporated

图 **40. IR Receiver Analog Front End Using TLV703x**

8.2.2.1 Design Requirements

For this design, follow these design requirements:

- Use a proper resistor (R_1) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current I_B (2 pA typical) ensures that a greater value of R1 to be used.
- The RC constant value (R_2 and C_1) must support the targeted data rate (that is, 9,600 bauds) in order to maintain a valid tripping threshold.
- The hysteresis introduced with R_3 and R_4 helps to avoid spurious output toggles.

Typical Applications (接下页)

8.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. R_1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. The RC network of R_2 and C_1 establishes a reference voltage V_{ref}, which tracks the mean amplitude of the IR signal. The noninverting input is directly connected to V_{ref} through R3. R3 and R4 are used to produce a hysteresis to keep transitions free of spurious toggles. To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

More technical details are provided in the TI TechNote *Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters* (SNVA808).

8.2.2.3 Application Curve
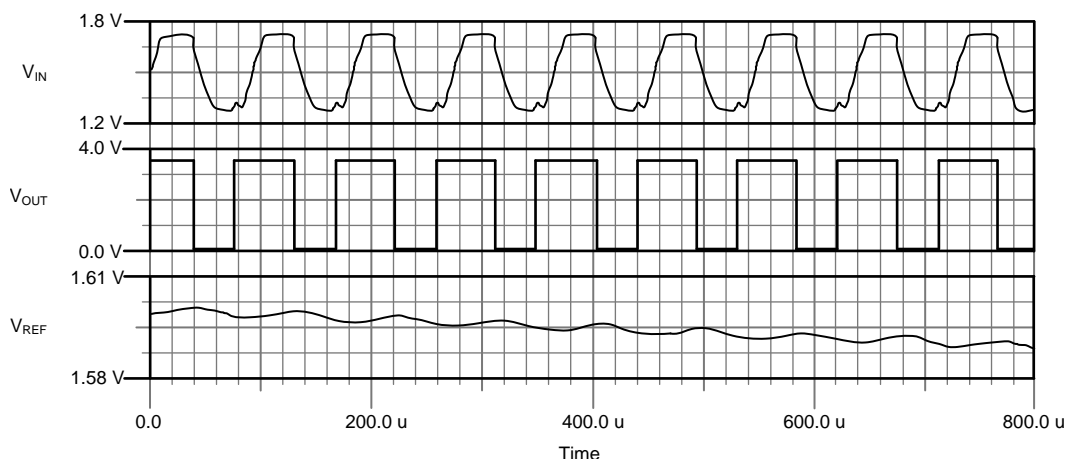
图 41. IR Receiver AFE Waveforms

Typical Applications (接下页)

8.2.3 Square-Wave Oscillator

A square-wave oscillator can be used as low-cost timing reference or system supervisory clock source.
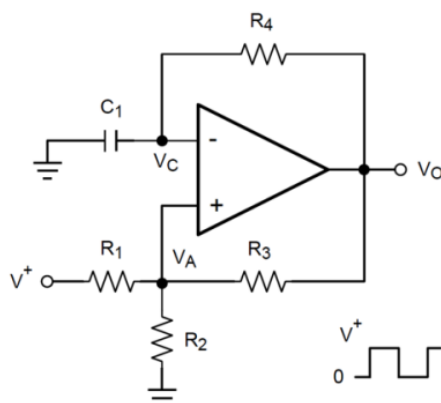
图 42. Square-Wave Oscillator

8.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by the propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help reduce BOM cost and board space.

8.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following section provides details to calculate these component values.
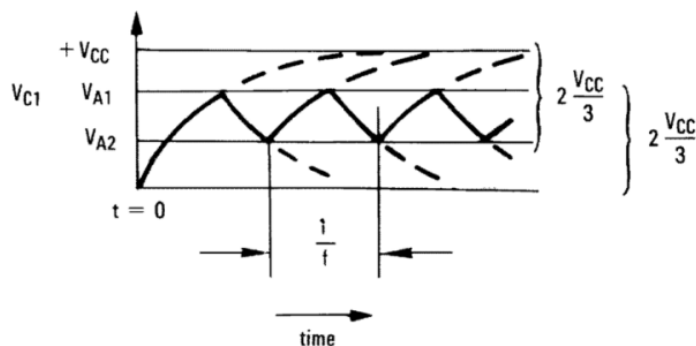
图 43. Square-Wave Oscillator Timing Thresholds

First consider the output of figure 图 42 is high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by 公式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3}$$

(7)

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\, V_{CC}/\, 3$

Typical Applications (接下页)

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by 公式 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3}$$

(8)

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$.

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals the time duration from 2 V_{CC} / 3 to V_{CC} / 3 then back to 2 V_{CC} / 3, which is given by $R_4 C_1$ × ln2 for each trip. Therefore, the total time duration is calculated as 2 $R_4 C_1$ × ln2. The oscillation frequency can be obtained by 公式 9:

$$f = 1/(2\ R4 \times C1 \times ln2)$$

(9)

8.2.3.3 Application Curve

图 44 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100\ pF$, $C_L = 20\ pF$
- $V+ = 5\ V$, $V- = GND$
- C_{stray} (not shown) from V_A to GND = 10 pF
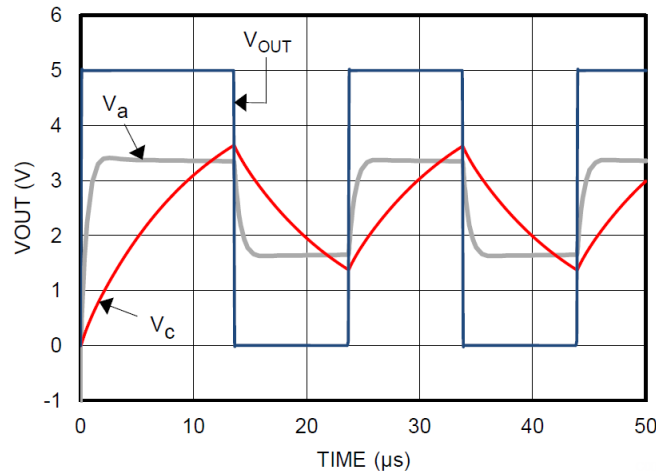
图 44. **Square-Wave Oscillator Output Waveform**

Typical Applications (接下页)

8.2.4 Quadrant Encoder Detector

A quadrant detector utilizing a Tunneling Magnetoresitance (TMR) Rotation Sensor and a line decoder can track the position of the encoder even when power is turned off, while the TLV7032 provides additional hysteresis to prevent unwanted output toggling between quadrants.
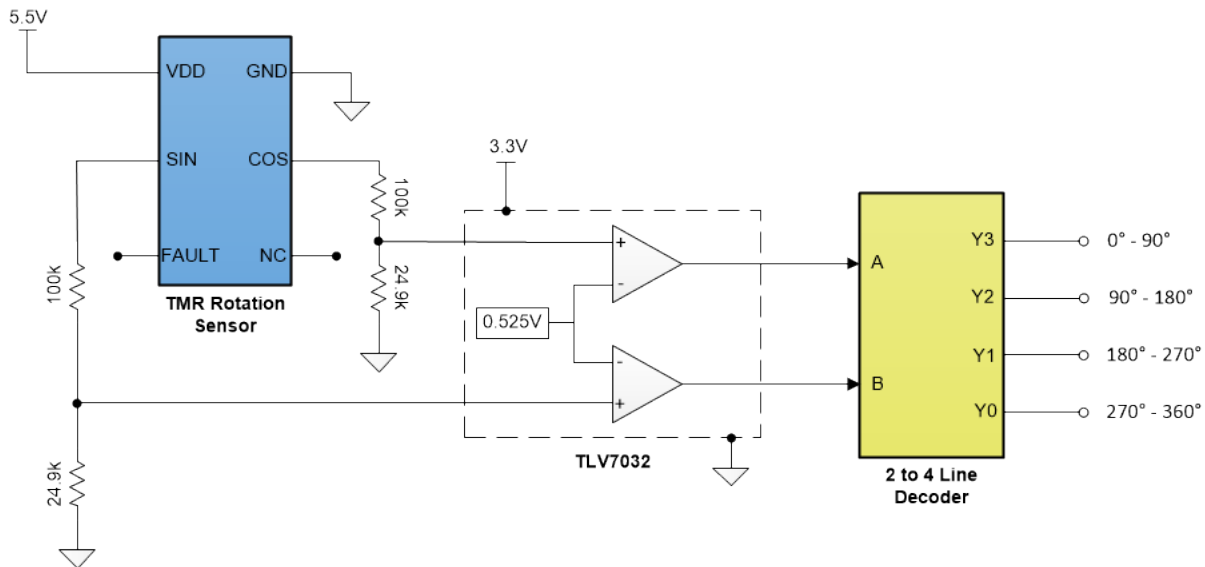
图 45. Quadrant Encoder Detector

8.2.4.1 Design Requirements

TMR Rotation Sensors general have two digital, binary outputs that are 90 degrees out of phase. The TLV7032 can be used to provide additional hysteresis to ensure there isn't any unwanted toggling of the output when the sensors are between the transition points of two quadrants. The TLV7032 already provides 10mV of typical internal hysteresis. By dividing down the output voltage from the rotation sensor using a voltage divider, the internal hysteresis will be scaled up by the same voltage divider ratio.

$$V_{OUT} = V_{IN} \times \frac{R2}{R1+R2}$$
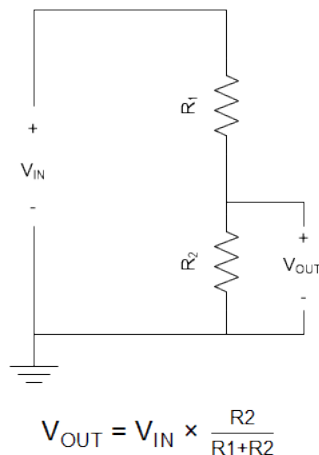
图 46. Voltage Divider Equation

Typical Applications (接下页)

8.2.4.2 Detailed Design Procedure

First, choose a target range of hysteresis to achieve. For this design example, 50mV of hysteresis will be the target. Since the TLV7032 already has 10mV (typ) of internal hysteresis, the voltage output from the TMR Rotation Sensor should be scaled down by a factor of 5. This way, the 10mV of internal hysteresis gets scaled up by a factor of 5, resulting in 50mV of hysteresis. The minimum output HIGH level for the TMR Rotation Sensor used in Figure 47 is 5.25 V. Since 5.25V will be the minimum output high value, it can be used to substitute V_{IN} from the Voltage Divider Equation in Figure 48. Since the voltage from the TMR rotation sensor needs to be scaled down by a factor of 5, the equation in Figure 48 can be rewritten as:

$$\frac{1}{5} = \frac{R_2}{R_1 + R_2}$$

The above equation can be solved for using standard resistor values, where R_1 = 100kΩ, and R_2 = 24.9kΩ. The minimum voltage seen at the noninverting pins of the comparator when the output is HIGH will be 1.05V. To make the device transition at 50% output high level, the inverting pins of the TLV7032 should be tied to a 0.525V reference.

8.2.4.3 Application Curve

Figure 49 shows the TLV7032 achieving approximately 50mV of hysteresis using the following component values:
- R_1 = 100kΩ
- R_2 = 24.9kΩ
- V_{REF} (IN-) = 0.525V
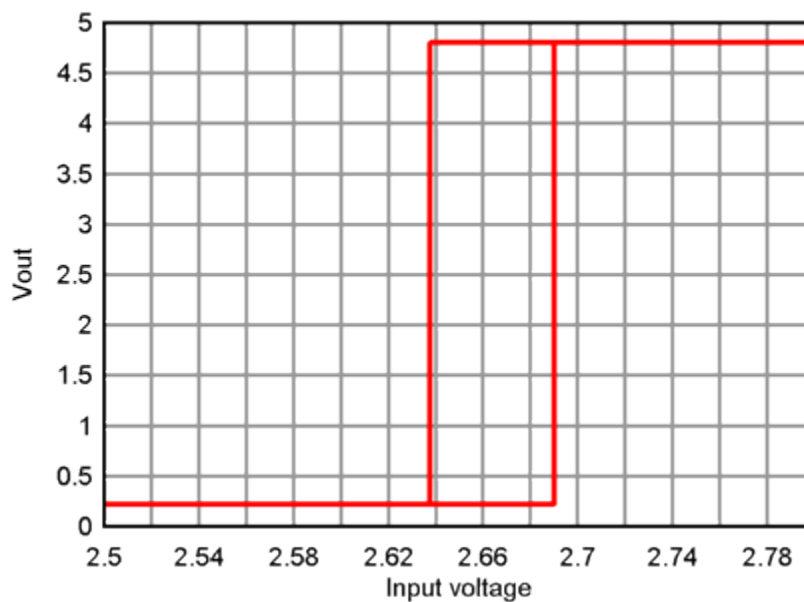
图 47. **DC Input Voltage Sweep**

9 Power Supply Recommendations

The TLV703x and TLV704x have a recommended operating voltage range (V_S) of 1.6 V to 6.5 V. V_S is defined as $V_{CC} - V_{EE}$. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to V_{EE}.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

To reduce PCB fabrication cost and improve reliability, TI recommends using a 4-mil via at the center pad connected to the ground trace or plane on the bottom layer.

TI recommends a power-supply bypass capacitor of 100 nF when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV703x and TLV704x output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

10.2 Layout Example

图 48. Layout Example

The application report *Designing and Manufacturing With TI's X2SON Packages* (SCEA055) helps PCB designers to achieve optimal designs.

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

我们为您提供了评估模块 (EVM)，可以借此来对使用 TLV70x1 器件系列的电路性能进行初始评估。TLV7011 微功耗比较器 DIP 适配器评估模块 可在德州仪器 (TI) 网站上的产品文件夹下申请，也可以直接从 TI 网上商店购买。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- *《使用 TI X2SON 封装进行设计和制造》* (SCEA055)
- *《智能仪表中的信号处理和唤醒电路的低功耗比较器》* (SNVA808)

11.3 相关链接

表 1 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具与软件，以及立即订购快速访问。

表 **1.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TLV7031	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV7041	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 *《使用条款》*。

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7031DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IE2	Samples
TLV7031DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19P	Samples
TLV7031DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19P	Samples
TLV7031DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7K	Samples
TLV7032DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22KF	Samples
TLV7032DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7032	Samples
TLV7032DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZXH	Samples
TLV7041DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IF2	Samples
TLV7041DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19Q	Samples
TLV7041DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19Q	Samples
TLV7041DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7L	Samples
TLV7042DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22LF	Samples
TLV7042DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7042	Samples
TLV7042DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZZH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7031DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV7031DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7031DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7031DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7032DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7032DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7032DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV7041DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV7041DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7041DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7041DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7042DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7042DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7042DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7031DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV7031DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7031DCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV7031DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7032DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7032DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV7032DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV7041DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV7041DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7041DCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV7041DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7042DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7042DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV7042DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

Pin 1
Index Area

2,15
1,85

2,40
1,80

1,40
1,10

0,65

1,30

5X 0,30
0,15

⊕ 0,10 Ⓜ

Gauge Plane
Seating Plane

0,22
0,08

0,15   0°−8°

0,46
0,26

1,10
0,80

0,10
0,00

□ 0,10

Seating Plane

4093553−3/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
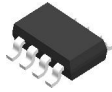   D.   Falls within JEDEC MO−203 variation AA.

TEXAS
INSTRUMENTS
www.ti.com

DCK (R—PDSO—G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

2x0,65

2x1,30

2x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356—2/C 07/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
        D. Publication IPC—7351 is recommended for alternate designs.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
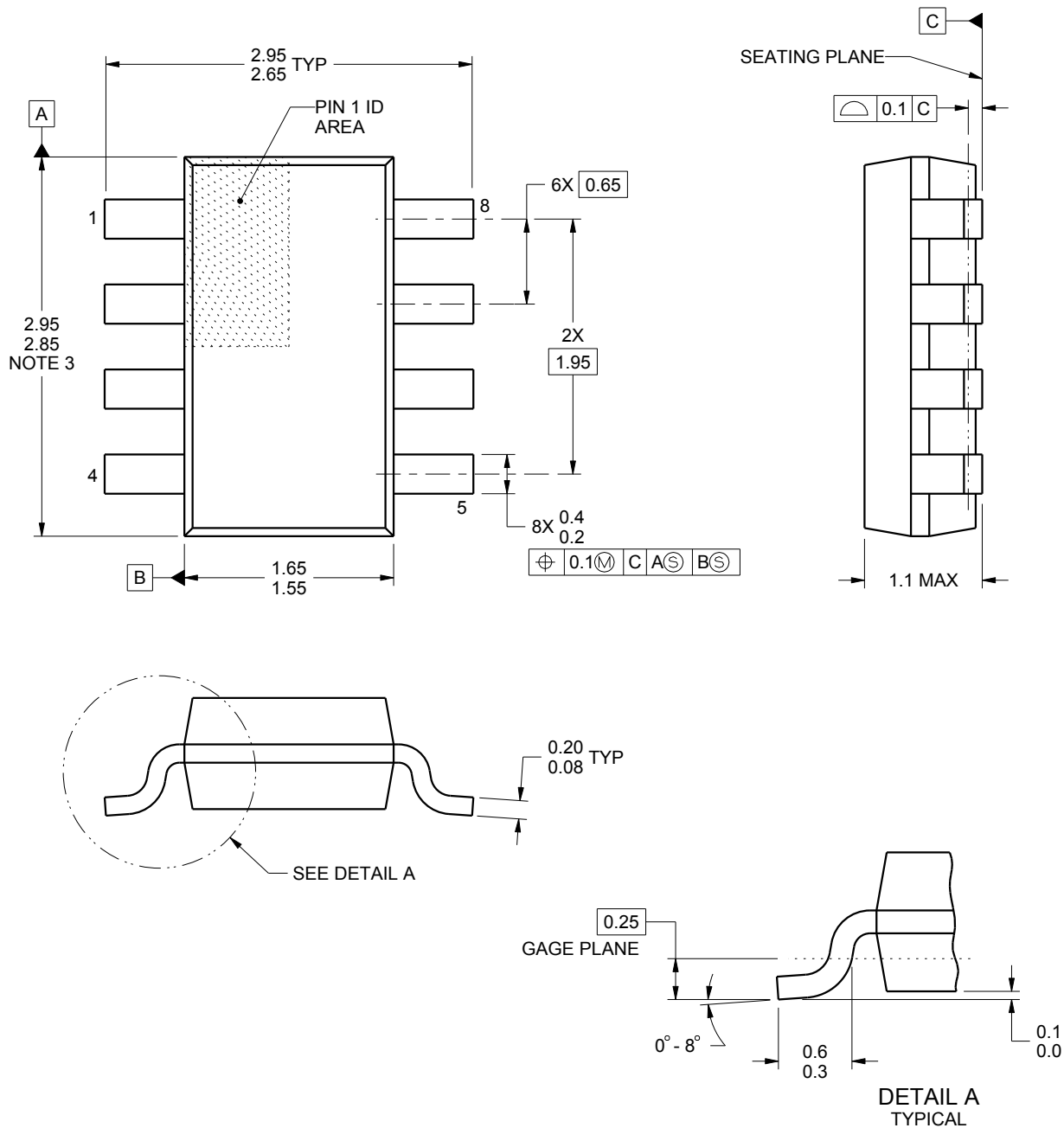   metal load solder paste. Refer to IPC—7525 for other stencil recommendations.

2.95 / 2.65 TYP

A

PIN 1 ID AREA

1

2.95 / 2.85 NOTE 3

4

B   1.65 / 1.55

8

6X [0.65]

2X [1.95]

5

8X 0.4 / 0.2

⊕ [0.1 Ⓜ] C AⓈ BⓈ

C

SEATING PLANE

⌒ [0.1] C

1.1 MAX

SEE DETAIL A

0.20 / 0.08 TYP

GAGE PLANE

[0.25]

0° - 8°

0.6 / 0.3

0.1 / 0.0

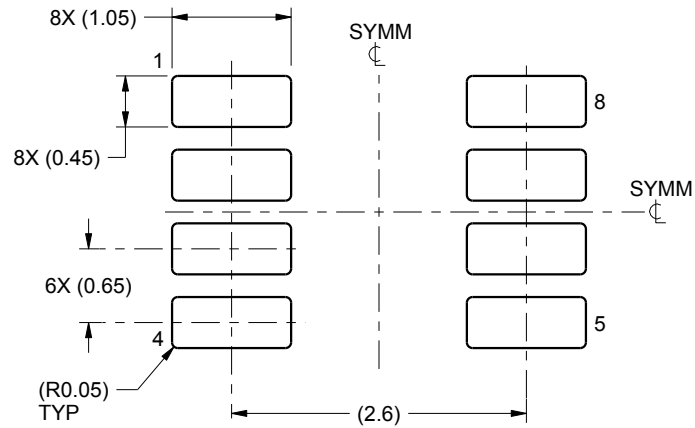**DETAIL A**
TYPICAL

4222047/B   11/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

8X (1.05)

SYMM

1

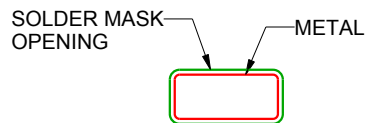8X (0.45)

8

6X (0.65)

SYMM

4

5

(R0.05)
TYP

(2.6)

LAND PATTERN EXAMPLE
SCALE:15X

SOLDER MASK
OPENING — METAL

METAL UNDER — SOLDER MASK
SOLDER MASK — OPENING

NON SOLDER MASK
DEFINED
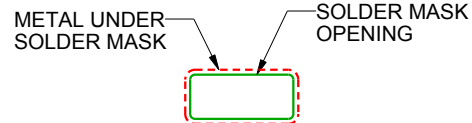
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

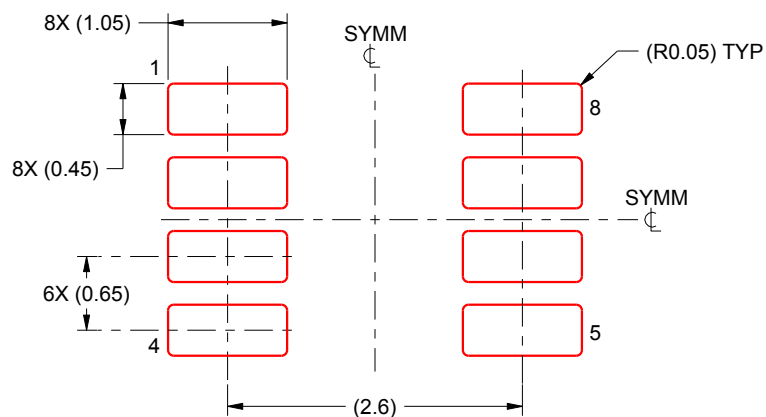4222047/B   11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.05)

SYMM

(R0.05) TYP

1

8X (0.45)

8

SYMM

6X (0.65)

4

5

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X
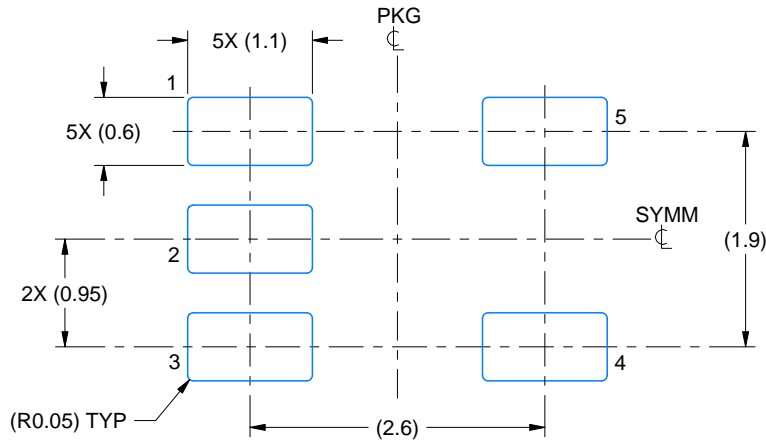
4222047/B   11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

4214839/F   06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK OPENING

METAL

EXPOSED METAL

0.07 MAX ARROUND

NON SOLDER MASK DEFINED (PREFERRED)

METAL UNDER SOLDER MASK

SOLDER MASK OPENING

EXPOSED METAL

0.07 MIN ARROUND

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/F   06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

5X (1.1)

PKG

1

5X (0.6)

5

2

SYMM

(1.9)

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
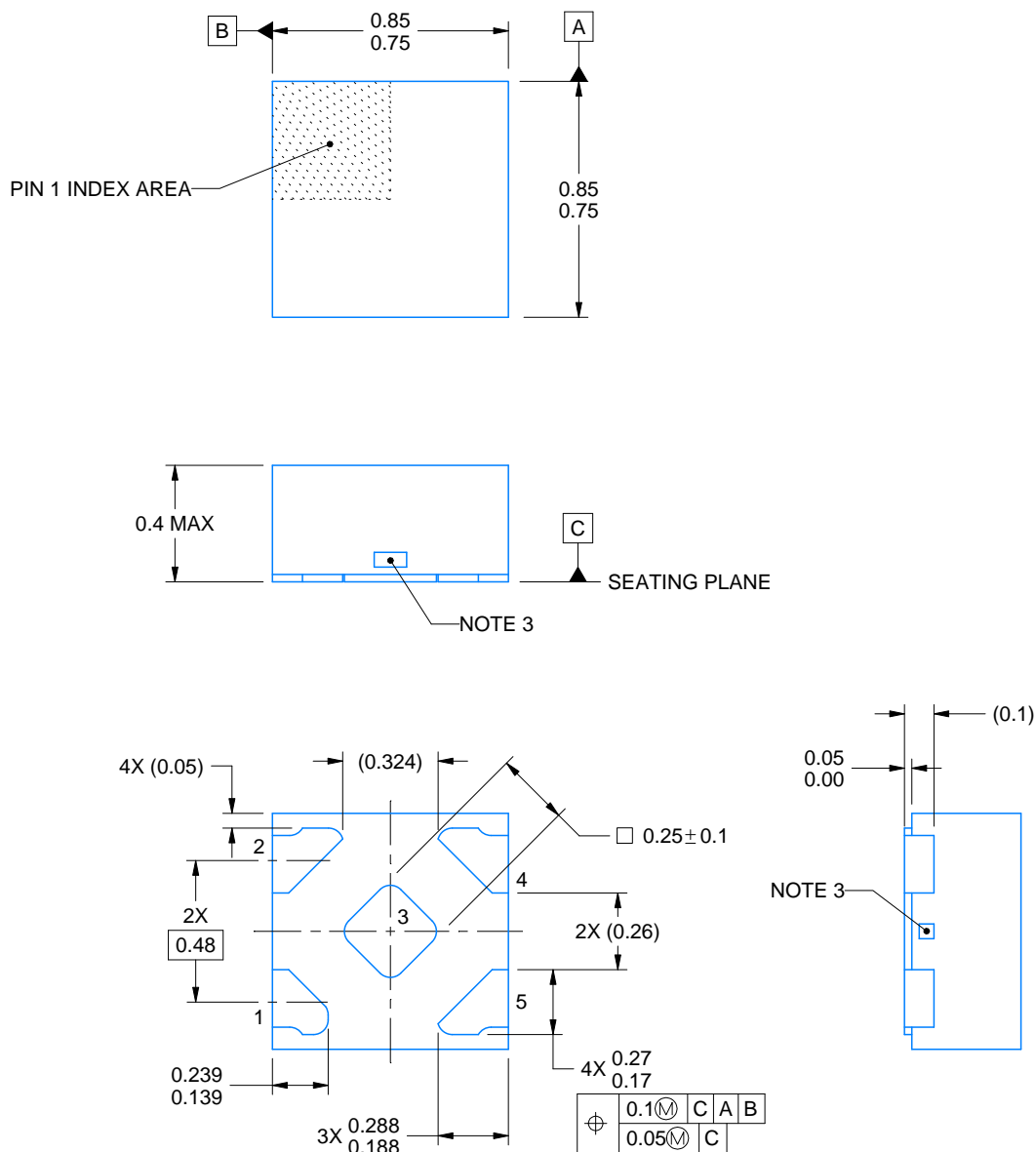8. Board assembly site may have different recommendations for stencil design.

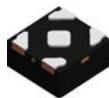Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D

TEXAS
INSTRUMENTS

B
0.85
0.75
A

PIN 1 INDEX AREA

0.85
0.75

0.4 MAX

C

SEATING PLANE

NOTE 3

4X (0.05)

(0.324)

(0.1)

0.05
0.00

□ 0.25±0.1

NOTE 3

2
2X
0.48
1

3

4

2X (0.26)

5

0.239
0.139

4X 0.27
0.17

3X 0.288
0.188

⊕ | 0.1 Ⓜ | C | A | B
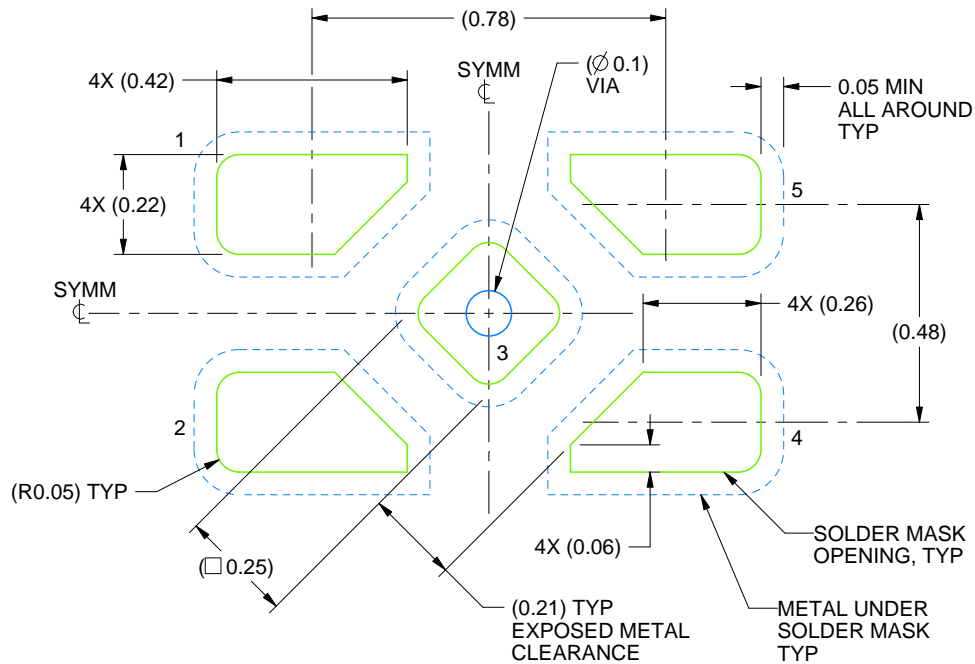| 0.05 Ⓜ | C

4223102/D   03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

(0.78)

4X (0.42)

SYMM

($\emptyset$ 0.1)
VIA

0.05 MIN
ALL AROUND
TYP

1

4X (0.22)

5

SYMM

4X (0.26)

(0.48)

3

2

4

(R0.05) TYP

4X (0.06)

SOLDER MASK
OPENING, TYP

($\square$ 0.25)

METAL UNDER
SOLDER MASK
TYP

(0.21) TYP
EXPOSED METAL
CLEARANCE

LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D   03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note
   in literature No. SLUA271 (www.ti.com/lit/slua271).

4X (0.42)

4X (0.06)

4X (0.22)

1

4X (0.26)

5

(□0.24)

SYMM

SOLDER MASK
EDGE

(0.21)
TYP

(0.48)

3

2

4

(R0.05) TYP

SYMM

(0.78)

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGK (S−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE

0,65

8

5

0,38
0,25   ⊕ 0,13 Ⓜ

3,10
2,90

5,05
4,75

1

4

3,10
2,90

0,23
0,13

Gauge Plane

0°−8°

0,25

0,70
0,40

1,10 MAX

0,15
0,05

Seating Plane

0,10

4073329/E 05/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.15 per end.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
         E.   Falls within JEDEC MO−187 variation AA, except interlead flash.

DGK (S−PDSO−G8) PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

|←→|(0,65)TYP.

8 5

PKG
℄

(4,4)

1 4

PKG
℄

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

←(0,45)

(1,45)

↓(0,05)
All Around

Pad Geometry
(See Note C)

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

8X(0,45) →| |← |←→|(0,65)TYP.

8X(1,45)

PKG
℄

(4,4)

PKG
℄

4221236/A 11/13

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
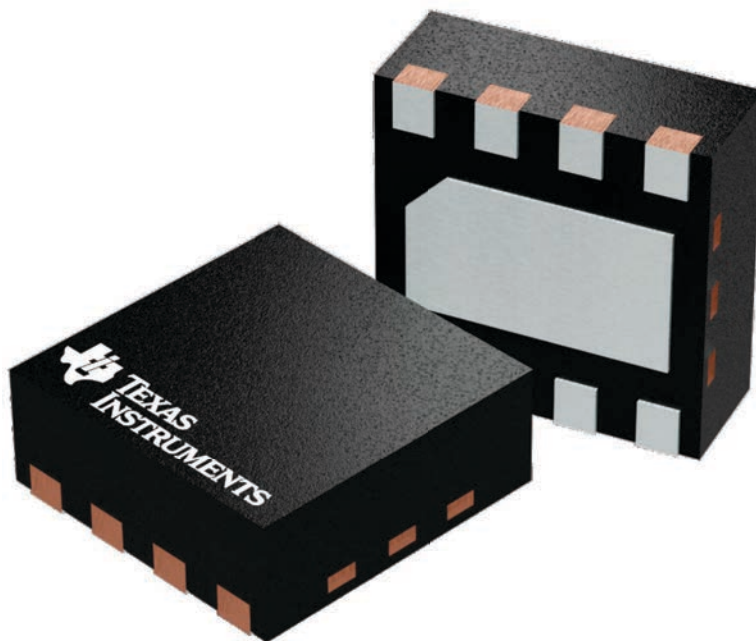
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224783/A

A | 2.1 / 1.9 | B
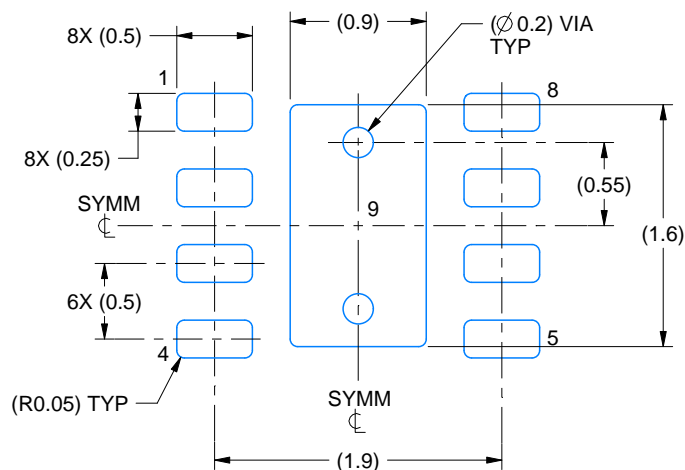
PIN 1 INDEX AREA

2.1 / 1.9

0.32 / 0.18

0.4 / 0.2

ALTERNATIVE TERMINAL SHAPE
TYPICAL

0.8 MAX

0.05 / 0.00

C

SEATING PLANE

⌒ | 0.08 | C

EXPOSED THERMAL PAD

0.9 ± 0.1

4

5

6X | 0.5

2X | 1.5

9

1.6 ± 0.1

1

8

PIN 1 ID

8X 0.4 / 0.2

8X 0.32 / 0.18

(0.2) TYP

⊕ | 0.1 Ⓜ | C | A | B
   | 0.05 Ⓜ | C
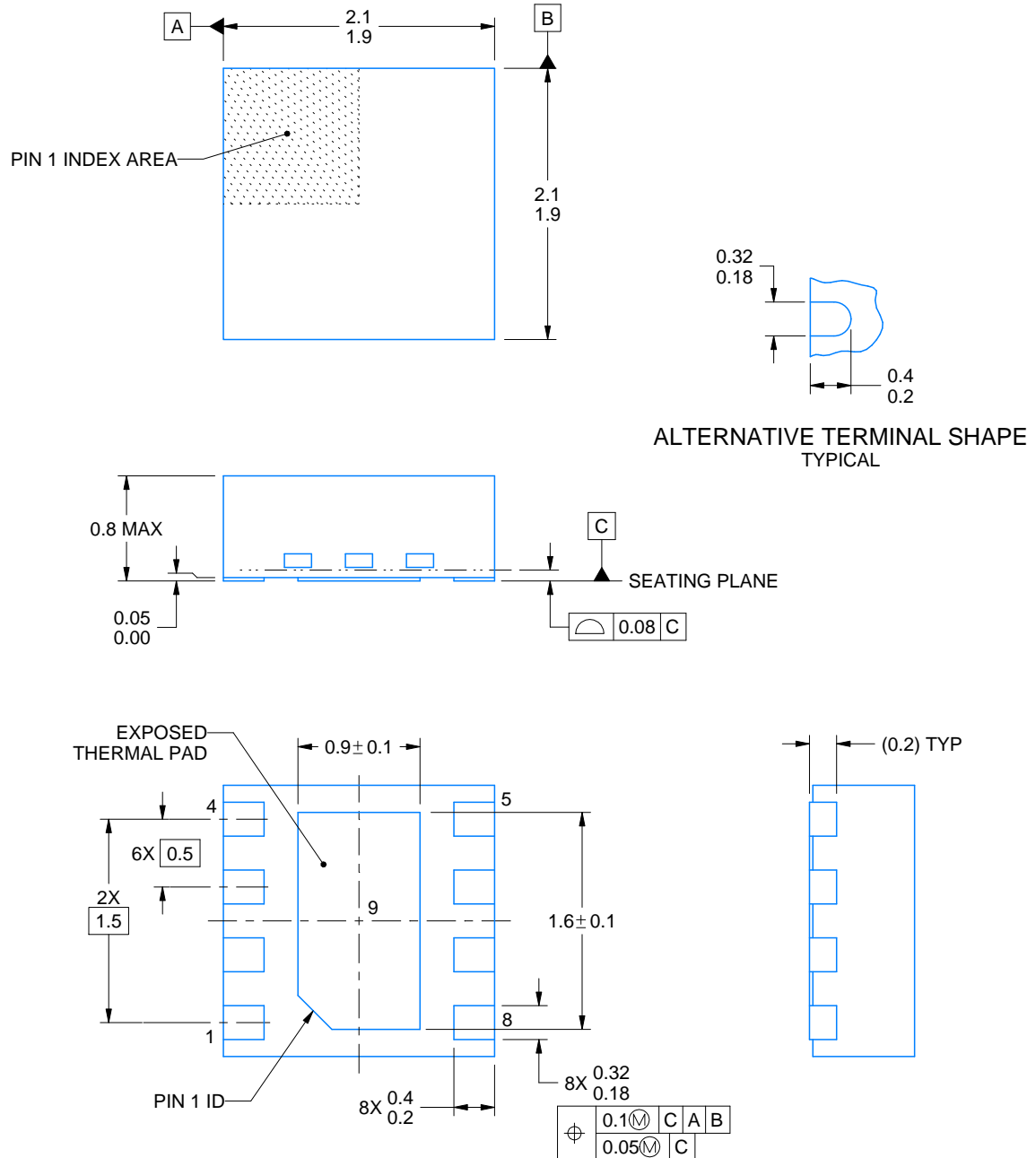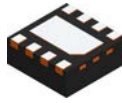
4218900/D   04/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
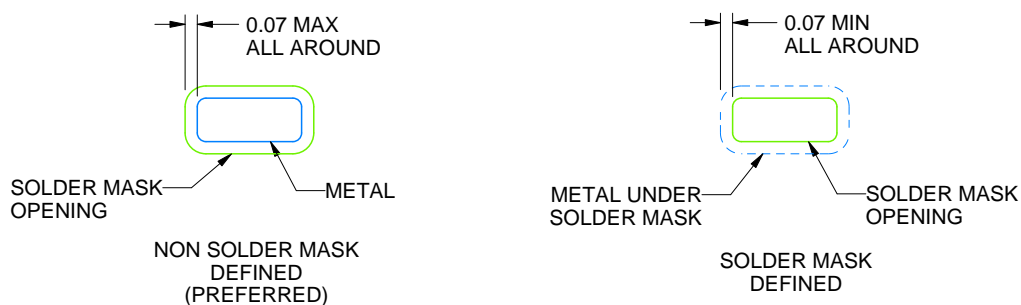
8X (0.5)

(0.9)

(⌀ 0.2) VIA
TYP

1

8

8X (0.25)

SYMM
℄

9

(0.55)

(1.6)

6X (0.5)

4

5

(R0.05) TYP

SYMM
℄

(1.9)

LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/D   04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
on this view. It is recommended that vias under paste be filled, plugged or tented.
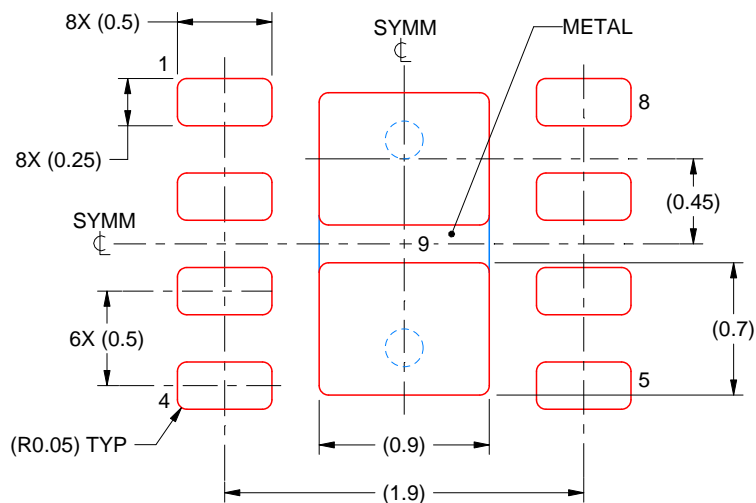
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明