UCC2720x-Q1 120-V Boot, 3-A Peak, High-Frequency High-Side and Low-Side Driver

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- Drives Two N-Channel MOSFETs in High-Side and Low-Side Configuration
- Maximum Boot Voltage: 120 V
- Maximum V_{DD} Voltage: 20 V
- On-Chip 0.65-V VF, 0.6-Ω RD Bootstrap Diode
- Greater than 1 MHz of Operation
- 20-ns Propagation Delay Times
- 3-A Sink, 3-A Source Output Currents
- 8-ns Rise and 7-ns Fall Time With 1000-pF Load
- 1-ns Delay Matching
- Specified from –40°C to 140°C (Junction Temperature)

2 Applications

- Power Supplies for Telecom, Datacom, and Merchant Markets
- Half-Bridge Applications and Full-Bridge Converters
- Isolated Bus Architecture
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- High-Voltage Synchronous-Buck Converters
- Class-D Audio Amplifiers

3 Description

The UCC2720x-Q1 family of high-frequency N-channel MOSFET drivers include a 120-V bootstrap diode and high-side and low-side drivers with independent inputs for maximum control flexibility. This allows for N-channel MOSFET control in half-bridge, full-bridge, two-switch forward, and active-clamp forward converters. The low-side and the high-side gate drivers are independently controlled and matched to 1 ns between the turnon and turnoff of each other.

An on-chip bootstrap diode eliminates the external discrete diodes. Undervoltage lockout is provided for both the high-side and the low-side drivers, forcing the outputs low if the drive voltage is below the specified threshold.

Two versions of the UCC2720x-Q1 are offered – the UCC27200-Q1 has high-noise-immune CMOS input thresholds, and the UCC27201-Q1 has TTL-compatible thresholds.

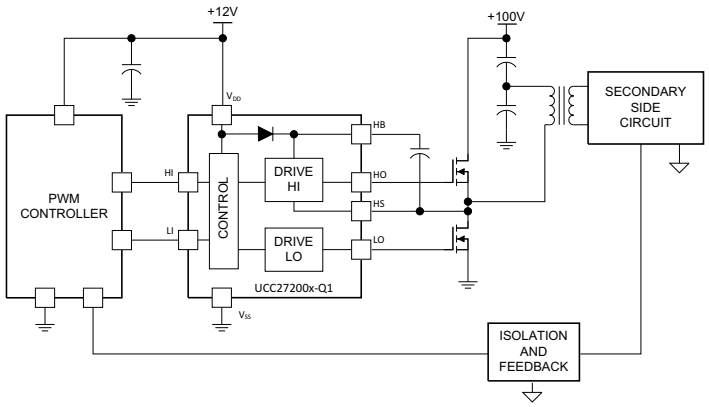
Both devices are offered in the 8-pin SO PowerPAD™ (DDA) package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC2720x-Q1	SO PowerPAD (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2016) to Revision C — **Page**

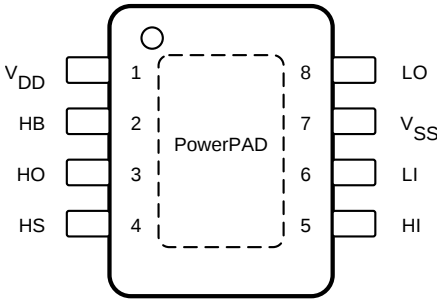
- Changed the device temperature grade in the *Features* section from Grade 0 (–40°C to 150°C) to Grade 1 (–40°C to 125°C) ... 1
- Added the *Receiving Notification of Documentation Updates* section ... 25

Changes from Revision A (November 2008) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added AEC-Q100 Qualification bullets ... 1
- Changed device numbers UCC2720x and UCC27200 to UCC2720x-Q1 and UCC27200-Q1 ... 1
- Deleted *Wirebond Life* figure ... 6
- Moved references from *Additional References* section to *Related Documentation* section ... 25

5 Pin Configuration and Functions

DDA Package
8-Pin SO With PowerPAD
Top View



The V_{SS} pin and the exposed thermal die pad are internally connected.

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	V_{DD}	P	Positive supply to the lower gate driver. Decouple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22 μF to 1 μF.
2	HB	I	High-side bootstrap supply. The bootstrap diode is on-chip, but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 μF to 0.1 μF, however, the value is dependant on the gate charge of the high-side MOSFET.
3	HO	O	High-side output. Connect to the gate of the high-side power MOSFET.
4	HS	I	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	I	High-side input
6	LI	I	Low-side input
7	V_{SS}	O	Negative supply terminal for the device which is generally grounded
8	LO	—	Low-side output. Connect to the gate of the low-side power MOSFET.
PowerPAD	PowerPAD	—	Electrically referenced to V_{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.3	20	V
V_{LI}, V_{HI}	Input voltages on LI and HI		–0.3	20	V
V_{LO}	Output voltage on LO	DC	–0.3	V_{DD} + 0.3	V
		Repetitive pulse < 100 ns	–2	V_{DD} + 0.3	V
V_{HO}	Output voltage on HO	DC	V_{HS} – 0.3	V_{HB} + 0.3	V
		Repetitive pulse < 100 ns	V_{HS} – 2	V_{HB} + 0.3, (V_{HB} – V_{HS} < 20)	V
V_{HS}	HS voltage	DC	–1	120	V
		Repetitive pulse < 100 ns	–5	120	V
V_{HB}	HB voltage		–0.3	120	V
	HB-HS voltage		–0.3	20	V
T_{lead}	Lead temperature	Soldering, 10 seconds		300	°C
P_D	Power dissipation	T_A = 25°C(3)		2.7	W
T_J	Operating virtual-junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to V_{SS}. Currents are positive into, negative out of the specified terminal.
(3) This data was taken using the JEDEC proposed high-K test PCB (see *Thermal Information* for details).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	8	12	17	V
V_{HS}	HS voltage	–1		105	V
	HS voltage (repetitive pulse <100 ns)	–5		110	
V_{HB}	HB voltage	V_{HS} + 8		V_{HS} + 17	V
		V_{DD} – 1		115	
	Voltage slew rate on HS			50	V/ns
T_J	Operating junction temperature	–40		140	°C
T_A	Operating ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		UCC2720x-Q1 DDA (SO) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, $V_{DD} = V_{HB} = 12$ V, $V_{HS} = V_{SS} = 0$ V, No load on LO or HO, $T_J = –40°C$ to 140°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENTS								
I_{DD}	V_{DD} quiescent current		$V_{LI} = V_{HI} = 0$			0.4	0.8	mA
I_{DDO}	V_{DD} operating current	UCC27200-Q1	f = 500 kHz, $C_{LOAD} = 0$			2.5	4	mA
		UCC27201-Q1				3.8	5.5	
I_{HB}	Boot voltage quiescent current		$V_{LI} = V_{HI} = 0$ V			0.4	0.8	mA
I_{HBO}	Boot voltage operating current		f = 500 kHz, $C_{LOAD} = 0$			2.5	4	mA
I_{HBS}	HB to V_{SS} quiescent current		$V_{HS} = V_{HB} = 110$ V			0.0005	1	µA
I_{HBSO}	HB to V_{SS} operating current		f = 500 kHz, $C_{LOAD} = 0$			0.1		mA
INPUT								
V_{HIT}	Input rising threshold	UCC27200-Q1				5.8	8	V
V_{LIT}	Input falling threshold	UCC27200-Q1			3	5.4		V
V_{IHYS}	Input voltage hysteresis	UCC27200-Q1				0.4		V
V_{HIT}	Input voltage threshold	UCC27201-Q1				1.7	2.5	V
V_{LIT}	Input voltage threshold	UCC27201-Q1			0.8	1.6		V
V_{IHYS}	Input voltage hysteresis	UCC27201-Q1				100		mV
R_{IN}	Input pulldown resistance				100	200	350	kΩ
UNDERVOLTAGE LOCKOUT (UVLO) PROTECTION								
	V_{DD} rising threshold				6.2	7.1	7.8	V
	V_{DD} threshold hysteresis					0.5		V
	VHB rising threshold				5.8	6.7	7.2	V
	VHB threshold hysteresis					0.4		V
BOOTSTRAP DIODE								
V_F	Low-current forward voltage		I_{VDD} – HB = 100 µA			0.65	0.85	V
V_{FI}	High-current forward voltage		I_{VDD} – HB = 100 mA			0.85	1.1	
R_D	Dynamic resistance, ΔVF/ΔI		I_{VDD} – HB = 100 mA and 80 mA			0.6	1	Ω
LO GATE DRIVER								
V_{LOL}	Low level output voltage		I_{LO} = 100 mA			0.18	0.4	V
V_{LOH}	High level output voltage		I_{LO} = –100 mA, $V_{LOH} = V_{DD} – V_{LO}$	T_J = –40°C to 125°C		0.25	0.4	V
				T_J = –40°C to 140°C		0.25	0.42	
	Peak pullup current		V_{LO} = 0 V			3		A
	Peak pulldown current		V_{LO} = 12 V			3		A

Electrical Characteristics (continued)

over operating free-air temperature range, V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_J = –40°C to 140°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HO GATE DRIVER							
V_{HOL}	Low-level output voltage	I_{HO} = 100 mA			0.18	0.4	V
V_{HOH}	High-level output voltage	I_{HO} = –100 mA, V_{HOH} = V_{HB} – V_{HO},	T_J = –40°C to 125°C		0.25	0.4	V
			T_J = –40°C to 140°C		0.25	0.42	
	Peak pullup current	V_{HO} = 0 V			3		A
	Peak pulldown current	V_{HO} = 12 V			3		A
PROPAGATION DELAYS							
T_{DLFF}	V_{LI} falling to V_{LO} falling	C_{LOAD} = 0	T_J = –40°C to 125°C		20	45	ns
			T_J = –40°C to 140°C		20	50	
T_{DHFF}	V_{HI} falling to V_{HO} falling	C_{LOAD} = 0	T_J = –40°C to 125°C		20	45	ns
			T_J = –40°C to 140°C		20	50	
T_{DLRR}	V_{LI} rising to V_{LO} rising	C_{LOAD} = 0	T_J = –40°C to 125°C		20	45	ns
			T_J = –40°C to 140°C		20	50	
T_{DHRR}	V_{HI} rising to V_{HO} rising	C_{LOAD} = 0	T_J = –40°C to 125°C		20	45	ns
			T_J = –40°C to 140°C		20	50	
DELAY MATCHING							
T_{MON}	LI ON, HI OFF				1	7	ns
T_{MOFF}	LI OFF, HI ON				1	7	ns
OUTPUT RISE AND FALL TIME							
t_R	LO, HO	C_{LOAD} = 1000 pF			8		ns
t_F	LO, HO	C_{LOAD} = 1000 pF			7		ns
t_R	LO, HO (3 V to 9 V)	C_{LOAD} = 0.1 µF			0.35	0.6	µs
t_F	LO, HO (3 V to 9 V)	C_{LOAD} = 0.1 µF			0.3	0.6	µs
MISCELLANEOUS							
	Minimum input pulse width that changes the output					50	ns
	Bootstrap diode turnoff time	I_F = 20 mA, I_{REV} = 0.5 A (1) (2)			20		ns

(1) Typical values for T_A = 25°C.
(2) I_F: Forward current applied to bootstrap diode. I_{REV}: Reverse current applied to bootstrap diode.

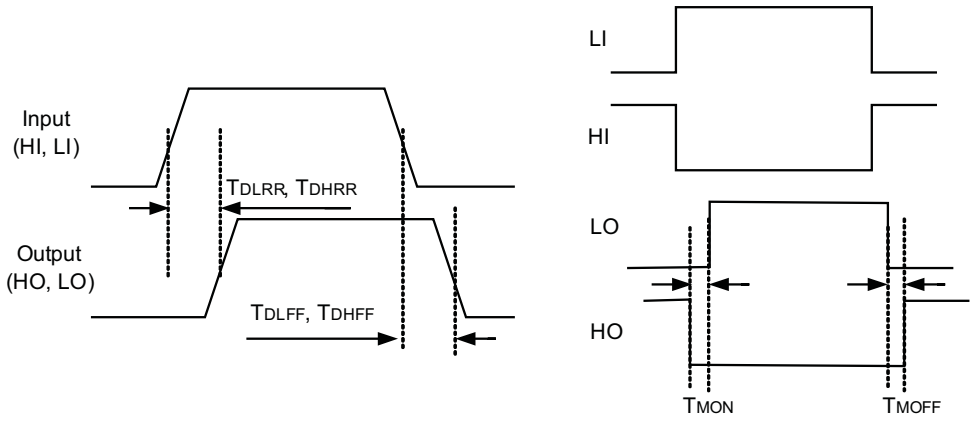


Figure 1. Timing Diagrams

6.6 Typical Characteristics

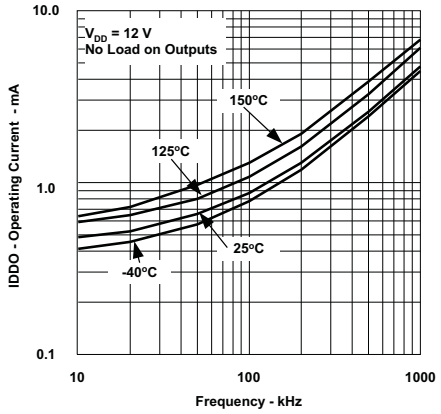


Figure 2. UCC27200-Q1 Operating Current vs Frequency

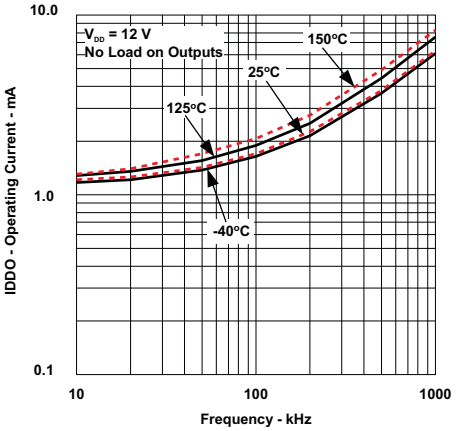


Figure 3. UCC27201-Q1 Operating Current vs Frequency

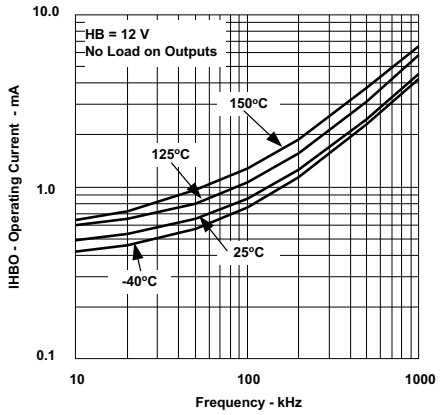


Figure 4. Boot Voltage Operating Current vs Frequency

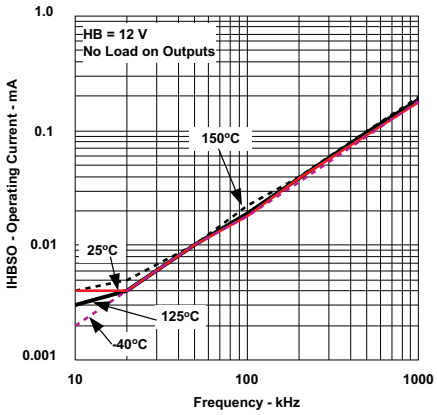


Figure 5. HB to VSS Operating Current vs Frequency

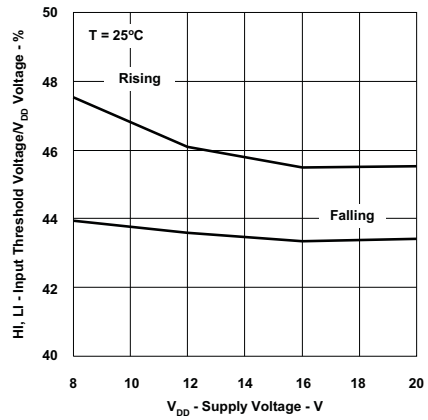


Figure 6. UCC27200-Q1 Input Threshold vs Supply Voltage

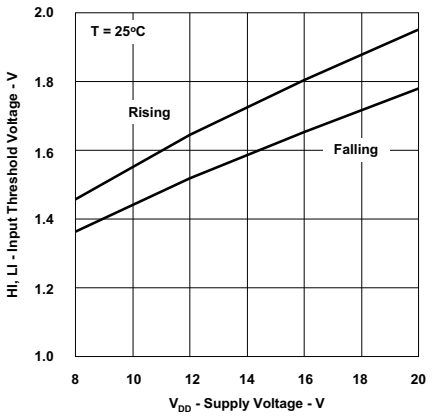


Figure 7. UCC27201-Q1 Input Threshold vs Supply Voltage

Typical Characteristics (continued)

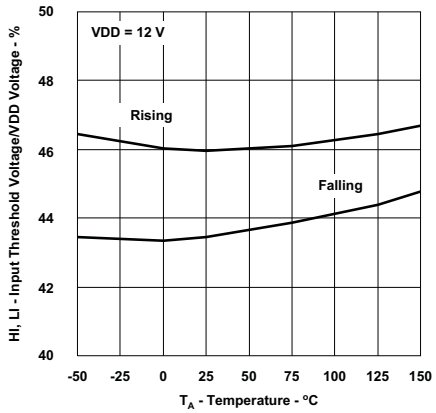


Figure 8. UCC27200-Q1 Input Threshold vs Temperature

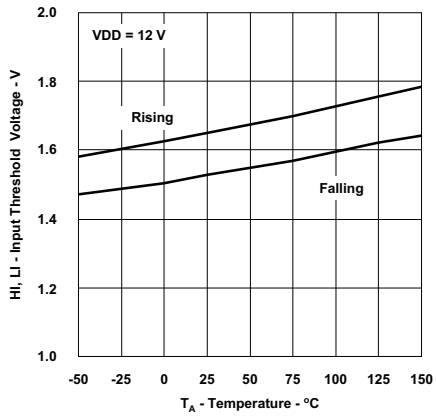


Figure 9. UCC27201-Q1 Input Threshold vs Temperature

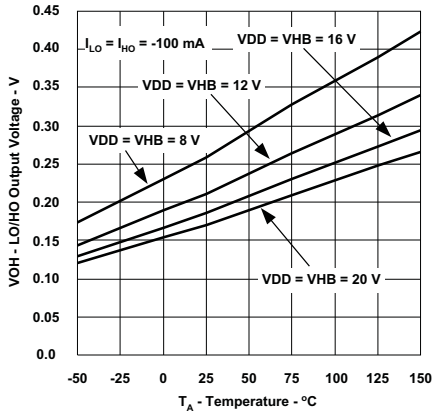


Figure 10. LO and HO High-Level Output Voltage vs Temperature

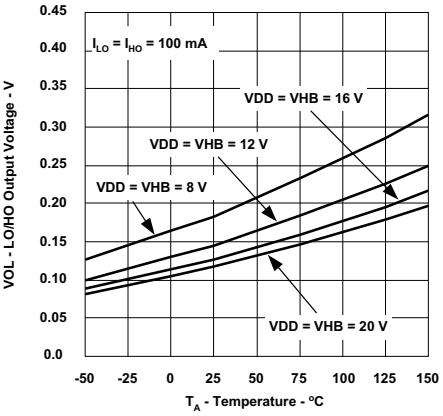


Figure 11. LO and HO Low-Level Output Voltage vs Temperature

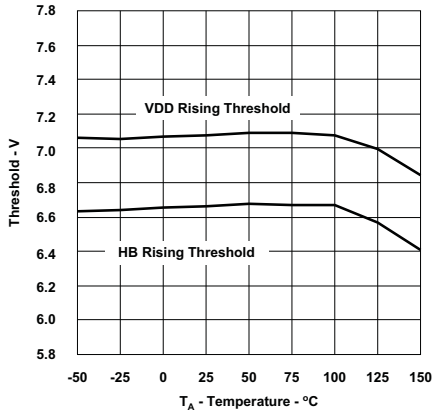


Figure 12. Undervoltage Lockout Threshold vs Temperature

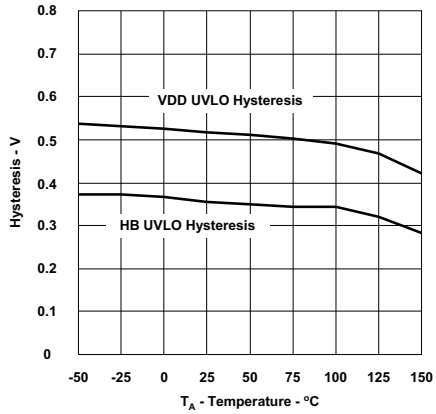


Figure 13. Undervoltage Lockout Threshold Hysteresis vs Temperature

Typical Characteristics (continued)

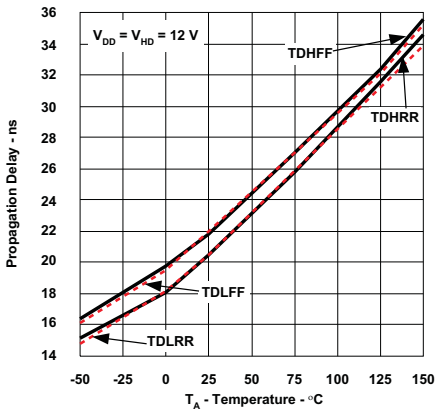


Figure 14. UCC27200-Q1 Propagation Delays vs Temperature

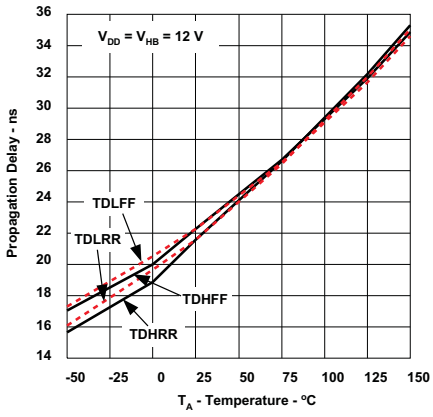


Figure 15. UCC27201-Q1 Propagation Delays vs Temperature

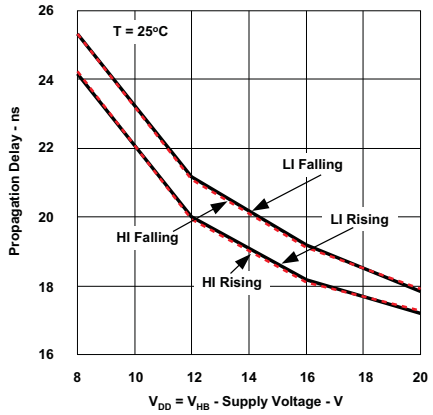


Figure 16. UCC27200-Q1 Propagation Delay vs Supply Voltage

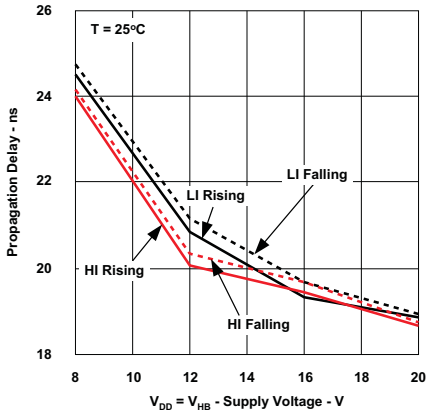


Figure 17. UCC27201-Q1 Propagation Delay vs Supply Voltage

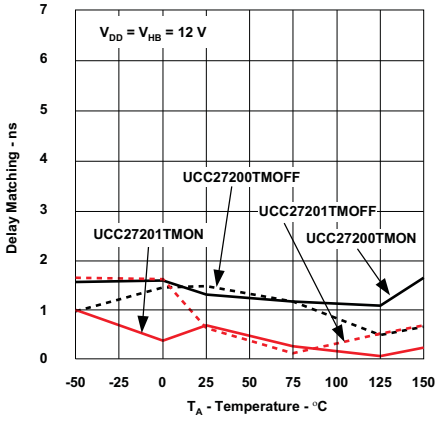


Figure 18. Delay Matching vs Temperature

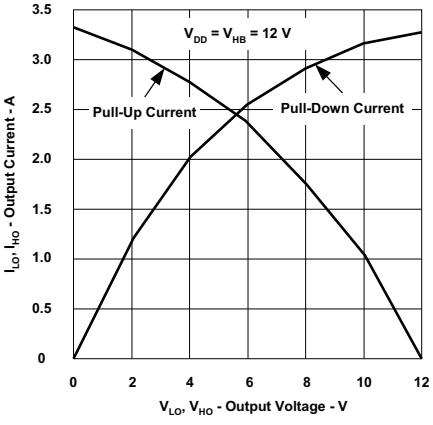


Figure 19. Output Current vs Output Voltage

Typical Characteristics (continued)

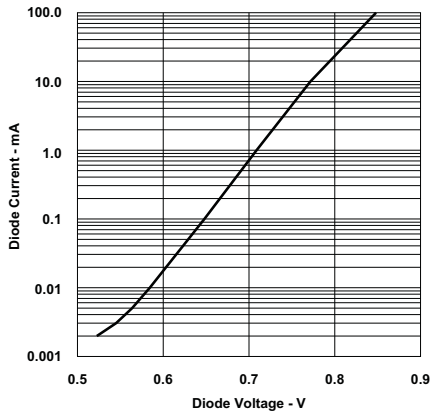


Figure 20. Diode Current vs Diode Voltage

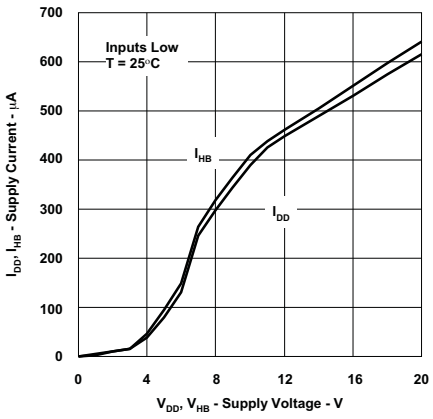


Figure 21. Quiescent Current vs Supply Voltage

7 Detailed Description

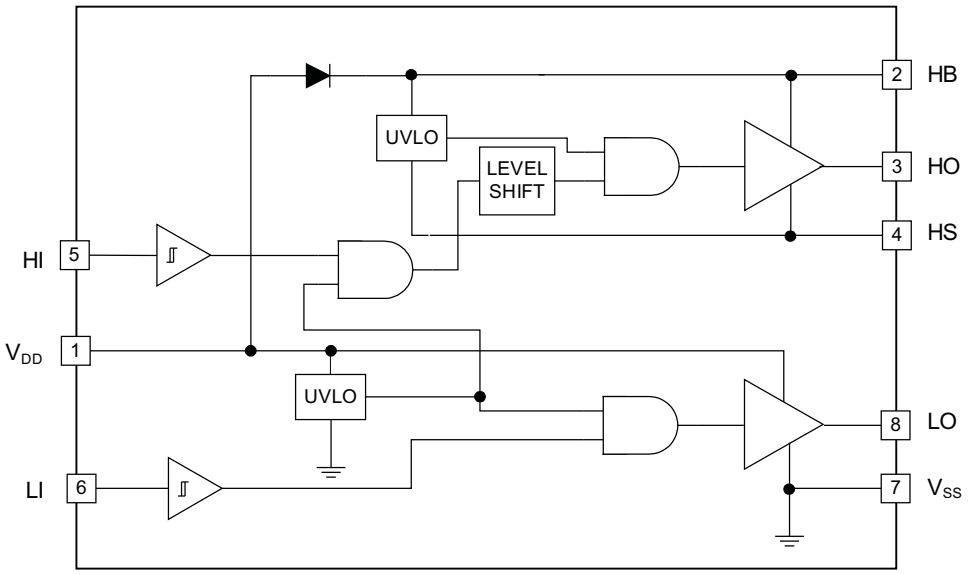
7.1 Overview

The UCC27200-Q1 and UCC27201-Q1 devices are high-side and low-side drivers. The high-side and low-side each have independent inputs, which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27200-Q1 and UCC27201-Q1. The UCC27200-Q1 is the CMOS-compatible input version and the UCC27201-Q1 is the TTL-version or logic-compatible version. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS}, which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

NOTE

The term UCC2720x-Q1 applies to both the UCC27200-Q1 and UCC27201-Q1.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27200-Q1 is 200 kΩ nominal and input capacitance is approximately 2 pF. The 200 kΩ is a pulldown resistance to V_{SS} (ground). The CMOS-compatible input of the UCC27200-Q1 provides a rising threshold of 48% of V_{DD} and falling threshold of 45% of V_{DD}. The inputs of the UCC27200-Q1 are intended to be driven from 0 to V_{DD} levels.

The input stages of the UCC27201-Q1 incorporate an open-drain configuration to provide the lower input thresholds. The input impedance is 200 kΩ nominal and input capacitance is approximately 4 pF. The 200 kΩ is a pulldown resistance to V_{SS} (ground). The logic level-compatible input provides a rising threshold of 1.7 V and a falling threshold of 1.6 V.

Feature Description (continued)

7.3.1.1 Undervoltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. V_{DD} as well as V_{HB} to V_{HS} differential voltages are monitored. The V_{DD} UVLO disables both drivers when V_{DD} is below the specified threshold. The rising V_{DD} threshold is 7.1 V with 0.5-V hysteresis. The V_{HB} UVLO disables only the high-side driver when the V_{HB} to V_{HS} differential voltage is below the specified threshold. The V_{HB} UVLO rising threshold is 6.7 V with 0.4-V hysteresis.

7.3.1.2 Level Shift

The level-shift circuit is the interface from the high-side input to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

7.3.1.3 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC2720x-Q1 family of drivers. The diode anode connects to V_{DD} and the cathode connects to VHB. With the VHB capacitor connected to HB and the HS pins, the V_{HB} capacitor charge refreshes every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and a voltage rating margin that allow for efficient and reliable operation.

7.3.1.4 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High-slew rate, low resistance, and high-peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage reference is from V_{DD} to V_{SS} and the high-side output stage reference is from V_{HB} to V_{HS}.

7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See *Undervoltage Lockout (UVLO)* for information on UVLO operation mode. In the normal mode, the output state is dependent on states of the HI and LI pins. Table 1 lists the output states for different input pin combinations.

Table 1. Device Logic Table

HI PIN	LI PIN	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.
(2) LO is measured with respect to V_{SS}.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

8.1.1 Switching the MOSFETs

Achieving optimum drive performance at high-frequency efficiently requires special attention to layout and minimizing parasitic inductances. Take care to reduce parasitic inductances at the driver die and package level and the PCB layout as much as possible. Figure 22 shows the main parasitic-inductance elements and current-flow paths during the turnon and turnoff of the MOSFET by charging and discharging its CGS capacitance.

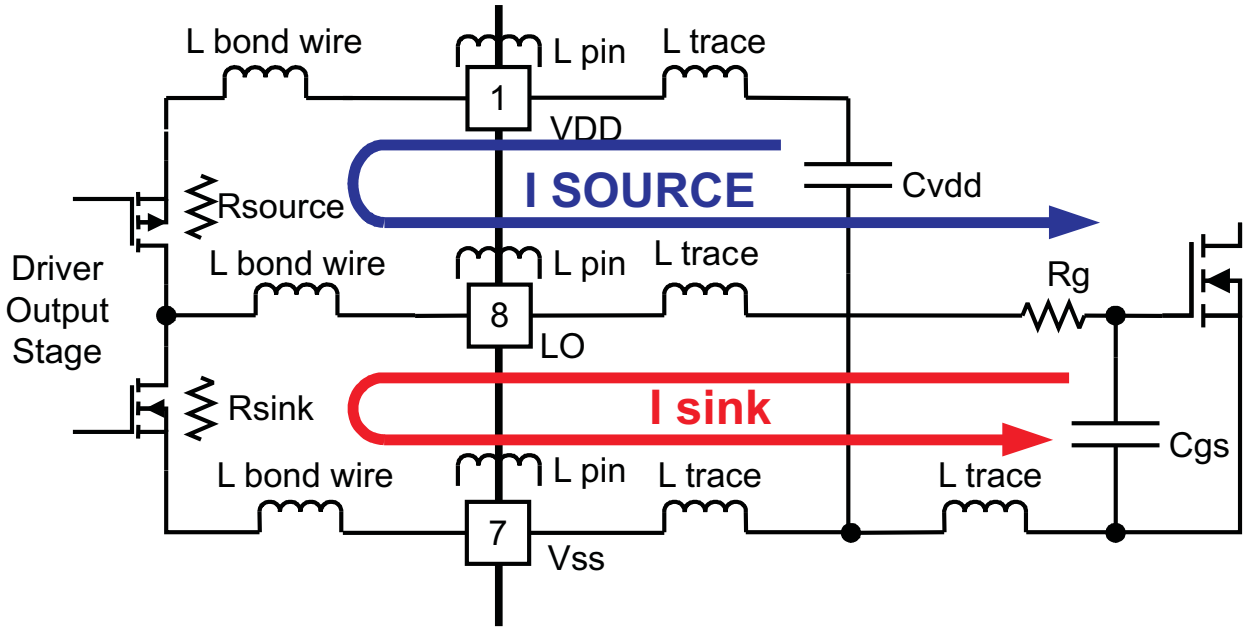


Figure 22. MOSFET Drive Paths and Circuit Parasitics

Application Information (continued)

The I_{SOURCE} current charges the C_{GS} gate capacitor and the I_{SINK} current discharges it. The rise and fall time of the voltage across the gate to source defines how quickly the MOSFET can switch. Based on actual measurements, the analytical curves in Figure 23 and Figure 24 indicate the output voltage and current of the drivers during the discharge of the load capacitor. Figure 23 shows voltage and current as a function of time. Figure 24 indicates the relationship of voltage and current during fast switching. These figures demonstrate the actual switching process and limitations due to parasitic inductances.

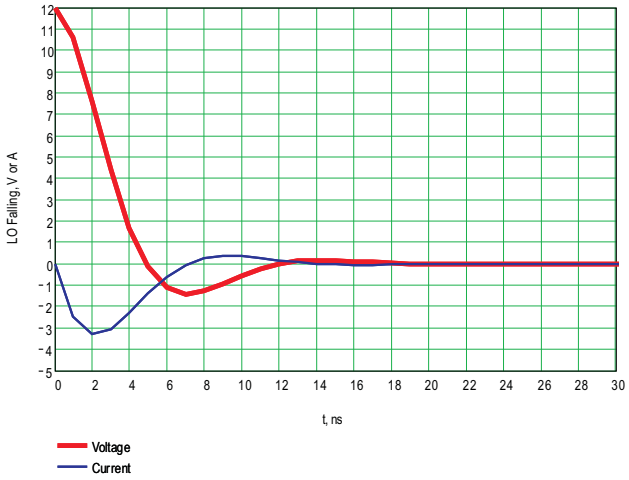


Figure 23. Turnoff Voltage and Current vs Time

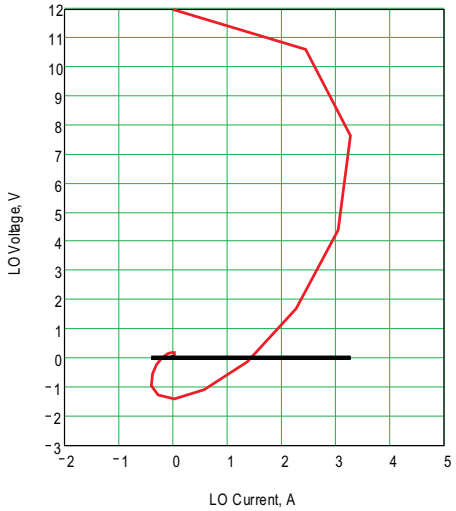


Figure 24. Turnoff Voltage and Current Switching

Turning off the MOSFET must be as fast as possible to minimize switching losses. For this reason, the UCC2720x-Q1 drivers are designed for high-peak currents and low-output resistance. The sink capability is specified as 0.18 V at 100-mA DC current, implying 1.8-Ω $R_{DS(on)}$. With 12-V drive voltage, no parasitic inductance, and a linear resistance, one would expect initial sink current amplitude of 6.7 A for both high-side and low-side drivers. Assuming a pure R-C discharge circuit of the gate capacitor, one would expect the voltage and current waveforms to be exponential. Due to the parasitic inductances and nonlinear resistance of the driver MOSFETs, the actual waveforms have some ringing, and the peak-sink current of the drivers is approximately 3.3 A, as shown in Figure 19. The overall parasitic inductance of the drive circuit estimate is 4 nH.

Actual measured waveforms are shown in Figure 25 and Figure 26. As shown, the typical rise time of 8 ns and fall time of 7 ns is rated conservatively.

Application Information (continued)

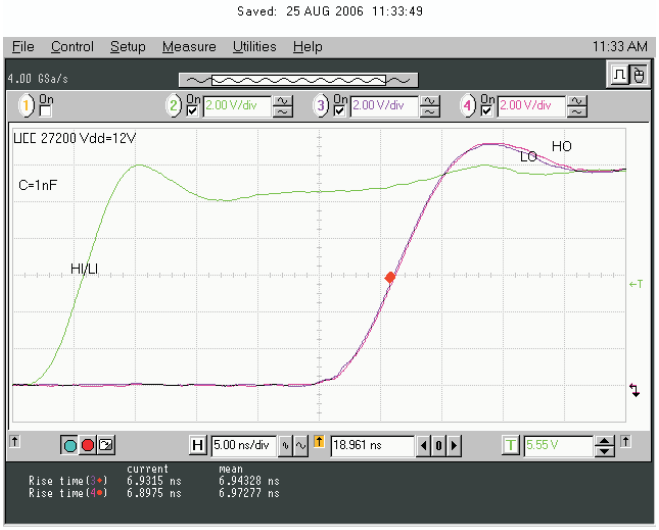


Figure 25. V_{LO} and V_{HO} Rise Time, 1-nF Load, 5 ns/Div

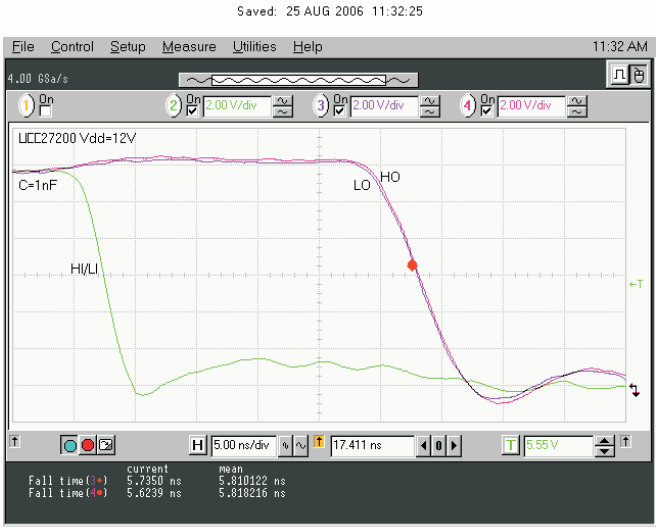


Figure 26. V_{LO} and V_{HO} Fall Time, 1-nF Load, 5-ns/Div

8.1.2 Dynamic Switching of the MOSFETs

The true behavior of MOSFETS presents a dynamic capacitive load primarily at the gate-to-source threshold voltage. Using the turnoff case as the example, when the device reaches the gate-to-source threshold voltage, the drain voltage starts to rise, and the drain-to-gate parasitic capacitance couples charge into the gate, which results in the turnoff plateau. The relatively low-threshold voltages of many MOSFETS and the increased charge that must be removed (Miller charge) makes good driver performance necessary for efficient switching. An open-loop, half-bridge power converter was used to evaluate performance in actual applications. The schematic of the half-bridge converter is shown in Figure 29. The turnoff waveforms of the UCC27200-Q1 driving two MOSFETs in parallel are shown in Figure 27 and Figure 28.

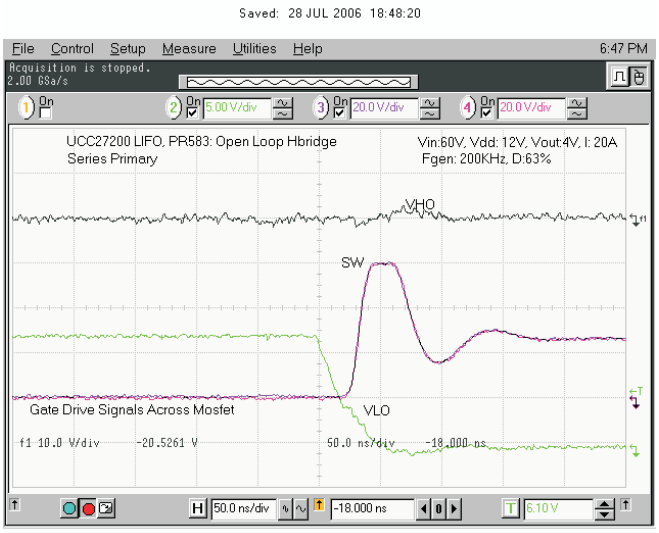


Figure 27. V_{LO} Fall Time in Half-Bridge Converter

Figure 28. V_{HO} Fall Time in Half-Bridge Converter

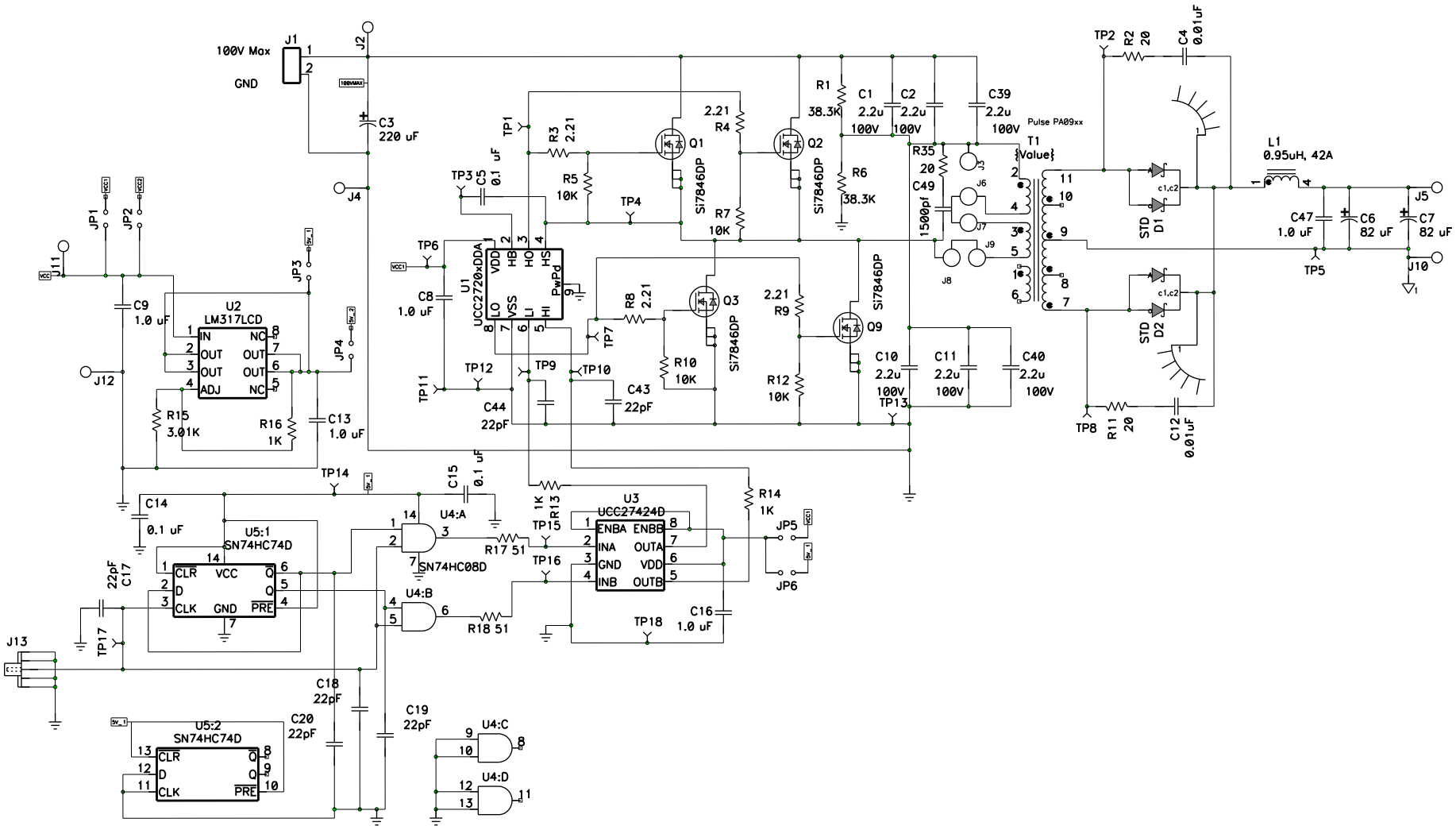


Figure 29. Open-Loop, Half-Bridge Converter

8.1.3 Delay Matching and Narrow Pulse Widths

The total delays encountered in the PWM, driver, and power stage must be considered for a number of reasons, primarily for the delay in current-limit response. Also, consider differences in delays between the drivers, which can lead to various concerns depending on the topology. The sync-buck topology switching requires careful selection of dead time between the high-side and low-side switches to avoid cross conduction and excessive body-diode conduction. Bridge topologies can be affected by a resulting volt-sec imbalance on the transformer, if there is imbalance in the high-side and low-side pulse widths in a steady-state condition.

Narrow pulse width performance is an important consideration when transient and short-circuit conditions are encountered. Although there may be relatively long steady-state PWM output-driver-MOSFET signals, very narrow pulses may be encountered in soft start, large load transients, and short-circuit conditions.

The UCC2720x-Q1 driver family offers excellent performance in high-side and low-side driver delay matching and narrow pulse-width performance. The delay matching waveforms are shown in Figure 30 and Figure 31. The UCC2720x-Q1 driver narrow pulse-width performance is shown in Figure 32 and Figure 33.

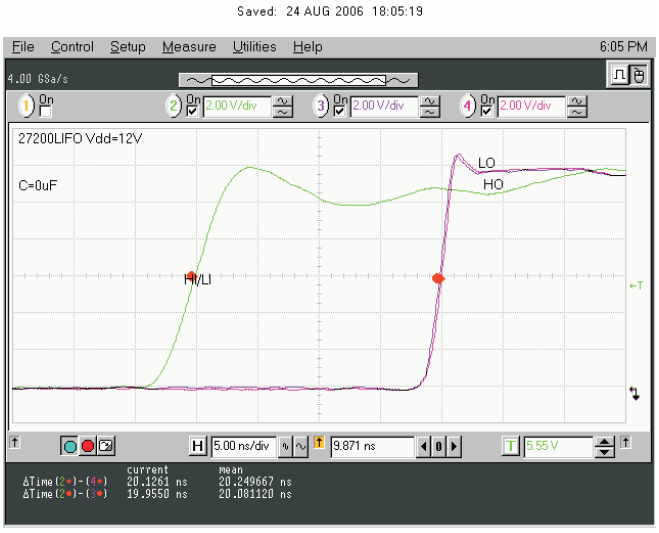


Figure 30. V_{LO} and V_{HO} Rising Edge Delay Matching

Figure 31. V_{LO} and V_{HO} Falling Edge Delay Matching

Figure 32. 20-ns Input Pulse Delay Matching

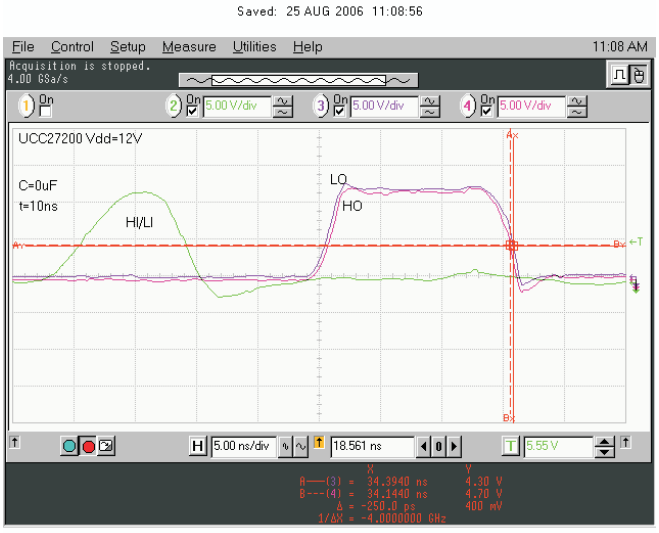


Figure 33. 10-ns Input Pulse Delay Matching

8.1.4 Boot-Diode Performance

The UCC2720x-Q1 family of drivers internally incorporates the bootstrap diode necessary to generate the high-side bias. The characteristics of this diode are important to achieve efficient reliable operation. The DC characteristics to consider are V_F and dynamic resistance. A low V_F and high dynamic resistance results in a high forward voltage during charging of the bootstrap capacitor. The UCC2720x-Q1 has a boot diode rated at 0.65-V V_F and dynamic resistance of 0.6 Ω for reliable charge transfer to the bootstrap capacitor. The dynamic characteristics to consider are diode recovery time and stored charge. Diode recovery times that are specified with no conditions can be misleading. Diode recovery times at no forward current (I_F) can be noticeably less than with forward current applied. The UCC2720x-Q1 boot diode recovery is specified at 20 ns at I_F = 20 mA, I_{REV} = 0.5 A. At 0-mA I_F, the reverse recovery time is 15 ns.

Another less obvious consideration is how applied voltage affects the stored charge of the diode. On every switching transition when the HS node transitions from low-to-high, charge is removed from the boot capacitor to charge the capacitance of the reverse-biased diode. This is a portion of the driver power losses and it reduces the voltage on the HB capacitor. At higher applied voltages, the stored charge of the UCC2720x-Q1 PN diode is often less than a comparable Schottky diode.

8.2 Typical Application

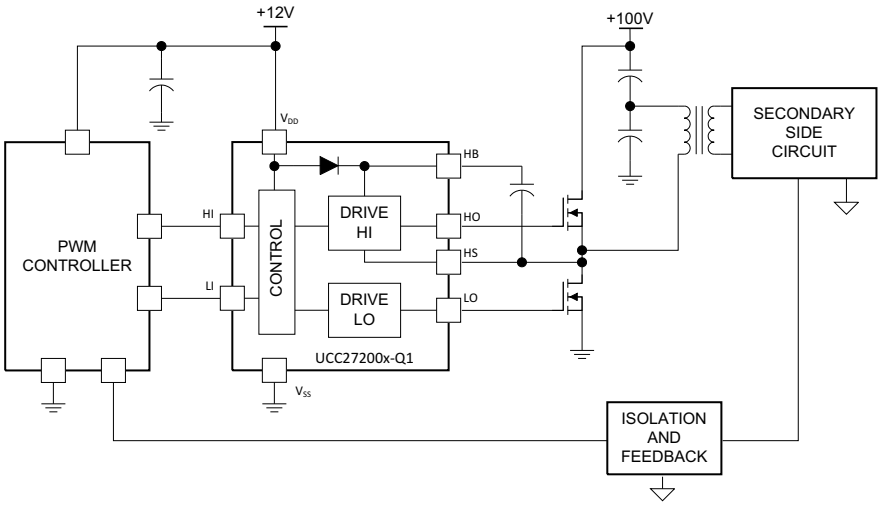


Figure 34. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, V_{DD}	12 V
Voltage on HS, VHS	0 V to 100 V
Voltage on HB, VHB	12 V to 112 V
Output current rating, IO	–3 A to 3 A
Operating frequency	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Input Threshold Type

The UCC27200-Q1 and UCC27201-Q1 devices have an input maximum voltage range from –0.3 V to 20 V. The UCC27200-Q1 and UCC27201-Q1 devices feature TTL-compatible input threshold logic with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See *Electrical Characteristics* for the actual input threshold voltage levels and hysteresis specifications for the device.

8.2.2.2 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device must never exceed the values listed in *Absolute Maximum Ratings*. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the V_{DD} bias supply equals the voltage differential. With a wide operating range from 8 V to 17 V, the UCC2720x-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs, IGBTs, and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

8.2.2.3 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff must be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a dV_{DS}/dt of 20 V/ns or higher with a DC bus voltage of 400 V in a continuous-conduction mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in ON state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in the SPP20N60C3 data sheet is 33 nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$.

To achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the Q_{GD} charge in 20 ns or less. In other words, a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC2720x-Q1 device gate driver is capable of providing 3-A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 2.4× overdrive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × I_{PEAK} × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET data sheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

8.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC2720x-Q1 device features 20-ns (typical) propagation delays, which ensures very little pulse distortion and allows operation at very high frequencies. See *Electrical Characteristics* for the propagation and switching characteristics of the UCC2720x-Q1 device.

8.2.3 Application Curves

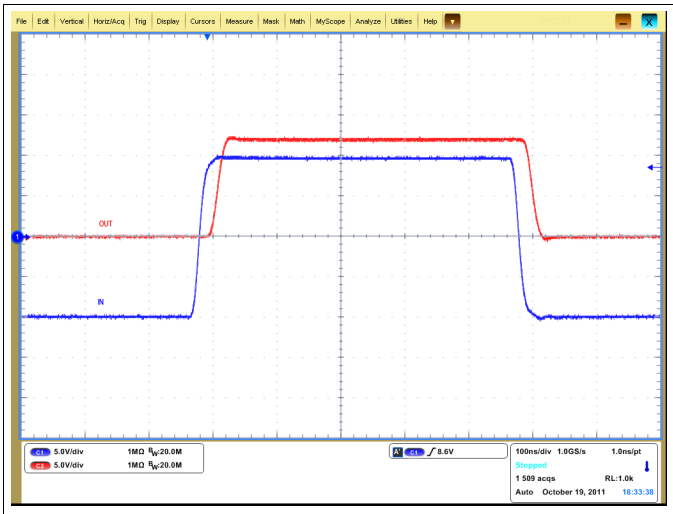


Figure 35. Negative 10-V Input

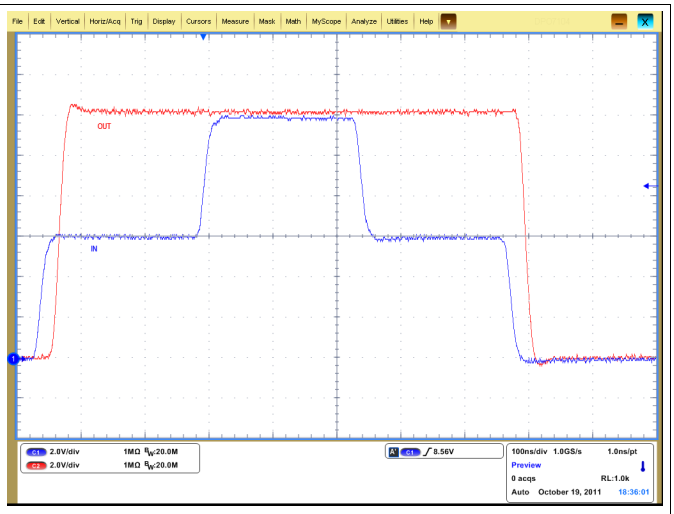


Figure 36. Step Input

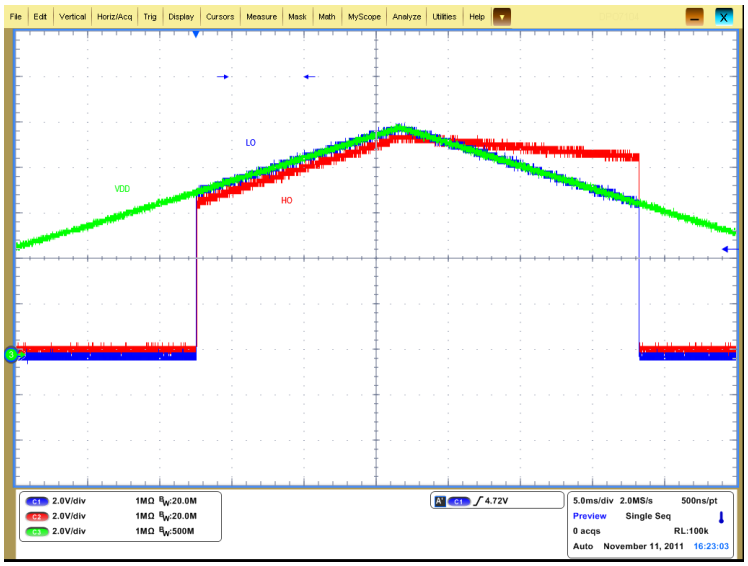


Figure 37. Symmetrical UVLO

9 Power Supply Recommendations

The bias supply voltage range for which the UCC2720x-Q1 device is recommended to operate from 8 V to 17 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 17 V. The UVLO protection feature also involves a hysteresis function, which means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. Therefore, ensuring that, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up the device does not begin operation until the V_{DD} pin voltage has exceeded the $V_{(ON)}$ threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, it is important to recognize that the charge for source current pulses delivered by the HO pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the HO pin, a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus, ensure that a local bypass capacitor is provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A lo-ESR, ceramic surface-mount capacitor is required. TI recommends using a capacitor in the range from 0.22 μF to 4.7 μF between V_{DD} and GND. In a similar manner, the current pulses delivered by the LO pin are sourced from the HB pin. Therefore, TI recommends placing a 0.022-μF to 0.1-μF local decoupling capacitor between the HB and HS pins.

10 Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and V_{HB} (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA package as GND by connecting it to the V_{SS} pin (GND).

NOTE

The GND trace from the driver goes directly to the source of the MOSFET, but must not be in the high-current path of the MOSFET(S) drain or source current.

- Use similar rules for the HS node as for GND for the high-side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. Where possible, widths of 60 mil to 100 mil are preferred.
- Use two or more vias if the driver outputs or SW node must be routed from one layer to another. For GND, consider the number of vias of the thermal pad requirements of the thermal pad requirements as well as parasitic inductance.
- Avoid L_I and H_I (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high-impedance leads.
- Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

10.2 Layout Example

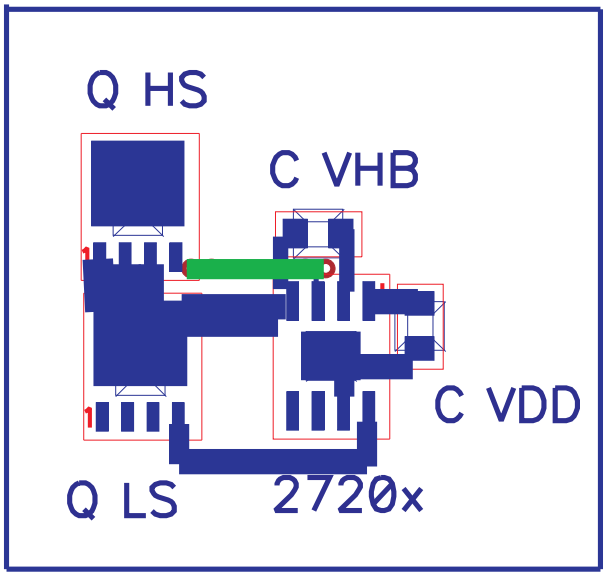


Figure 38. Example Component Placement

10.3 Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Use Equation 2 to calculate the DC portion of the power dissipation (PDC).

$$PDC = I_Q \times V_{DD} \quad (2)$$

where

- I_Q is the quiescent current for the driver.

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC2720x-Q1 device features very low quiescent currents (see *Electrical Characteristics*) and contain internal logic to eliminate any shoot through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage VG, which is very close to input bias supply voltage V_{DD})
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 3.

$$EG = ½C_{LOAD} \times V_{DD}^2 \quad (3)$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by Equation 4.

$$PG = C_{LOAD} \times V_{DD}^2 \times f_{SW} \quad (4)$$

where

- f_{SW} is the switching frequency

Power Dissipation (continued)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when switching a capacitor which is calculated using the equation $Q_G = C_{LOAD} \times V_{DD}$ to provide Equation 5 for power.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (5)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For more related documentation, see the following:

- *QFN/SON PCB Attachment* (SLUA271)
- *PowerPAD™ Thermally Enhanced Package* (SLMA002)
- *PowerPAD™ Made Easy* (SLMA004)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27200-Q1	Click here	Click here	Click here	Click here	Click here
UCC27201-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27200QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	27200Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27200-Q1 :

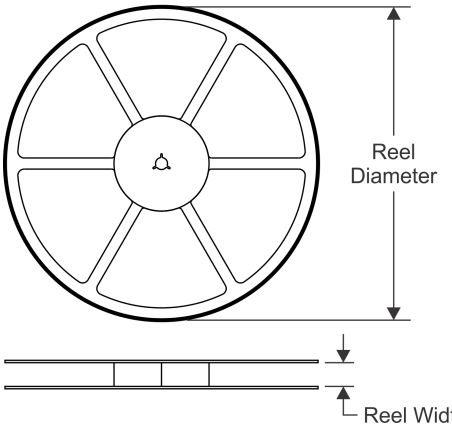
- Catalog: UCC27200

NOTE: Qualified Version Definitions:

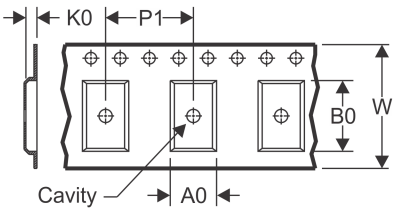
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

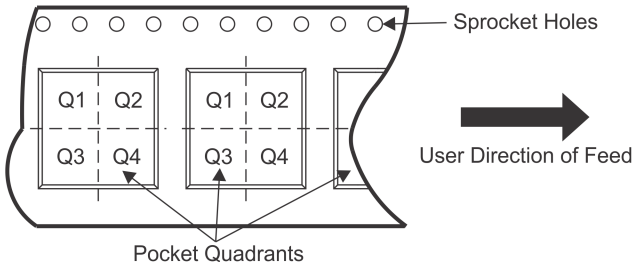


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

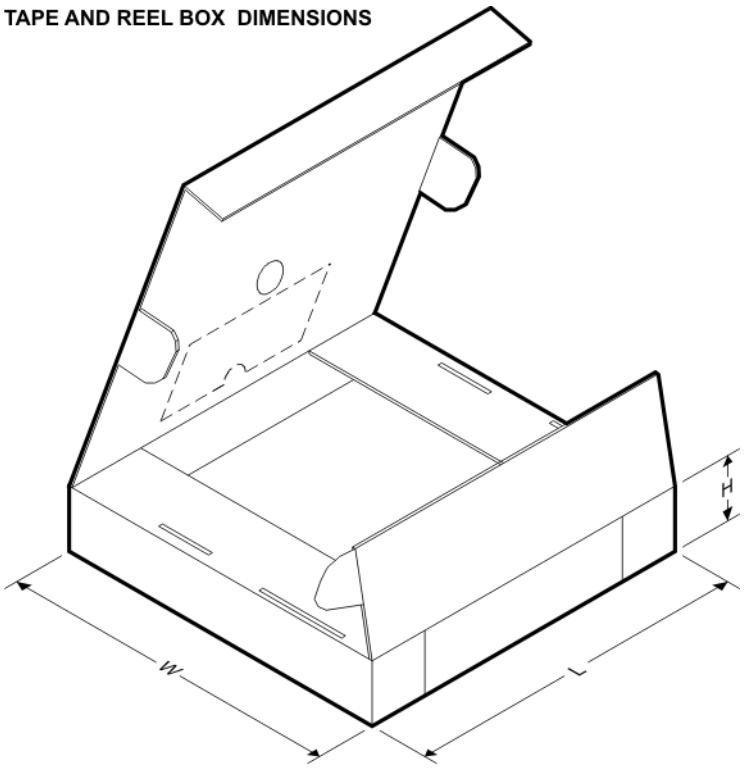
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27200QDDARQ1	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

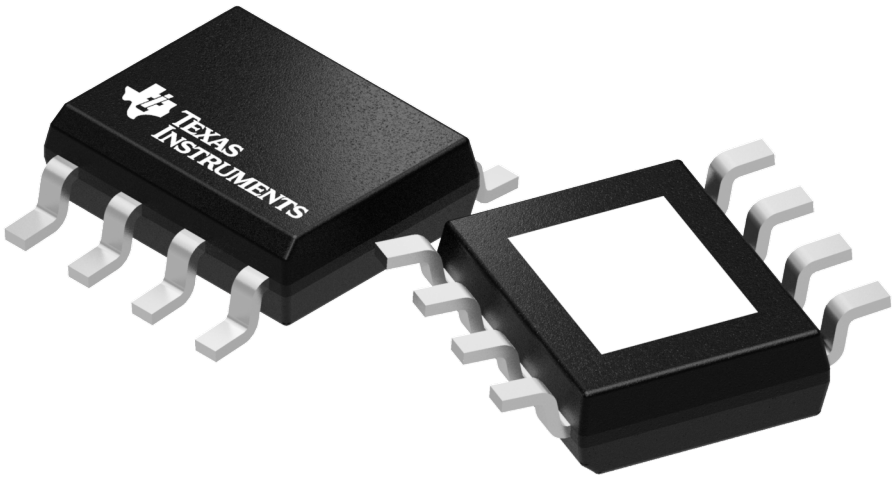


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27200QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

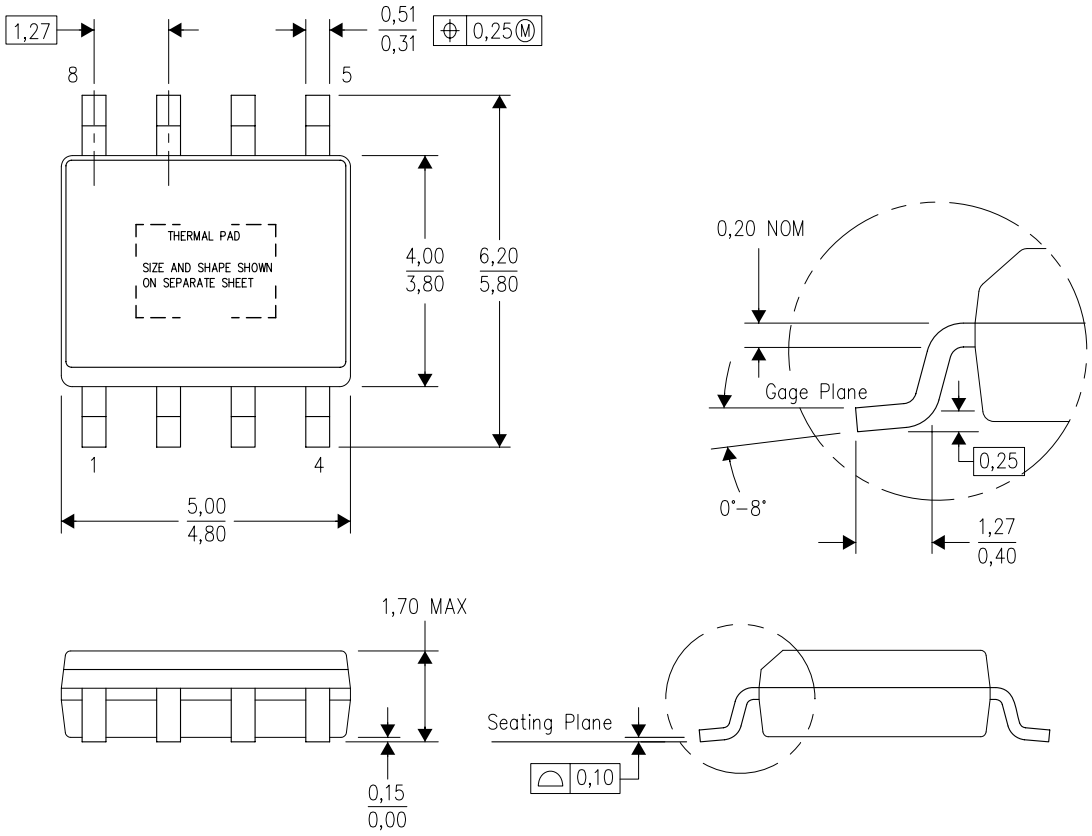
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

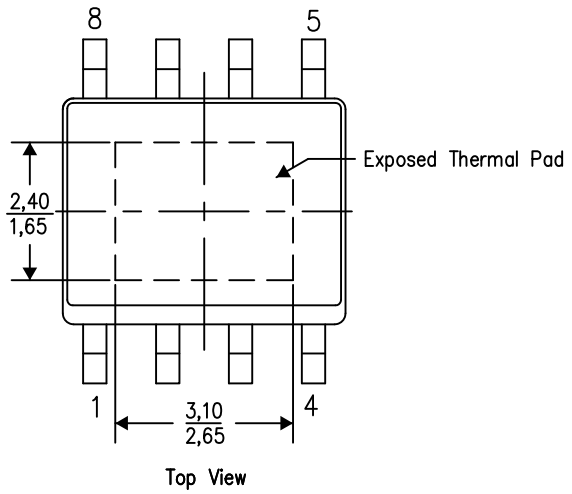
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



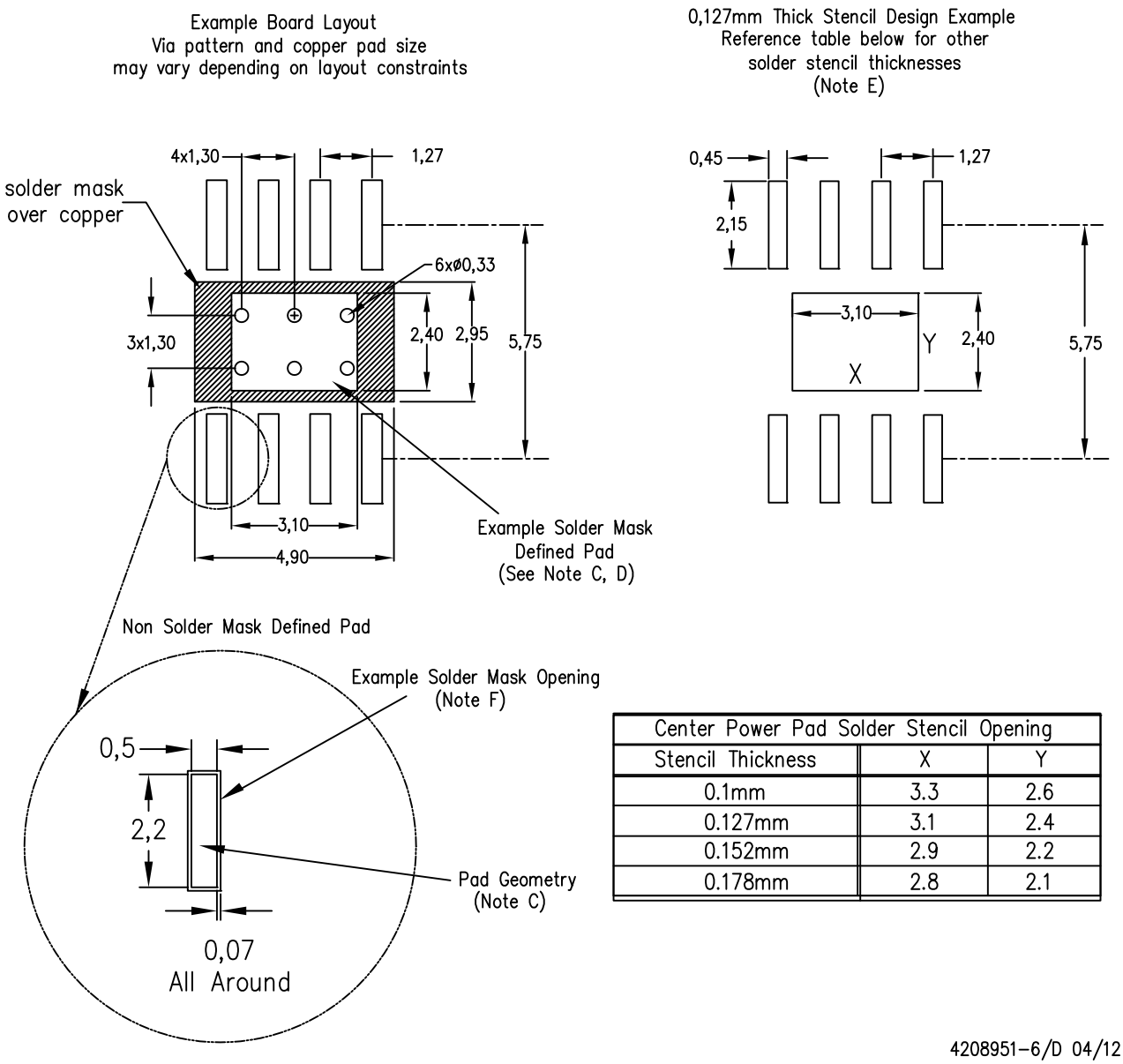
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265