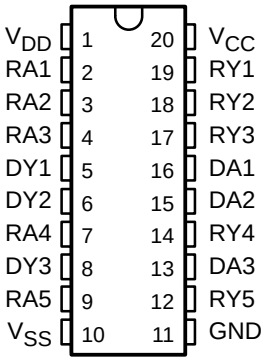
- **Single-Chip TIA/EIA-232-F Interface for IBM™ PC/AT™ Serial Port**
- **Designed to Transmit and Receive 4-μs Pulses (Equivalent to 256 kbit/s)**
- **Less Than 21-mW Power Consumption**
- **Wide Supply-Voltage Range . . . 4.75 V to 15 V**
- **Driver Output Slew Rates Are Internally Controlled to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1000 mV Typical**
- **TIA/EIA-232-F Bus-Pin ESD Protection Exceeds:**
  – 15-kV, Human-Body Model
- **Three Drivers and Five Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU V.28**
- **Complements the SN75LP196**
- **Designed to Replace the Industry-Standard SN75185 and SN75C185 With the Same Flow-Through Pinout**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Dual-In-Line (N) Packages**

DB, DW, OR N PACKAGE
(TOP VIEW)



description

The SN75LP1185 is a low-power bipolar device containing three drivers and five receivers, with 15 kV of ESD protection on the bus pins with respect to each other. Bus pins are defined as those pins that tie directly to the serial-port connector, including GND. The pinout matches the flow-through design of the industry-standard SN75185 and SN75C185. The flow-through pinout of the SN75LP1185 allows easy interconnection of the UART and serial-port connector of the IBM PC/AT and compatibles. The SN75LP1185 provides a rugged, low-cost solution for this function with the combination of the bipolar processing and 15 kV of ESD protection.

The SN75LP1185 has internal slew-rate control to provide a maximum rate of change in the output signal of 30 V/μs. The driver output swing is nominally clamped at ±6 V to enable the higher data rates associated with this device and to reduce EMI emissions. Even though the driver outputs are clamped, they can handle voltages up to ±15 V without damage. All the logic inputs can accept 3.3-V or 5-V input signals.

The SN75LP1185 complies with the requirements of TIA/EIA-232-F and ITU V.28. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75LP1185 support rates up to 256 kbit/s.

The SN75LP1185 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		
	PLASTIC SHRINK SMALL-OUTLINE (DB)	PLASTIC SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	SN75LP1185DBR	SN75LP1185DW	SN75LP1185N

The DB package is only available taped and reeled. The DW package also is available taped and reeled. Add the suffix R to device type (e.g., SN75LP1185DWR).

Function Tables

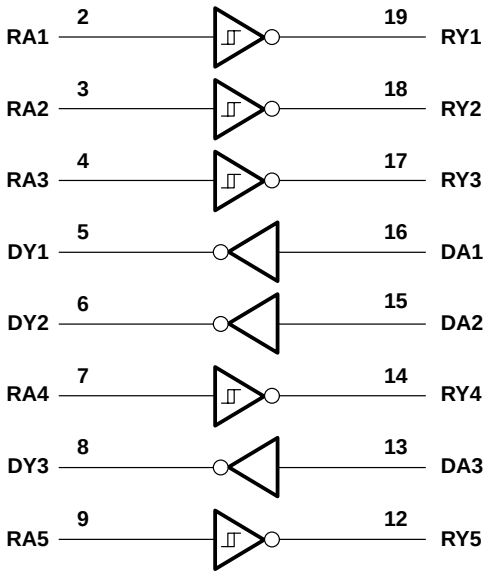
DRIVER

INPUT DA	OUTPUT DY
H	L
L	H
Open	L

RECEIVER

INPUT RA	OUTPUT RY
H	L
L	H
Open	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply-voltage range (see Note 1): V_{CC} . . . . . –0.5 V to 7 V
V_{DD} . . . . . –0.5 V to 15 V
Negative supply-voltage range, V_{SS} (see Note 1) . . . . . 0.5 V to –15 V
Input-voltage range, V_I: Receiver (RA) . . . . . –30 V to 30 V
Driver (DA) . . . . . –0.5 V to V_{CC} + 0.4 V
Output-voltage range, V_O: Receiver (RY) . . . . . –0.5 V to 6 V
Driver (DY) . . . . . –15 V to 15 V
Electrostatic discharge: Bus pins (human-body model) (see Note 2) . . . . . Class 3: 15 kV
Bus pins (machine model) . . . . . 500 V
All pins (human-body model) (see Note 2) . . . . . Class 3: 5 kV
All pins (machine model) . . . . . 400 V
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal, unless otherwise noted.
2. Per MIL-STD-883, Method 3015.7
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 4)		4.75	5	5.25	V
V_{DD}	Supply voltage (see Note 5)		9	12	15	V
V_{SS}	Supply voltage (see Note 5)		–9	–12	–15	V
V_{IH}	High-level input voltage	DA	2			V
V_{IL}	Low-level input voltage	DA			0.8	V
V_I	Receiver input voltage	RA	–25		25	V
I_{OH}	High-level output current	RY			–1	mA
I_{OL}	Low-level output current	RY			2	mA
T_A	Operating free-air temperature		0		70	°C

NOTES: 4. V_{CC} cannot be greater than V_{DD}.
5. The device operates down to $V_{DD} = V_{CC}$ and $|V_{SS}| = V_{CC}$, but supply currents increase and other parameters may vary slightly from the data sheet limits.

supply currents over the recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply current for V_{CC}, I_{CC}	No load, All inputs at minimum V_{OH} or maximum V_{OL}	V_{DD} = 9 V,	V_{SS} = –9 V			1000	µA
		V_{DD} = 12 V,	V_{SS} = –12 V			1000	
Supply current for V_{DD}, I_{DD}		V_{DD} = 9 V,	V_{SS} = –9 V			800	
		V_{DD} = 12 V,	V_{SS} = –12 V			800	
Supply current for V_{SS}, I_{SS}		V_{DD} = 9 V,	V_{SS} = –9 V			–625	
		V_{DD} = 12 V,	V_{SS} = –12 V			–625	

driver electrical characterisitics over the recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 9 V,	V_{SS} = –9 V		5	5.8	6.6	V
			V_{DD} = 12 V,	V_{SS} = –12 V,	See Note 6	5	5.8	6.6	
V_{OL}	Low-level output voltage	V_{IH} = 2 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 9 V,	V_{SS} = –9 V		–5	–5.8	–6.9	V
			V_{DD} = 12 V,	V_{SS} = –12 V,	See Note 6	–5	–5.9	–6.9	
I_{IH}	High-level input current	V_I at V_{CC}						1	µA
I_{IL}	Low-level input current	V_I at GND						–1	µA
$I_{OS(H)}$	Short-circuit high-level output current	V_O = GND or V_{SS},		See Figure 2 and Note 7			–30	–55	mA
$I_{OS(L)}$	Short-circuit low-level output current	V_O = GND or V_{DD},		See Figure 2 and Note 7			30	55	mA
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0,		V_O = 2 V		300			Ω

NOTES: 6. Maximum output swing is clamped nominally at ±6 V to enable the higher data rates associated with this device and to reduce EMI emissions. The driver outputs may slightly exceed the maximum output voltage over the full V_{CC} and temperature ranges.
7. Not more than one output should be shorted at one time.

driver switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 1		300	800	1600	ns
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 1		300	800	1600	ns
t_{TLH}	Transition time, low- to high-level output	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, R_L = 3 kΩ to 7 kΩ, See Figure 1 and Note 9	Using V_{TR} = 10%-to-90% transition region, Driver speed = 250 kbit/s, C_L = 15 pF, See Note 8	375		2240	ns
			Using V_{TR} = ±3 V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	200		1500	
			Using V_{TR} = ±2 V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	133		1000	
			Using V_{TR} = ±3 V transition region, Driver speed = 125 kbit/s, C_L = 2500 pF			2750	
t_{THL}	Transition time, high- to low-level output	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, R_L = 3 kΩ to 7 kΩ, See Figure 1 and Note 9	Using V_{TR} = 10%-to-90% transition region, Driver speed = 250 kbit/s, C_L = 15 pF, See Note 8	375		2240	ns
			Using V_{TR} = ±3 V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	200		1500	
			Using V_{TR} = ± 2 V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	133		1000	
			Using V_{TR} = ±3 V transition region, Driver speed = 125 kbit/s, C_L = 2500 pF			2750	
SR	Output slew rate	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V	Using V_{TR} = ±3 V transition region, Driver speed = 0 to 250 kbit/s, C_L = 15 pF	4	20	30	V/µs

NOTES: 8. Equivalent to the SN75C185. The SN75LP1185 output-voltage swing is clamped to about 70% of the typical SN75C185 output-voltage swing, and the specified limits reflect the reduced output swing.
9. Maximum output swing is limited to ±6 V to enable the higher data rates associated with this device and to reduce EMI emissions.

receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

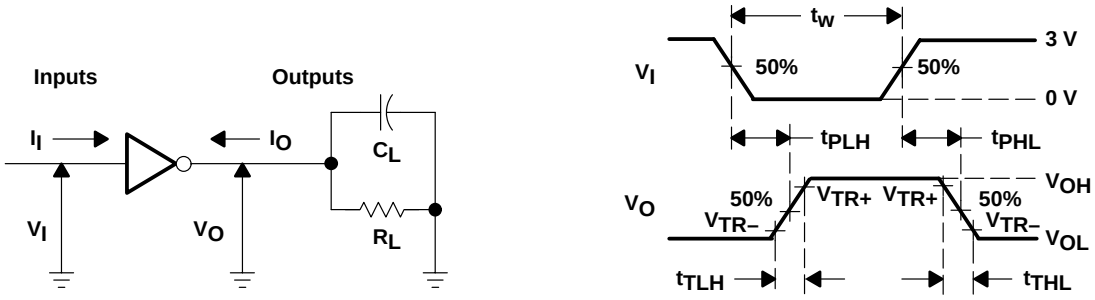
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 3		1.6	2	2.55	V
$V_{IT–}$	Negative-going input threshold voltage	See Figure 3		0.6	1	1.45	V
V_{HYS}	Input hysteresis, V_{IT+} $V_{IT–}$	See Figure 3		600	1000		mV
V_{OH}	High-level output voltage	I_{OH} = –1 mA		2.5	3.9		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.33	0.5	V
I_{IH}	High-level input current	V_I = 3 V		0.43	0.6	1	mA
		V_I = 25 V		3.6	5.1	8.3	
I_{IL}	Low-level input current	V_I = –3 V		–0.43	–0.6	–1	mA
		V_I = –25 V		–3.6	–5.1	–8.3	
$I_{OS(H)}$	Short-circuit high-level output current	V_O = 0,	See Figure 5 and Note 7			–20	mA
$I_{OS(L)}$	Short-circuit low-level output current	V_O = V_{CC},	See Figure 5 and Note 7			20	mA
R_{IN}	Input resistance	V_I = ±3 V to ±25 V		3	5	7	kΩ

NOTE 7: Not more than one output should be shorted at one time.

receiver switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output		400	900	ns
t_{PLH}	Propagation delay time, low- to high-level output		400	900	ns
t_{TLH}	Transition time, low- to high-level output		200	500	ns
t_{THL}	Transition time, high- to low-level output		200	400	ns
$t_{SK(p)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$		200	425	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:
For C_L < 1000 pF: t_W = 4 µs, PRR = 250 kbit/s, Z_O = 50 Ω, t_r and t_f < 50 ns.
For C_L = 2500 pF: t_W = 8 µs, PRR = 125 kbit/s, Z_O = 50 Ω, t_r and t_f < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 1. Driver Parameter Test Circuit and Waveform

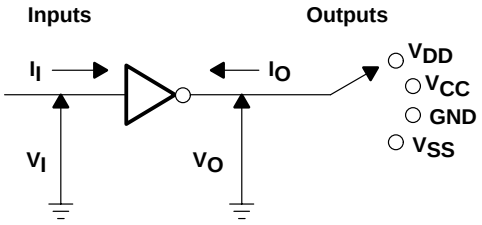


Figure 2. Driver I_{OS} Test

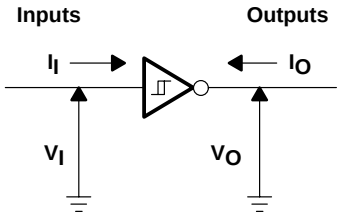
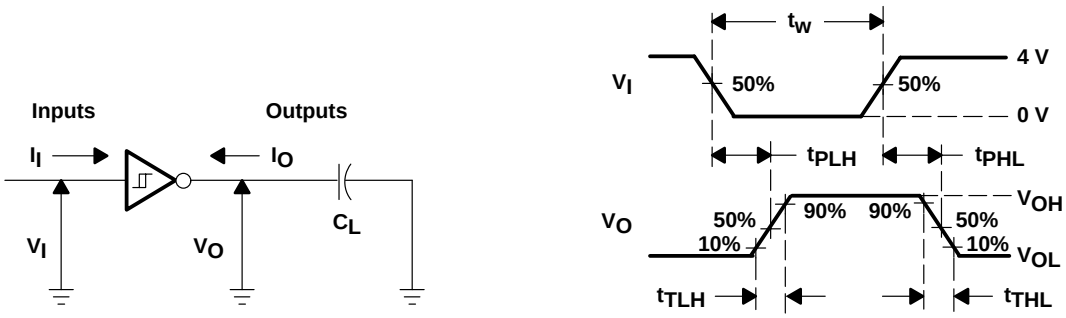


Figure 3. Receiver V_{IT} Test

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_W = 4 µs, PRR = 250 kbit/s, Z_O = 50 Ω, t_r and t_f < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 4. Receiver Parameter Test Circuit and Waveform

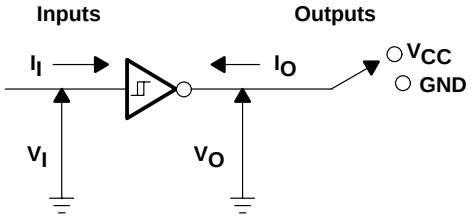


Figure 5. Receiver I_{OS} Test

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75LP1185 in the fault condition when the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to ground (see Figure 6).

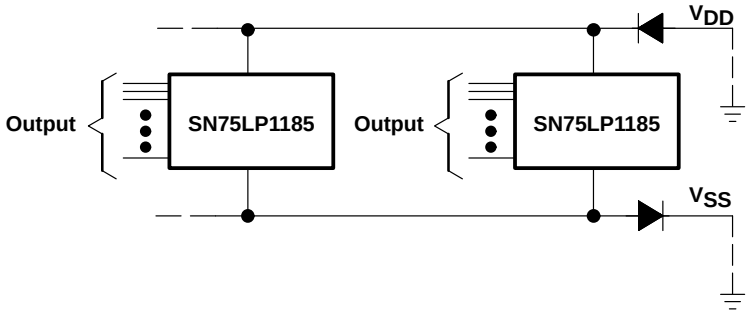


Figure 6. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LP1185DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	5LP1185	Samples
SN75LP1185DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LP1185	Samples
SN75LP1185DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LP1185	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

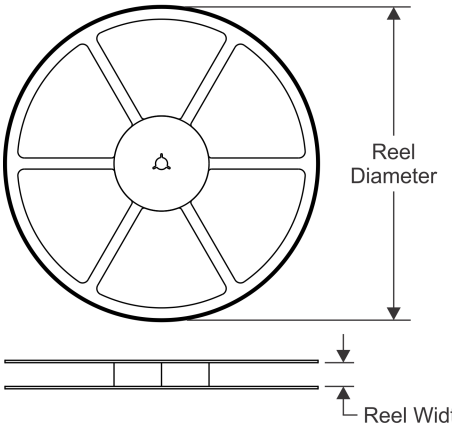
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

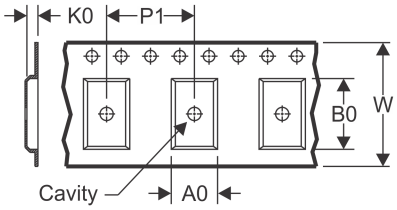
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

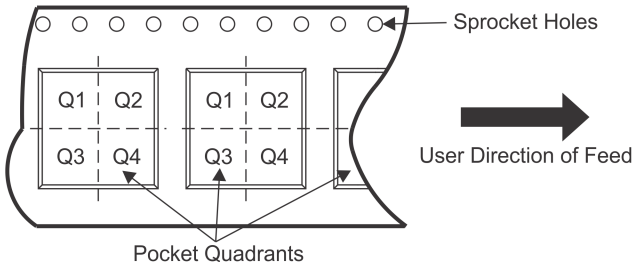


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

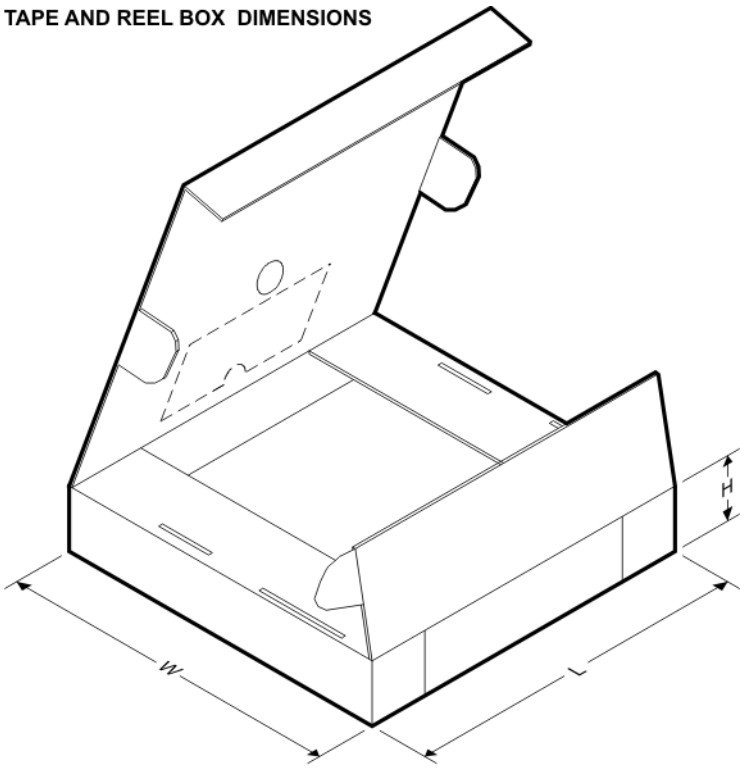
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LP1185DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75LP1185DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

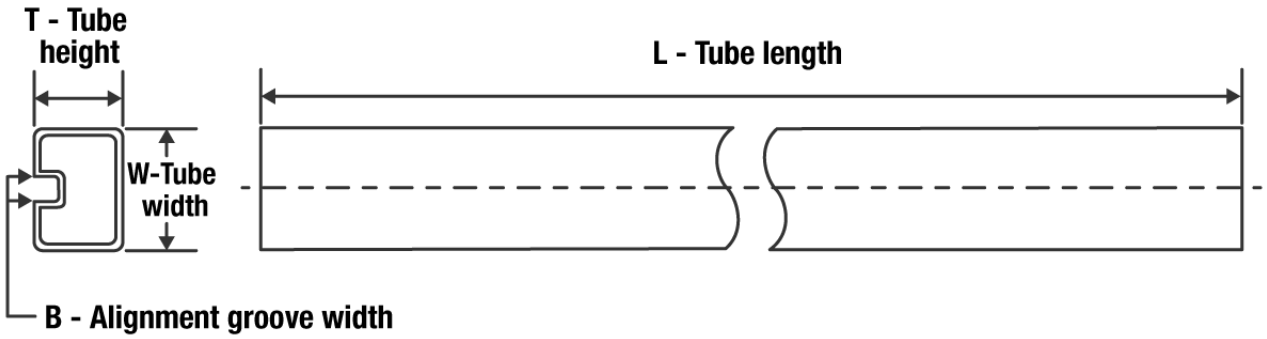
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LP1185DBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN75LP1185DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

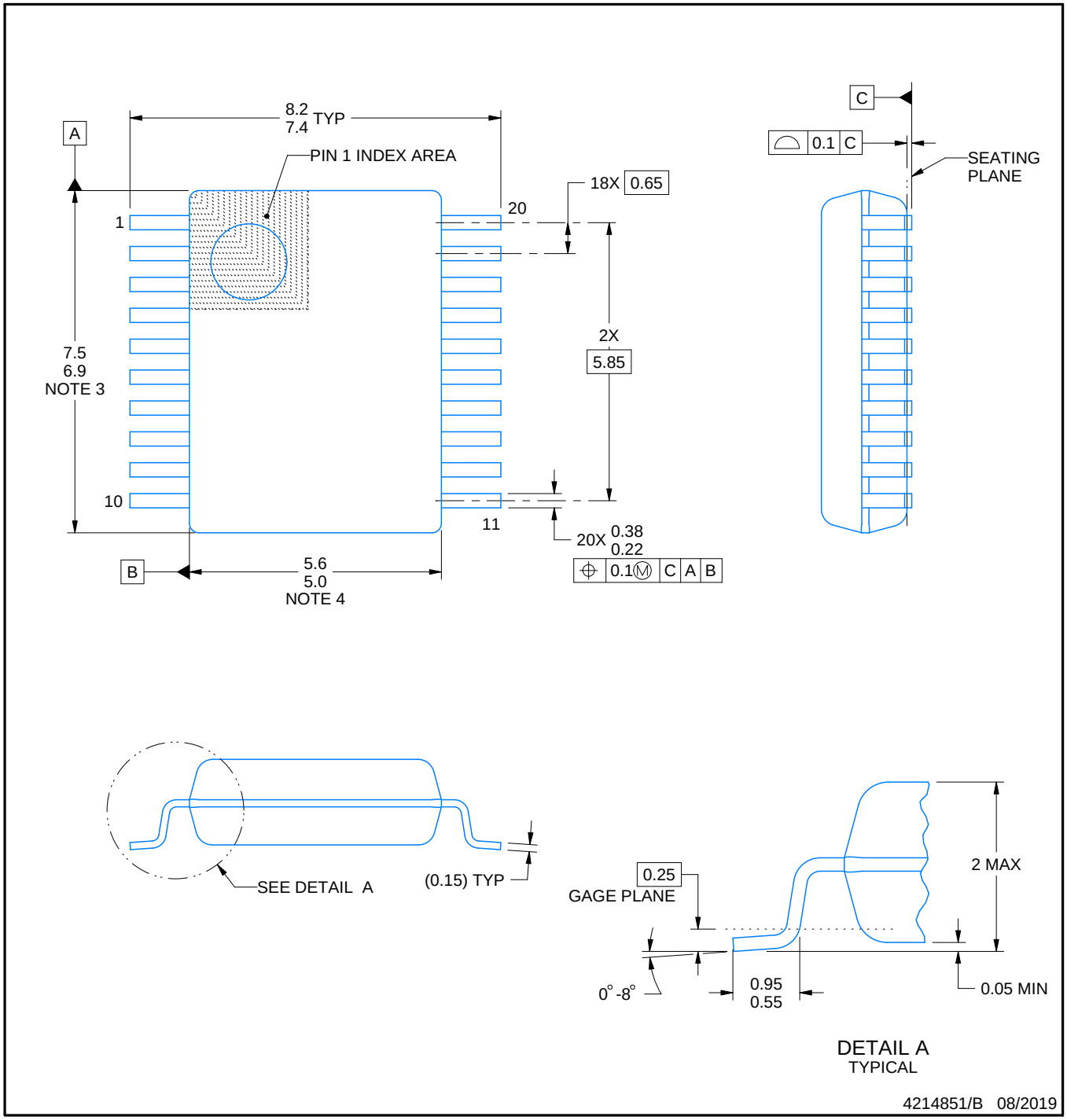
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LP1185DW	DW	SOIC	20	25	507	12.83	5080	6.6

PACKAGE OUTLINE

DB0020A

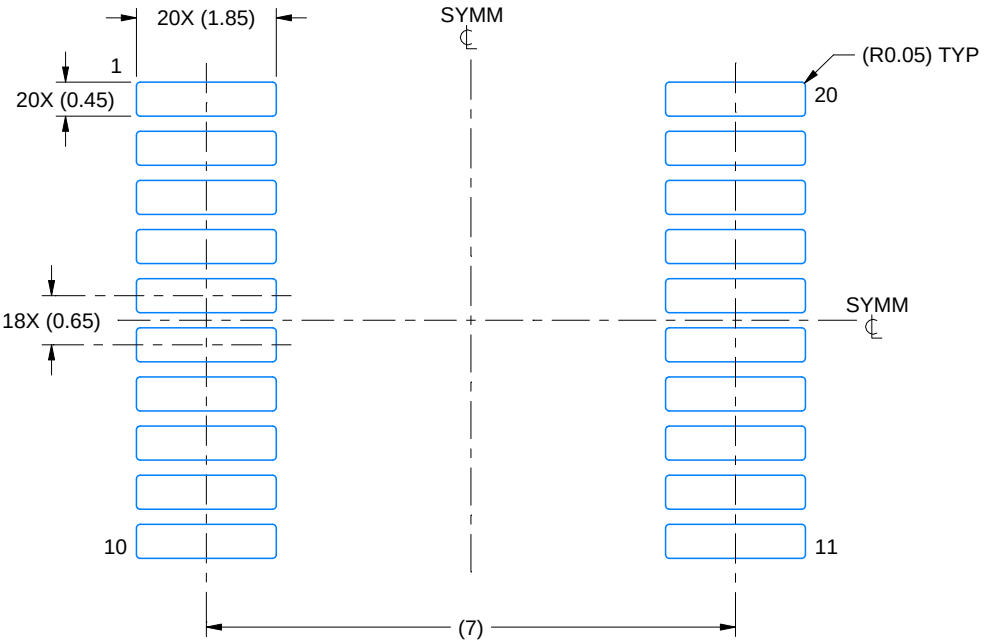
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

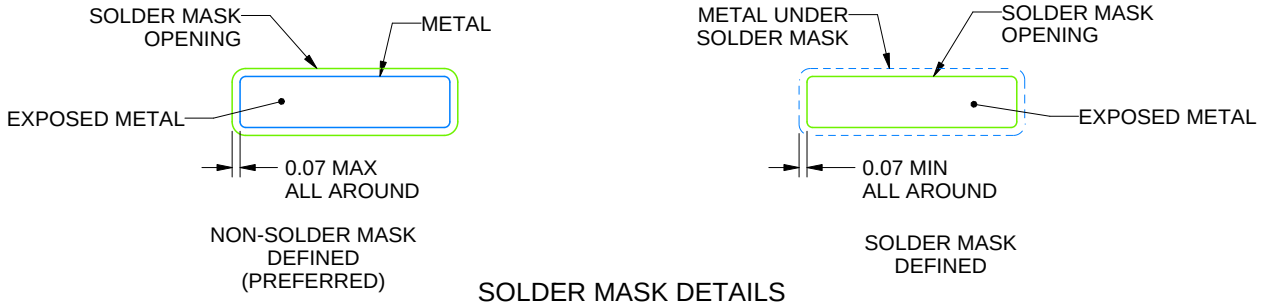


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

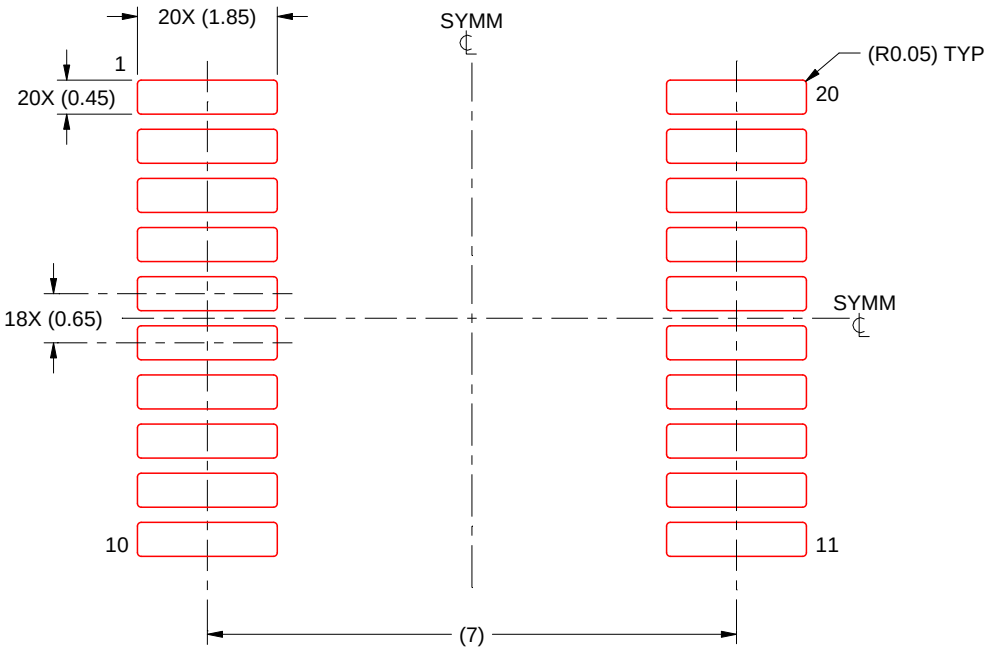
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

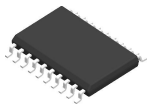


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

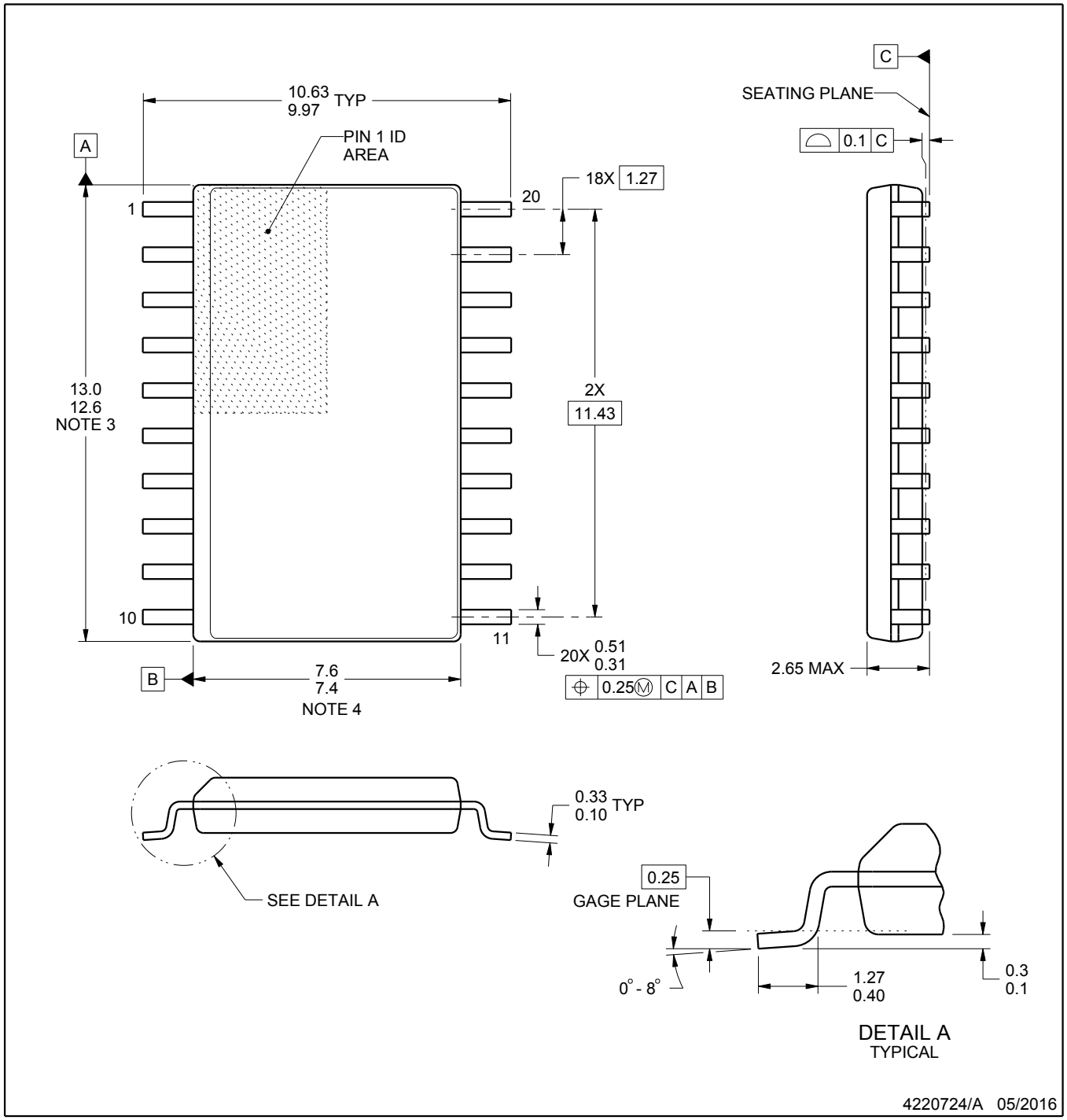


PACKAGE OUTLINE

DW0020A

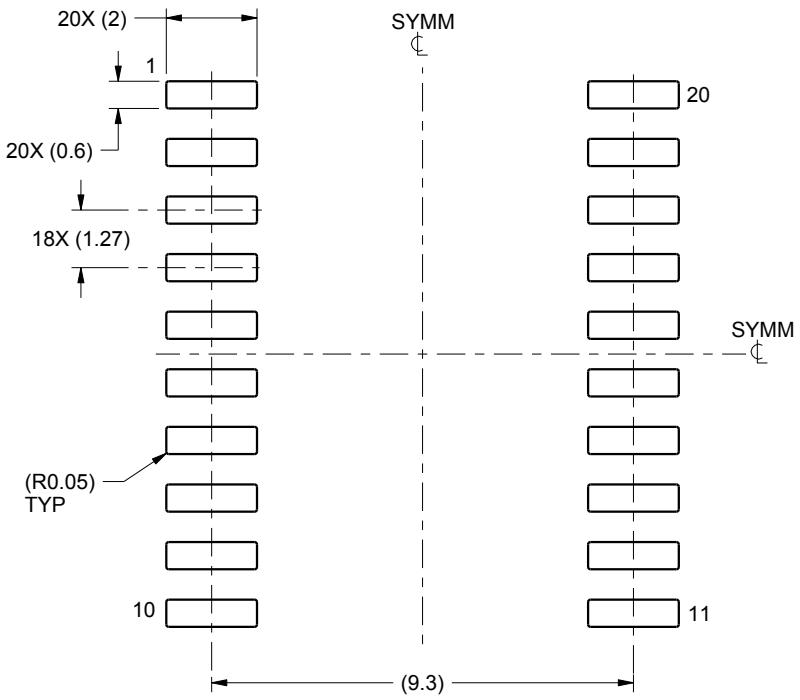
SOIC - 2.65 mm max height

SOIC

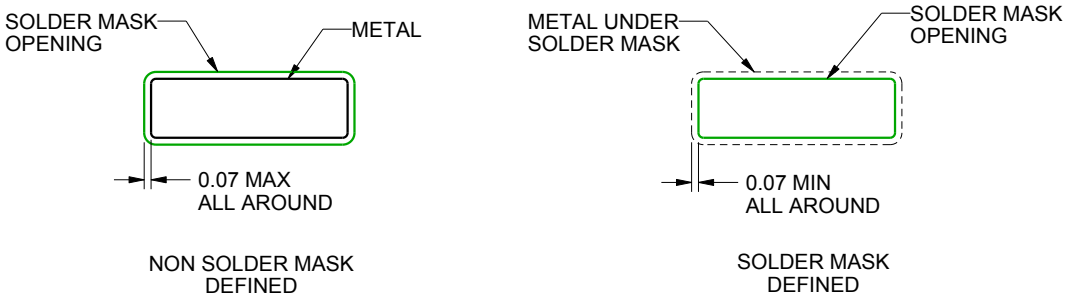


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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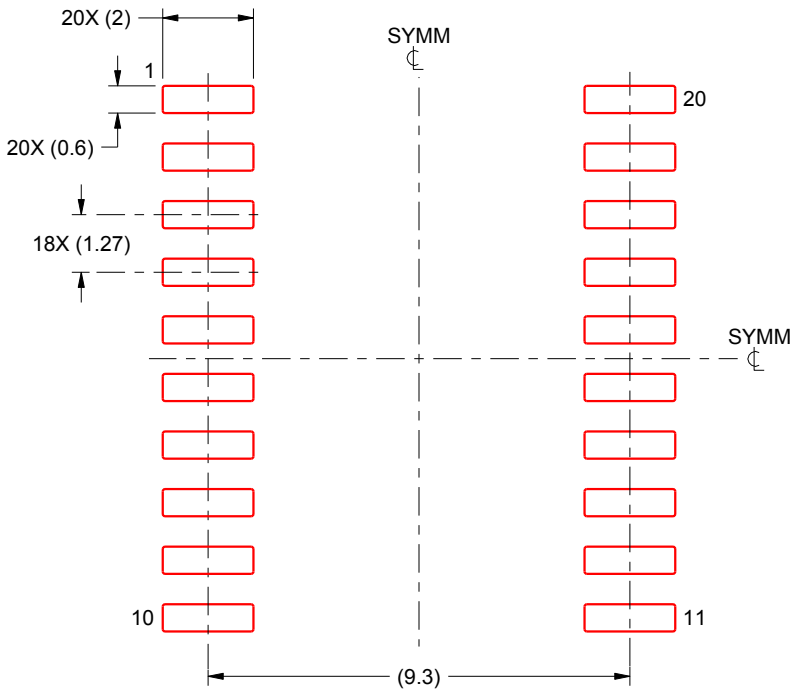
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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