

## MICROPOWER SUPPLY VOLTAGE SUPERVISORS

Check for Samples: [TLC7701-EP](#), [TLC7705-EP](#), [TLC7733-EP](#)

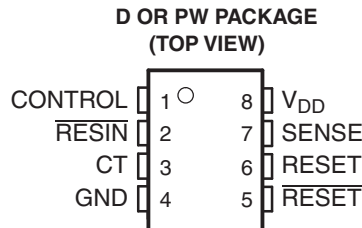
### FEATURES

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- Programmable Delay Time by External Capacitor
- Supply Voltage Range . . . 2 V to 6 V
- Defined RESET Output from  $V_{DD} \geq 1$  V
- Power-Down Control Support for Static RAM With Battery Backup
- Maximum Supply Current of 16 mA
- Power Saving Totem-Pole Outputs

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extended ( $-40^{\circ}\text{C}/125^{\circ}\text{C}$  and  $-55^{\circ}\text{C}/125^{\circ}\text{C}$ ), Temperature Ranges<sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(1) Additional temperature ranges available - contact factory



### DESCRIPTION

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, RESET is asserted when  $V_{DD}$  reaches 1 V. After minimum  $V_{DD}$  ( $\geq 2$  V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ( $V_{I(\text{SENSE})}$ ) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time ( $t_d$ ) is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T \quad (1)$$

Where

$C_T$  is in farads

$t_d$  is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed sense threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time ( $t_d$ ) has expired.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

In addition to the power-on reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ( $\overline{CS}$ ) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ( $\overline{CSH1}$ ) of the microprocessor (see Figure 11), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

**ORDERING INFORMATION**

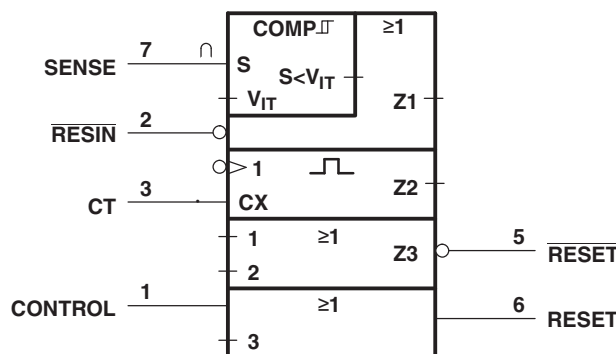
$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-40°C to 125°C	TSSOP - PW	Tape and reel	TLC7701QPWREP	7701QE	V62/04604 - 01XE
			TLC7705QPWREP	7705QE	V62/04604 - 02XE
			TLC7733QPWREP	7733QE	V62/04604 - 03XE
-55°C to 125°C	TSSOP - PW	Tape and reel	TLC7701MPWREP	7701ME	V62/04604 - 04XE
			TLC7733MPWREP	7733ME	V62/04604 - 06XE
	SOIC - D	Tape and reel	TLC7701MDREP	7701ME	V62/04604 - 04YE

(1) The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7701QPWREP).

**Table 1. FUNCTION TABLE**

CONTROL	RESIN	$V_{I(SENSE)} > V_{IT+}$	RESET	$\overline{RESET}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L <sup>(1)</sup>	H <sup>(1)</sup>
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H <sup>(1)</sup>

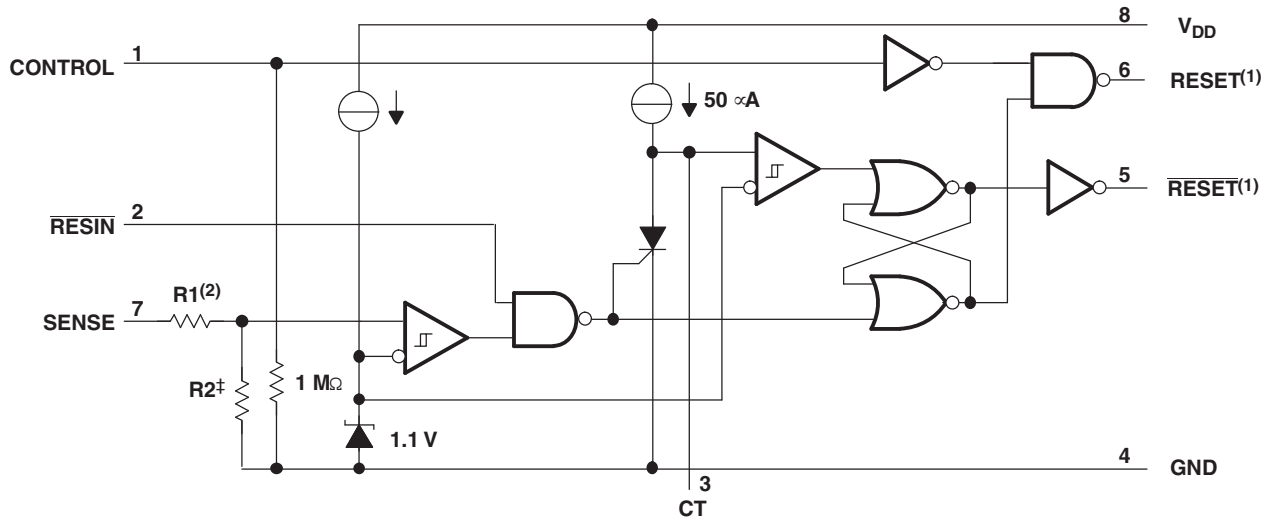
(1) RESET and  $\overline{RESET}$  states shown are valid for  $t > t_d$ .



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**Figure 1. Logic Symbol**

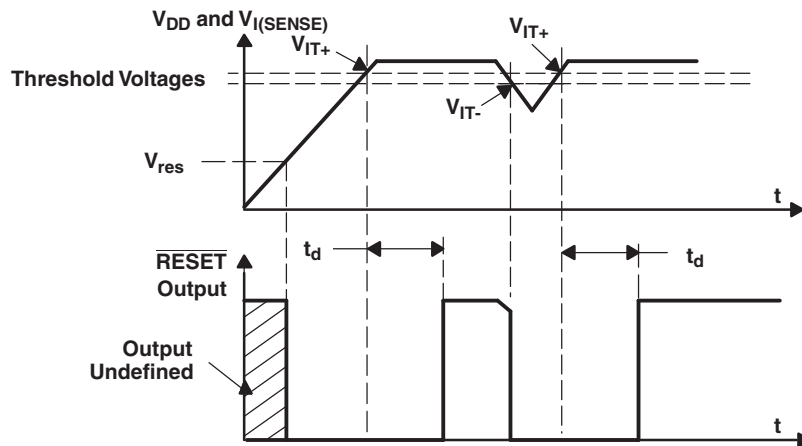
FUNCTIONAL BLOCK DIAGRAM



- (1) Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.
- (2) Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	$\infty$
TLC7705	910 k $\Omega$	290 k $\Omega$
TLC7733	750 k $\Omega$	450 k $\Omega$

TIMING DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT	
V <sub>DD</sub>	Supply voltage <sup>(2)</sup>	7	V	
Input voltage range, CONTROL, RESIN, SENSE <sup>(2)</sup>		-0.3 to 7	V	
I <sub>OL</sub>	Maximum low output current	10	mA	
I <sub>OH</sub>	Maximum high output current	10	mA	
I <sub>IK</sub>	Input clamp current, (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub> )	±10	mA	
I <sub>OK</sub>	Output clamp current, (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> )	±10	mA	
T <sub>A</sub>	Operating free-air temperature range	TL77xxQ	-40 to 125	°C
		TL77xxM	-55 to 125	
T <sub>stg</sub>	Storage temperature range	-65 to 150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TLC77xx-EP	TLC77xx-EP	UNITS
		D	PW	
		8 PINS	8 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	97.1	168	°C/W
θ <sub>JC</sub>	Junction-to-case thermal resistance	39.4	38.9	
θ <sub>JB</sub>	Junction-to-board thermal resistance	-	96.6	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	-	1.5	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	-	94.7	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	2		6	V
V <sub>I</sub>	Input voltage	0		V <sub>DD</sub>	V
V <sub>IH</sub>	High-level input voltage at $\overline{\text{RESIN}}$ and CONTROL <sup>(2)</sup>	0.7×V <sub>DD</sub>			V
V <sub>IL</sub>	Low-level input voltage at $\overline{\text{RESIN}}$ and CONTROL			0.2×V <sub>DD</sub>	V
I <sub>OH</sub>	High-level output current, V <sub>DD</sub> ≥ 2.7 V			-2	mA
I <sub>OL</sub>	Low-level output current, V <sub>DD</sub> ≥ 2.7 V			2	mA
Δt/ΔV	Input transition rise and fall rate at $\overline{\text{RESIN}}$ and CONTROL			100	ns/V
T <sub>A</sub>	Operating free-air temperature range	Q temperature range	-40	125	°C
		M temperature range	-55	125	

- (1) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.
- (2) To ensure a low supply current, V<sub>IL</sub> should be kept <0.3 V and V<sub>IH</sub> > -0.3 V.

## ELECTRICAL CHARACTERISTICS

 over recommended operating conditions<sup>(1)</sup> (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T <sub>A</sub> = -40°C to 125°C			T <sub>A</sub> = -55°C to 125°C			UNIT	
				MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = - 20 μA	V <sub>DD</sub> = 2 V	1.8			1.8			V	
			V <sub>DD</sub> = 2.7 V	2.5			2.5				
			V <sub>DD</sub> = 4.5 V	4.3			4.3				
		I <sub>OH</sub> = - 20 mA	V <sub>DD</sub> = 4.5 V	3.7			3.7				
V <sub>OL</sub>	Low-level output voltage	I <sub>OH</sub> = - 20 μA	V <sub>DD</sub> = 2 V	0.2			0.2			V	
			V <sub>DD</sub> = 2.7 V	0.2			0.2				
			V <sub>DD</sub> = 4.5 V	0.2			0.2				
		I <sub>OH</sub> = - 20 mA	V <sub>DD</sub> = 4.5 V	0.5			0.5				
V <sub>IT-</sub>	Negative-going input threshold voltage, SENSE <sup>(3)</sup>	TLC7701	V <sub>DD</sub> = 2 V to 6 V	1.04	1.1	1.16				V	
		TLC7705		4.43	4.5	4.63					
		TLC7733		2.855	2.93	3.03	2.8	2.93	3.03		
V <sub>hys</sub>	Hysteresis voltage, SENSE	TLC7701	V <sub>DD</sub> = 2 V to 6 V	30						mV	
		TLC7705		70							
		TLC7733		70			70				
V <sub>res</sub>	Power-up reset voltage <sup>(4)</sup>	I <sub>OL</sub> = 20 μA				1			V		
I <sub>I</sub>	Input current	RESIN	V <sub>I</sub> = 0 V to V <sub>DD</sub>				2			μA	
		CONTROL	V <sub>I</sub> = V <sub>DD</sub>				7	15	7		15
		SENSE	V <sub>I</sub> = 5 V				5	10	5		10
		SENSE, TLC7701 only	V <sub>I</sub> = 5 V				2				
I <sub>DD</sub>	Supply current	RESIN = V <sub>DD</sub> , SENSE = V <sub>DD</sub> ≥ V <sub>ITmax</sub> + 0.2 V, CONTROL = 0 V, Outputs open					9	16	9	18	μA
I <sub>DD(d)</sub>	Supply current during t <sub>d</sub>	V <sub>DD</sub> = 5 V, V <sub>CT</sub> = 0 , RESIN = V <sub>DD</sub> , SENSE = V <sub>DD</sub> , CONTROL = 0 V, Outputs open					120	150	120	150	μA
C <sub>I</sub>	Input capacitance, SENSE	V <sub>I</sub> = 0 V to V <sub>DD</sub>					50			pF	

 (1) All characteristics are measured with C<sub>T</sub> = 0.1 μF.

 (2) Typical values apply at T<sub>A</sub> = 25°C.

(3) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be connected near the supply terminals.

 (4) The lowest supply voltage at which RESET becomes active. The symbol V<sub>res</sub> is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V<sub>DD</sub> ≥ 15 ms/V.

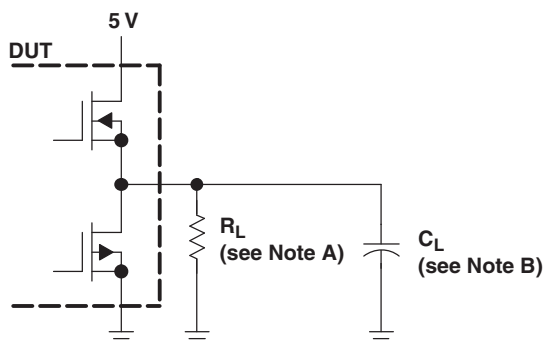
### SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MEASURED		TEST CONDITIONS	T <sub>A</sub> = -40°C to 125°C			T <sub>A</sub> = -55°C to 125°C			UNIT
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>d</sub>	Delay time			RESIN = 0.7 × V <sub>DD</sub> , CONTROL = 0.2 × V <sub>DD</sub> , C <sub>T</sub> = 100 nF, T <sub>A</sub> = Full range, See timing diagram	1.1	2.1	4.2		2.1		ms
t <sub>PLH</sub>	Propagation delay time, low-to-high level output	SENSE	$\overline{\text{RESET}}$	V <sub>IH</sub> = V <sub>IT+max</sub> + 0.2 V, V <sub>IL</sub> = V <sub>IT-min</sub> - 0.2 V, RESIN = 0.7 × V <sub>DD</sub> , CONTROL = 0.2 × V <sub>DD</sub> , C <sub>T</sub> = NC <sup>(1)</sup>			20			20	μs
t <sub>PLH</sub>	Propagation delay time, high-to-low level output						5		5		
t <sub>PLH</sub>	Propagation delay time, low-to-high level output		RESET				5		5		
t <sub>PLH</sub>	Propagation delay time, high-to-low level output						20		20		
t <sub>PLH</sub>	Propagation delay time, low-to-high level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V <sub>IH</sub> = 0.7 × V <sub>DD</sub> , V <sub>IL</sub> = 0.2 × V <sub>DD</sub> , SENSE = V <sub>IT+max</sub> + 0.2 V, CONTROL = 0.2 × V <sub>DD</sub> , C <sub>T</sub> = NC <sup>(1)</sup>			20			20	μs
t <sub>PLH</sub>	Propagation delay time, high-to-low level output						60		60	ns	
t <sub>PLH</sub>	Propagation delay time, low-to-high level output		RESET				65		65		
t <sub>PLH</sub>	Propagation delay time, high-to-low level output						20		20	μs	
t <sub>PLH</sub>	Propagation delay time, low-to-high level output	CONTROL	RESET	V <sub>IH</sub> = 0.7 × V <sub>DD</sub> , V <sub>IL</sub> = 0.2 × V <sub>DD</sub> , SENSE = V <sub>IT+max</sub> + 0.2 V, RESIN = 0.7 × V <sub>DD</sub> , C <sub>T</sub> = NC <sup>(1)</sup>			58			58	ns
t <sub>PLH</sub>	Propagation delay time, high-to-low level output						58		58	ns	
	Low-level minimum pulse duration to switch $\overline{\text{RESET}}$ and RESET	SENSE		V <sub>IH</sub> = V <sub>IT+max</sub> + 0.2 V, V <sub>IL</sub> = V <sub>IT-min</sub> - 0.2 V	3			4			μs
		$\overline{\text{RESIN}}$		V <sub>IL</sub> = 0.2 × V <sub>DD</sub> , V <sub>IH</sub> = 0.7 × V <sub>DD</sub>	1			1			
t <sub>r</sub>	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%		8		8			ns/V
t <sub>f</sub>	Fall time			90% to 10%		4		4			

(1) NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



- A. For switching characteristics,  $R_L = 2\text{ k}\Omega$
- B.  $C_L = 50\text{ pF}$  includes jig and probe capacitance

Figure 2. RESET AND  $\overline{\text{RESET}}$  Output Configurations

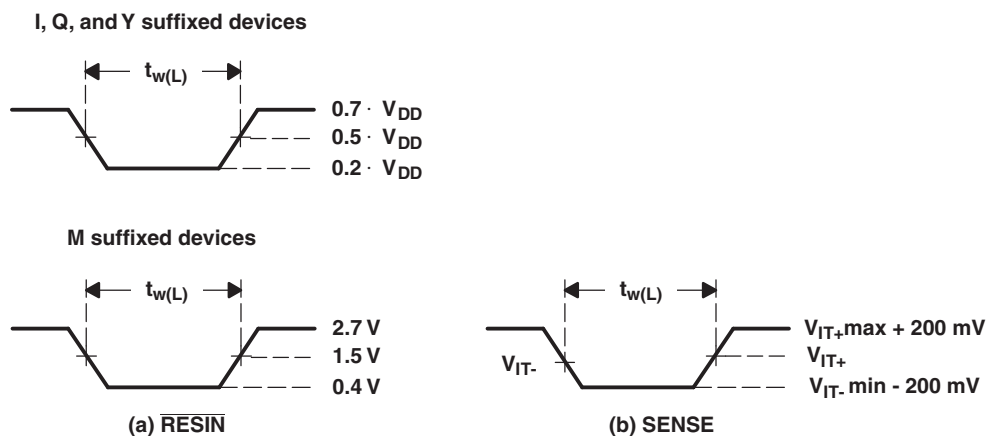


Figure 3. Input Pulse Definition Waveforms

**TYPICAL CHARACTERISTICS**

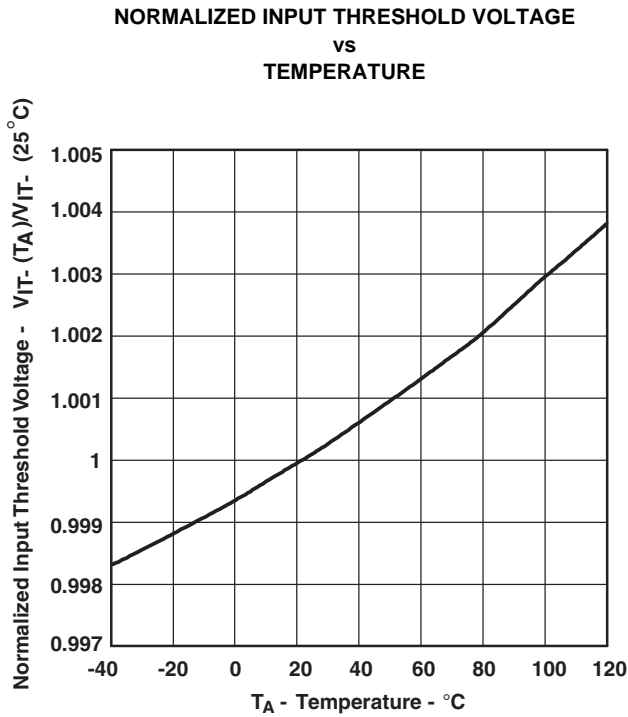


Figure 4.

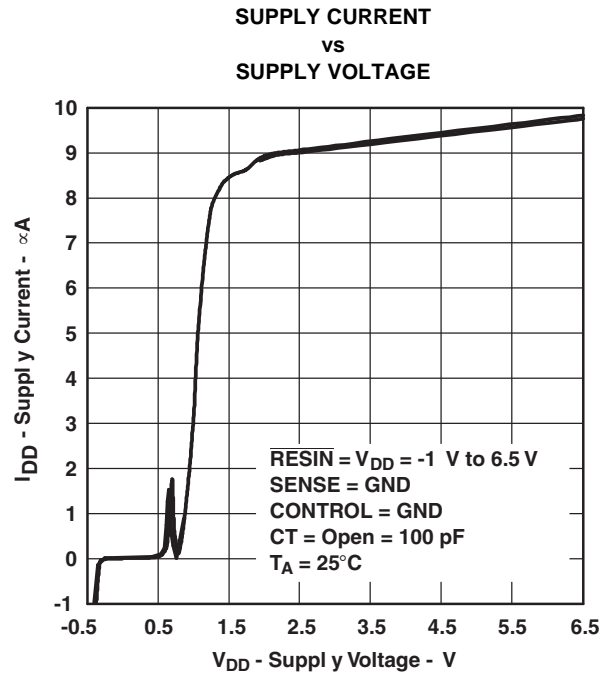


Figure 5.

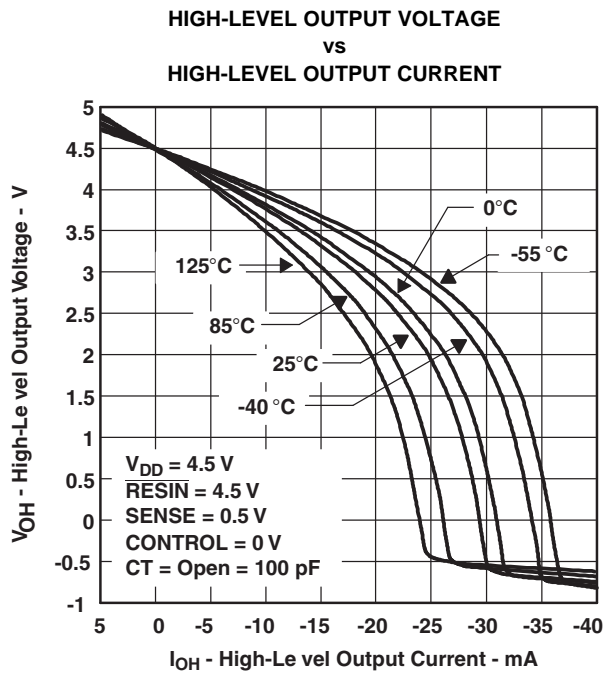


Figure 6.

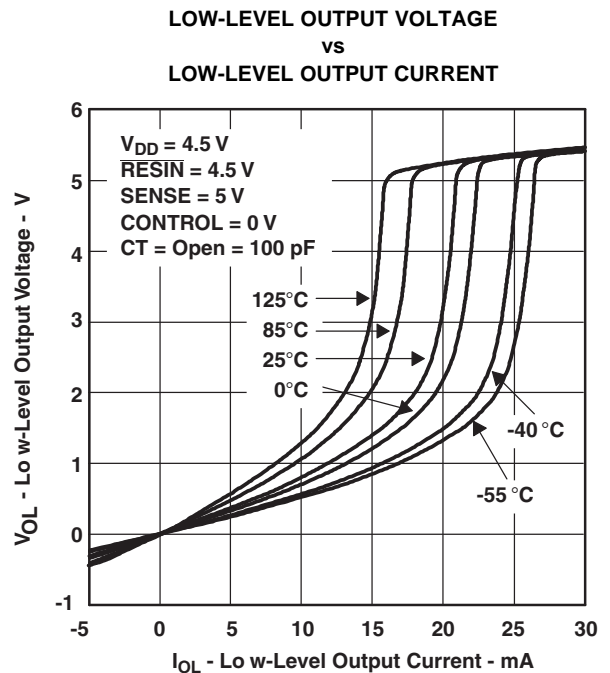
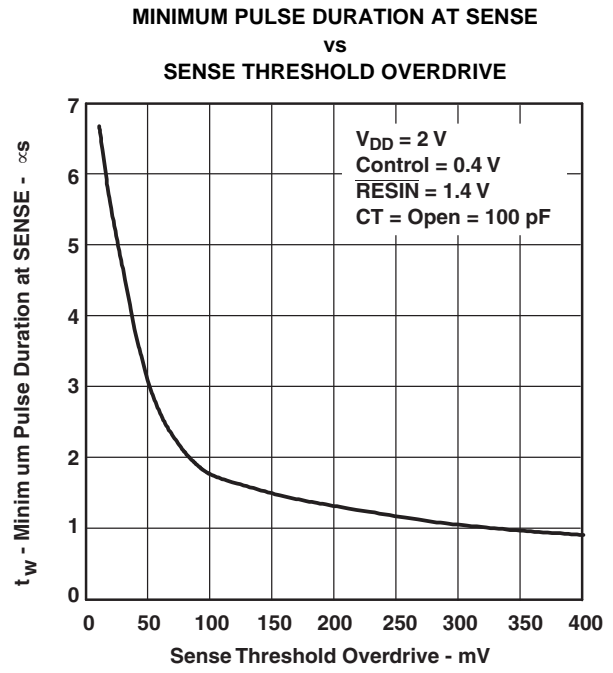
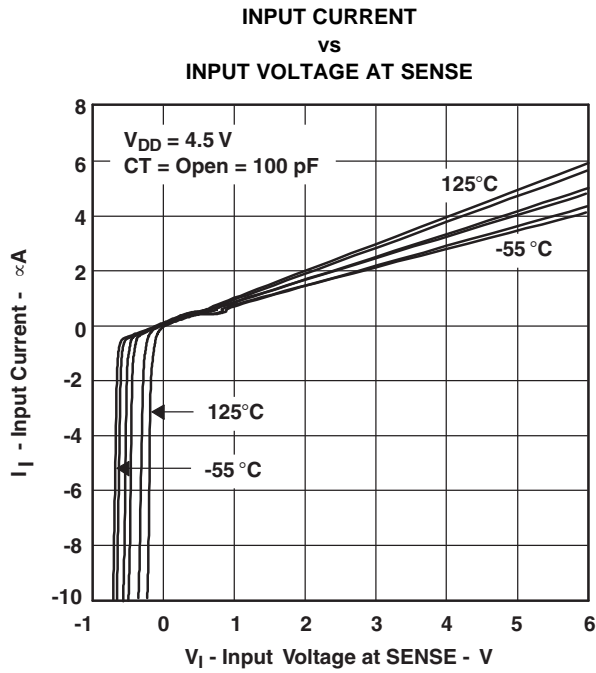


Figure 7.

**TYPICAL CHARACTERISTICS (continued)**



APPLICATION INFORMATION

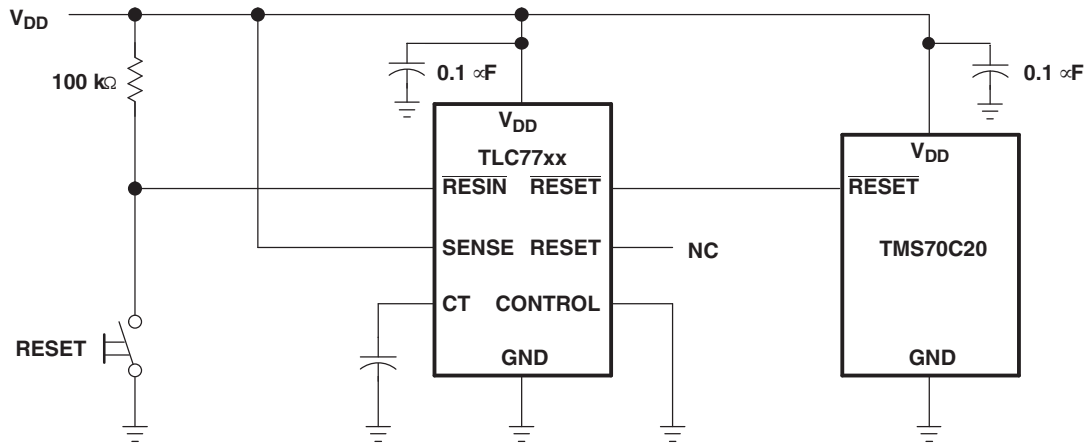


Figure 10. Reset Controller in a Microcomputer System

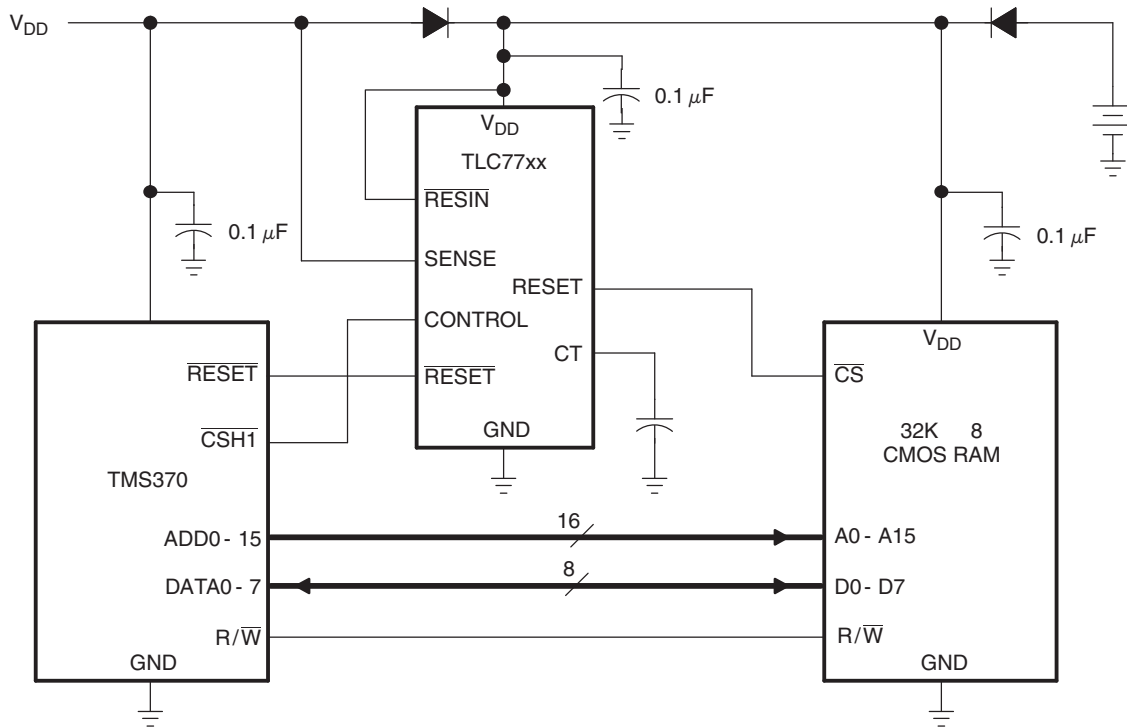


Figure 11. Data Retention During Power Down Using Static CMOS RAMs

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC7701MDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	<a href="#">Samples</a>
TLC7701MPWREP	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	<a href="#">Samples</a>
TLC7701MPWREPG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	<a href="#">Samples</a>
TLC7701QPWREP	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701QE	<a href="#">Samples</a>
TLC7705QPWREP	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705QE	<a href="#">Samples</a>
TLC7733MPWREP	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7733ME	<a href="#">Samples</a>
TLC7733QPWREP	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733QE	<a href="#">Samples</a>
V62/04604-01XE	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701QE	<a href="#">Samples</a>
V62/04604-02XE	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705QE	<a href="#">Samples</a>
V62/04604-03XE	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733QE	<a href="#">Samples</a>
V62/04604-04XE	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	<a href="#">Samples</a>
V62/04604-04YE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	<a href="#">Samples</a>
V62/04604-06XE	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7733ME	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TLC77-EP :**

● Catalog: [TLC77](#)

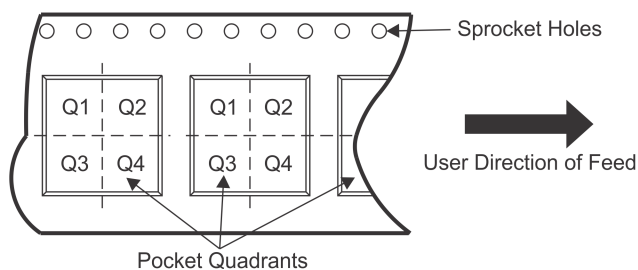
● Automotive: [TLC77-Q1](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7701MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7701MPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7701QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7705QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7733MPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7733QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7701MDREP	SOIC	D	8	2500	340.5	336.1	25.0
TLC7701MPWREP	TSSOP	PW	8	2000	853.0	449.0	35.0
TLC7701QPWREP	TSSOP	PW	8	2000	853.0	449.0	35.0
TLC7705QPWREP	TSSOP	PW	8	2000	853.0	449.0	35.0
TLC7733MPWREP	TSSOP	PW	8	2000	853.0	449.0	35.0
TLC7733QPWREP	TSSOP	PW	8	2000	853.0	449.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

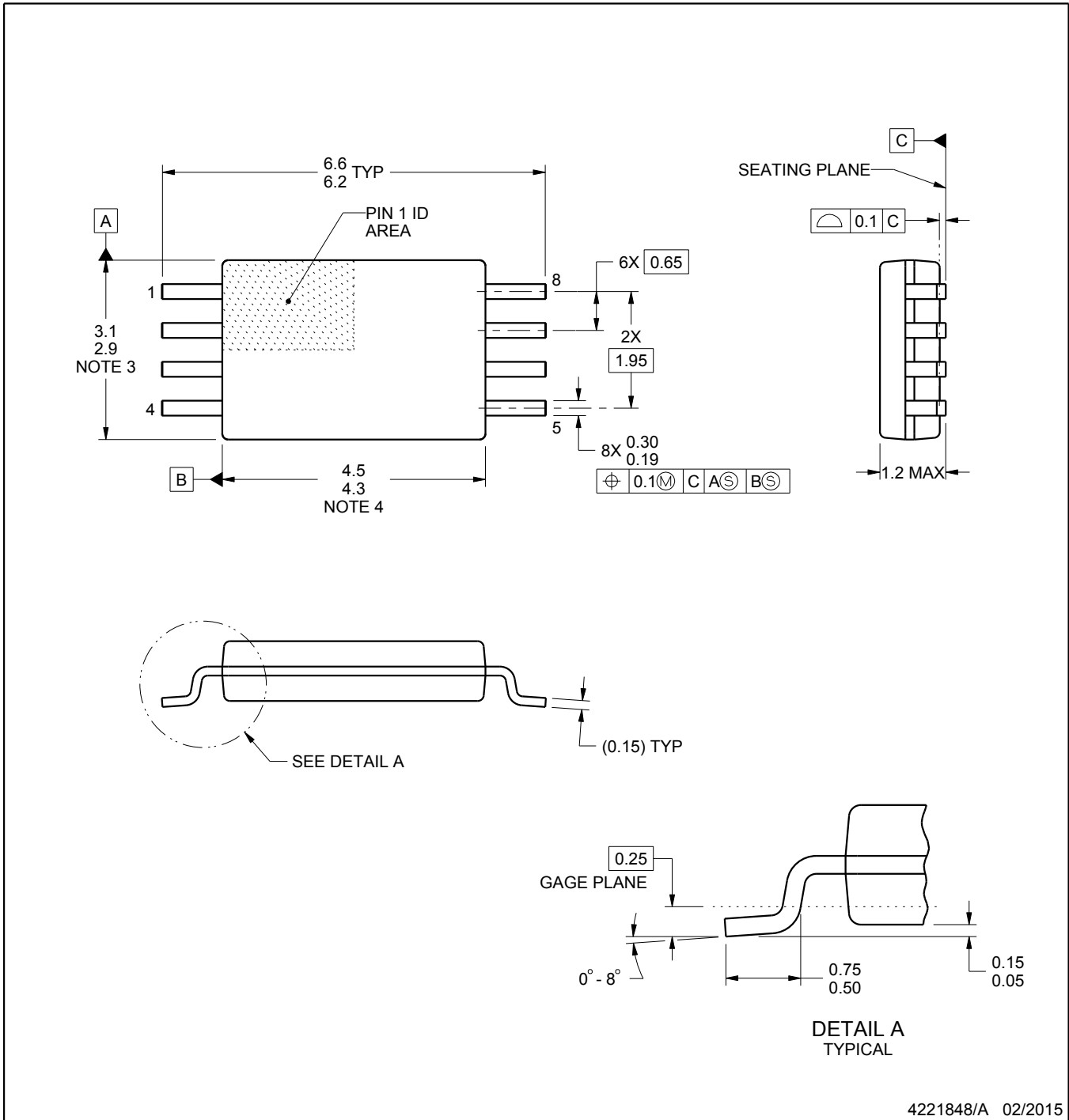
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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