MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Low Supply Voltage Range: 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption**
  - **Active Mode: 250 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%**
  - **32-kHz Crystal**
  - **High-Frequency Crystal up to 16 MHz**
  - **Resonator**
  - **External Digital Clock Source**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On Chip Emulation Module**
- **Family Members:**
  - **MSP430F2101**
    - **1KB + 256B Flash Memory**
    - **128B RAM**
  - **MSP430F2111**
    - **2KB + 256B Flash Memory**
    - **128B RAM**
  - **MSP430F2121**
    - **4KB + 256B Flash Memory**
    - **256B RAM**
  - **MSP430F2131**
    - **8KB + 256B Flash Memory**
    - **256B RAM**
- **Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package, 20-Pin Plastic Small-Outline Thin (TSSOP) Package, 20-Pin TVSOP Package, and 24-Pin QFN Package**
- **For Complete Module Descriptions, See the MSP430x2xx Family User's Guide (SLAU144)**

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430x21x1 series is an ultra-low-power mixed signal microcontroller with a built-in 16-bit timer, versatile analog comparator, and sixteen I/O pins.

Typical applications include sensor systems that capture analog signals, convert themto digital values, and then process the data for display or for transmission to a host system. Stand-alone RF sensor front end is another area of application. The analog comparator provides slope A/D conversion capability.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Table 1. Available Options

T_A	PACKAGED DEVICES			
	PLASTIC 20-PIN SOWB (DW)	PLASTIC 20-PIN TSSOP (PW)	PLASTIC 20-PIN TVSOP (DGV)	PLASTIC 24-PIN QFN (RGE)
-40°C to 85°C	MSP430F2101IDW	MSP430F2101IPW	MSP430F2101IDGV	MSP430F2101IRGE
	MSP430F2111IDW	MSP430F2111IPW	MSP430F2111IDGV	MSP430F2111IRGE
	MSP430F2121IDW	MSP430F2121IPW	MSP430F2121IDGV	MSP430F2121IRGE
	MSP430F2131IDW	MSP430F2131IPW	MSP430F2131IDGV	MSP430F2131IRGE
-40°C to 105°C	MSP430F2101TDW	MSP430F2101TPW	MSP430F2101TDGV	MSP430F2101TRGE
	MSP430F2111TDW	MSP430F2111TPW	MSP430F2111TDGV	MSP430F2111TRGE
	MSP430F2121TDW	MSP430F2121TPW	MSP430F2121TDGV	MSP430F2121TRGE
	MSP430F2131TDW	MSP430F2131TPW	MSP430F2131TDGV	MSP430F2131TRGE

Development Tool Support

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) that allows advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and Programming Interface with Target Board
  - MSP-FET430U28 (PW package)
- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Target Board
  - MSP-TS430PW28 (PW package)
- Production Programmer
  - MSP-GANG430

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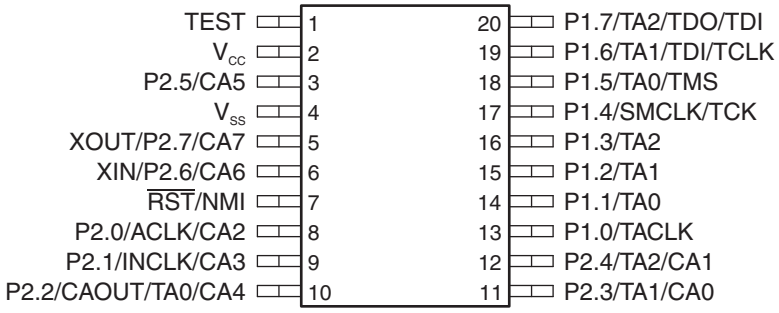
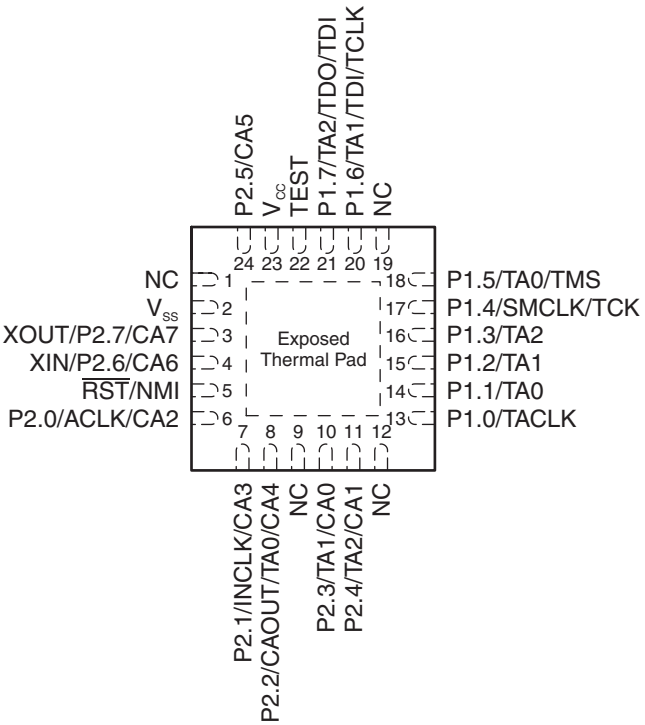
Device Pinout

DW, PW, or DGV PACKAGE
(TOP VIEW)



RGE PACKAGE
(TOP VIEW)



A. NC = Not internally connected

B. Exposed thermal pad connection to V_{SS} recommended.

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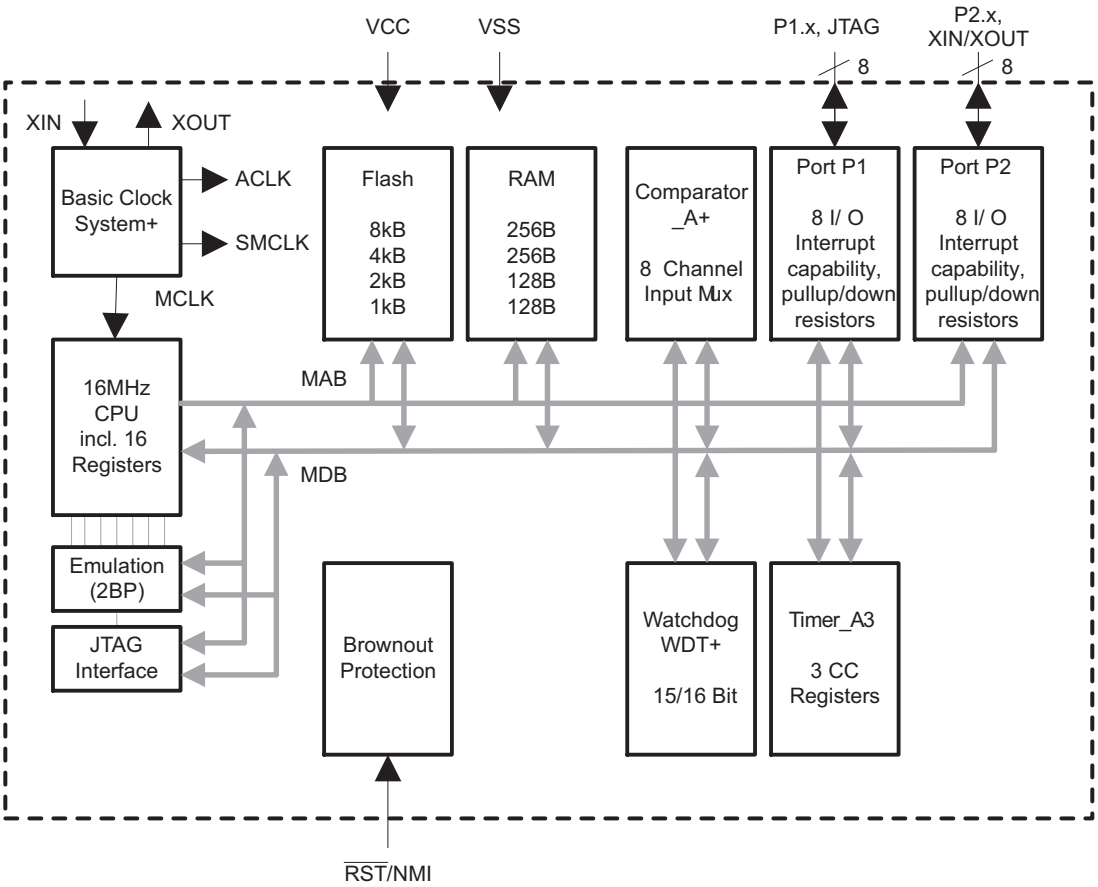
Functional Block Diagram



NOTE: See port schematics section for detailed I/O information.

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Table 2. Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DW, PW, or DGV	RGE		
P1.0/TACLK	13	13	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input
P1.1/TA	14	14	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	15	15	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	16	16	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK/TCK	17	17	I/O	General-purpose digital I/O pin / SMCLK signal output Test Clock input for device programming and test
P1.5/TA/TMS	18	18	I/O	General-purpose digital I/O pin / Timer_A, compare: Out0 output Test Mode Select input for device programming and test
P1.6/TA1/TDI/TCLK	19	20	I/O	General-purpose digital I/O pin / Timer_A, compare: Out1 output Test Data Input or Test Clock Input for programming and test
P1.7/TA2/TDO/TDI (1)	20	21	I/O	General-purpose digital I/O pin / Timer_A, compare: Out2 output Test Data Output or Test Data Input for programming and test
P2.0/ACLK/CA2	8	6	I/O	General-purpose digital I/O pin / ACLK output Comparator_A+, CA2 input
P2.1/INCLK/CA3	9	7	I/O	General-purpose digital I/O pin / Timer_A, clock signal at INCLK Comparator_A+, CA3 input
P2.2/CAOUT/TA/CA4	10	8	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input/BSL receive Comparator_A+, output / CA4 input
P2.3/CA0/TA1	11	10	I/O	General-purpose digital I/O pin / Timer_A, compare: Out1 output Comparator_A+, CA0 input
P2.4/CA1/TA2	12	11	I/O	General-purpose digital I/O pin / Timer_A, compare: Out2 output Comparator_A+, CA1 input
P2.5/CA5	3	24	I/O	General-purpose digital I/O pin Comparator_A+, CA5 input
XIN/P2.6/CA6	6	4	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Comparator_A+, CA6 input
XOUT/P2.7/CA7 (2)	5	3	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin Comparator_A+, CA7 input
$\overline{RST}$/NMI	7	5	I	Reset or nonmaskable interrupt input
TEST	1	22	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST.
V_{CC}	2	23		Supply voltage
V_{SS}	4	2		Ground reference
QFN Pad	NA	Pad	NA	QFN package thermal pad. Connect to V_{SS}.

(1) TDO or TDI is selected via JTAG instruction.
(2) If XOUT/P2.7/CA7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

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SHORT-FORM DESCRIPTION

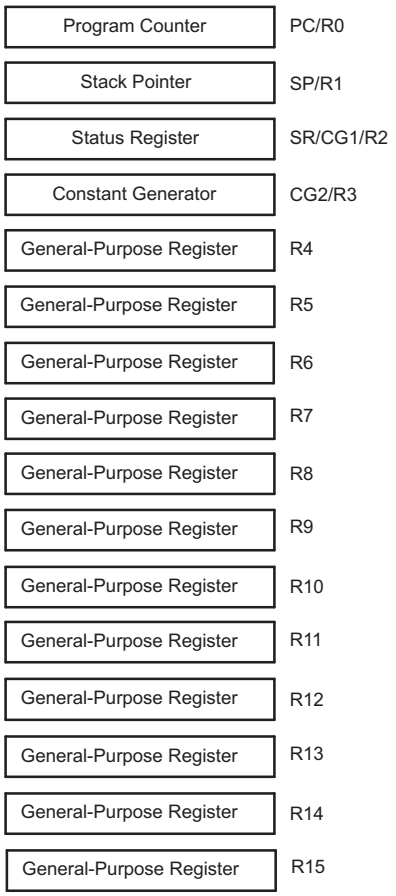
CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

Table 3. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional/conditional	JNE	Jump-on-equal bit = 0

Table 4. Address Mode Descriptions

ADDRESS MODE	S(1)	D(2)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source
(2) D = destination

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Operating Modes

The MSP430 microcontrollers have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled ACLK and SMCLK remain active. MCLK is disabled.
  - DCO dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - Crystal oscillator is stopped.

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Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0xFFFE) contains 0xFFFF (for example, if flash is not programmed), the CPU goes into LPM4 immediately after power up.

Table 5. Interrupt Vector Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out of range(2)	PORIFG RSTIFG WDTIFG KEYV(1)	Reset	0xFFFE	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(1)(3)	(non)-maskable (non)-maskable (non)-maskable	0xFFFC	30
			0xFFFA	29
			0xFFF8	28
Comparator_A+	CAIFG	maskable	0xFFF6	27
Watchdog Timer+	WDTIFG	maskable	0xFFF4	26
Timer_A3	TACCR0 CCIFG(4)	maskable	0xFFF2	25
Timer_A3	TACCR2, TACCR1 CCIFG, TAIFG(1)(4)	maskable	0xFFF0	24
			0xFFEE	23
			0xFFEC	22
			0xFFEA	21
			0xFFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7(1)(4)	maskable	0xFFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7(1)(4)	maskable	0xFFE4	18
			0xFFE2	17
			0xFFE0	16
See (5)			0xFFDE	15
See (6)			0xFFDC to 0xFFC0	14 to 0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0x0000 to 0x01FF) or from within unused address range.
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) This location is used as bootstrap loader security key (BSLSKEY).
A value of 0xAA55 at this location disables the BSL completely.
A value of 0x0 disables the erasure of the flash if an invalid password is supplied.
(6) The interrupt vectors at addresses 0xFFDC to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

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Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend

rw	Bit can be read and written.
rw-0, 1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), (1)	Bit can be read and written. It is Reset or Set by POR.
	SFR bit is not present in device.

Table 6. Interrupt Enable 1

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Table 7. Interrupt Enable 2

Address	7	6	5	4	3	2	1	0
01h								

Table 8. Interrupt Flag Register 1

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.
PORIFG	Power-on reset interrupt flag. Set on V_{CC} power up.
NMIIFG	Set via $\overline{RST}$/NMI pin

Table 9. Interrupt Flag Register 2

Address	7	6	5	4	3	2	1	0
03h								

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Memory Organization

Table 10. Memory Organization

		MSP430F2101	MSP430F2111	MSP430F2121	MSP430F2131
Memory	Size	1 KB Flash	2 KB Flash	4 KB Flash	8 KB Flash
Main: interrupt vector	Flash	0xFFFF to 0xFFE0	0xFFFF to 0xFFE0	0xFFFF to 0xFFE0	0xFFFF to 0xFFE0
Main: code memory	Flash	0xFFFF to 0xFC00	0xFFFF to 0xF800	0xFFFF to 0xF000	0xFFFF to 0xE000
Information memory	Size	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	0x10FF to 0x1000	0x10FF to 0x1000	0x10FF to 0x1000	0x10FF to 0x1000
Boot memory	Size	1 KB	1 KB	1 KB	1 KB
	ROM	0x0FFF to 0x0C00	0x0FFF to 0x0C00	0x0FFF to 0x0C00	0x0FFF to 0x0C00
RAM	Size	128 B	128 B	256 Byte	256 Byte
		0x027F to 0x0200	0x027F to 0x0200	0x02FF to 0x0200	0x02FF to 0x0200
Peripherals	16-bit	0x01FF to 0x0100	0x01FF to 0x0100	0x01FF to 0x0100	0x01FF to 0x0100
	8-bit	0x0FF to 0x010	0x0FF to 0x010	0x0FF to 0x010	0x0FF to 0x010
	8-bit SFR	0x0F to 0x00	0x0F to 0x00	0x0F to 0x00	0x0F to 0x00

Bootstrap Loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to theMSP430memoryvia theBSLis protected by user-defined password.Abootstrap loader security key is provided at address 0FFDEh to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide*, literature number SLAU319.

Table 11. BSL Keys

BSLKEY	DESCRIPTION
00000h	Erasure of flash disabled if an invalid password is supplied
0AA55h	BSL disabled
any other value	BSL enabled

Table 12. BSL Function Pins

BSL FUNCTION	DW, PW, DGV PACKAGE PINS	RGE PACKAGE PINS
Data transmit	14 - P1.1	14 - P1.1
Data receive	10 - P2.2	8 - P2.2

Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

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Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules

Table 13. DCO Calibration Data, Provided From Factory In Flash Info Memory Segment A

DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
1 MHz	CALBC1_1MHZ	byte	0x010FF
	CALBC0_1MHZ	byte	0x010FE
8 MHz	CALBC1_8MHZ	byte	0x010FD
	CALBC0_8MHZ	byte	0x010FC
12 MHz	CALBC1_12MHZ	byte	0x010FB
	CALBC0_12MHZ	byte	0x010FA
16 MHz	CALBC1_16MHZ	byte	0x010F9
	CALBC0_16MHZ	byte	0x010F8

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There are two 8-bit I/O ports implemented—ports P1 and P2.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

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Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 14. Timer_A3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
DW, PW, DGV	RGE					DW, PW, DGV	RGE
13 - P1.0	13 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	INCLK	INCLK				
14 - P1.1	14 - P1.1	TA	CCI0A	CCR0	TA	14 - P1.1	14 - P1.1
10 - P2.2	8 - P2.2	TA	CCI0B			18 - P1.5	18 - P1.5
		VSS	GND				
		VCC	VCC				
15 - P1.2	15 - P1.2	TA1	CCI1A	CCR1	TA1	11 - P2.3	10 - P2.3
		CAOUT (internal)	CCI1B			15 - P1.2	15 - P1.2
		VSS	GND			19 - P1.6	20 - P1.6
		VCC	VCC				
16 - P1.3	16 - P1.3	TA2	CCI2A	CCR2	TA2	12 - P2.4	11 - P2.4
		ACLK (internal)	CCI2B			16 - P1.3	16 - P1.3
		VSS	GND			20 - P1.7	21 - P1.7
		VCC	VCC				

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Peripheral File Map

Table 15. Peripherals With Word Access

MODULE	REGISTER NAME	SHORT NAME	ADDRESS OFFSET
Timer_A	Capture/compare register	TACCR2	0x0176
	Capture/compare register	TACCR1	0x0174
	Capture/compare register	TACCR0	0x0172
	Timer_A3 register	TAR	0x0170
	Capture/compare control	TACCTL2	0x0166
	Capture/compare control	TACCTL1	0x0164
	Capture/compare control	TACCTL0	0x0162
	Timer_A3 control	TACTL	0x0160
	Timer_A3 interrupt vector	TAIV	0x012E
Flash Memory	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog Timer+	Watchdog/timer control	WDTCTL	0x0120

Table 16. Peripherals With Byte Access

MODULE	REGISTER NAME	SHORT NAME	ADDRESS OFFSET
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control 2	CACTL2	0x005A
	Comparator_A control 1	CACTL1	0x0059
Basic Clock	Basic clock system control 3	BCSCTL3	0x0053
	Basic clock system control 2	BCSCTL2	0x0058
	Basic clock system control 1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Function	SFR interrupt flag 2	IFG2	0x0003
	SFR interrupt flag 1	IFG1	0x0002
	SFR interrupt enable 2	IE2	0x0001
	SFR interrupt enable 1	IE1	0x0000

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Absolute Maximum Ratings[(1)]

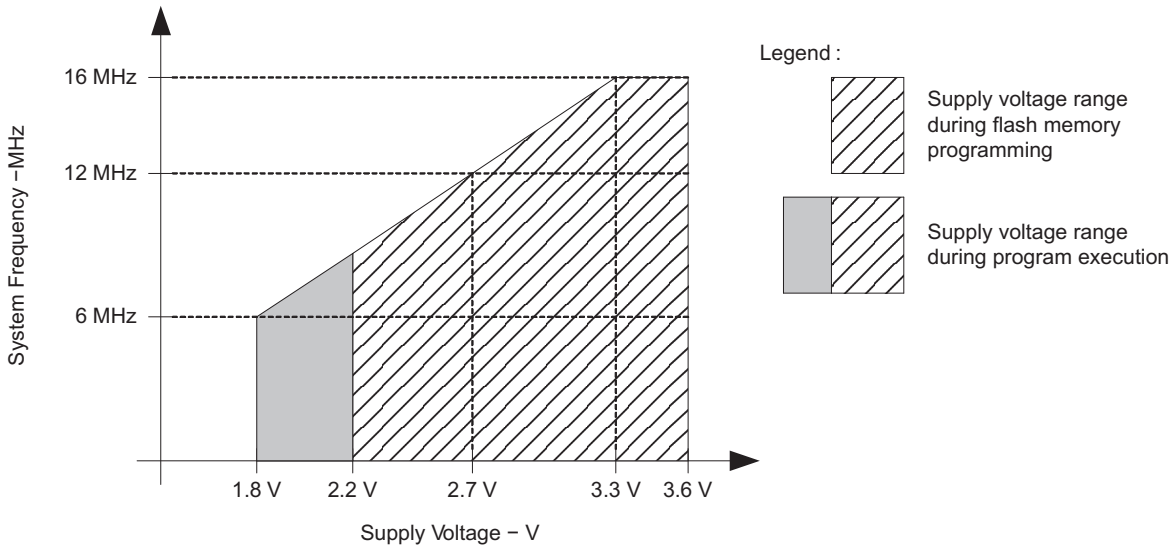
Voltage applied at V_{CC} to V_{SS}		-0.3 V to 4.1 V
Voltage applied to any pin [(2)]		-0.3 V to (V_{CC} + 0.3 V)
Diode current at any device terminal		±2 mA
Storage temperature, T_{stg} [(3)]	Unprogrammed device	-55°C to 150°C
	Programmed device	-55°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions[(1)]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, $AV_{CC} = DV_{CC} = V_{CC}$	During program execution	1.8		3.6	V
		During flash memory programming	2.2		3.6	
V_{SS}	Supply voltage, $AV_{SS} = DV_{SS} = V_{SS}$			0		V
T_A	Operating free-air temperature	I version	-40		85	°C
		T version	-40		105	
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)[(2)(1)] (see Figure 1)	V_{CC} = 1.8 V, Duty cycle = 50% ±10%	0		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ±10%	0		12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ±10%	0		16	

(1) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(2) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

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Active Mode Supply Current (into DV_{CC} + AV_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		250	300	µA
				3 V		350	410	
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		200		µA
				3 V		300		
$I_{AM,4kHz}$	Active mode (AM) current (4 kHz)	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32768 Hz / 8 = 4096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		2	5	µA
			105°C				6	
			-40°C to 85°C	3 V		3	9	
			105°C				9	
$I_{AM,100kHz}$	Active mode (AM) current (100 kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)}$ ≈ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1		2.2 V		60	85	µA
				3 V		72	95	

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics - Active-Mode Supply Current (Into V_{CC})

ACTIVE-MODE CURRENT vs SUPPLY VOLTAGE T_A = 25°C

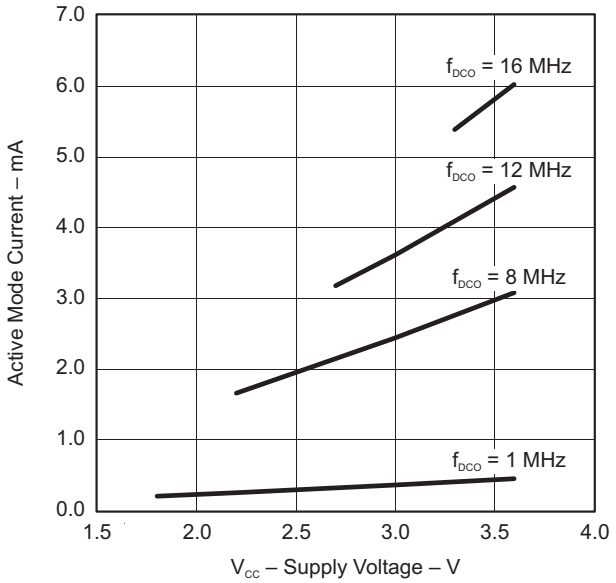

Figure 2.

ACTIVE-MODE CURRENT vs DCO FREQUENCY

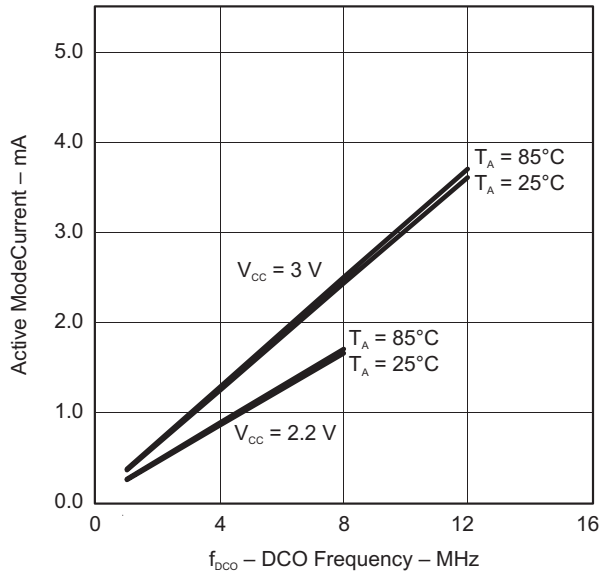

Figure 3.

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Low-Power-Mode Supply Currents (Into V_{CC}) Excluding External Current (1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		65	80	µA
				3 V		85	100	
$I_{LPM0,100kHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO}(0, 0) ≈ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1		2.2 V		37	48	µA
				3 V		41	52	
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		22	29	µA
			105°C				31	
			-40°C to 85°C	3 V		25	32	
			105°C				34	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.7	1.2	µA
			25°C			0.7	1	
			85°C			1.6	2.3	
			105°C			3	6	
			-40°C	3 V		0.9	1.2	
			25°C			0.9	1.2	
			85°C			1.6	2.8	
			105°C			3	7	
I_{LPM4}	Low-power mode 4 (LPM4) current(5)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V/3 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			0.8	1.9	
			105°C			2	4	

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

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Schmitt-Trigger Inputs (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			2.2 V	1		1.65	
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			2.2 V	0.55		1.20	
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})		2.2 V	0.2		1	V
			3 V	0.3		1	
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

Inputs (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag (1)	2.2 V/3 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set with trigger signals shorter than $t_{(int)}$.

Leakage Current (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	2.2 V/3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

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Outputs (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = -1.5 mA(1)	2.2 V	V_{CC} - 0.25	V_{CC}	V
		$I_{OH(max)}$ = -6 mA(2)		V_{CC} - 0.6	V_{CC}	
		$I_{OH(max)}$ = -1.5 mA(1)	3 V	V_{CC} - 0.25	V_{CC}	
		$I_{OH(max)}$ = -6 mA(2)		V_{CC} - 0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA(1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{OL(max)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.6	
		$I_{OL(max)}$ = 1.5 mA(1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{OL(max)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.6	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ(1)(2)	2.2 V		10	MHz
			3 V		12	
f_{Port_CLK}	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF(2)	2.2 V		12	MHz
			3 V		16	

(1) Alternatively, a resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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Typical Characteristics - Outputs

One output loaded at a time.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

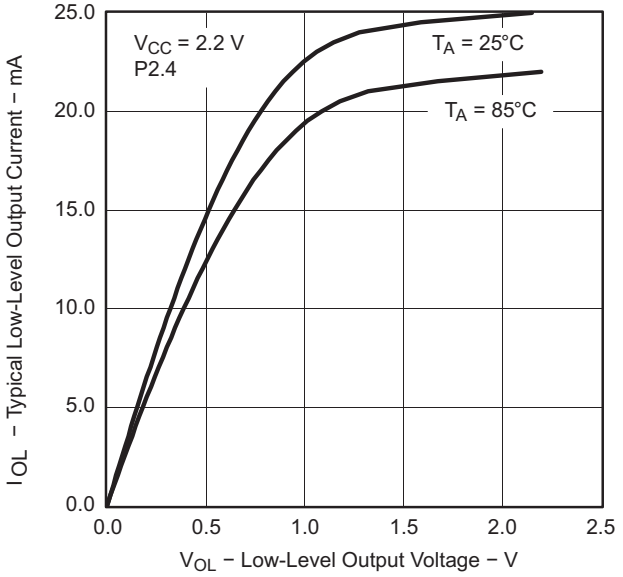

Figure 4.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

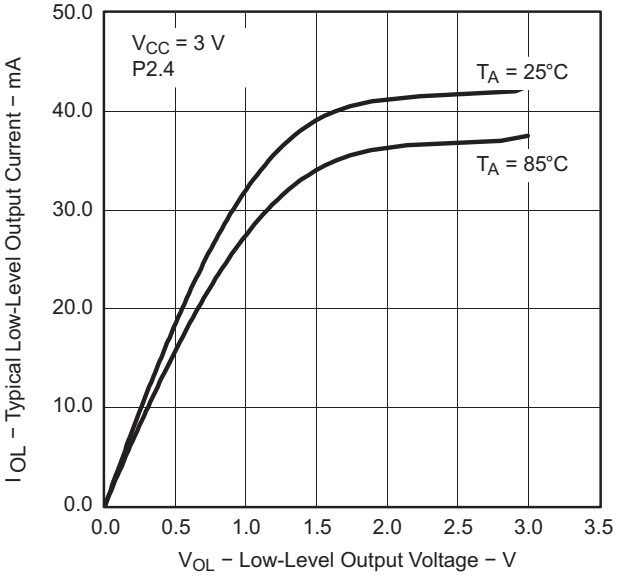

Figure 5.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

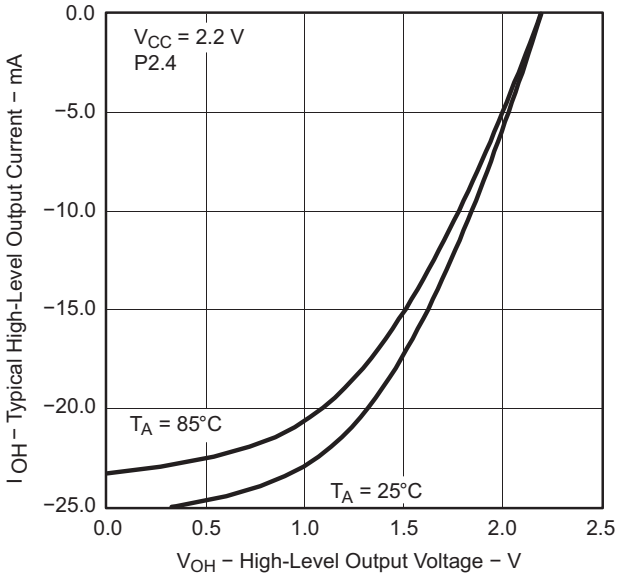

Figure 6.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

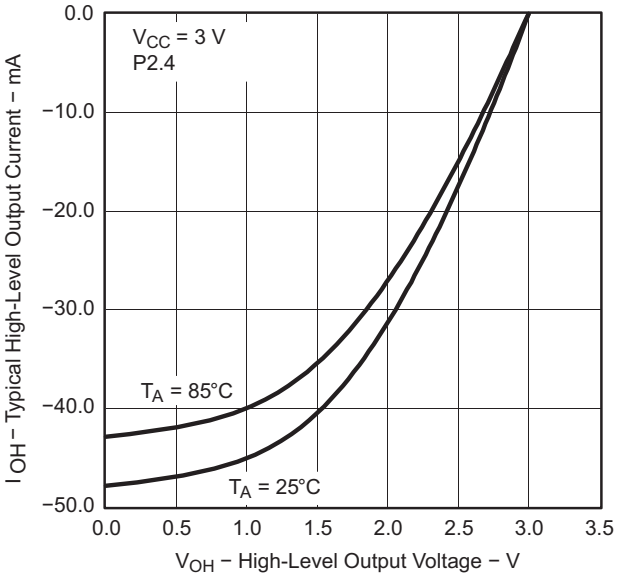

Figure 7.

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POR/Brownout Reset (BOR)(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 8	$dV_{CC}/dt \le 3$ V/s				0.7 × $V_{(B_IT-)}$		V
$V_{(B_IT-)}$	See Figure 8 through Figure 10	$dV_{CC}/dt \le 3$ V/s					1.71	V
$V_{hys(B_IT-)}$	See Figure 8	$dV_{CC}/dt \le 3$ V/s	-40°C to 85°C		70	130	180	mV
			105°C		70	130	210	
$t_{d(BOR)}$	See Figure 8						2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally			2.2 V/3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)} + V_{hys(B_IT-)}$ is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

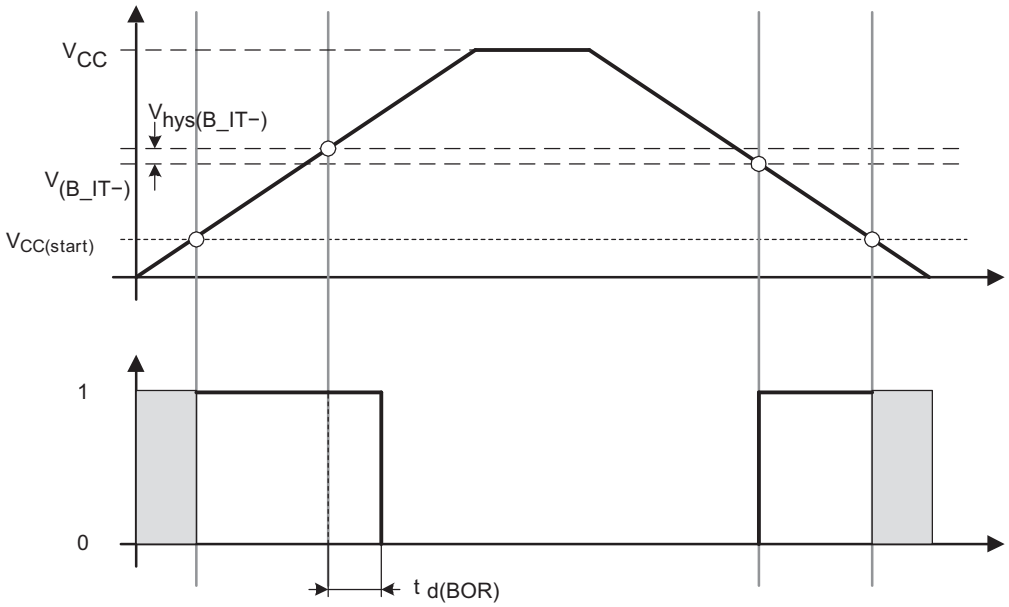

Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

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Typical Characteristics - POR/Brownout Reset (BOR)

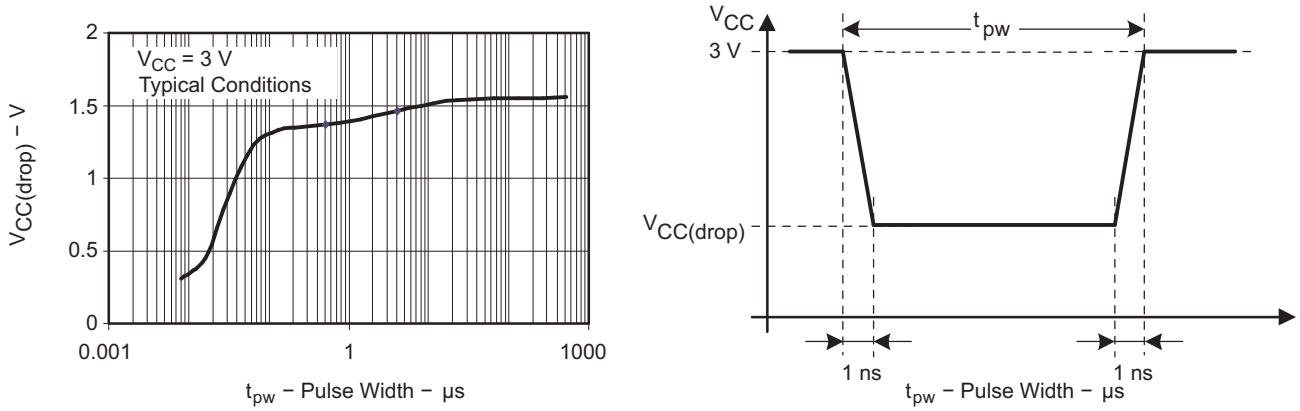

Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

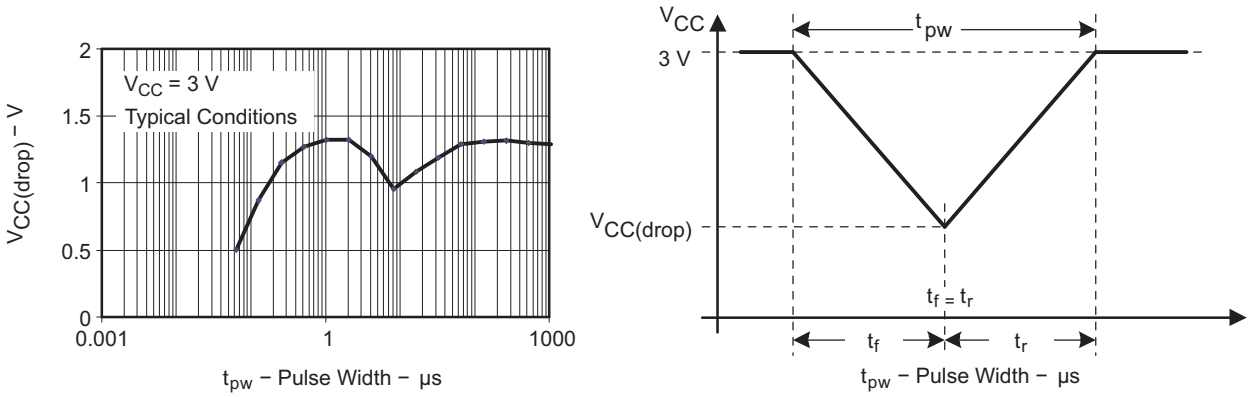

Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

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Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.05	1.08	1.12	ratio
	Duty cycle	Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

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Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	Frequency tolerance at calibration		25°C	3 V	-1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±0.5	+2.5	%
	8-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1	+2.5	%
	12-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1	+2.5	%
	16-MHz tolerance over temperature		0°C to 85°C	3 V	-3	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	0.97	1	1.03	MHz
				3 V	0.975	1	1.025	
				3.6 V	0.97	1	1.03	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	7.76	8	8.4	MHz
				3 V	7.8	8	8.2	
				3.6 V	7.6	8	8.24	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	11.7	12	12.3	MHz
				3 V	11.7	12	12.3	
				3.6 V	11.7	12	12.3	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0°C to 85°C	3 V	15.52	16	16.48	MHz
				3.6 V	15	16	16.48	

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Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
	8-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
	12-MHz tolerance over V_{CC}		25°C	2.2 V to 3.6 V	-3	±2	+3	%
	16-MHz tolerance over V_{CC}		25°C	3 V to 3.6 V	-3	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.97	1	1.03	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.76	8	8.24	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V to 3.6 V	15	16	16.48	MHz

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance overall		I: -40°C to 85°C T: -40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
	8-MHz tolerance overall		I: -40°C to 85°C T: -40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
	12-MHz tolerance overall		I: -40°C to 85°C T: -40°C to 105°C	2.2 V to 3.6 V	-5	±2	+5	%
	16-MHz tolerance overall		I: -40°C to 85°C T: -40°C to 105°C	3 V to 3.6 V	-6	±3	+6	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	I: -40°C to 85°C T: -40°C to 105°C	1.8 V to 3.6 V	0.95	1	1.05	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	I: -40°C to 85°C T: -40°C to 105°C	1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	I: -40°C to 85°C T: -40°C to 105°C	2.2 V to 3.6 V	11.4	12	12.6	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	I: -40°C to 85°C T: -40°C to 105°C	3 V to 3.6 V	15	16	17	MHz

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Typical Characteristics - Calibrated 1-MHz DCO Frequency

CALIBRATED 1-MHz FREQUENCY vs TEMPERATURE

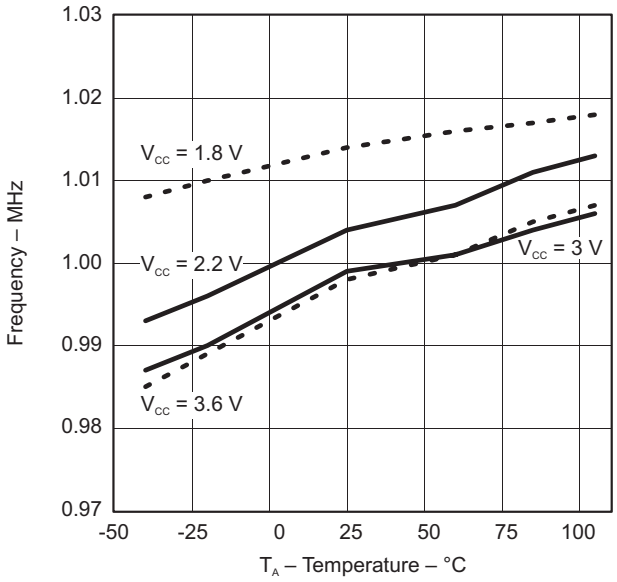

Figure 11.

CALIBRATED 1-MHz FREQUENCY vs SUPPLY VOLTAGE

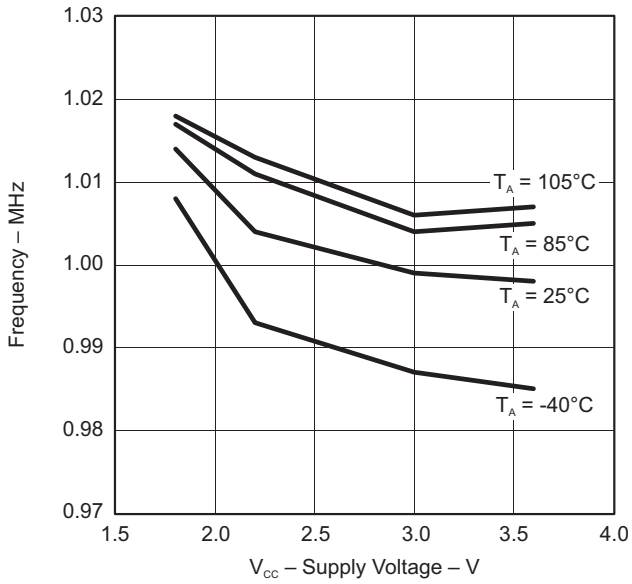

Figure 12.

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Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V/3 V			2	µs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ				1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ				1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (2)				$1 / f_{MCLK} + t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics - DCO Clock Wake-Up Time From LPM3/4

DCO WAKE-UP TIME FROM LPM3
vs
DCO FREQUENCY

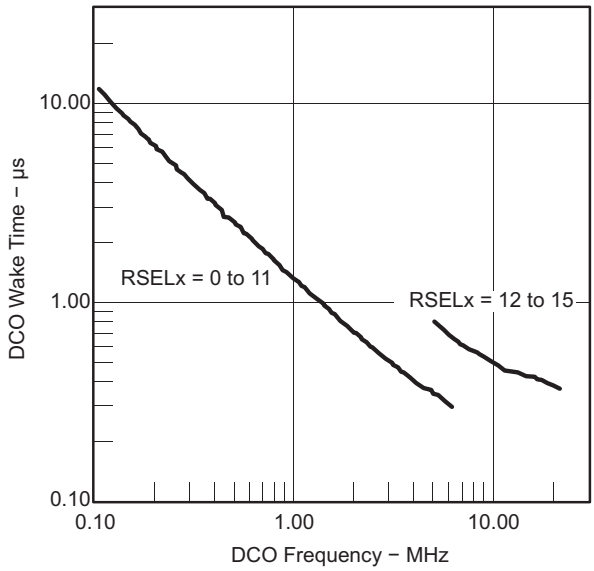

Figure 13.

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Crystal Oscillator LFXT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(2)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(3)	XTS = 0, LFXT1Sx = 3(4)	2.2 V/3 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.

(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(4) Measured with logic-level input frequency but also applies to operation with crystals.

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Crystal Oscillator LFXT1, High-Frequency Mode(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 14 and Figure 15)	XTS = 1, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 1, LFXT1Sx = 1, $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 1, LFXT1Sx = 2, $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(2)	XTS = 1(3)			1		pF
	Duty cycle, HF mode	XTS = 1, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V	40	50	60	%
		XTS = 1, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 16 MHz		40	50	60	
$f_{Fault,HF}$	Oscillator fault frequency (4)	XTS = 1, LFXT1Sx = 3(5)	2.2 V/3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

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Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1)

OSCILLATION ALLOWANCE vs CRYSTAL FREQUENCY
$C_{L,eff}$ = 15 pF, T_A = 25°C

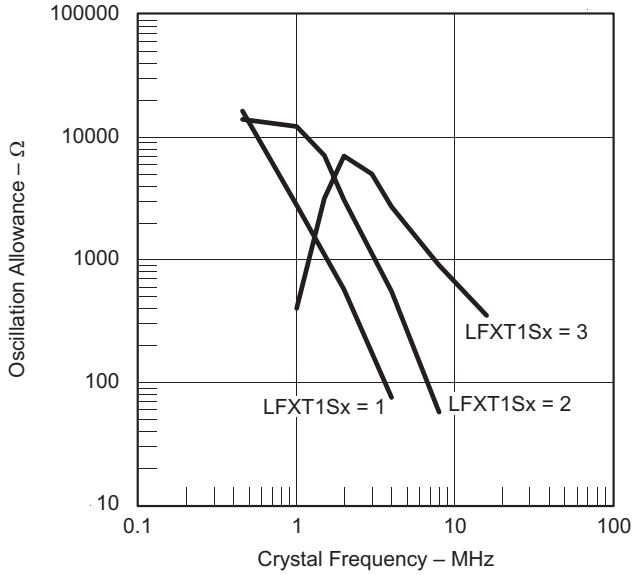

Figure 14.

OSCILLATOR SUPPLY CURRENT vs CRYSTAL FREQUENCY
$C_{L,eff}$ = 15 pF, T_A = 25°C

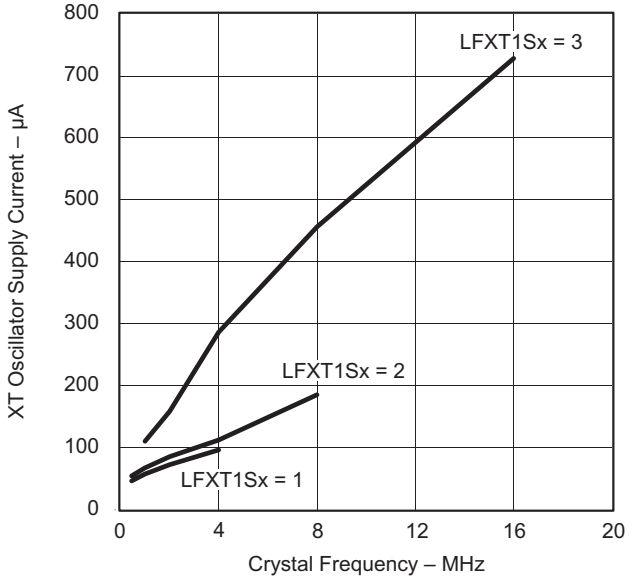

Figure 15.

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Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V/3 V	20			ns

Comparator_A+ (1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	µA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage range	CAON = 1	2.2 V/3 V	0		V_{CC} - 1	V
$V_{(Ref025)}$	(Voltage at 0.25 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	(Voltage at 0.5 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 19 and Figure 20	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage (2)		2.2 V/3 V	-30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response)}$	Response time (low-high and high-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0 (3) (see Figure 16 and Figure 17)	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1 (3) (see Figure 16 and Figure 17)	2.2 V	1.4	1.9	2.8	µs
			3 V	0.9	1.5	2.2	

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
(3) Response time measured at P2.2/CAOUT.

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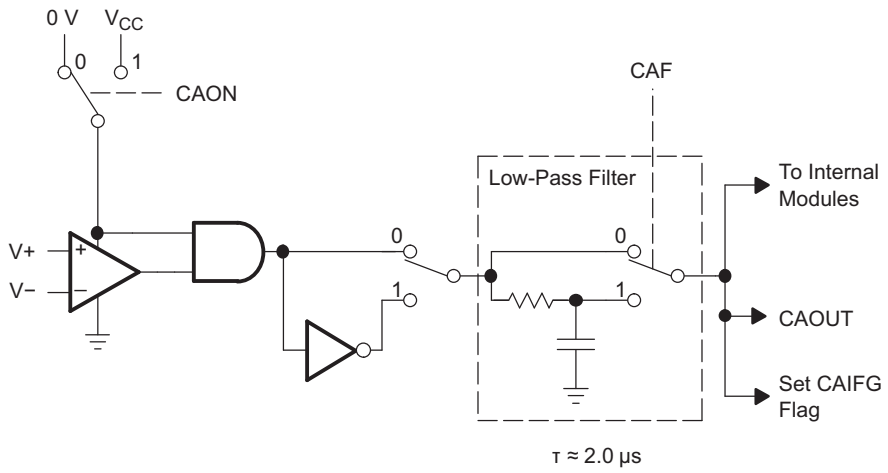

Figure 16. Comparator_A+ Module Block Diagram

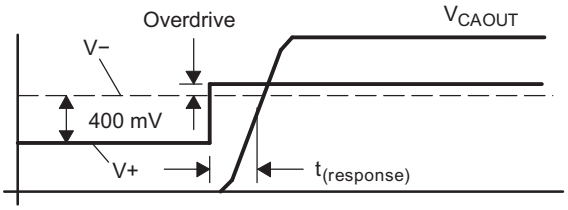

Figure 17. Overdrive Definition

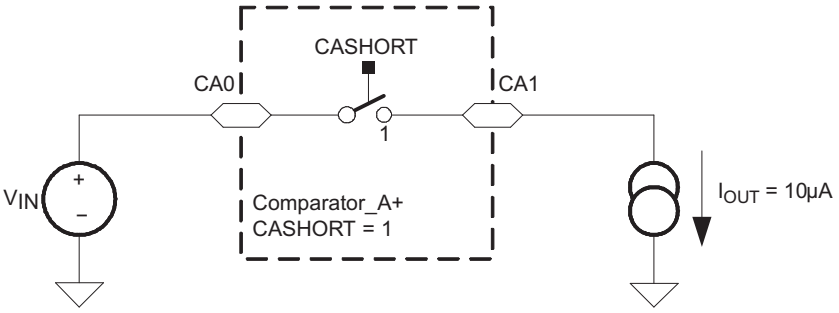

Figure 18. Comparator_A+ Short Resistance Test Condition

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Typical Characteristics - Comparator_A+

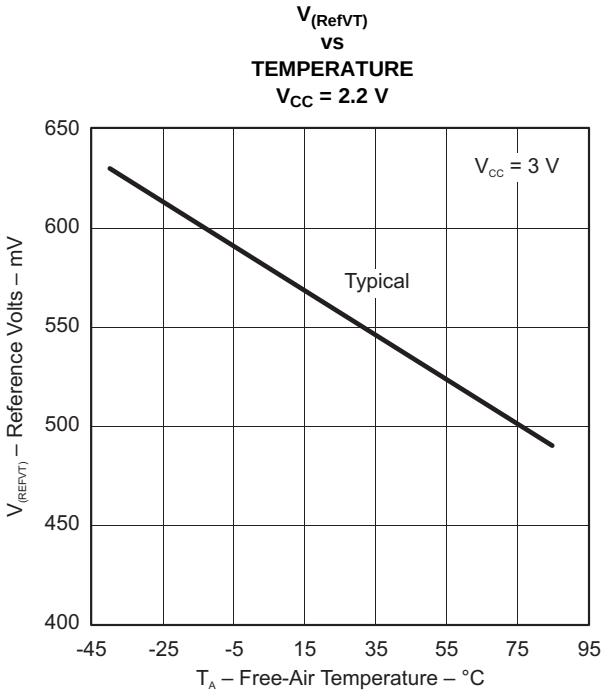

Figure 19.

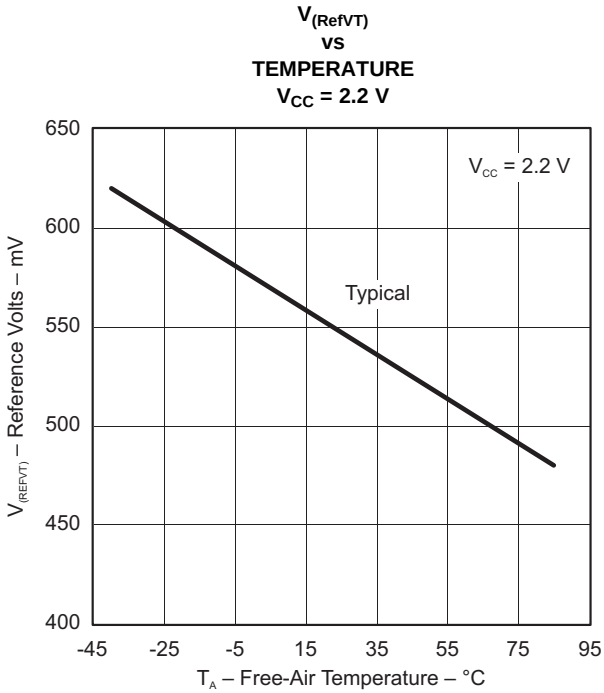

Figure 20.

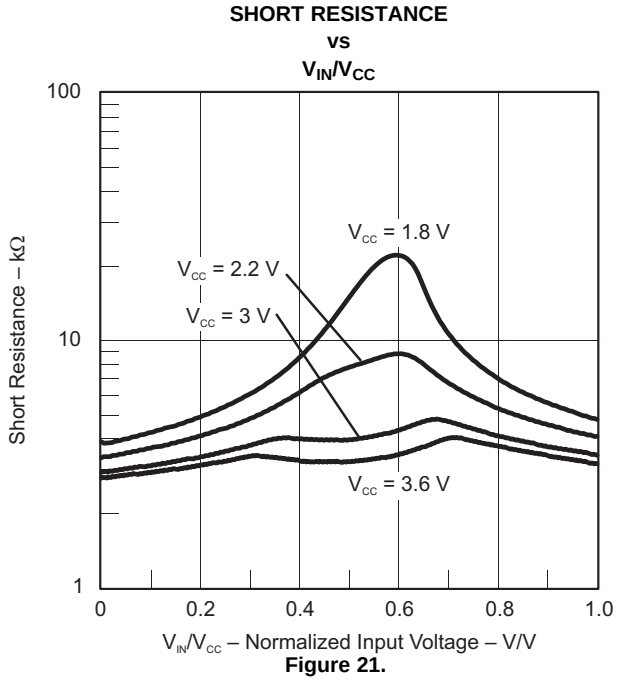

Figure 21.

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Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC\ (PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		3	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		3	7	mA
t_{CPT}	Cumulative program time (1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See (2)			30		t_{FTG}
$t_{Block,\ 0}$	Block program time for first byte or word	See (2)			25		t_{FTG}
$t_{Block,\ 1-63}$	Block program time for each additional byte or word	See (2)			18		t_{FTG}
$t_{Block,\ End}$	Block program end-sequence wait time	See (2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	See (2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	See (2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the flash controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency (1)	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{Internal}$	Internal pulldown resistance on TEST	2.2 V/3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow	25°C	6	7	V
I_{FB}	Supply current into TEST during fuse blow	25°C		100	mA
t_{FB}	Time to blow fuse	25°C		1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test and emulation features is possible, and the JTAG block is switched to bypass mode.

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APPLICATION INFORMATION

Port P1 Pin Schematic: P1.0 to P1.3, Input/Output With Schmitt Trigger

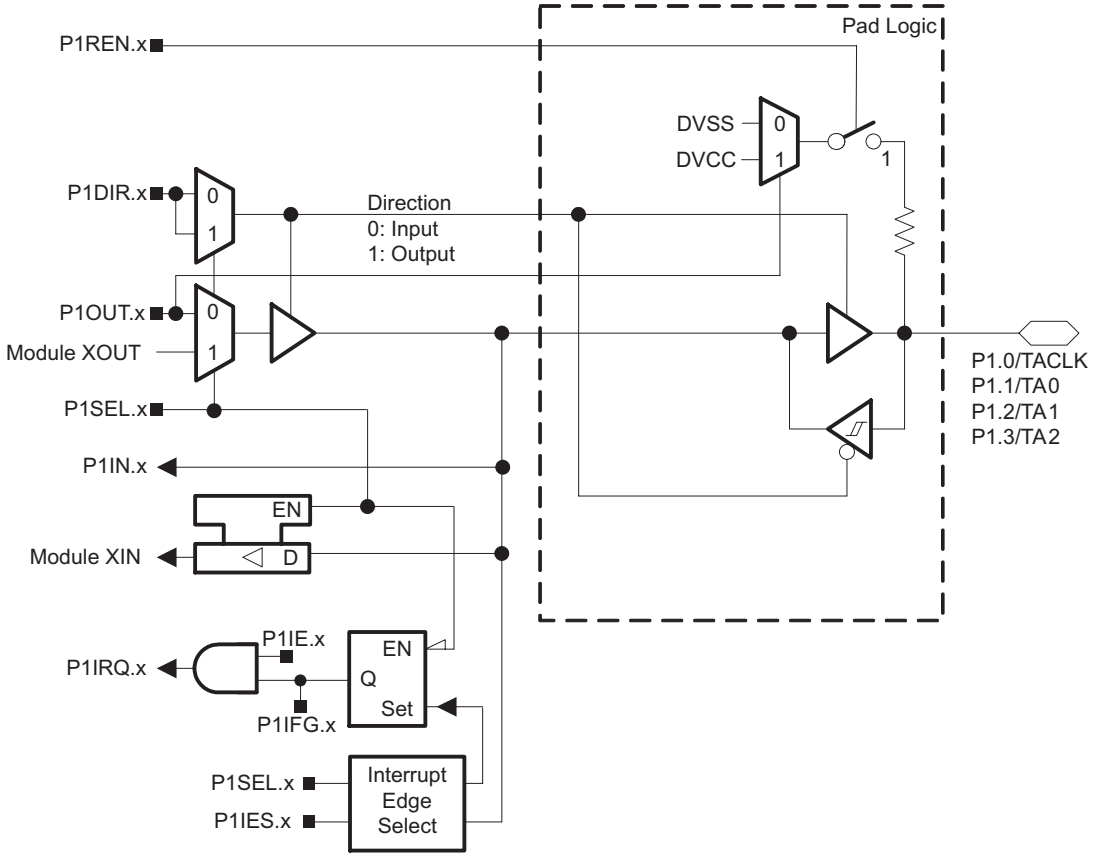

Table 17. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK	0	P1.0(1) (I/O)	I: 0; O: 1	0
		TACLK	0	1
		DVSS	1	1
P1.1/TA0	1	P1.1(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.3/TA2	3	P1.3(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1

(1) Default after reset (PUC/POR)

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Port P1 Pin Schematic: P1.4 to P1.7, Input/Output With Schmitt Trigger

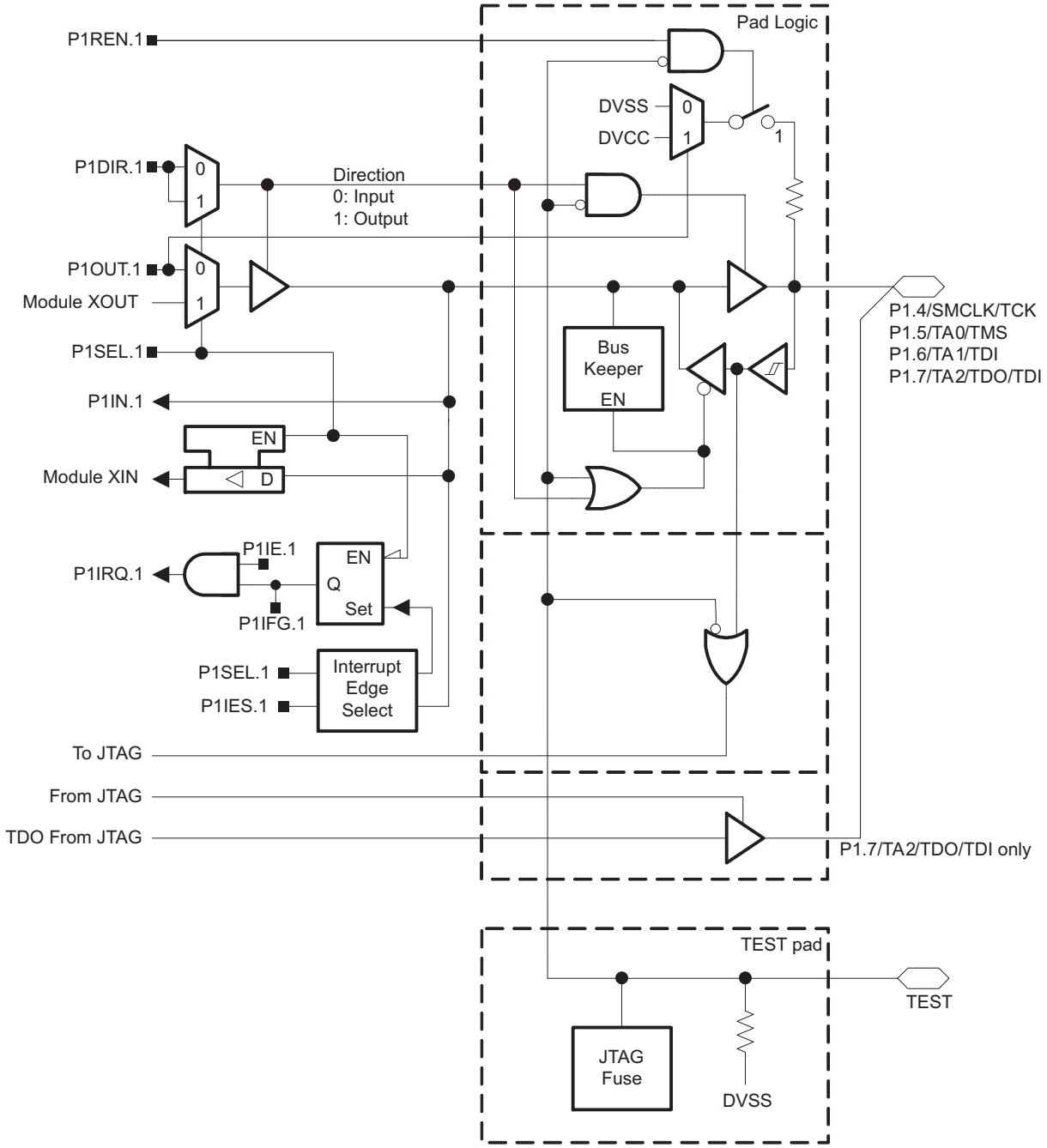

Table 18. Port P1 (P1.4 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P1DIR.x	P1SEL.x	TEST
P1.4/SMCLK/TCK	4	P1.4[2] (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK	X	X	1
P1.5/TA0/TMS	5	P1.5[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA0	1	1	0
		TMS	X	X	1
P1.6/TA1/TDI/TCLK	6	P1.6[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		TDI/TCLK[3]	X	X	1
P1.7/TA2/TDO/TDI	7	P1.7[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		TDO/TDI[3]	X	X	1

(1) X = don't care
(2) Default after reset (PUC/POR)
(3) Function controlled by JTAG

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Port P2 Pin Schematic: P2.0 to P2.5, Input/Output With Schmitt Trigger

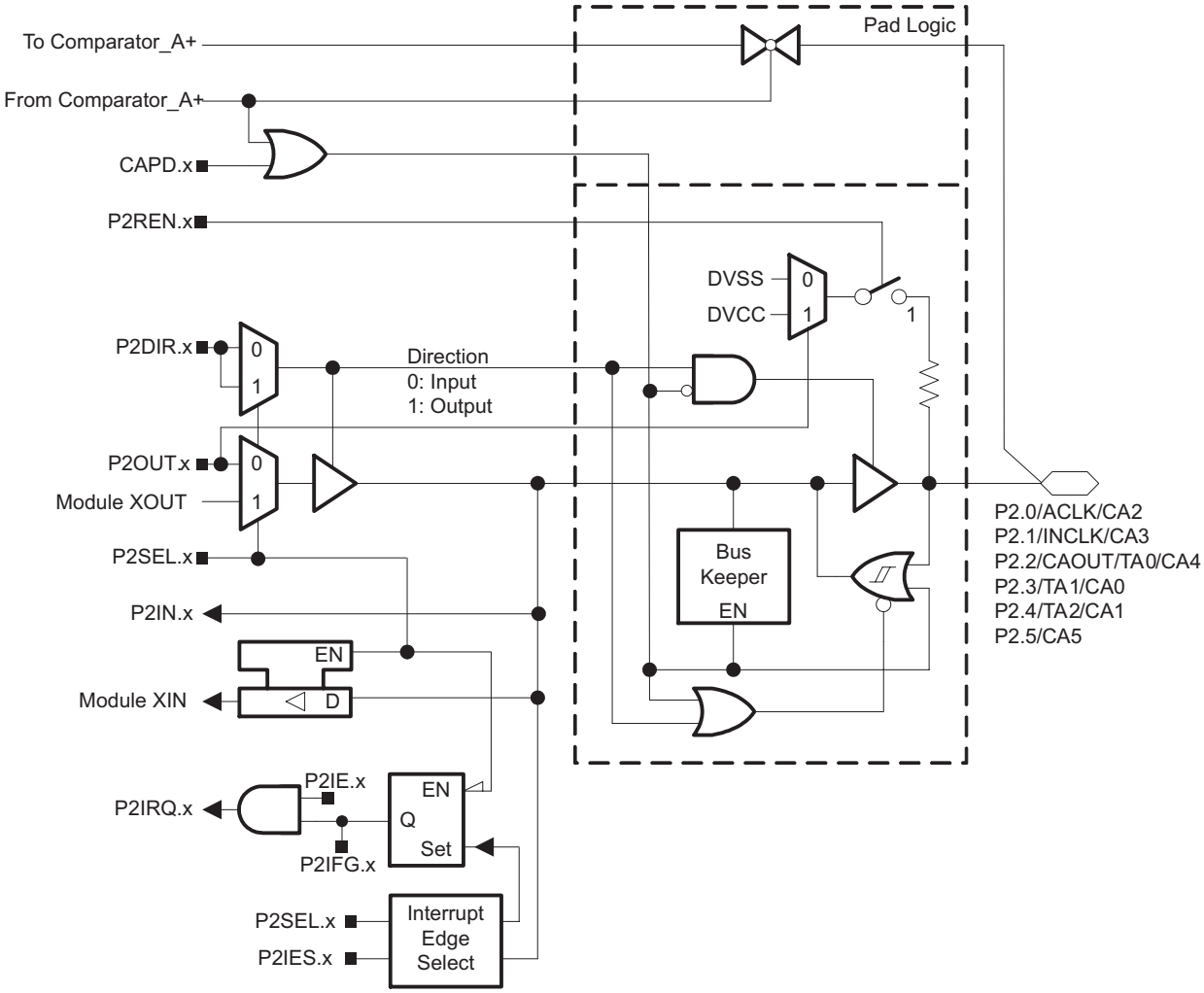

Table 19. Control Signal "From Comparator_A+"

PIN NAME	FUNCTION	SIGNAL "From Comparator_A+" = 1[(1)]					
		P2CA4	P2CA0		P2CA3	P2CA2	P2CA1
P2.0/ACLK/CA2	CA2	1	1		0	1	0
P2.1/INCLK/CA3	CA3	N/A	N/A		0	1	1
P2.2/CAOUT/TA0/CA4	CA4	N/A	N/A		1	0	0
P2.3/TA1/CA0	CA0	0	1	OR	N/A	N/A	N/A
P2.4/TA2/CA1	CA1	1	0		0	0	1
P2.5/CA5	CA5	N/A	N/A		1	0	1

(1) N/A = Not available or not applicable

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Table 20. Port P2 (P2.0 to P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P2DIR.x	P2SEL.x	CAPD.x
P2.0/ACLK/CA2	0	P2.0[2] (I/O)	I: 0; O: 1	0	0
		ACLK	1	1	0
		CA2[3]	X	X	1
P2.1/INCLK/CA3	1	P2.1[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.INCLK	0	1	0
		DVSS	1	1	0
		CA3[3]	X	X	1
P2.2/CAOUT/TA0/CA4	2	P2.2[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.CCI0B	0	1	0
		CAOUT	1	1	0
		CA4[3]	X	X	1
P2.3/TA1/CA0	3	P2.3[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		CA0[3]	X	X	1
P2.4/TA2/CA1	4	P2.4[2] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		CA1[3]	X	X	1
P2.5/CA5	5	P2.5[2] (I/O)	I: 0; O: 1	0	0
		CA5[3]	X	X	1

(1) X = don't care
(2) Default after reset (PUC/POR)
(3) Setting theCAPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currentswhen applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

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Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger and Crystal Oscillator Input

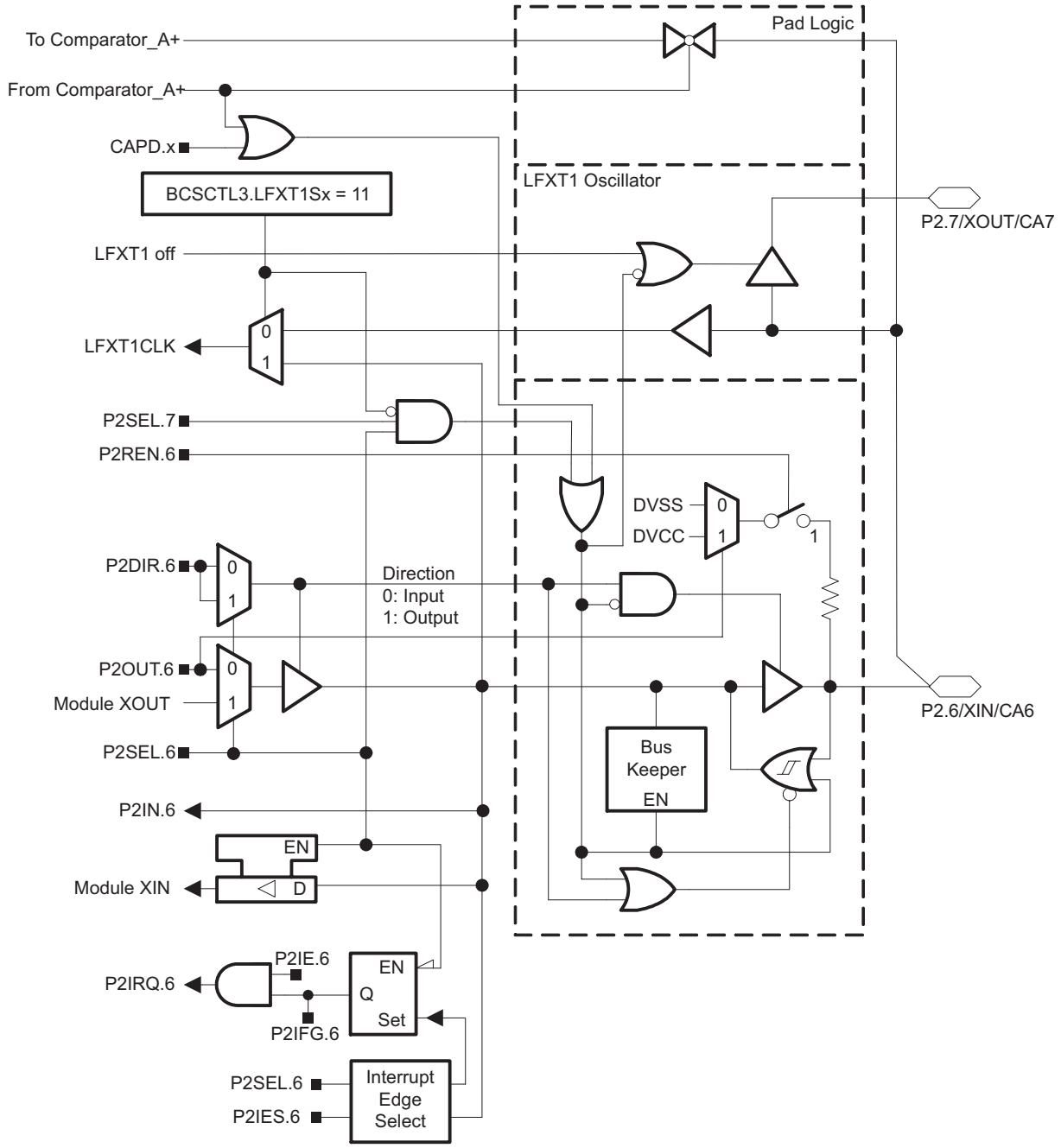

Table 21. Control Signal "From Comparator_A+"

PIN NAME	FUNCTION	SIGNAL "From Comparator_A+" = 1		
		P2CA3	P2CA2	P2CA1
P2.6/XIN/CA6	CA6	1	1	0

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Table 22. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P2DIR.x	P2SEL.x	CAPD.x
P2.6/XIN/CA6	6	P2.6 (I/O)	I: 0; O: 1	0	0
		XIN[2]	X	1	0
		CA6[3]	X	X	1

(1) X = don't care
(2) Default after reset (PUC/POR)
(3) Setting theCAPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currentswhen applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

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Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger and Crystal Oscillator Output

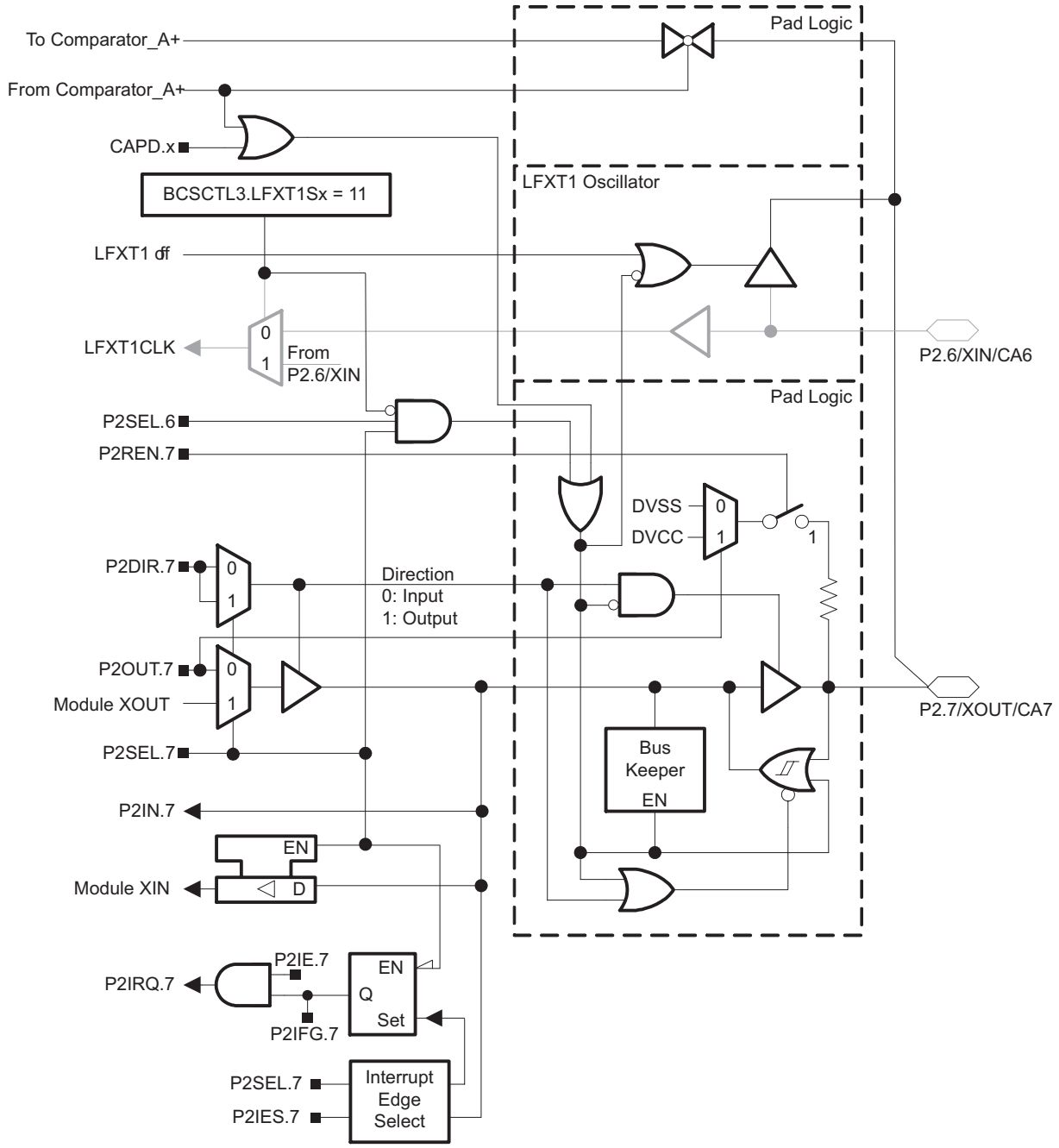

Table 23. Control Signal "From Comparator_A+"

PIN NAME	FUNCTION	SIGNAL "From Comparator_A+" = 1		
		P2CA3	P2CA2	P2CA1
P2.7/XOUT/CA7	CA7	1	1	1

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Table 24. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P2DIR.x	P2SEL.x	CAPD.x
P2.7/XOUT/CA7	6	P2.7 (I/O)	I: 0; O: 1	0	0
		XOUT[2][3]	X	1	0
		CA7[4]	X	X	1

(1) X = don't care
(2) Default after reset (PUC/POR)
(3) If the pin XOUT/P2.7/CA7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.
(4) Setting theCAPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currentswhen applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

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JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 22). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

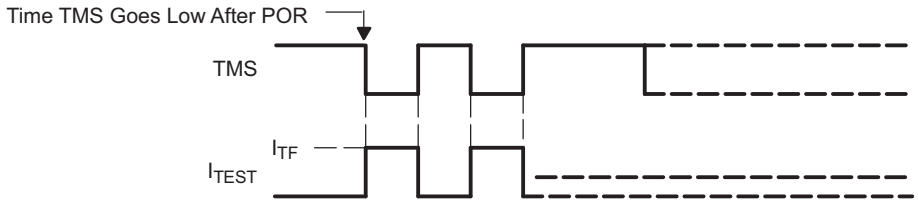

Figure 22. Fuse Check Mode Current

NOTE

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the Bootstrap Loader section for more information.

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REVISION HISTORY

Literature Number	Summary
SLAS439	PRODUCT PREVIEW release
SLAS439A	PRODUCTION DATA release
SLAS439B	Corrected instruction cycle time to 62.5ns, pg 1. Updated Figure 1, pg 12. Updated Figures 2 and 3, pg 13. R_{Pull} unit corrected from Ω to kΩ, pg 15. MAX load current specification and Note 3 removed from "outputs" table, pg 16. MIN and MAX percentages for "calibrated DCO frequencies - tolerance over supply voltage VCC" corrected from 2.5% to 3% to match the specified frequency ranges., pg 22.
SLAS439C	MSP430x21x1T production data sheet release. 105°C characterization results added.
SLAS439D	Corrected Timer_A2 to Timer_A3 and added TACCR2 to Interrupt Flag column in "interrupt vector addresses", pg 6
SLAS439E	Changed T_{stg}, Programmed device, to -40°C to 150°C in Absolute Maximum Ratings. Corrected Test Conditions for OA_{HF} row and and Duty Cycle row in Crystal Oscillator LFXT1, High-Frequency Mode.
SLAS439F	Changed T_{stg}, Programmed device, to -55°C to 150°C in Absolute Maximum Ratings.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2101IDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F2101	Samples
MSP430F2101IDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F2101	Samples
MSP430F2101IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F2101	Samples
MSP430F2101IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F2101	Samples
MSP430F2101IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F2101	Samples
MSP430F2101IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F2101	Samples
MSP430F2101IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 2101	Samples
MSP430F2101IRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 2101	Samples
MSP430F2101TDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	4F2101T	Samples
MSP430F2101TDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	4F2101T	Samples
MSP430F2101TDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M430F2101T	Samples
MSP430F2101TDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M430F2101T	Samples
MSP430F2101TPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	4F2101T	Samples
MSP430F2101TPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	4F2101T	Samples
MSP430F2101TRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M430F 2101T	Samples
MSP430F2111IDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F2111	Samples
MSP430F2111IDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F2111	Samples
MSP430F2111IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F2111	Samples
MSP430F2111IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F2111	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2111IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F2111	Samples
MSP430F2111IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F2111	Samples
MSP430F2111IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 2111	Samples
MSP430F2111IRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 2111	Samples
MSP430F2111TDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	4F2111T	Samples
MSP430F2111TDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M430F2111T	Samples
MSP430F2111TDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M430F2111T	Samples
MSP430F2111TPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	4F2111T	Samples
MSP430F2111TPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	4F2111T	Samples
MSP430F2111TRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M430F 2111T	Samples
MSP430F2111TRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M430F 2111T	Samples
MSP430F2121IDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F2121	Samples
MSP430F2121IDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F2121	Samples
MSP430F2121IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F2121	Samples
MSP430F2121IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F2121	Samples
MSP430F2121IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F2121	Samples
MSP430F2121IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F2121	Samples
MSP430F2121IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 2121	Samples
MSP430F2121IRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 2121	Samples
MSP430F2121TDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	4F2121T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2121TDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M430F2121T	Samples
MSP430F2121TDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M430F2121T	Samples
MSP430F2121TPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	4F2121T	Samples
MSP430F2121TPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	4F2121T	Samples
MSP430F2121TRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M430F 2121T	Samples
MSP430F2131IDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F2131	Samples
MSP430F2131IDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F2131	Samples
MSP430F2131IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F2131	Samples
MSP430F2131IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F2131	Samples
MSP430F2131IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F2131	Samples
MSP430F2131IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F2131	Samples
MSP430F2131IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 2131	Samples
MSP430F2131IRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 2131	Samples
MSP430F2131TDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	4F2131T	Samples
MSP430F2131TDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	4F2131T	Samples
MSP430F2131TDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M430F2131T	Samples
MSP430F2131TDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M430F2131T	Samples
MSP430F2131TPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	4F2131T	Samples
MSP430F2131TPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	4F2131T	Samples
MSP430F2131TRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M430F 2131T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2131TRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M430F 2131T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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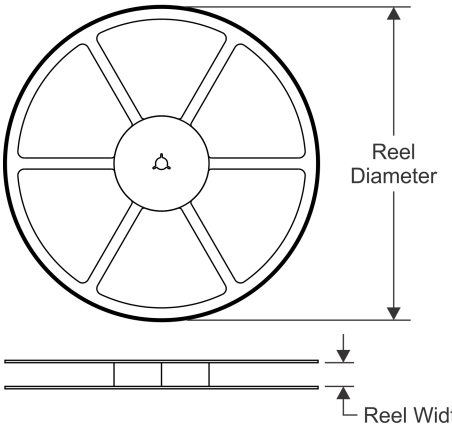
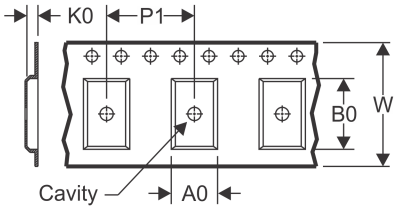
TAPE AND REEL INFORMATION

REEL DIMENSIONS

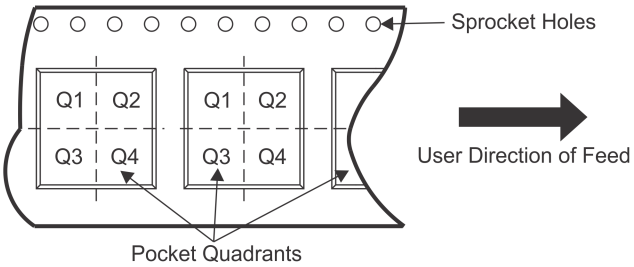


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

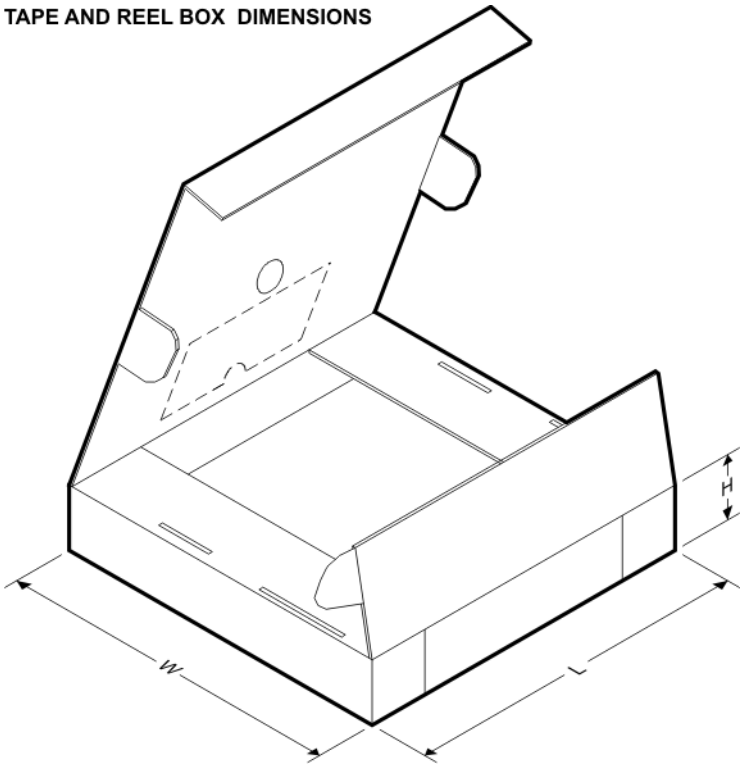


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2101IDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2101IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F2101IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2101IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2101IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2101TDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2101TDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F2101TPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2101TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2111IDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2111IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F2111IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2111IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2111IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2111TDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2111TDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F2111TPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2111TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2111TRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2121IDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2121IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F2121IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2121IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2121IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2121TDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2121TDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F2121TPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2121TRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2131IDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2131IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F2131IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
MSP430F2131IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2131IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2131TDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2131TDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F2131TPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2131TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2131TRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

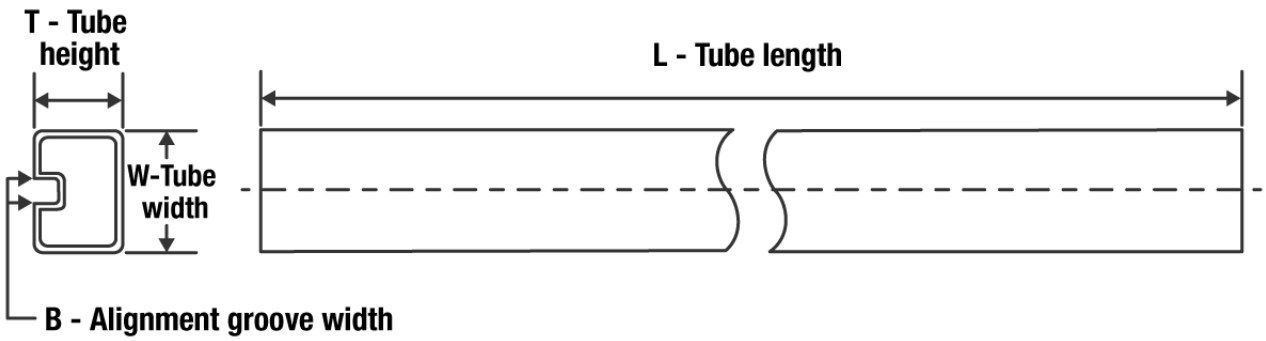
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2101IDGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
MSP430F2101IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F2101IPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MSP430F2101IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSP430F2101IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F2101TDGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
MSP430F2101TDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F2101TPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MSP430F2101TRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSP430F2111IDGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
MSP430F2111IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F2111IPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MSP430F2111IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSP430F2111IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F2111TDGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
MSP430F2111TDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F2111TPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MSP430F2111TRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSP430F2111TRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F2121IDGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
MSP430F2121IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F2121IPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MSP430F2121IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSP430F2121IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F2121TDGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
MSP430F2121TDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F2121TPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MSP430F2121TRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F2131IDGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
MSP430F2131IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F2131IPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MSP430F2131IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSP430F2131IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F2131TDGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
MSP430F2131TDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F2131TPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MSP430F2131TRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSP430F2131TRGET	VQFN	RGE	24	250	210.0	185.0	35.0

TUBE

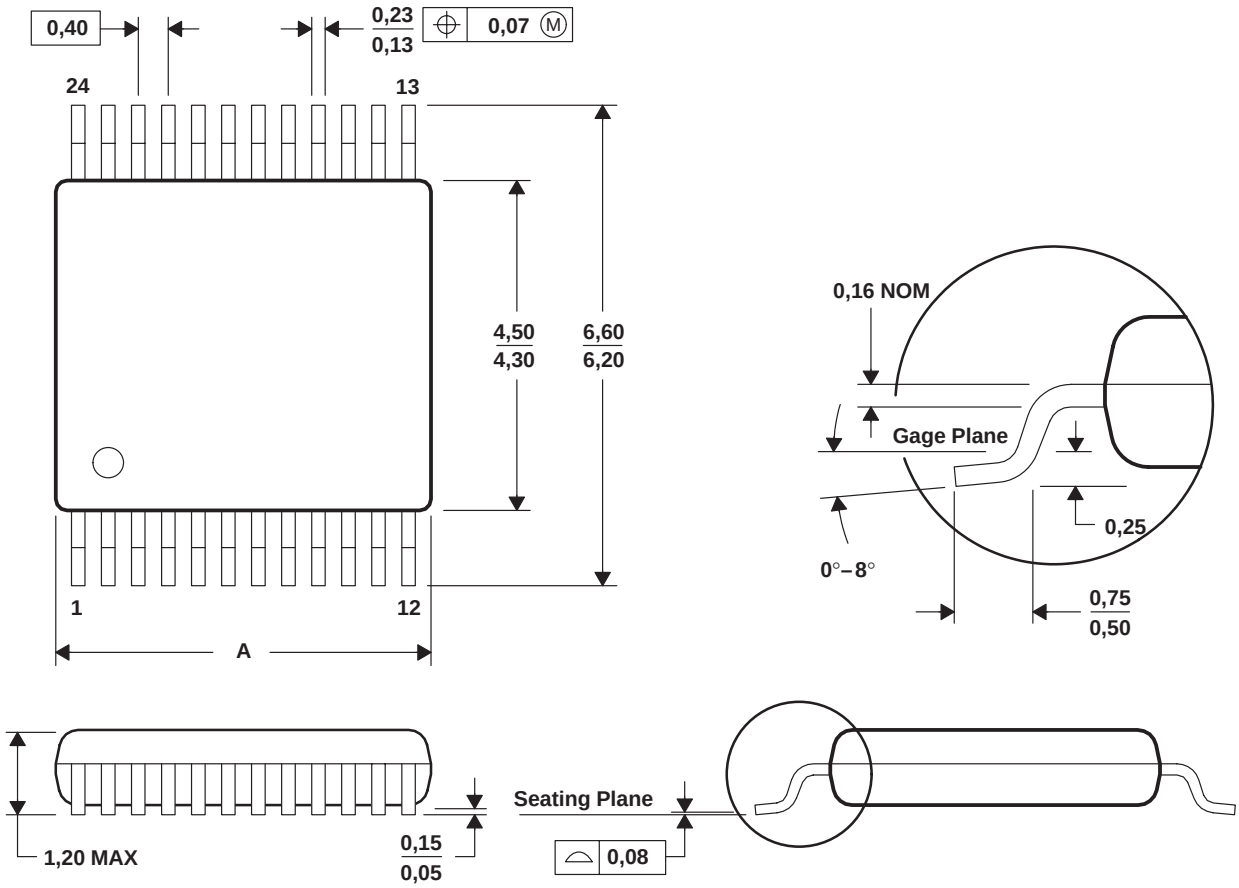


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430F2101IDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F2101IDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F2101IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F2101TDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F2101TDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F2101TPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F2111IDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F2111IDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F2111IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F2111TDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F2111TPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F2121IDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F2121IDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F2121IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F2121TDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F2121TPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F2131IDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F2131IDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F2131IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F2131TDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F2131TDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F2131TPW	PW	TSSOP	20	70	530	10.2	3600	3.5

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

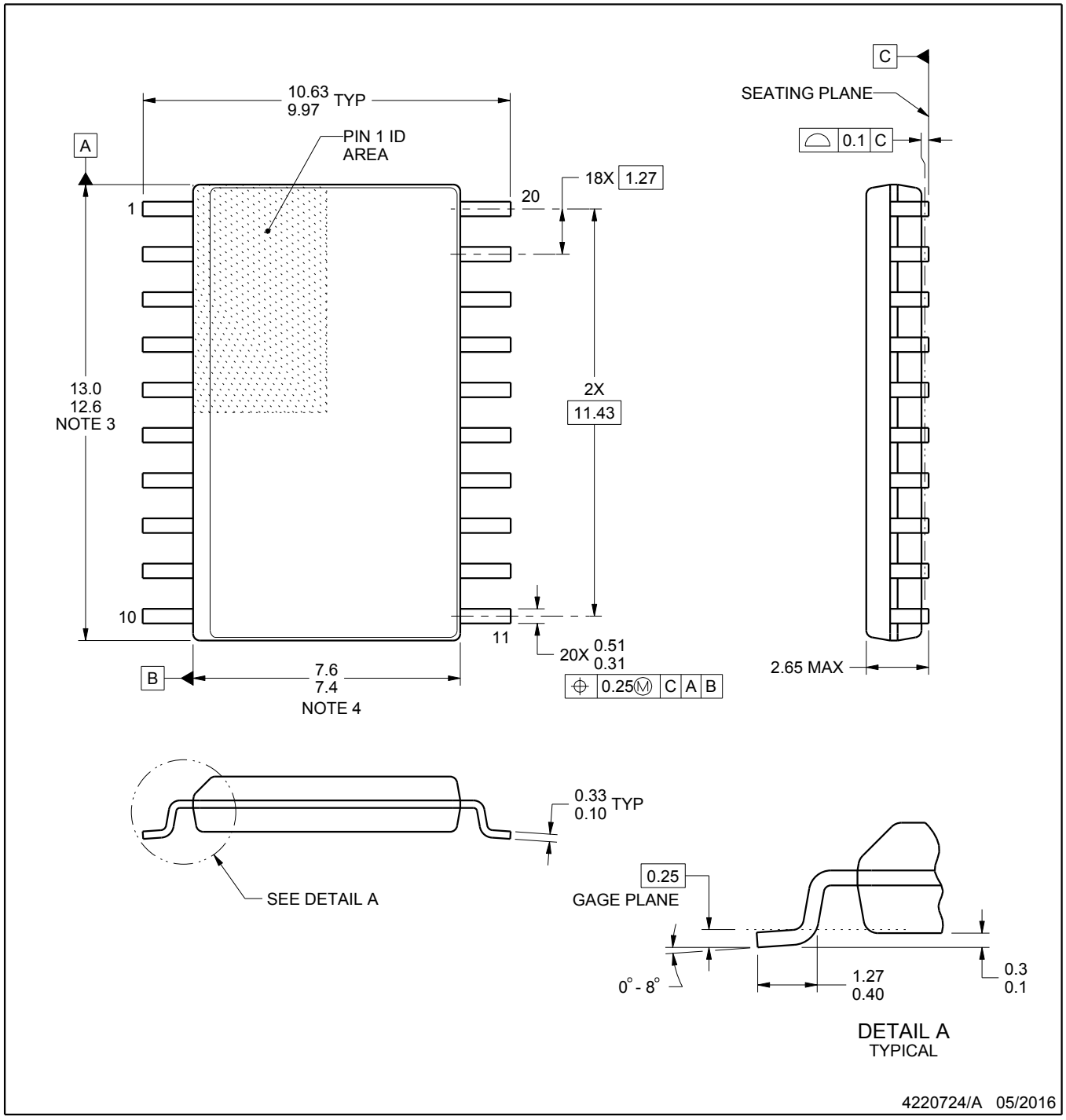
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

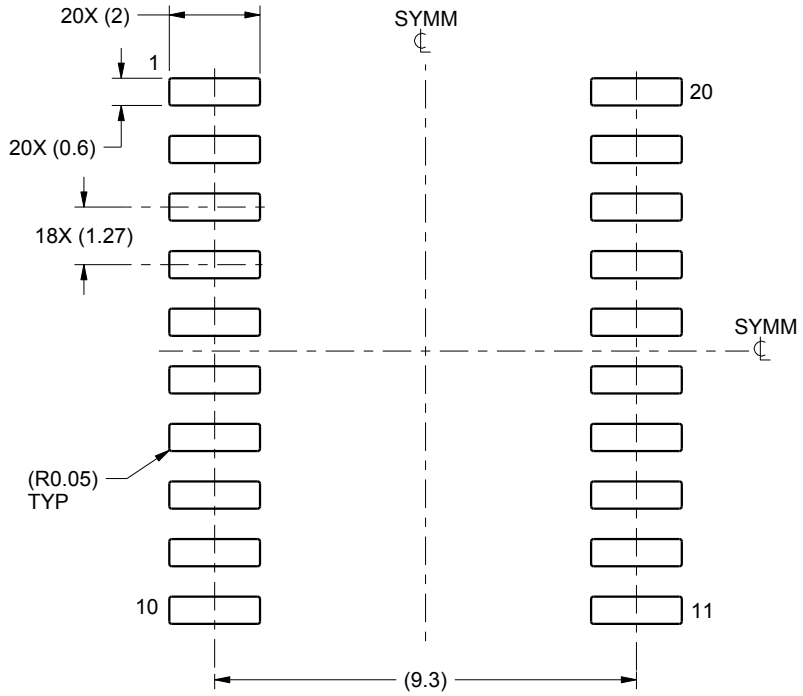
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

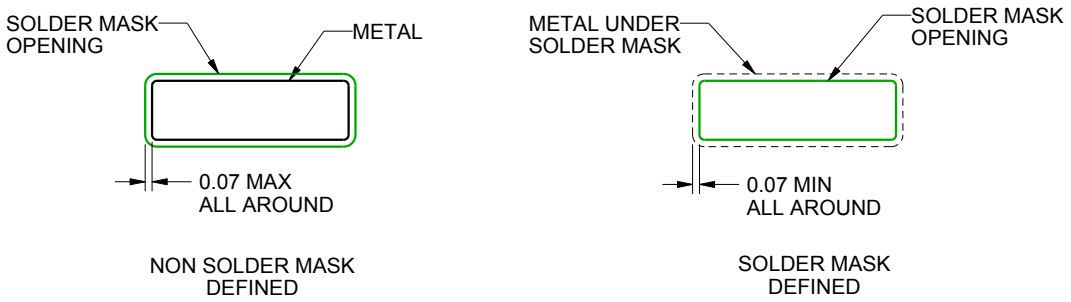


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

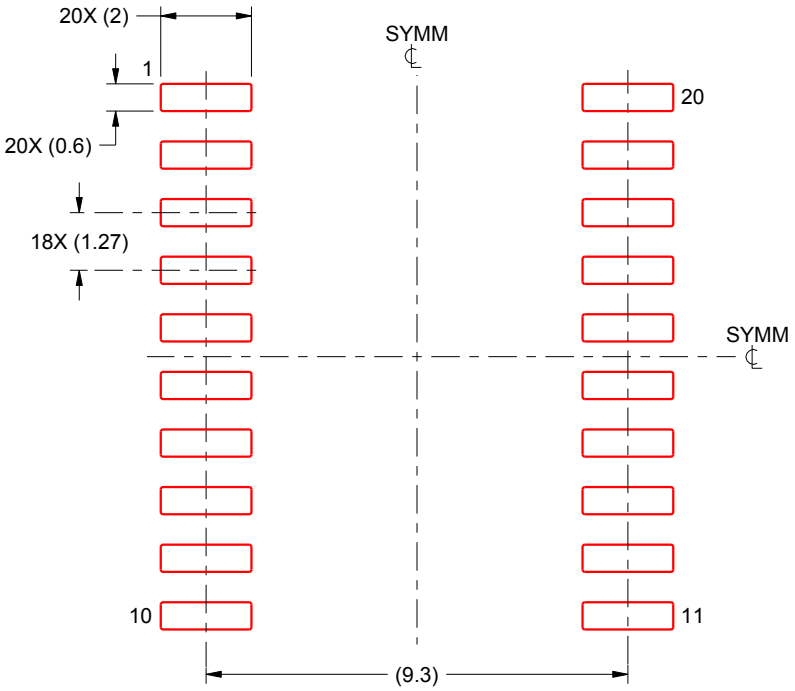


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

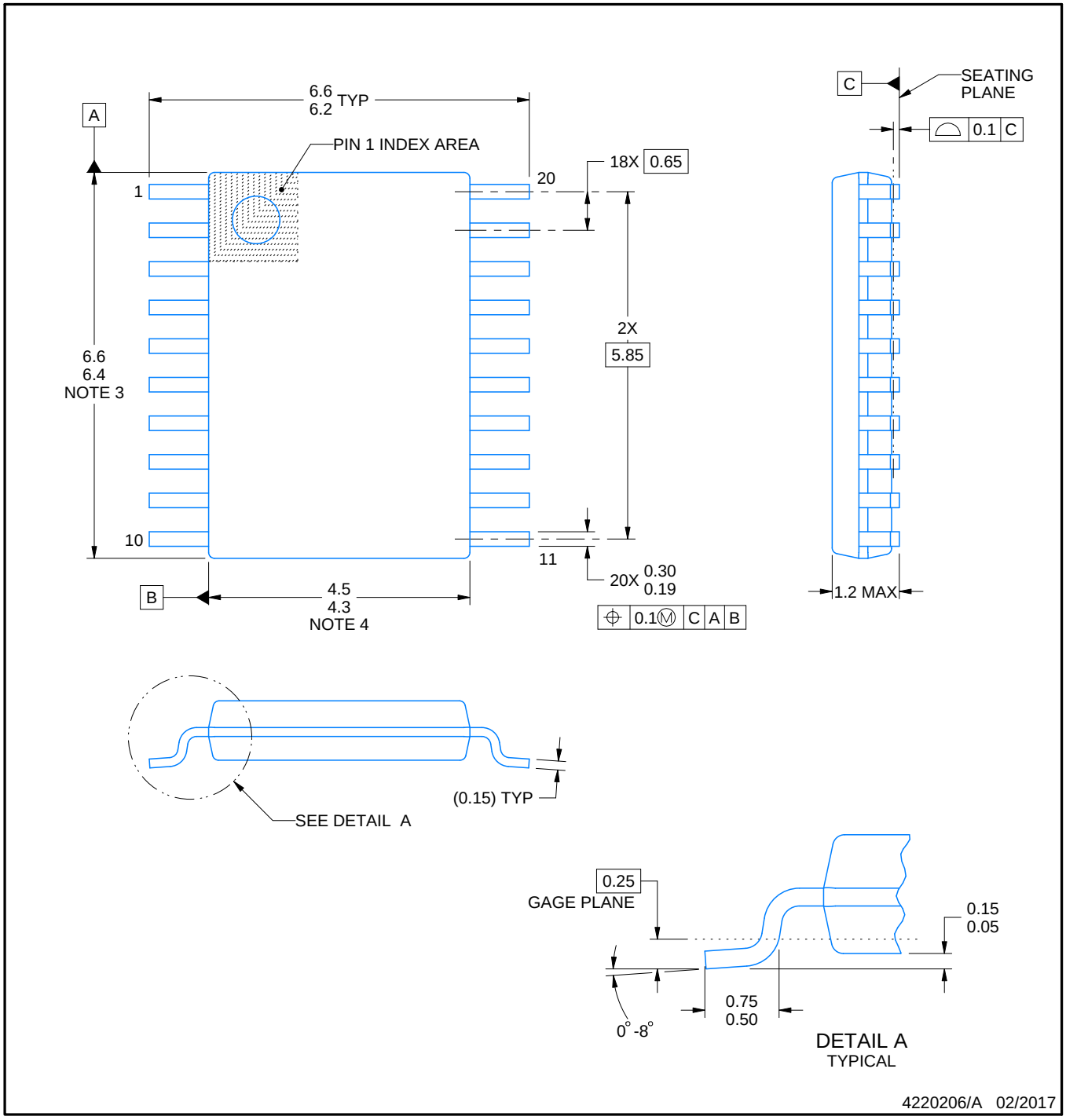


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

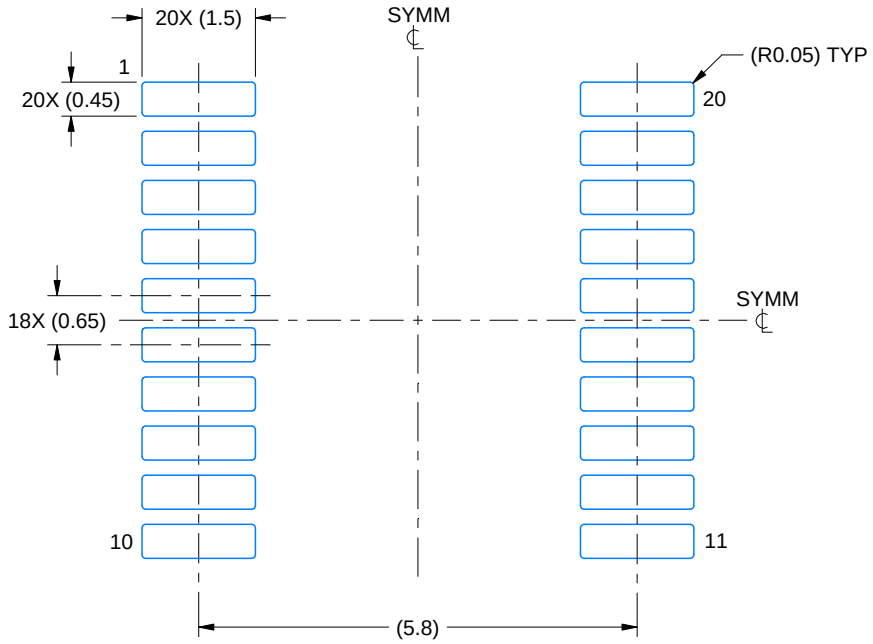
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

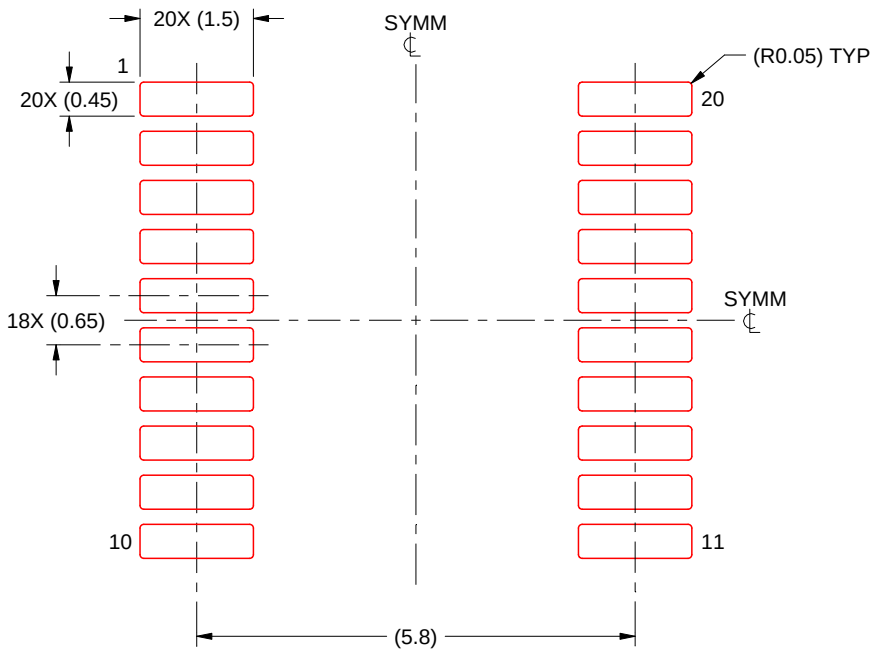
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



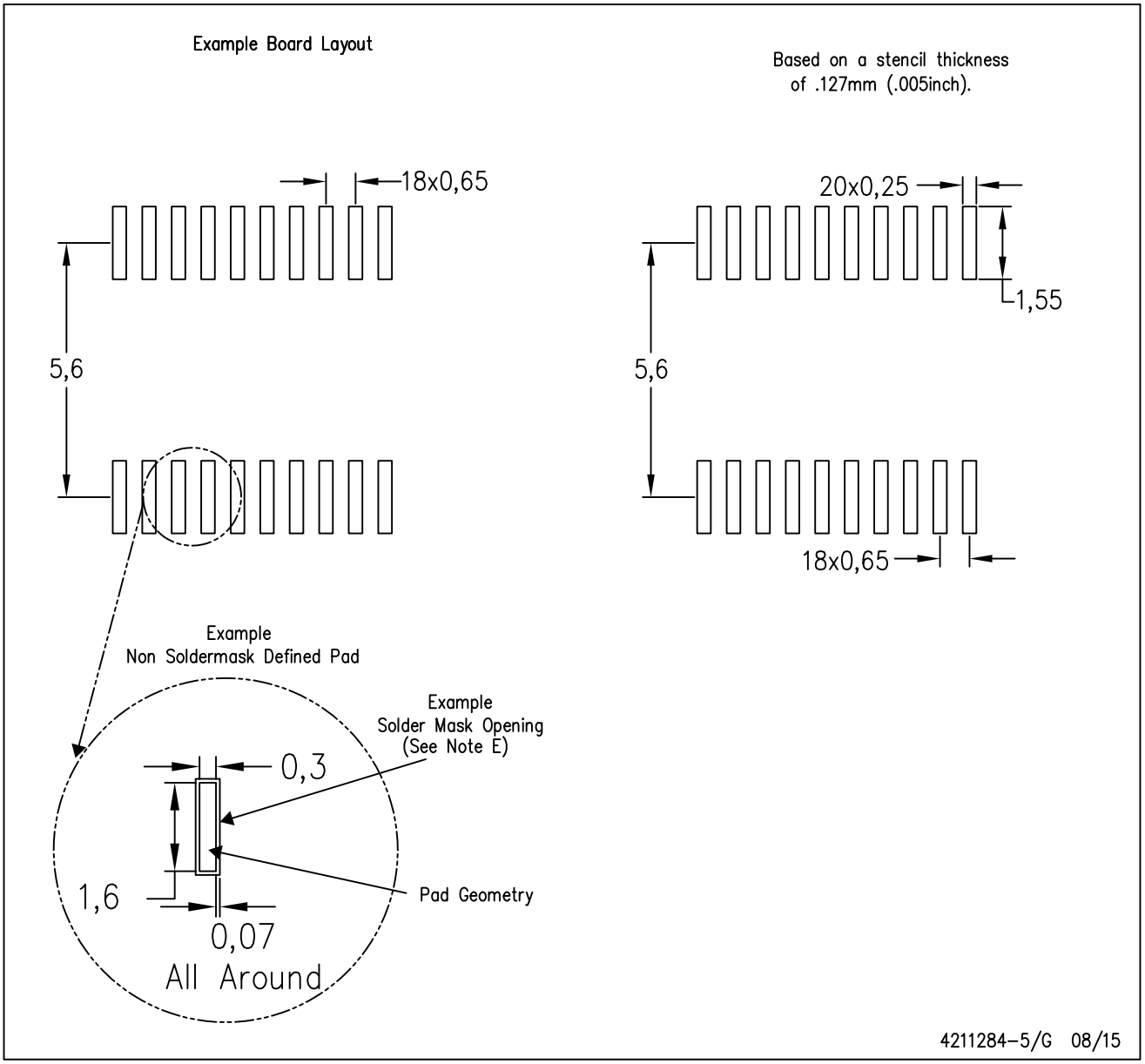
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

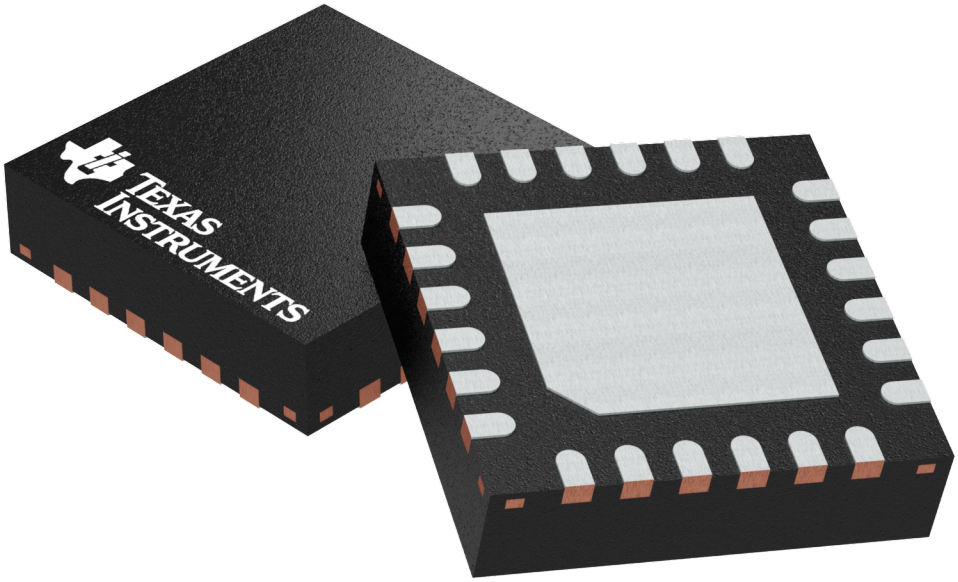
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



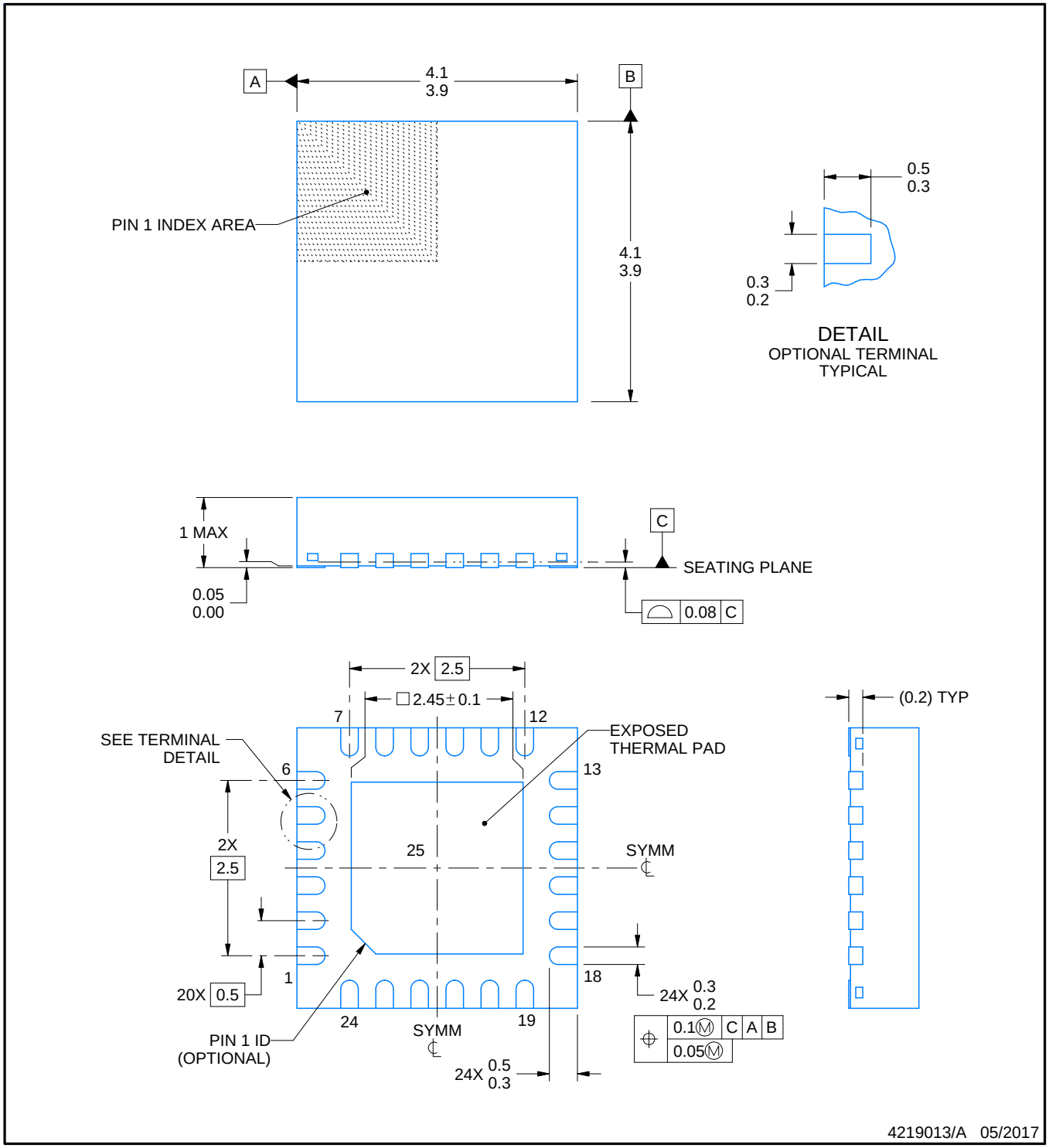
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

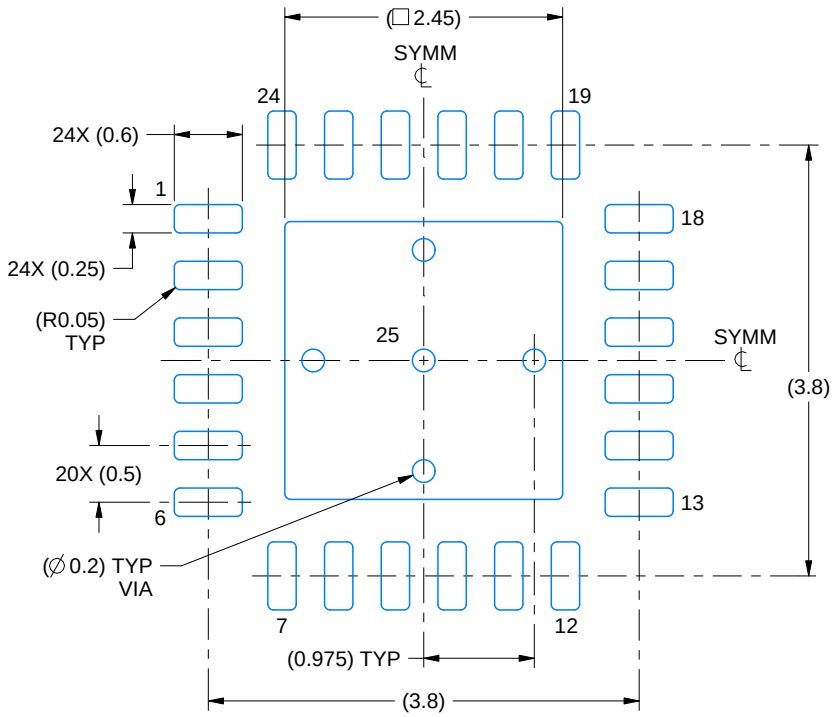


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

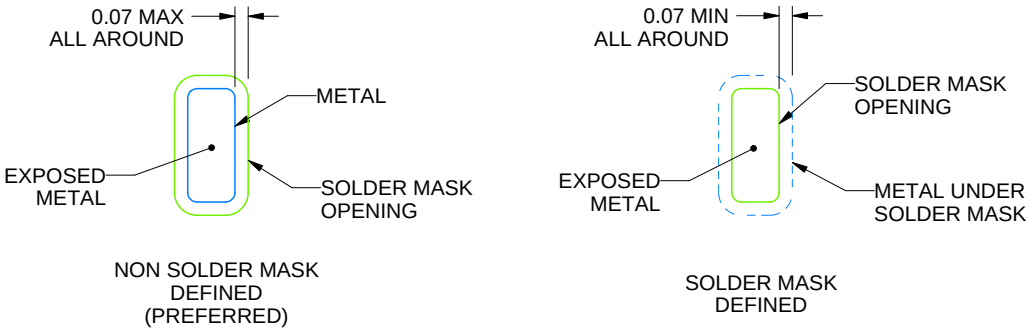


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

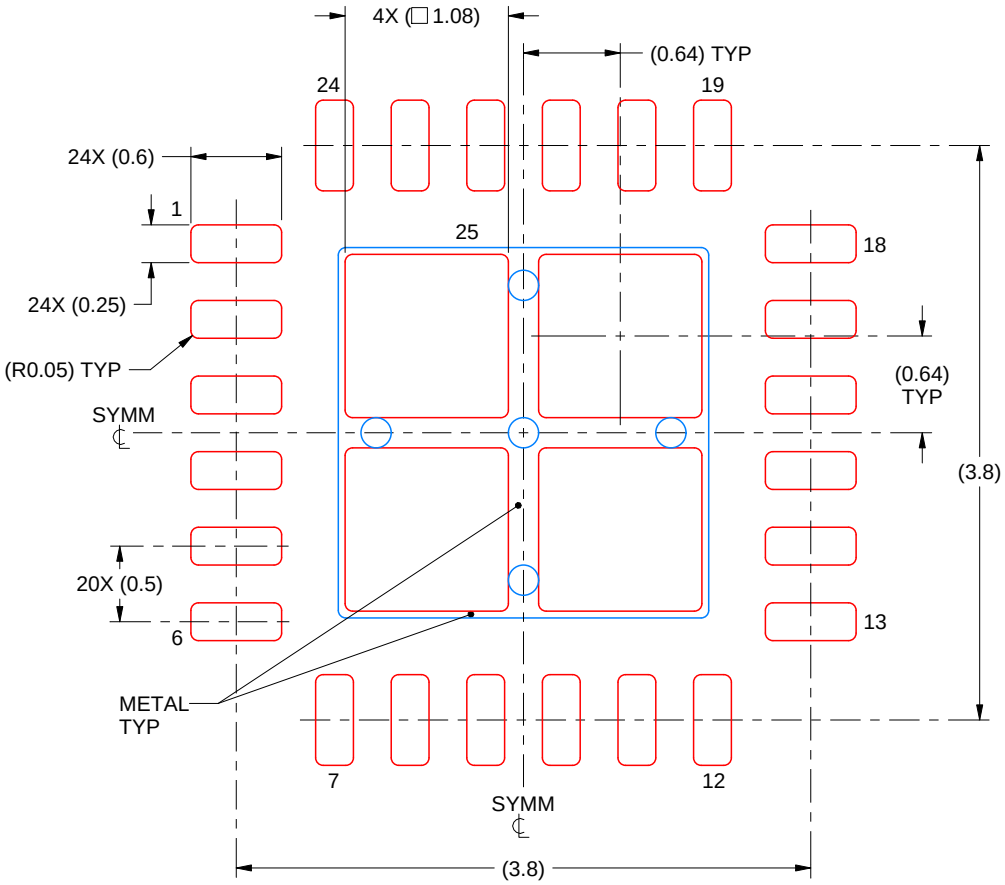


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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