16-Channel, 12-Bit PWM LED Driver with 6-Bit Dot Correction

FEATURES

- 16 Channels, Constant Current Sink Output
- 40-mA Capability (Constant Current Sink)
- 12-Bit (4096 Steps) Grayscale PWM Control
- 6-Bit (64 Steps) Dot Correction
- LED Power-Supply Voltage up to 17 V
- V_{CC} = 3.0 V to 5.5 V
- Constant Current Accuracy:
  - Channel-to-Channel = ±1% (typ)
  - Device-to-Device = ±2% (typ)
- 30-MHz Data Transfer Rate
- 33-MHz Grayscale PWM Clock
- Extended Serial Interface
- CMOS Level I/O
- Schmitt Buffer Input
- Readable Error Information:
  - Continuous Base LED Open Detection (LOD)
  - Thermal Error Flag (TEF)
- Noise Reduction:
  - 4-Channel Grouped Delay
- Operating Temperature: –40°C to +85°C

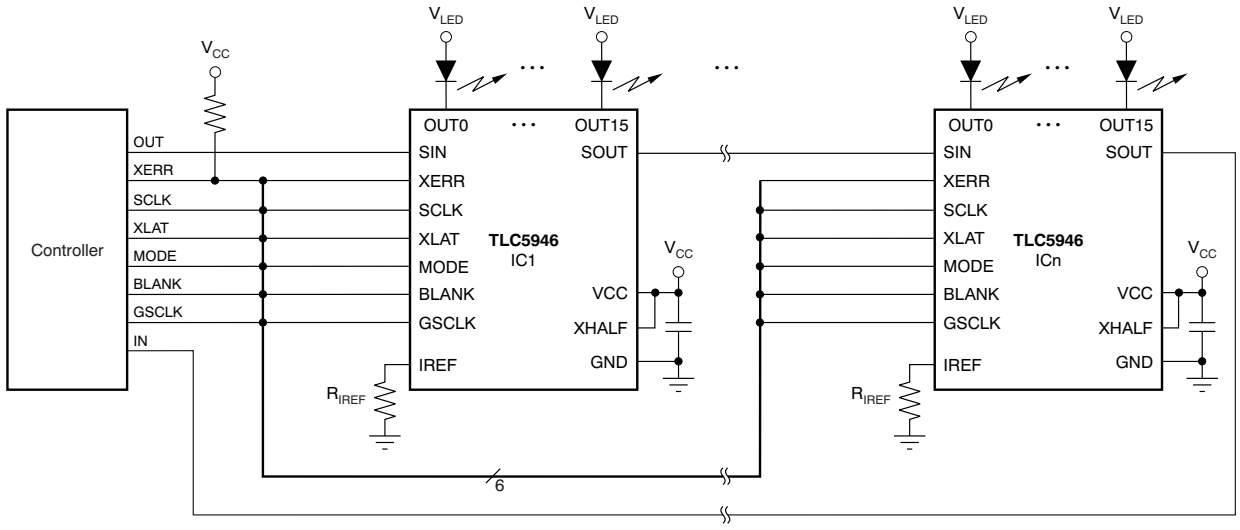
APPLICATIONS

- Monochrome, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Backlighting

DESCRIPTION

The TLC5946 is a 16-channel, constant current sink LED driver. Each channel is individually adjustable with 4096 pulse-width modulated (PWM) steps and 64 constant current sink steps for dot correction. The dot correction adjusts the brightness variations between LEDs. Both grayscale control and dot correction are accessible via a serial interface. The maximum current value of all 16 channels can be set by a single external resistor.

The TLC5946 has two error information circuits: one for LED open detection (LOD), and a thermal error flag (TEF). LOD detects a broken or disconnected LED during display period. TEF indicates an over-temperature condition.



Typical Application Circuit (Multiple Daisy-Chained TLC5946s)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER
TLC5946	TSSOP-28	TLC5946PW
TLC5946	HTSSOP-28 PowerPAD™	TLC5946PWP
TLC5946	5 mm × 5 mm QFN-32	TLC5946RHB

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC5946	UNIT
V_{CC}	Supply voltage: V_{CC}		–0.3 to +6.0	V
I_{OUT}	Output current (dc)	OUT0 to OUT15	50	mA
		XERR	6	mA
V_{IN}	Input voltage range: SIN, SCLK, GSCLK, XLAT, BLANK, MODE, XHALF, IREF		–0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltage range	SOUT, XERR	–0.3 to V_{CC} + 0.3	V
		OUT0 to OUT15	–0.3 to +18	V
$T_{J(ABS)}$	Operating temperature range: junction temperature		–40 to +150	°C
T_{STG}	Storage temperature range		–55 to +150	°C
	ESD rating	Human body model (HBM), JEDEC JESD22-A114	2	kV
		Charged device model (CDM), JEDEC JESD22-C101	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	OPERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
TSSOP-28	16.21 mW/°C	2026 mW	1296 mW	1053 mW
HTSSOP-28 with PowerPAD soldered(1)	31.67 mW/°C	3958 mW	2533 mW	2058 mW
HTSSOP-28 with PowerPAD not soldered(2)	16.21 mW/°C	2026 mW	1296 mW	1053 mW
QFN-32(3)	27.86 mW/°C	3482 mW	2228 mW	1811 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2 oz. copper. For more information, see SLMA002 (available for download at www.ti.com).
(2) With PowerPAD not soldered onto copper area on PCB.
(3) The package thermal impedance is calculated in accordance with JESD51-5.

RECOMMENDED OPERATING CONDITIONS

At T_A= –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5946			UNIT
			MIN	NOM	MAX	
DC Characteristics: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output	OUT0 to OUT15			17	V
V_{IH}	High-level input voltage		0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–1	mA
I_{OL}	Low-level output current	SOUT			1	mA
		XERR			5	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15, DC = 3Fh	4		40	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C
AC Characteristics: V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (sclk)}$	Data shift clock frequency	SCLK, XHALF = H			30	MHz
		GSCLK, XHALF = L			15	MHz
$f_{CLK\ (gsclk)}$	Grayscale control clock frequency	GSCLK			33	MHz
T_{WH0} / T_{WL0}	SCLK pulse duration	SCLK = H/L (see Figure 12)	10			ns
T_{WH1} / T_{WL1}	GSCLK pulse duration	GSCLK = H/L (see Figure 12)	10			ns
T_{WH2}	XLAT pulse duration	XLAT = H (see Figure 12)	20			ns
T_{WH3}	BLANK pulse duration	BLANK = H (see Figure 12)	20			ns
T_{SU0}	Setup time	SIN–SCLK↑ (see Figure 12)	5			ns
T_{SU1}		XLAT↑–SCLK↑ (see Figure 38, Figure 12)	100			ns
T_{SU2}		MODE–SCLK↑ (see Figure 12)	10			ns
T_{SU3}		MODE–XLAT↑ (see Figure 12)	10			ns
T_{SU4}		BLANK↓–GSCLK↑ (see Figure 12)	10			ns
T_{SU5}		XLAT↑–GSCLK↑ (see Figure 12)	30			ns
T_{SU6}		SCLK↓–XLAT↑ (see Figure 38, Figure 12)	10			ns
T_{H0}	Hold time	SIN–SCLK↑ (see Figure 12)	3			ns
T_{H1}		MODE–SCLK↓ (see Figure 12)	10			ns
T_{H2}		MODE–XLAT↑ (see Figure 12)	100			ns
AC Characteristics: V_{CC} = 3 V to 5.5 V, XHALF = L						
T_{WL2}	XLAT pulse duration	XLAT = L (see Figure 38)	20			ns
T_{SU7}	Setup time	BLANK↑–XLAT↑ (see Figure 38)	20			ns
T_{H3}	Hold time	BLANK↓–XLAT↓ (see Figure 38)	20			ns

ELECTRICAL CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V, T_A = –40°C to +85°C, and R_{IREF} = 1.3kΩ. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5946			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA at SOUT	V_{CC} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA at SOUT			0.4	V
		I_{OL} = 5 mA at XERR			0.5	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at BLANK, XHALF, GSCLK, SCLK, SIN, XLAT, and MODE pins	–1		1	µA
I_{CC1}	Supply current	No data transfer, all OUTn = OFF, V_{OUTn} = 1 V, DCn = 3Fh, R_{IREF} = 13 kΩ		0.9	3	mA
I_{CC2}		No data transfer, all OUTn = OFF, V_{OUTn} = 1 V, DCn = 3Fh, R_{IREF} = 2.7 kΩ		4	8	mA
I_{CC3}		Data transfer at 30 MHz, all OUTn = ON, V_{OUTn} = 1 V, DCn = 3Fh, R_{IREF} = 2.7 kΩ		13	25	mA
I_{CC4}		Data transfer at 30 MHz, all OUTn = ON, V_{OUTn} = 1 V, DCn = 3Fh		20	45	mA
I_{OLC}	Constant output current	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, DCn = 3Fh	35.5	39.0	42.5	mA
I_{OLK1}	Output leakage current	All OUTn = OFF, V_{OUTn} = 17 V, DCn = 3Fh At OUT0 to OUT15			0.1	µA
I_{OLK2}	Output leakage current	No error condition, V_{XERR} = 5.5 V, at XERR			1	µA
ΔI_{OLC}	Constant current error (channel-to-channel)(1)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, DCn = 3Fh		±1	±3	%
ΔI_{OLC1}	Constant current error (device-to-device)(2)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, DCn = 3Fh		±2	±6	%
ΔI_{OLC2}	Line regulation(3)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, V_{CC} = 3.0 V to 5.5 V, DCn = 3Fh		±0.5	±1	%
ΔI_{OLC3}	Load regulation(4)	All OUTn = ON, V_{OUTn} = 1 V to 3 V, V_{OUTfix} = 1 V, DCn = 3Fh		±1	±3	%/V
T_{TEF}	Thermal error flag threshold	Junction temperature(5)	+150	+162	+175	°C
T_{HYS}	Thermal error hysteresis	Junction temperature(5)	+5	+10	+20	°C
V_{LOD}	LED open detection threshold	All OUTn = ON	0.2	0.3	0.4	V
V_{IREF}	Reference voltage output		1.16	1.20	1.24	V

(1) The deviation of each output from the average of OUT0–OUT15 constant current. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT15})}{16}} - 1 \right) \times 100$$

(2) The deviation of the OUT0–OUT15 constant current average from the ideal constant current value. Deviation is calculated by the following formula:

$$\Delta\,(\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 42.5 \times \left(\frac{1.20}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5 \text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0 \text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3.0 \text{ V})} \right) \times \frac{100}{5.5 \text{ V} - 3 \text{ V}}$$

(4) Load regulation is calculated by the equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3 \text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1 \text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1 \text{ V})} \right) \times \frac{100}{3 \text{ V} - 1 \text{ V}}$$

(5) Not tested. Specified by design.

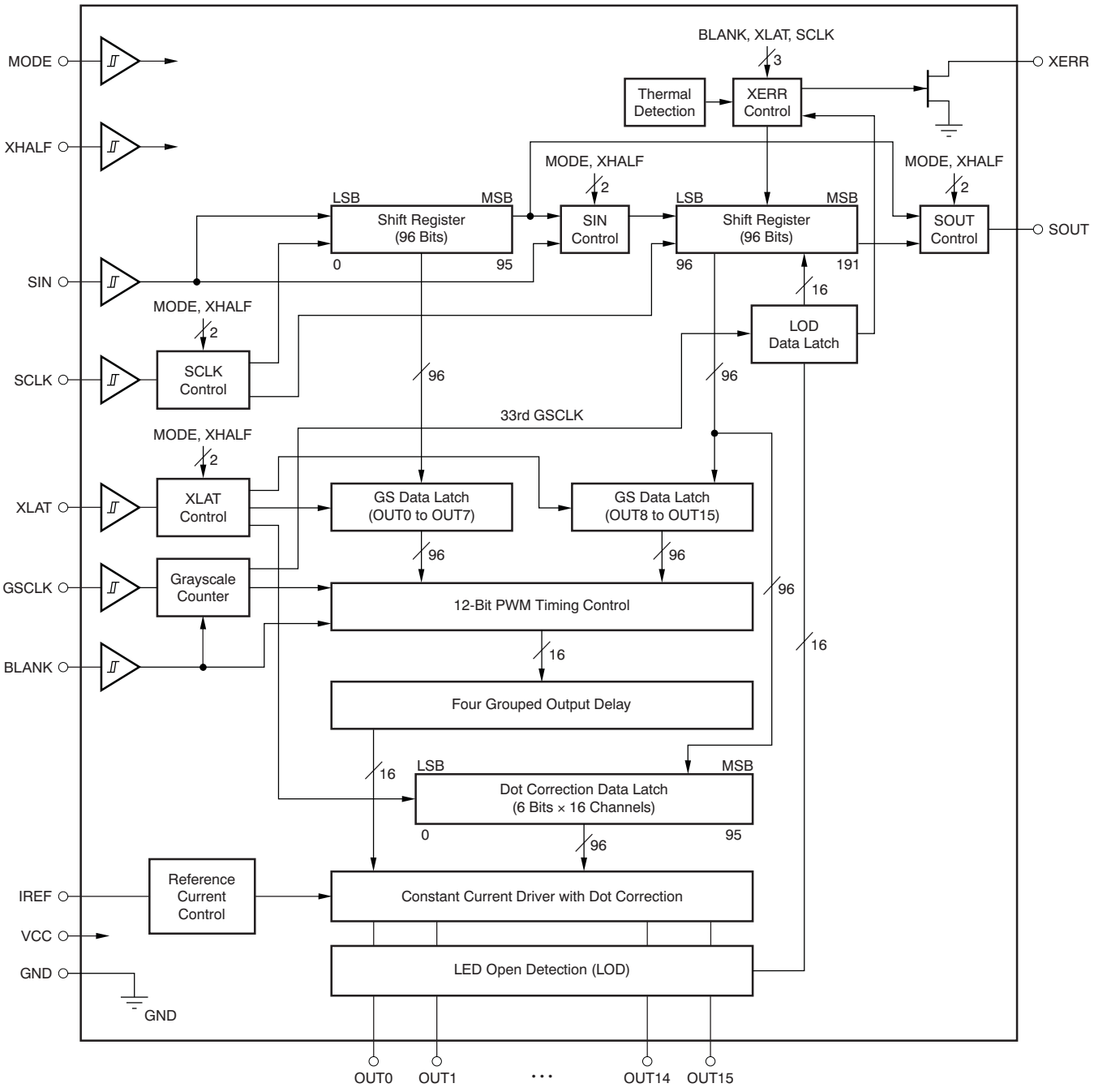
SWITCHING CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V, T_A = –40°C to +85°C, C_{L0} = 15 pF, R_{L0} = 100 Ω, C_{L1} = 100 pF, R_{L1} = 1 kΩ, R_{IREF} = 1.3 kΩ, V_{LED} = 5 V, and V_{XERR} = 5 V. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5946			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT (see Figure 11)			16	ns
t_{R1}		OUTn, V_{CC} = 5 V, DC = 3Fh (see Figure 11)		10	30	
t_{F0}	Fall time	SOUT (see Figure 11)			16	ns
t_{F1}		OUTn, V_{CC} = 5 V, DC = 3Fh (see Figure 11)		10	30	
t_{F2}		XERR (see Figure 11)			100	ns
t_{D0}	Propagation delay time	SCLK to SOUT (see Figure 12)(1)			25	ns
t_{D1}		BLANK↑ to OUT0 sink current off (see Figure 12)		20	40	ns
t_{D2}		GSCLK↑ to OUT0/4/8/12 (see Figure 12)	5	18	40	ns
t_{D3}		GSCLK↑ to OUT1/5/9/13 (see Figure 12)	20	42	73	ns
t_{D4}		GSCLK↑ to OUT2/6/10/14 (see Figure 12)	35	66	106	ns
t_{D5}		GSCLK↑ to OUT3/7/11/15 (see Figure 12)	50	90	140	ns
t_{D6}		XLAT↑ to OUTn (dot correction) 00h to 3Fh, 3Fh to 00h (see Figure 12)			100	ns
t_{ON_ERR}	Output on-time error	t_{OUTON} – t_{GSCLK}, GSn = 001h, GSCLK = 33 MHz (see Figure 13)	–20		10	ns

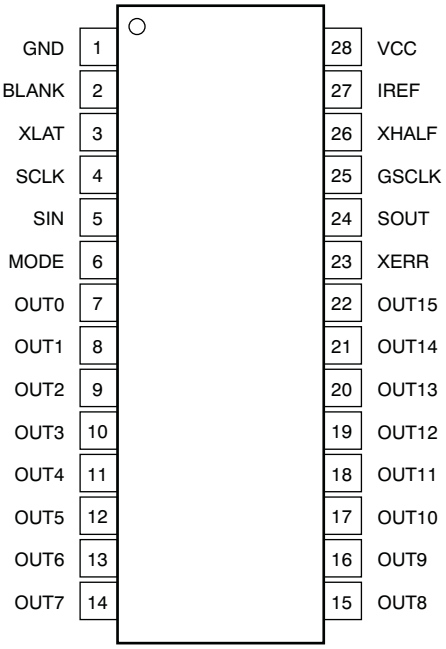
(1) XHALF = H: rising edge of SCLK to SOUT; XHALF = L: falling edge of SCLK to SOUT.

FUNCTIONAL BLOCK DIAGRAM

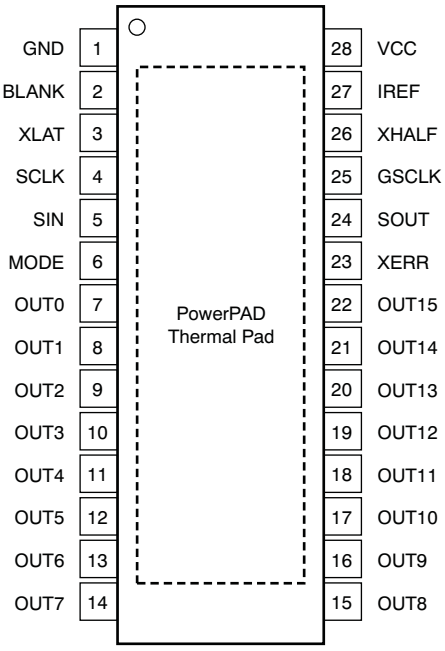


DEVICE INFORMATION

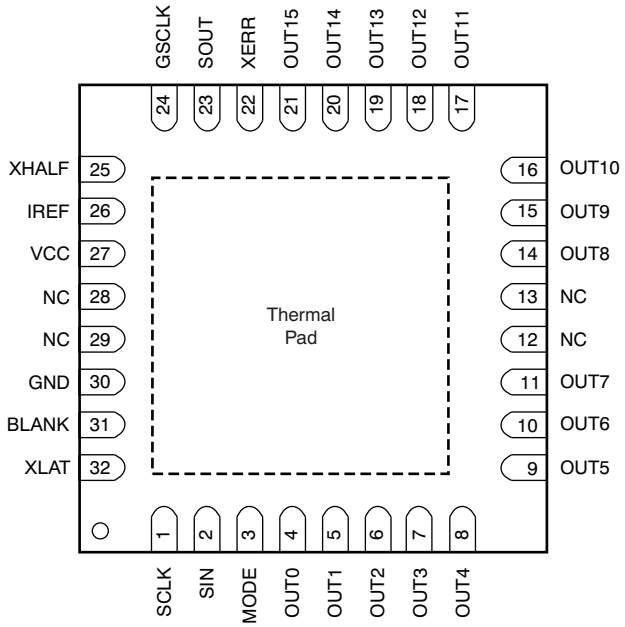
TSSOP-28
PW PACKAGE
(TOP VIEW)



HTSSOP-28
PWP PACKAGE
(TOP VIEW)



QFN-32
RHB PACKAGE
(TOP VIEW)



NC = No internal connection.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	PW/PWP	RHB		
BLANK	2	31	I	Blank (all constant current outputs off). When BLANK is high, all constant current outputs (OUT0 through OUT15) are forced off, the Grayscale PWM timing controller initializes and the Grayscale counter resets to '0'. When BLANK is low, all constant current outputs are controlled by the Grayscale PWM timing controller.
GND	1	30	—	Ground
GSCLK	25	24	I	Reference clock for Grayscale PWM control.
IREF	27	26	I/O	This pin sets the constant current value. OUT0 through OUT15 sink constant current is set to desired value by connecting an external resistor between IREF and GND.
MODE	6	3	I	Input mode pin. When MODE is high, the input mode is dot correction (DC). When MODE is low, the input mode is grayscale (GS).
NC	—	12, 13, 28, 29	—	No connection
OUT0	7	4	O	Constant current output
OUT1	8	5	O	Constant current output
OUT2	9	6	O	Constant current output
OUT3	10	7	O	Constant current output
OUT4	11	8	O	Constant current output
OUT5	12	9	O	Constant current output
OUT6	13	10	O	Constant current output
OUT7	14	11	O	Constant current output
OUT8	15	14	O	Constant current output
OUT9	16	15	O	Constant current output
OUT10	17	16	O	Constant current output
OUT11	18	17	O	Constant current output
OUT12	19	18	O	Constant current output
OUT13	20	19	O	Constant current output
OUT14	21	20	O	Constant current output
OUT15	22	21	O	Constant current output
SCLK	4	1	I	Serial data shift clock
SIN	5	2	I	Serial data input
SOUT	24	23	O	Serial data output
VCC	28	27	I	Power-supply voltage
XERR	23	22	O	Error output. Open-drain output. XERR goes low when LOD or TEF is detected.
XHALF	26	25	I	Extended serial interface. When XHALF is high, the device operates normally. When XHALF is low, the extended serial interface is activated.
XLAT	3	32	I	Edge triggered latch signal. At the rising edge of XLAT, the TLC5946 writes data from the input shift register to either the Dot Correction register (MODE = high) or the Grayscale register (MODE = low).

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

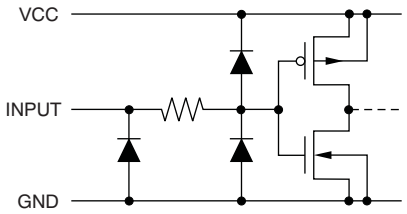


Figure 1. SIN, SCLK, GSCLK, XLAT, BLANK, MODE, XHALF

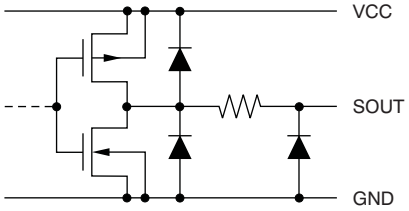


Figure 2. SOUT

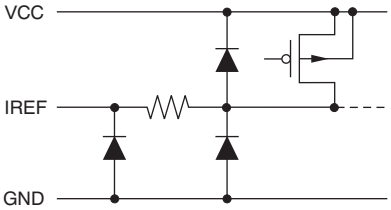


Figure 3. IREF

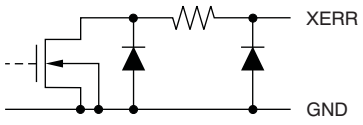


Figure 4. XERR

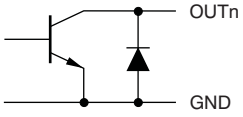
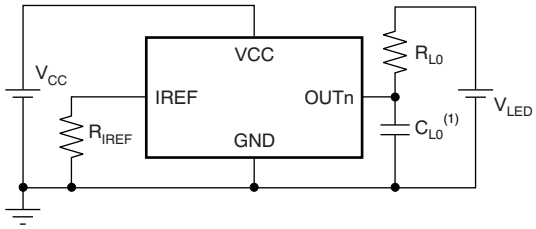


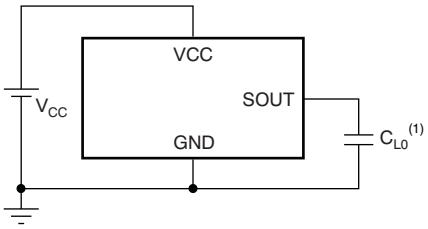
Figure 5. OUT0 Through OUT15

TEST CIRCUITS



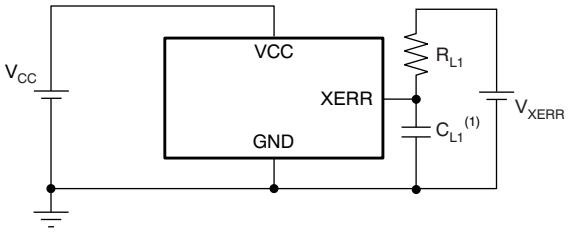
(1) C_{L0} includes measurement probe and jig capacitance.

Figure 6. Rise Time and Fall Time Test Circuit for OUTn



(1) C_{L0} includes measurement probe and jig capacitance.

Figure 7. Rise Time and Fall Time Test Circuit for SOUT



(1) C_{L1} includes measurement probe and jig capacitance.

Figure 8. Rise Time and Fall Time Test Circuit for XERR

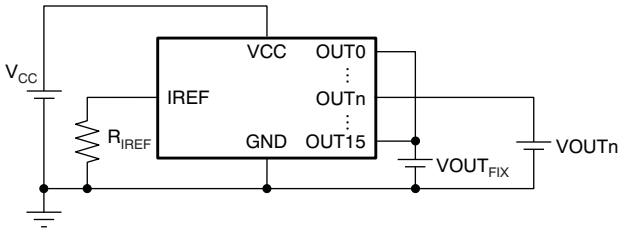
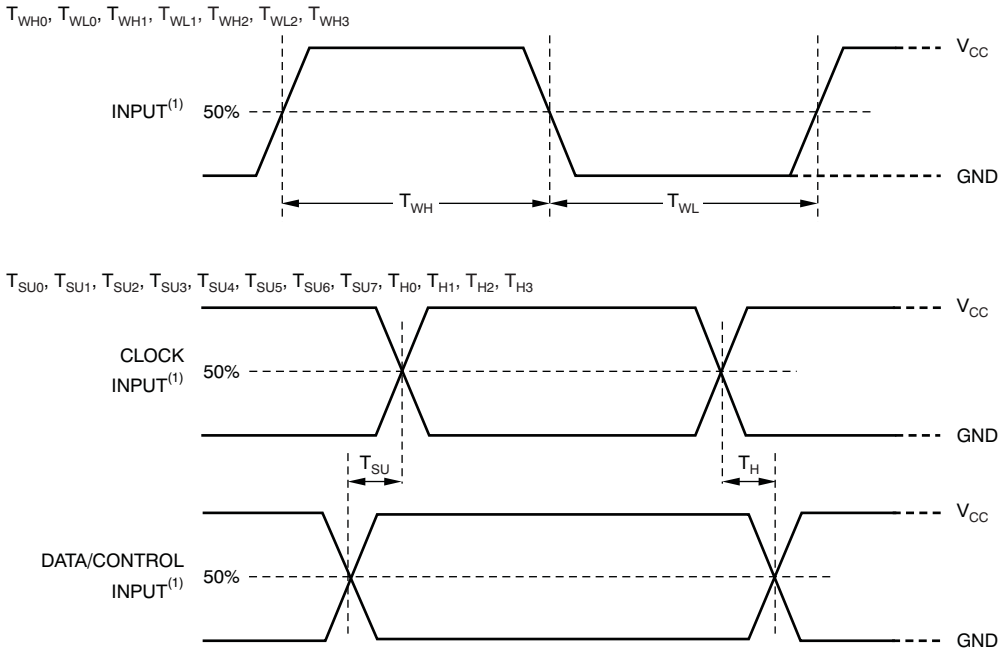


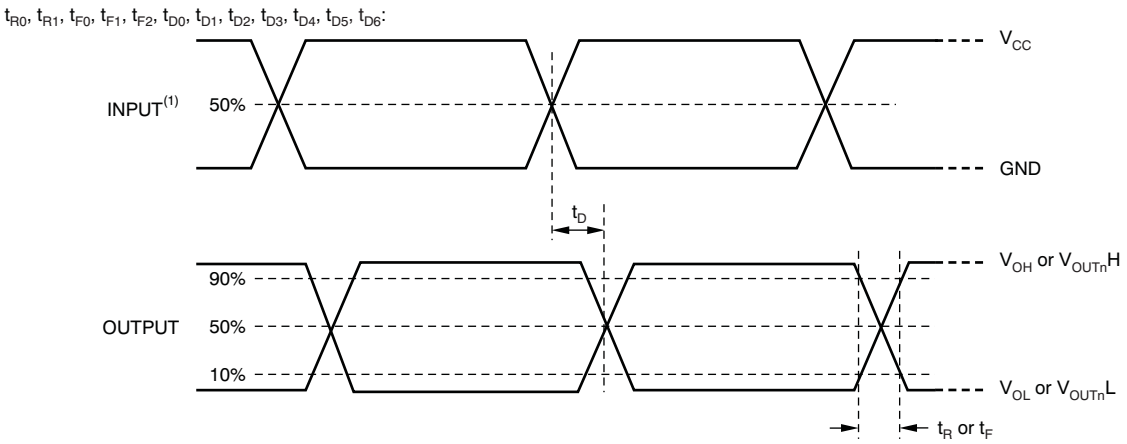
Figure 9. Constant Current Test Circuit for OUTn

TIMING DIAGRAMS



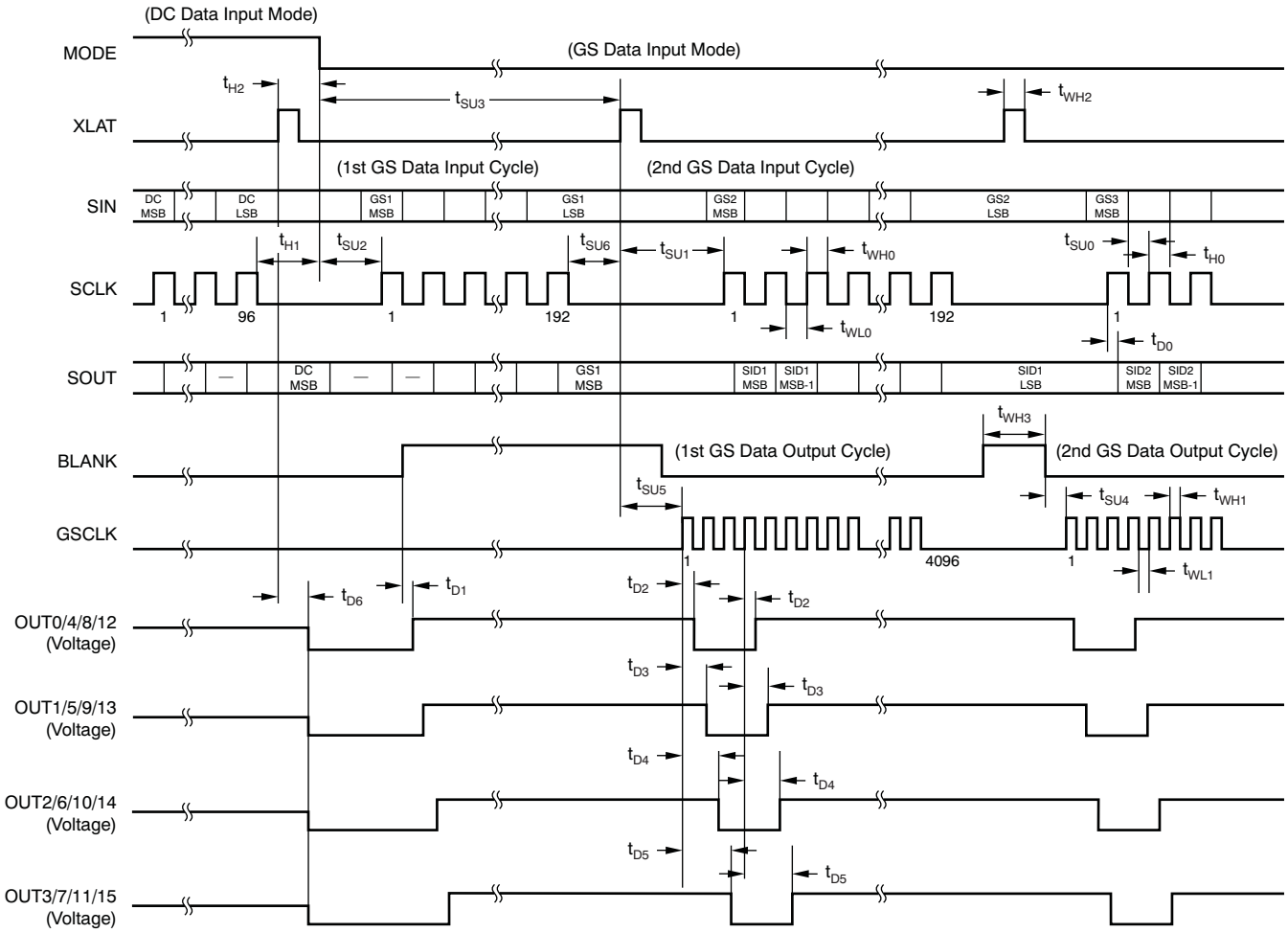
(1) Input pulse rise and fall time is 1 ns to 3 ns. Input pulse high level is VCC and low level is GND.

Figure 10. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 11. Output Timing



NOTE: DC = Dot Correction, GS = Grayscale.

Figure 12. Timing Diagram (GS Data = 003h, XHALF = High)

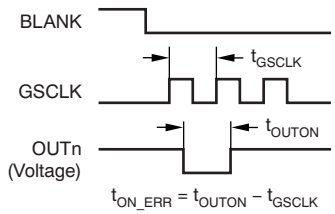


Figure 13. Output On-Time Error Timing Diagram (GS Data = 001h, GSCLK = 33 MHz)

TYPICAL CHARACTERISTICS

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

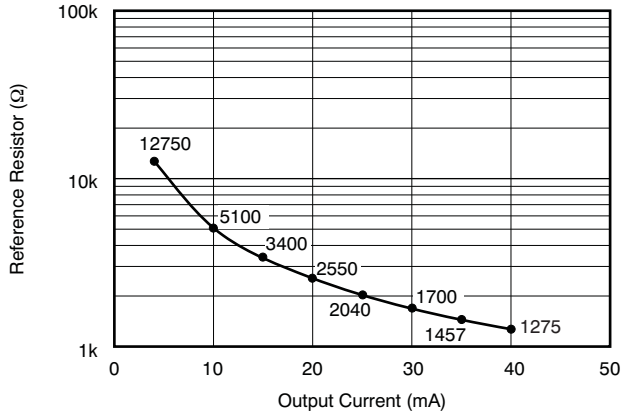


Figure 14.

POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE

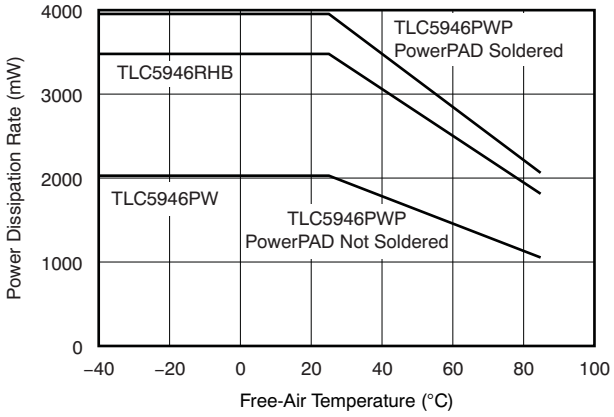


Figure 15.

OUTPUT CURRENT vs OUTPUT VOLTAGE

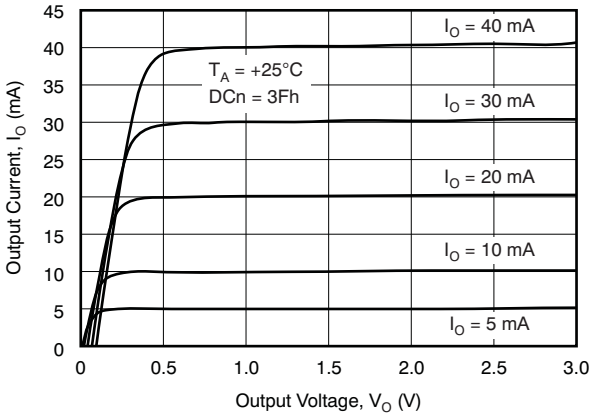


Figure 16.

OUTPUT CURRENT vs OUTPUT VOLTAGE

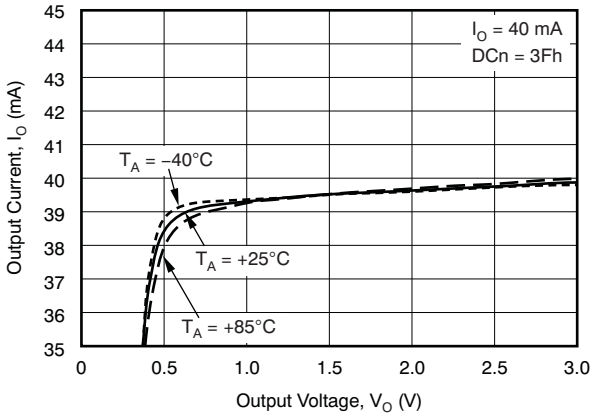


Figure 17.

CONSTANT CURRENT ERROR vs AMBIENT TEMPERATURE

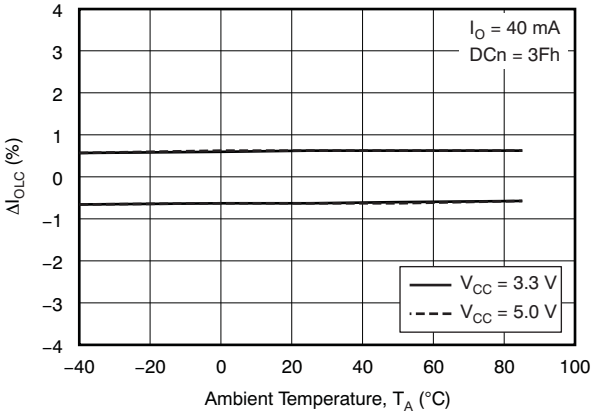


Figure 18.

CONSTANT CURRENT ERROR vs OUTPUT CURRENT

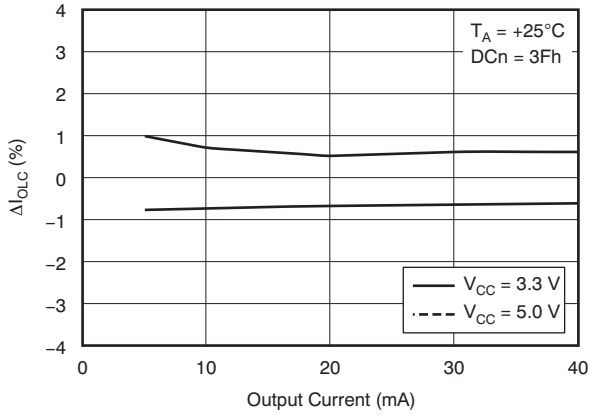


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

DOT CORRECTION LINEARITY (ABS Value)

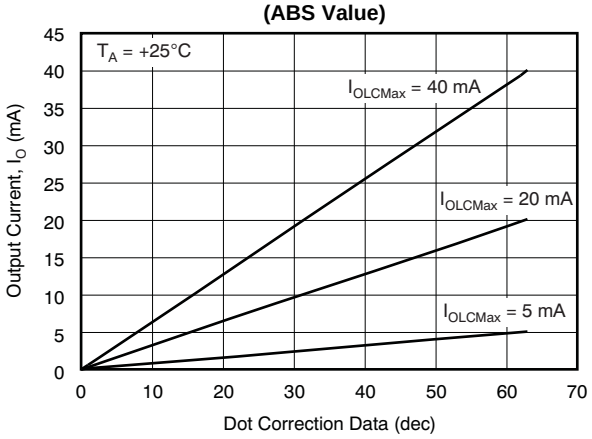


Figure 20.

DOT CORRECTION LINEARITY (ABS Value)

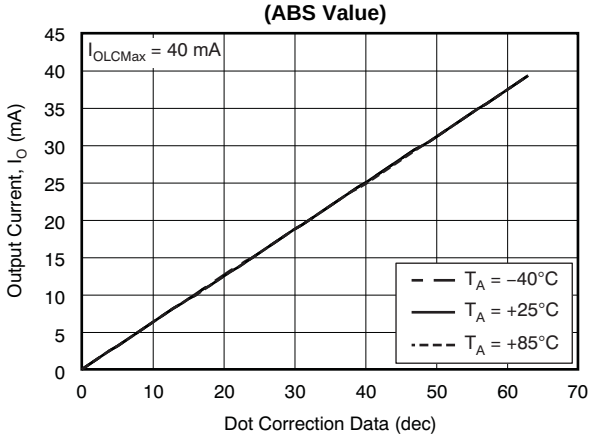


Figure 21.

CONSTANT CURRENT OUTPUT VOLTAGE WAVEFORM

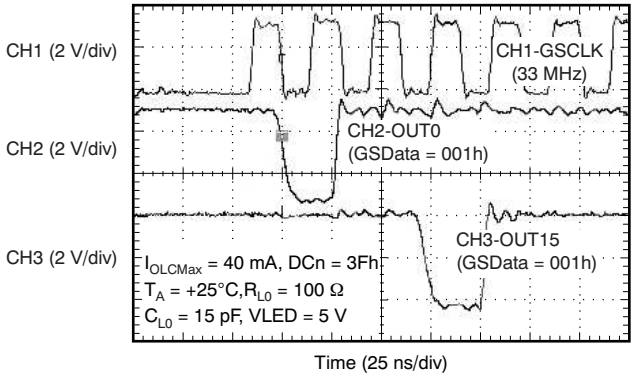


Figure 22.

DETAILED DESCRIPTION

SETTING FOR THE MAXIMUM OUTPUT CURRENT VALUE

The maximum output current of each channel (I_{OLCMax}) is set by a single external resistor (R_{IREF}), placed between the IREF pin and the GND pin. The voltage on IREF is made with an internal bandgap, V_{IREF}, which has a typical value of 1.20 V. The R_{IREF} resistor value is calculated by Equation 1:

$$R_{IREF}\ (\Omega) = 42.5 \times \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \quad (1)$$

Where:

- V_{IREF} = 1.20 V
- R_{IREF} = User-selected external resistor

I_{OLCMax} is the largest current for all outputs. Each output sinks the I_{OLCMax} current when it is turned on and its dot correction is set to the maximum value of 3Fh (63d). The sink current for each output can be reduced by lowering the respective output dot correction value.

R_{IREF} must be between 1.275 kΩ (typ) and 12.75 kΩ (typ) in order to keep I_{OLCMax} between 4 mA and 40 mA. The output current may be unstable if I_{OLCMax} is less than 4 mA. Output currents lower than 4 mA can be achieved by setting I_{OLCMax} to 4 mA or higher and then using dot correction.

Figure 14 illustrates the maximum output current versus R_{IREF}. R_{IREF} is the value of the resistor between the IREF terminal to GND. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per output. The maximum output current is 42.5 times the current flowing out of the IREF pin.

DOT CORRECTION (DC) FUNCTION

The TLC5946 is able to individually adjust the output current of each channel (OUT0 to OUT15). This function is called *dot correction* (DC). The DC function allows the user to individually adjust the brightness and color deviations of LEDs connected to the outputs OUT0 to OUT15. Each respective channel output current can be adjusted in 64 steps from 0% to 100% of the maximum output current, I_{OLCMax}. The dot correction data are entered into the TLC5946 via the serial interface.

The output current is calculated by Equation 2:

$$I_{OUTn} = I_{OLCMax} \times \frac{DCn}{63} \quad (2)$$

Where:

- I_{OLCMax} = the maximum output current of each output
- DCn = the programmed dot correction value of output n (DCn = 0 to 63)

When MODE is high, the input shift register works as a DC shift register. The shift registers and data latches are each 96 bits in length, and are used to individually adjust the constant current values for each constant current driver. Each channel can be adjusted from 0% to 100% of the maximum LED current with 6-bit resolution. Figure 23 illustrates the DC serial data configuration. Figure 12 illustrates the timing chart for writing data into the shift registers and data latches. Each channel LED current is dot-corrected by the percentage corresponding to the data in its DC data latch. DC data present on the SIN pin are clocked into the shift register with each rising edge of the SCLK pin. Data are shifted in MSB first. The data are latched from the shift register into the DC data latch with a rising edge on the XLAT pin.

The BLANK signal does not need to be high to latch in new data. When XLAT goes high, the new dot-correction data immediately become valid and change the output currents if the output is on. When the IC is powered on, the data in the shift register and DC data latch are not set to any default values. Therefore, DC data must be written to the DC latch before turning on the constant current output.

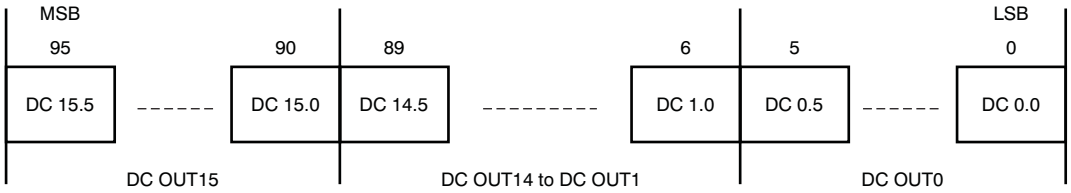


Figure 23. Dot Correction Serial Data Configuration

GRAYSCALE (GS) FUNCTION (PWM Operation)

The pulse width modulation (PWM) operation is controlled by a 12-bit grayscale counter that is clocked on each rising edge of the grayscale reference clock (GSCLK). The counter is reset to zero when the BLANK signal is set high. The counter value is held at zero while BLANK is high, even if the GSCLK input toggles high and low. After the falling edge of BLANK, the counter increments with each rising edge of GSCLK. Any constant current sink output (OUT0 through OUT15) with a non-zero value in its corresponding grayscale latch starts to sink current after the first rising edge of GSCLK following a high-to-low transition of BLANK. The internal counter keeps track of the number of GSCLK pulses. Each output channel stays on as long as the internal counter is equal to or less than the respective output GS data. Each channel turns off at the rising edge of GSCLK when the grayscale counter value is larger than the grayscale latch value.

For example, an output that has a grayscale latch value of '1' turns on at the first rising edge of GSCLK after BLANK goes low. It turns off at the second rising edge of GSCLK. Figure 24 shows the PWM output timing. When the counter becomes FFFh, the counter stops and output does not turn on until the next grayscale cycle. Pulling BLANK high before the counter becomes FFFh immediately resets the counter to zero.

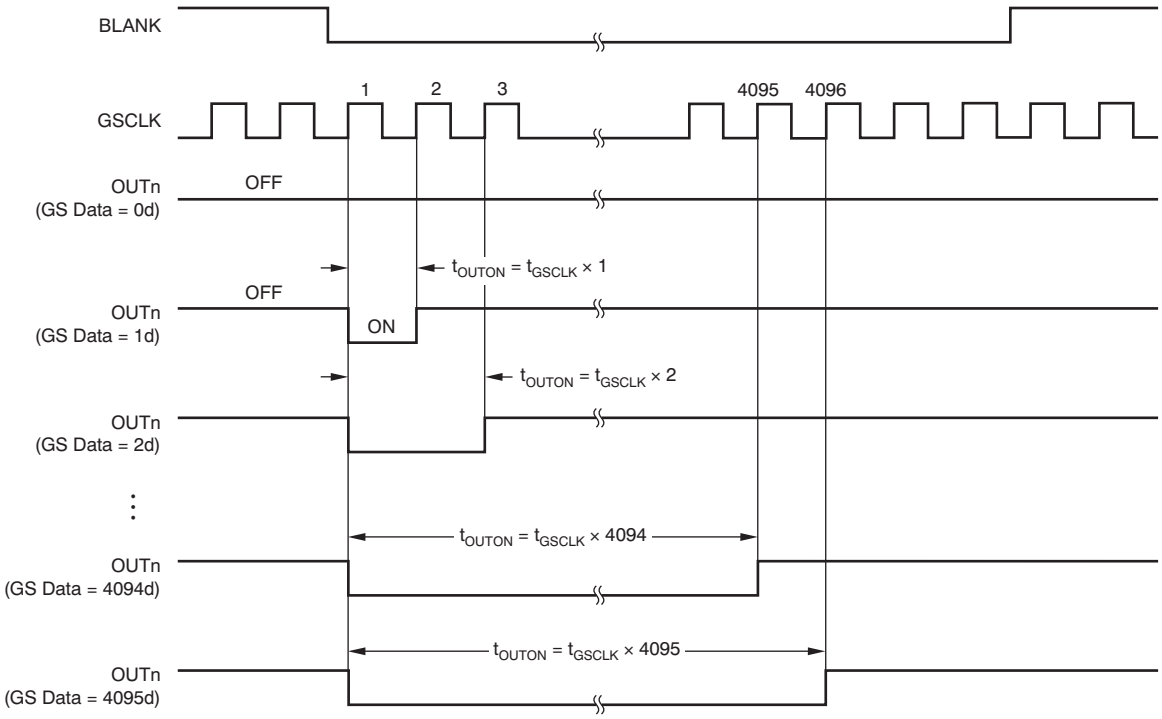


Figure 24. PWM Output Timing

When the IC powers on, the data in the shift register and latch are not set to any default value. Therefore, GS data must be written to the GS latch before turning the constant current output on. Additionally, BLANK should be high when the device is powered on, to prevent the outputs from turning on before the proper grayscale and dot correction values are written. All constant current outputs are always off when BLANK is high.

Each output (OUTn) on-time (t_{OUTON}) is calculated by Equation 3:

$$t_{OUTON}\ (ns) = t_{GSCLK}\ (ns) \times GSn \quad (3)$$

Where:

- t_{GSCLK} = the period of GSCLK
- GSn = the programmed grayscale value of output n (GSn = 0 to 4095d)

If XLAT goes high during a grayscale cycle, then new GS data are immediately latched into the GS latch. This action can cause the outputs to turn on or off unexpectedly. For proper operation, GS data should only be latched into the IC at the end of a GS period when BLANK is high.

When MODE is low, the input shift register works as a GS shift register. The shift registers and data latches are each 192 bits in length, and are used to set the PWM timing for each constant current driver. Figure 25 shows the GS serial data configuration. Refer to Figure 12 for a timing diagram for writing data into the shift register and latch. The driver on-time is set by the data in the GS data latch. GS data present on the SIN pin are clocked into the shift register with each rising edge of the SCLK pin. Data are shifted in MSB first. Data are latched from the shift register into the GS data latch with a rising edge on the XLAT pin.

When the IC powers on, the data in the shift register and data latch are not set to any default value. Therefore, grayscale data must be written to the GS latch before turning on the constant current output. Also, BLANK should be high when powered on because the constant current may also turn on. All constant current outputs are off when BLANK is high. The status information data (SID) byte overwrites on the most significant 17 bits of the input shift register at the rising edge of the first SCLK after XLAT goes low.

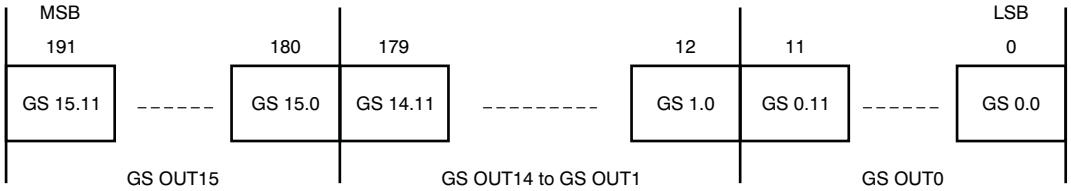


Figure 25. Grayscale Serial Data Configuration

STATUS INFORMATION DATA (SID)

Status information data (SID) are 17-bit, read-only data, accessible in the grayscale data input mode (MODE = GND). Both the LED open detection (LOD) error and the thermal error flag (TEF) are shifted out of the SOUT pin with each rising edge of SCLK. The 16 LOD bits for each channel and the TEF bit are written into the 17 most significant bits (MSBs) of the shift register at the rising edge of the first SCLK after XLAT goes low. As a result, the previous data in the 17 MSBs are lost at the same time. Figure 26 shows the bit assignments, Table 1 describes the SID data definition, and Figure 27 illustrates the read timing for the status information data.

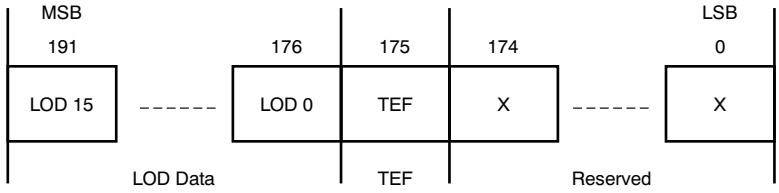


Figure 26. Status Information Data Configuration (XHALF = High)

Table 1. SID Data Definition

SID DATA	DEFINITION	
	LODn	TEF
0	No LED open error	No thermal error
1	LED is open or shorted to GND	Over temperature

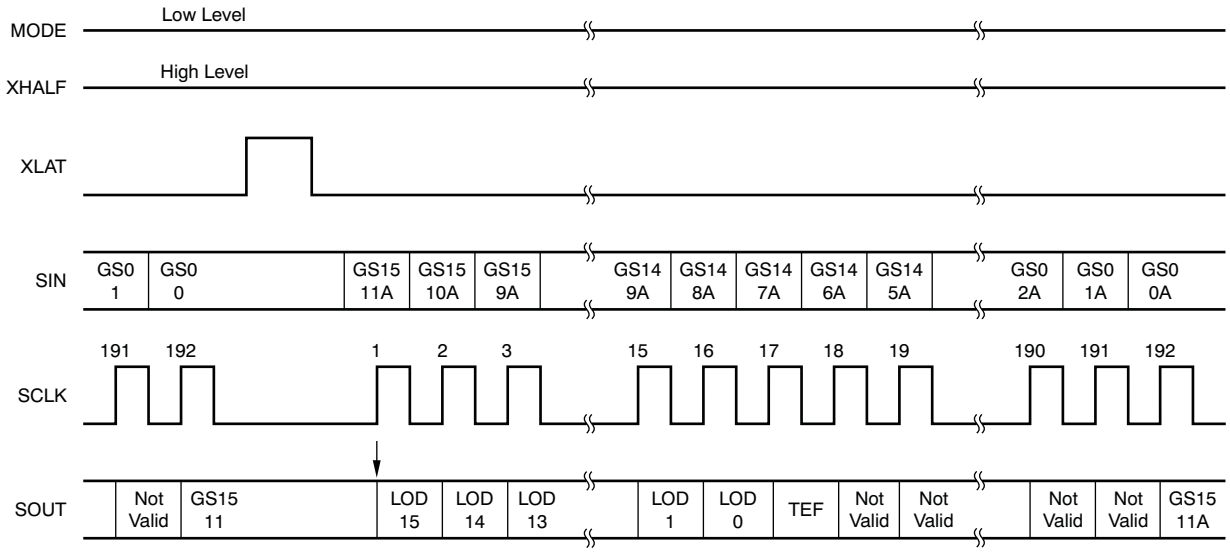


Figure 27. Status Information Data Read Timing (XHALF = High)

The LOD data are updated at the rising edge of the 33rd GSCLK pulse after BLANK goes low; the LOD data are retained until the next 33rd GSCLK. LOD data are only checked for outputs that are turned on during the rising edge of the 33rd GSCLK pulse. A '1' in a LOD bit indicates an open LED condition for the corresponding channel. A '0' indicates normal operation. The GS data should be equal to or higher than 21h (33d) to detect an open LED in every PWM cycle. When the IC is powered on, LOD data do not show correct values. Therefore, LOD data must be read at the rising edge of the 33rd GSCLK pulse after BLANK goes low.

The TEF bit indicates that the IC temperature is too high. A '1' in the TEF bit means that the IC temperature exceeds the detect temperature threshold, T_{TEF}. A '0' in the TEF bit indicates normal operating temperature conditions.

ERROR INFORMATION OUTPUT

The TLC5946 has two error detection circuits: LED open detection (LOD) and a thermal error flag (TEF). LOD detects a broken or disconnected LED during the display period. The TEF indicates an over-temperature condition. A low-level output of XERR indicates that an LOD error or TEF is detected. XERR pins of more than two ICs can be connected together and pulled up to V_{CC} with a single resistor because XERR is an open-drain output; see the *SCLK and GSCLK Frequency* section. Table 2 shows the XERR truth table. BLANK = H masks LOD to distinguish between LOD and TEF. When the IC is powered on, XERR does not show correct values. XERR shows a correct signal when LOD data become valid at the rising edge of the 33rd GSCLK pulse after BLANK goes low. Also, both the LOD error and the TEF are shifted out of the SOUT pin; see the *Status Information Data (SID)* section.

Table 2. XERR Truth Table

CONDITION			
ERROR DATA		INPUT	
LOD (Internal)	TEF (Internal)	BLANK	XERR
0	0	L	H
0	1		L
1	0		L
1	1		L
0	0	H	H
0	1		L
1	0		H
1	1		L

CONTINUOUS BASE LED OPEN DETECTION (LOD)

The LOD function automatically updates LOD data at the rising edge of the 33rd GSCLK pulse after BLANK goes low; the LOD data are retained until the next 33rd GSCLK. LOD data are only checked for outputs that are turned on during the rising edge of the 33rd GSCLK pulse. The internal LOD data becomes '1' when the voltage of the OUTn pin is less than the LED open detection threshold (V_{LOD} = 0.3 V, typical).

To eliminate false detection of open LEDs, the LED driver design must ensure that the TLC5946 output voltage is greater than V_{LOD} when the outputs are on. The GS data should be equal to or higher than 21h (33d) to detect LED open in every PWM cycle.

AUTO OUTPUT OFF

The V_{CC} current (ICC) increases during an LED open detection. When the TLC5946 detects an open or shorted to ground LED at OUTn, the TLC5946 turns off OUTn to reduce the ICC at the 33rd falling edge of GSCLK after the falling edge of BLANK, as shown in Figure 28. This feature minimizes supply current during fault conditions. If there are any unconnected output LED lamps (including connection failures or short-circuits), the grayscale data corresponding to the unconnected output should be set to '0' before turning on the LEDs.

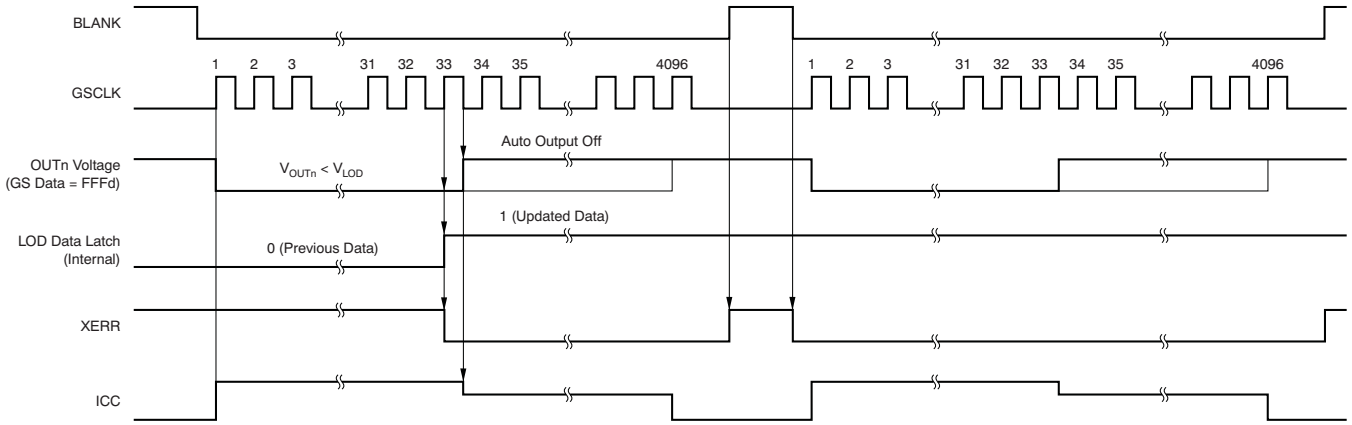


Figure 28. LOD and Auto Output Off Timing

THERMAL ERROR FLAG (TEF)

The TLC5946 has a thermal error flag (TEF) function to indicate an over-temperature condition. If the junction temperature exceeds the threshold temperature, +162°C typical, TEF toggles to '1' and the XERR pin goes to a low level. Once TEF becomes '1', it remains a '1' until the first falling edge of SCLK after XLAT goes low, as shown in Figure 29. If the junction temperature (T_J) remains higher than the threshold temperature, TEF remains '1', even after the first falling edge of SCLK. TEF is also shifted out of the SOUT pin; see the *Status Information Data (SID)* section.

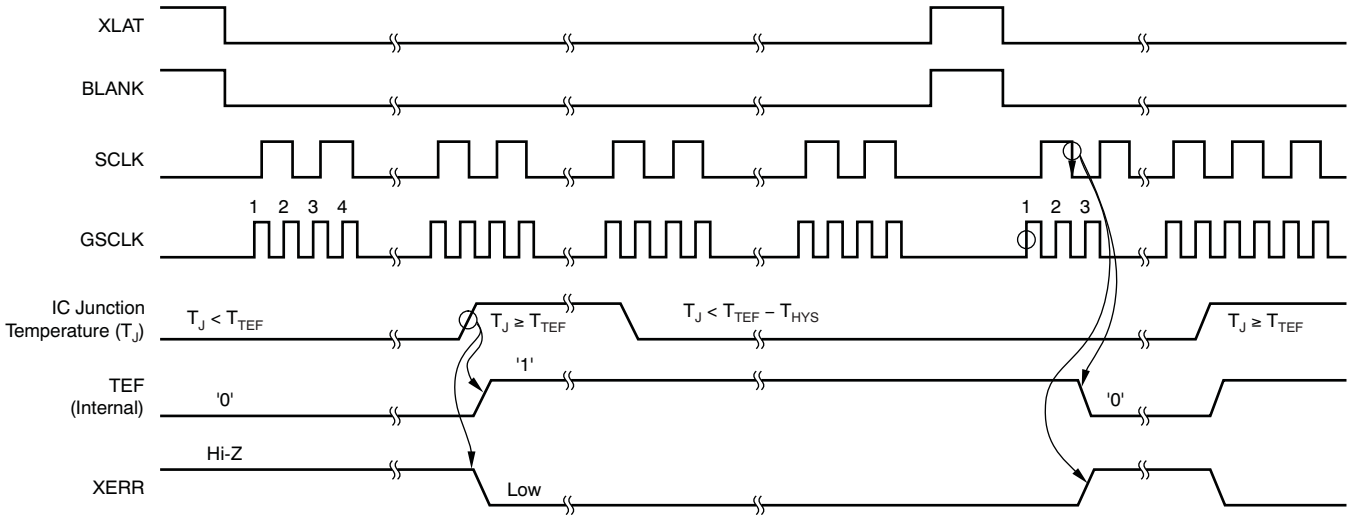


Figure 29. TEF and XERR Timing

NOISE REDUCTION

Large surge currents can flow through the IC and the board if all 16 LED channels fully turn on simultaneously at the start of each grayscale cycle. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5946 turns on the LED channels in a series delay, to provide a current soft-start feature. The output current sinks are grouped into four groups of four channels each. The first group is OUT0, 4, 8, 12; the second group is OUT1, 5, 9, 13; the third group is OUT2, 6, 10, 14; and the fourth group is OUT3, 7, 11, 15. Each group turns on sequentially with a small delay between groups; see Figure 12. Both turn-on and turn-off are delayed.

OUTPUT ENABLE

When BLANK is high, all constant current outputs turn off and the grayscale counter is reset. When BLANK is low, all constant current outputs are controlled by the GS PWM timing controller. If BLANK goes low and then toggles high again in a very short time, all outputs that are programmed to turn on do so, for either the programmed number of grayscale clocks or the length of time that the BLANK signal was low, whichever is lower. For example, if all outputs are programmed to turn on for 1 ms, but the BLANK signal is only low for 50 ns, all outputs turn on for 50 ns, even though some outputs will turn on after the BLANK signal has already gone high.

SERIAL INTERFACE

The TLC5946 has a flexible serial interface that can be connected to microcontrollers or digital signal processors in various ways. Only three pins are needed to input data into the device. More than two TLC5946s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. Cascaded two TLC5946s are shown in Figure 30 and Figure 31. The SOUT pin can also be connected to the controller to receive status information from the TLC5946; see the *SCLK and GSCLK Frequency* section.

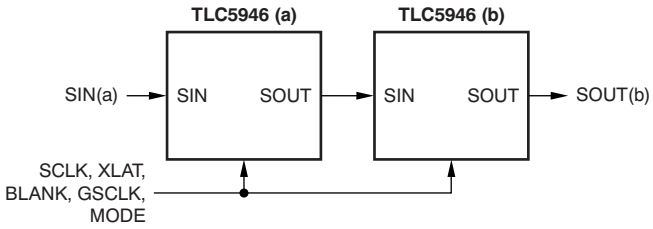


Figure 30. Cascading Two TLC5946 Devices

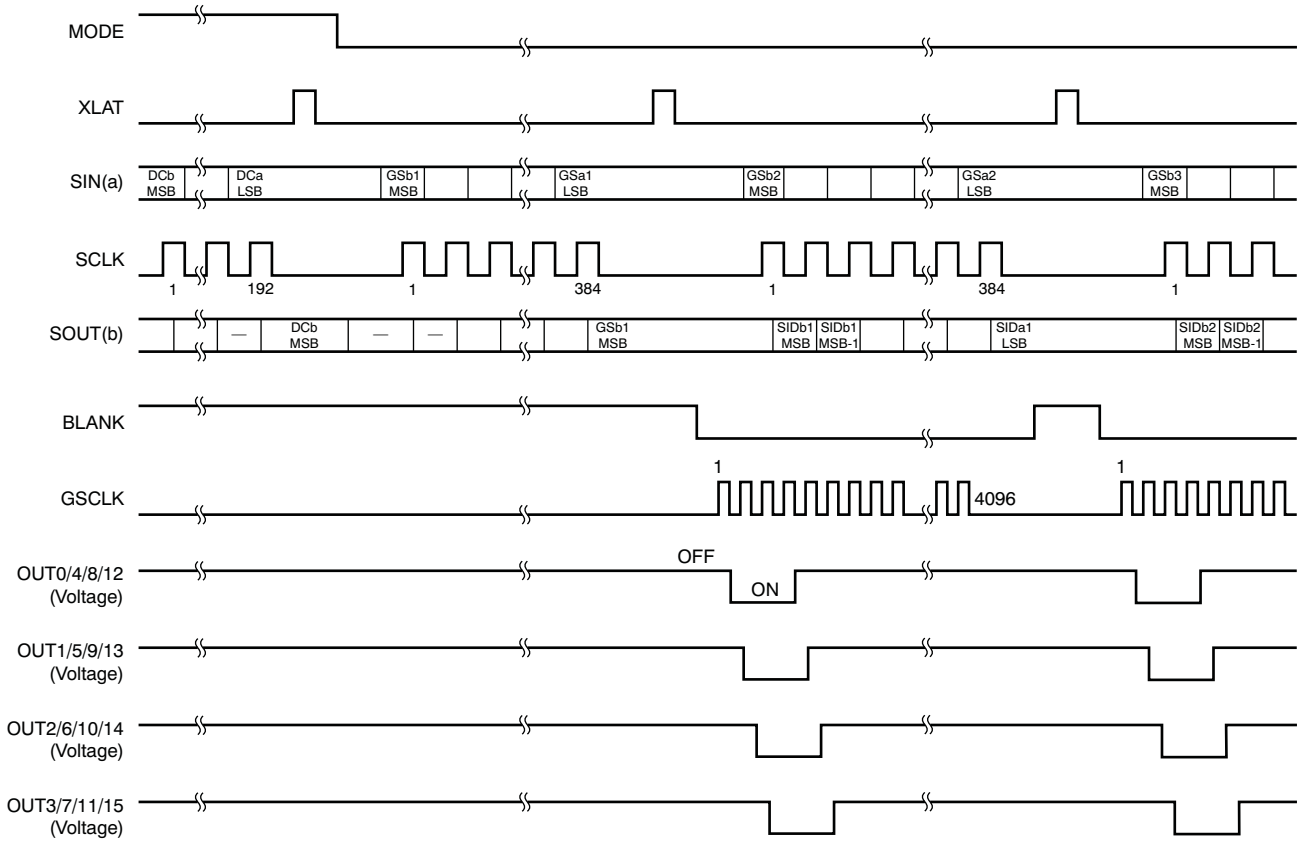


Figure 31. Timing Diagram of Two Cascaded TLC5946 Devices (XHALF = High)

SERIAL INTERFACE MODE

The serial interface has two input modes defined by the MODE pin, as Table 3 shows. XLAT must be low when the MODE pin goes high-to-low or low-to-high to change back and forth between GS mode and DC mode.

Table 3. Serial Interface Input Mode

MODE	INPUT MODE	INPUT SHIFT REGISTER
GND	Grayscale PWM data	192 bits
VCC	Dot correction data	96 bits

SCLK AND GSCLK FREQUENCY

Figure 32 shows a cascading connection of *n* TLC5946 devices connected to a single controller, building a basic module of an LED display system. There is no limitation to the maximum number of ICs that can be cascaded. However, the maximum number of cascading TLC5946 devices depends on the application system and is in the range of 40 devices. Equation 4 and Equation 5 show the minimum frequencies for GSCLK and SCLK.

$$f_{GSCLK} = 4096 \times f_{UPDATE} \quad (4)$$

$$f_{SCLK} = 192 \times f_{UPDATE} \times n \quad (5)$$

where:

- f_{GSCLK} = minimum frequency of GSCLK
- f_{SCLK} = minimum frequency of SCLK
- f_{UPDATE} = update rate of entire cascading system
- n = number of cascaded TLC5946 devices

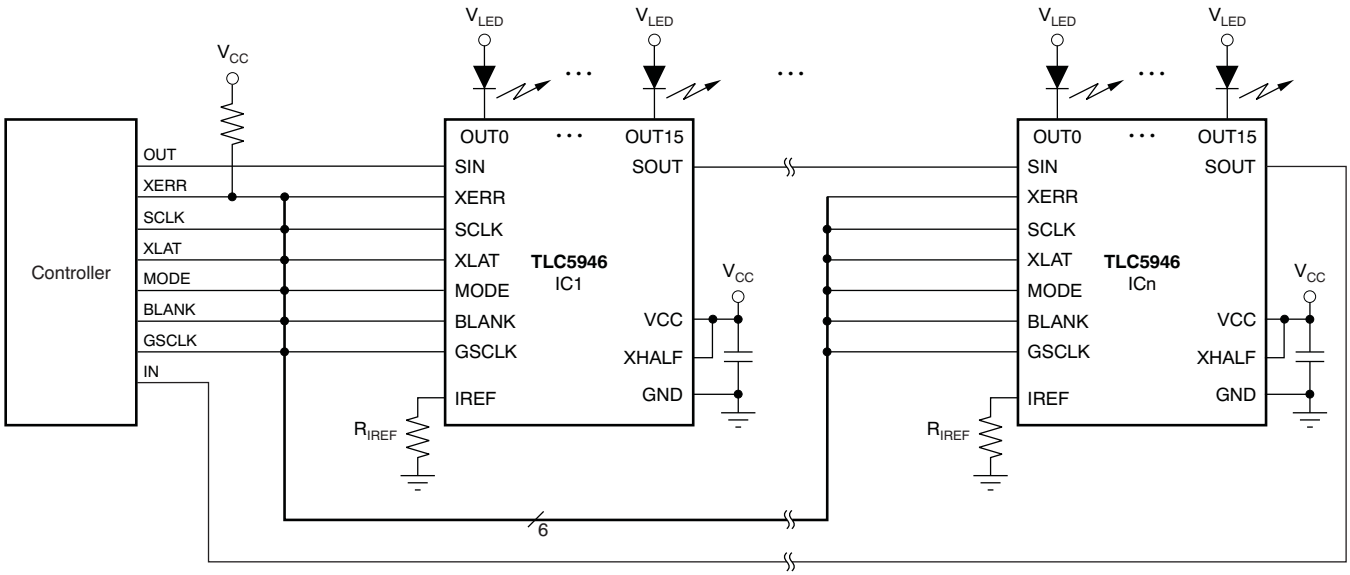


Figure 32. Cascading Device Connections

POWER DISSIPATION CALCULATION

The device power dissipation must be below the power dissipation rate of the device package to ensure correct operation. Equation 6 calculates the power dissipation of the device:

$$P_D = (V_{CC} \times I_{CC}) + \left(V_{OUT} \times I_{OLCMax} \times N \times \frac{DCn}{63d} \times d_{PWM} \right) \quad (6)$$

Where:

- P_D = device power dissipation
- V_{CC} = device supply voltage
- I_{CC} = device supply current
- V_{OUT} = OUTn voltage when driving LED current
- I_{OLCMax} = LED current adjusted by R_{IREF} resistor
- DCn = maximum DC value for OUTn
- N = number of OUTn driving LED at the same time
- d_{PWM} = duty cycle defined by BLANK pin or GS PWM value

EXTENDED SERIAL INTERFACE

The TLC5946 has an extended serial interface with the following functions:

1. Independently accessible GS shift register of OUT0 to OUT7 or OUT8 to OUT15
2. SOUT half clock delay

When XHALF is low, the extended serial interface becomes active. Either the OUT0 to OUT7 GS shift register or the OUT8 to OUT15 GS shift register is selected in advance by counting the XLAT pulses while BLANK is high (one XLAT pulse selects the OUT0 to OUT7 GS shift register and two XLAT pulses select the OUT8 to OUT15 GS shift register), as shown in Figure 33. One or two XLAT pulses while BLANK is high must be input before sending the serial data.

SOUT outputs serial data at the falling edge of SCLK, delaying half a clock longer than the normal serial interface mode. SIN reads data at the rising edge of SCLK at the same as the normal serial interface mode. This configuration ensures a longer distance serial interface. Figure 34 shows the output timing of the extended serial interface mode.

SOUT outputs the status information data only when the data of OUT8 to OUT15 are shifted in, as shown in Figure 35 and Figure 36. The status information data configuration when XHALF is low is shown in Figure 37.

Figure 38 shows the recommended ac timing widths of the extended serial interface. Note that t_{WL2}, t_{SU7}, and t_{H3} are only effective when XHALF is low.

Figure 39 and Figure 40 are power-on sequence examples of this mode. BLANK should be high when the device is powered on to prevent the outputs from turning on before the proper GS and DC values are written. The extended serial interface mode is available only in the GS PWM mode (MODE = low). When MODE is high in the extended serial interface mode (XHALF = low), the TLC5946 becomes the DC mode that is the same as the normal DC mode.

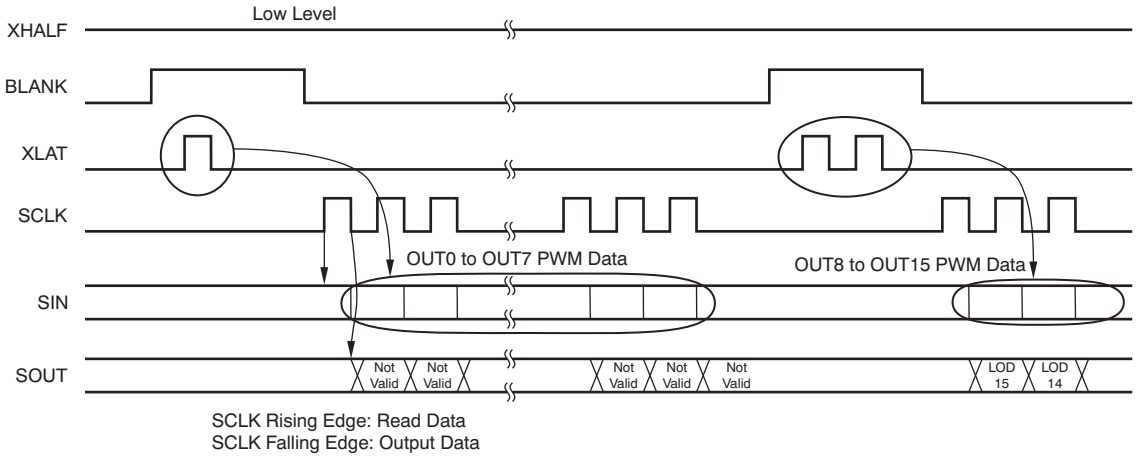


Figure 33. Extended Serial Interface

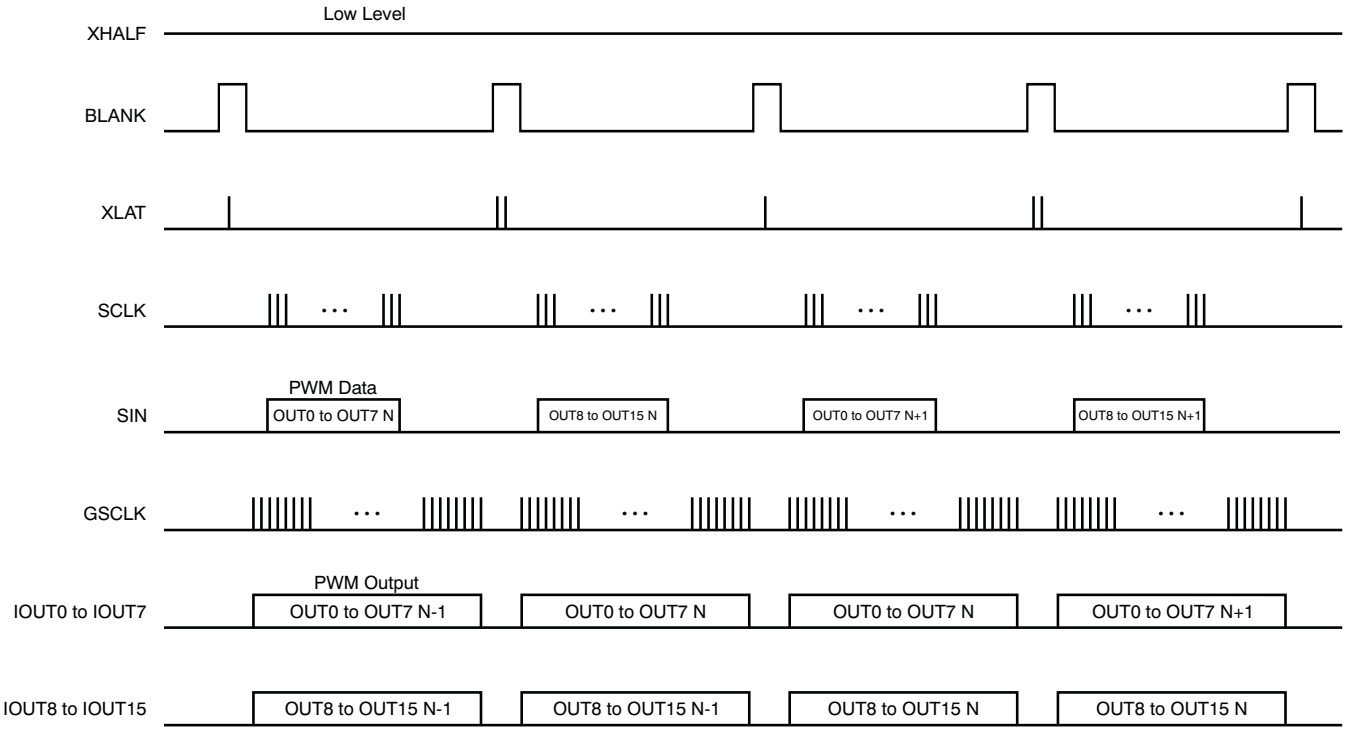


Figure 34. Output Timing of Extended Serial Interface

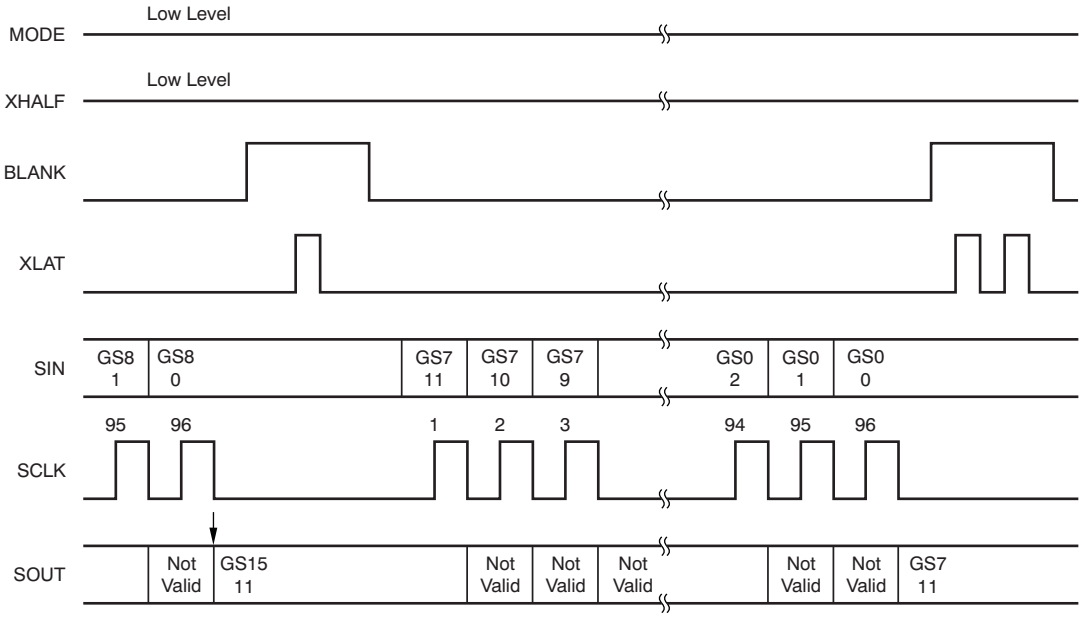


Figure 35. Extended Serial Interface (OUT0 to OUT7)

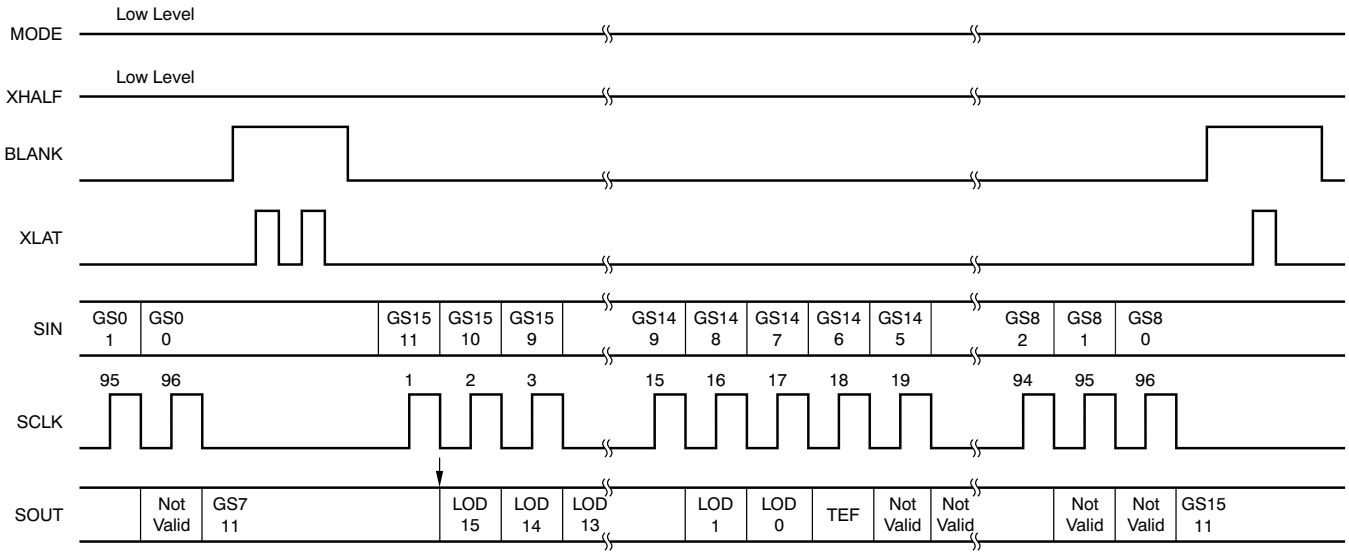


Figure 36. Extended Serial Interface (OUT8 to OUT15)

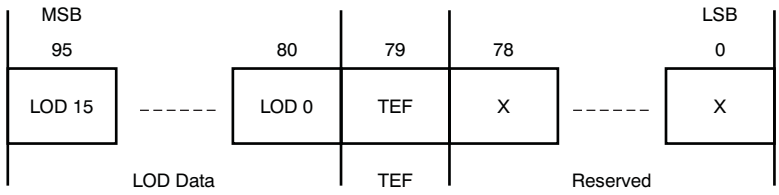


Figure 37. Status Information Data Configuration (XHALF = Low)

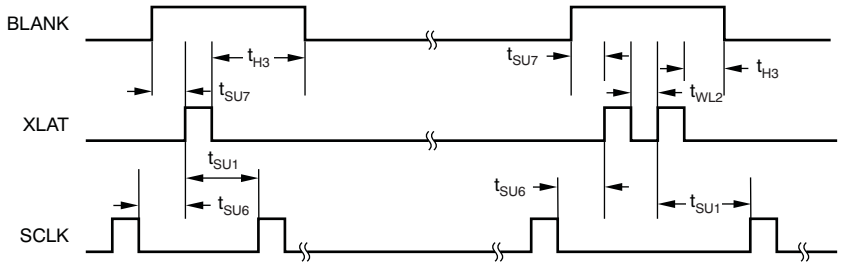


Figure 38. AC Timing in Extended Serial Interface Mode (XHALF = Low)

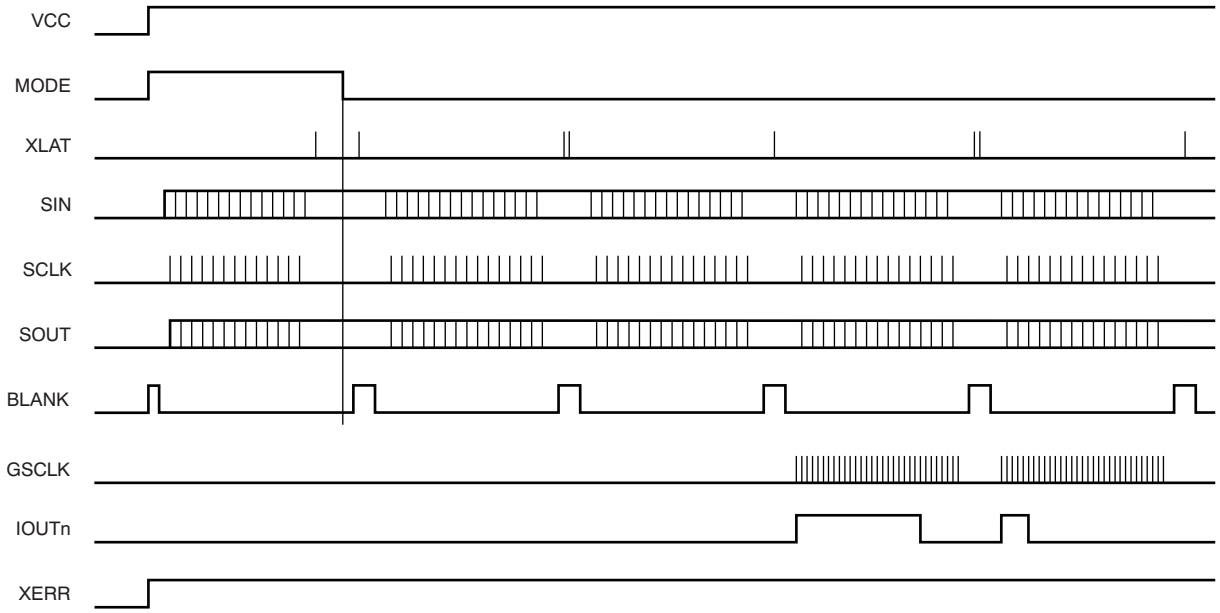


Figure 39. Power-On Sequence—1 (XHALF = Low)
(BLANK goes high immediately after power-on)

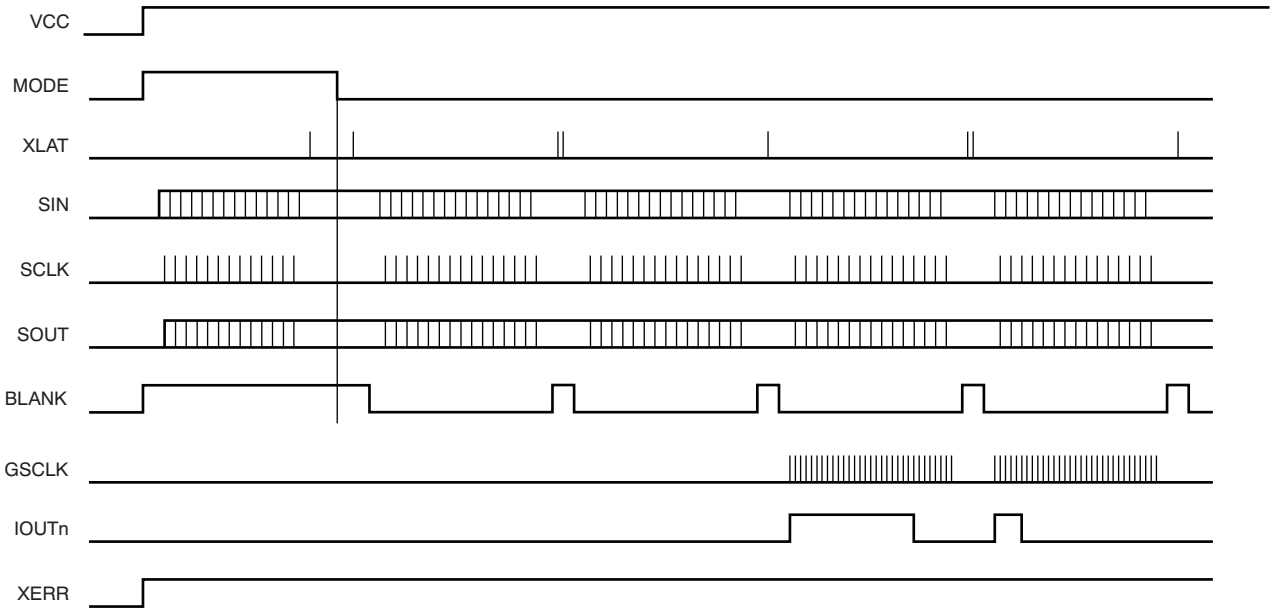


Figure 40. Power-On Sequence—2 (XHALF = Low)
(BLANK stays high after power-on, GS mode starts with BLANK = High)

Revision History

Changes from Revision A (April 2008) to Revision B **Page**

- Changed device status from Mixed Status to Production Data for QFN package 1
- Updated front page graphic 1
- Deleted footnote 2 from *Package/Ordering Information* table; device status for the TLC5946RHB is now Production Data..... 2
- Updated Figure 32 22

Changes from Revision original (March 2008) to Revision A **Page**

- Added footnote 2 to Package/Ordering Information table to indicate device status for the TLC5946RHB is now Product Preview..... 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00479PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5946	Samples
TLC5946PW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJ5946	Samples
TLC5946PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5946	Samples
TLC5946PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5946	Samples
TLC5946PWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJ5946	Samples
TLC5946RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5946	Samples
TLC5946RHBRG4	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5946	Samples
TLC5946RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5946	Samples
TLC5946RHBTG4	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5946	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

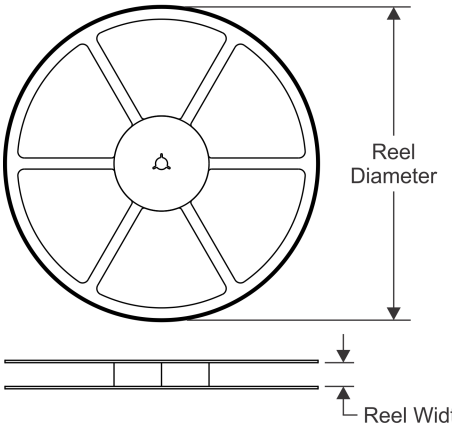
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

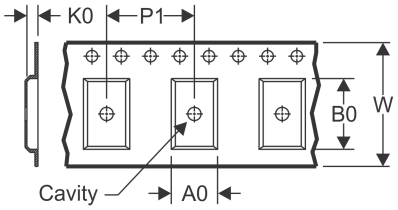
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

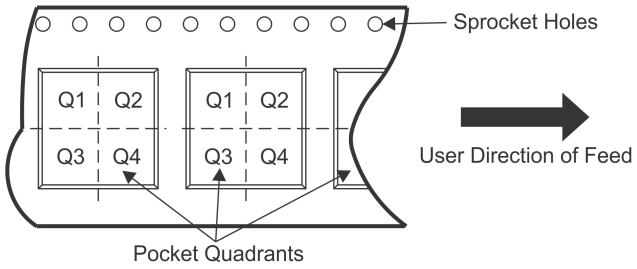


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

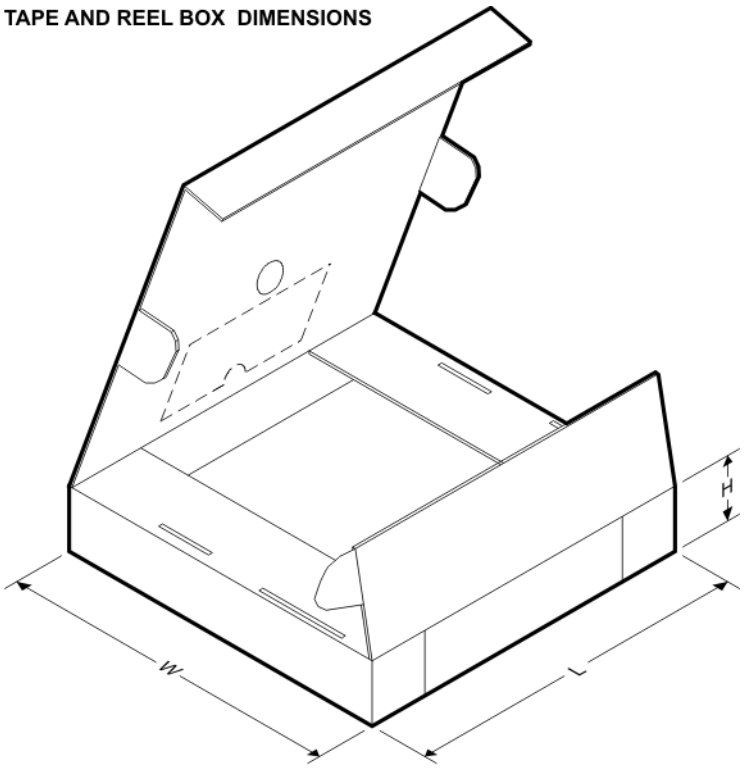
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5946PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC5946PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC5946RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TLC5946RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

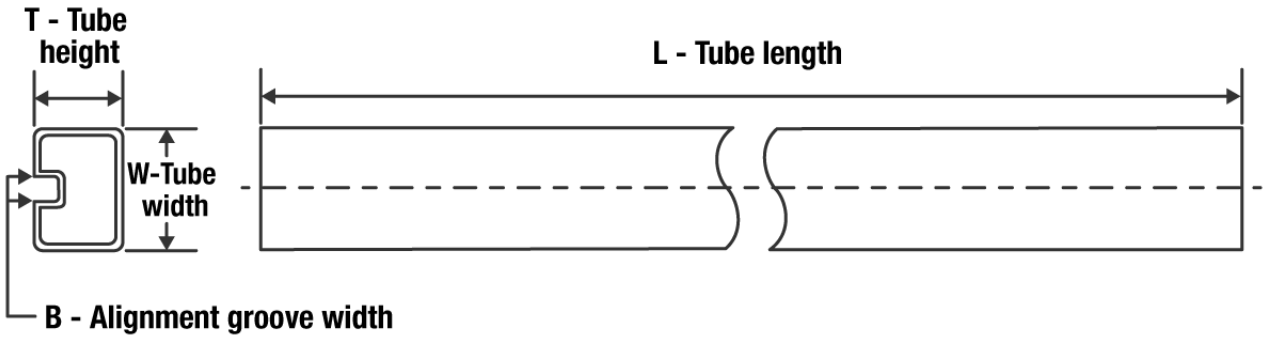
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5946PWPR	HTSSOP	PWP	28	2000	853.0	449.0	35.0
TLC5946PWR	TSSOP	PW	28	2000	853.0	449.0	35.0
TLC5946RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TLC5946RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

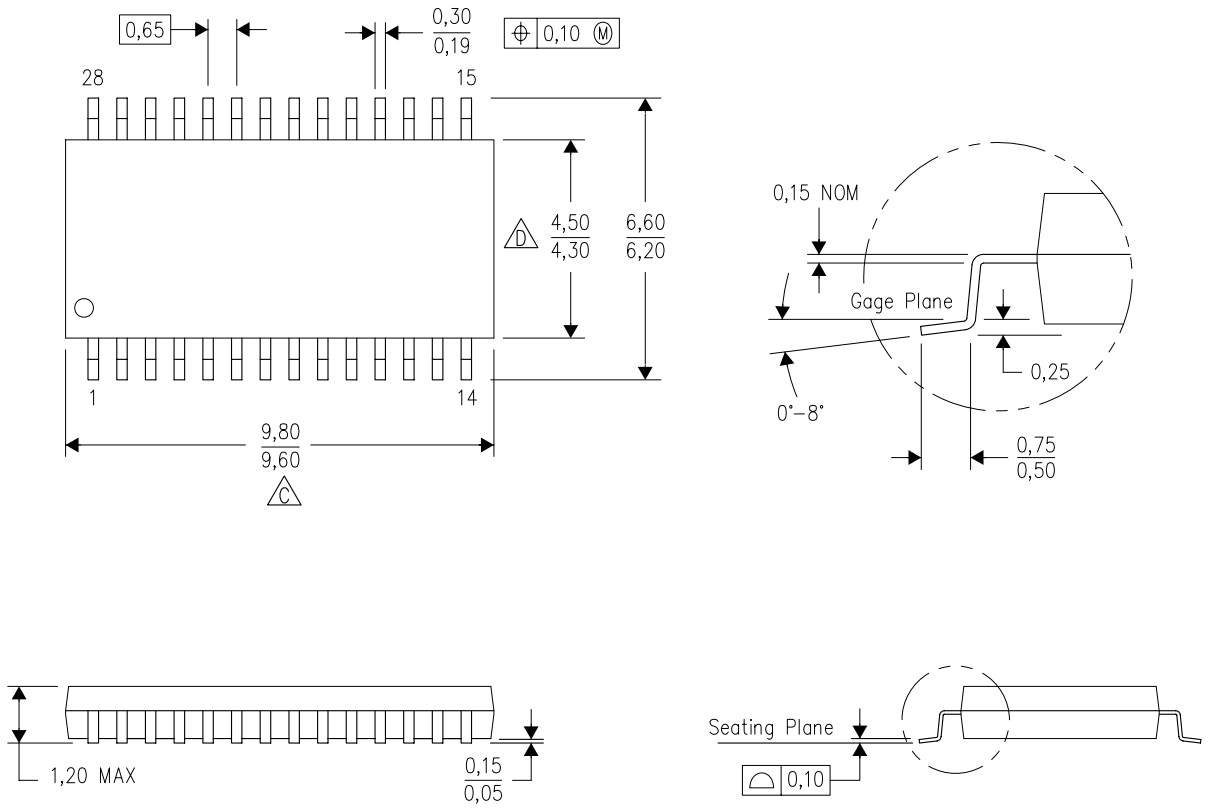
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5946PW	PW	TSSOP	28	50	530	10.2	3600	3.5
TLC5946PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5

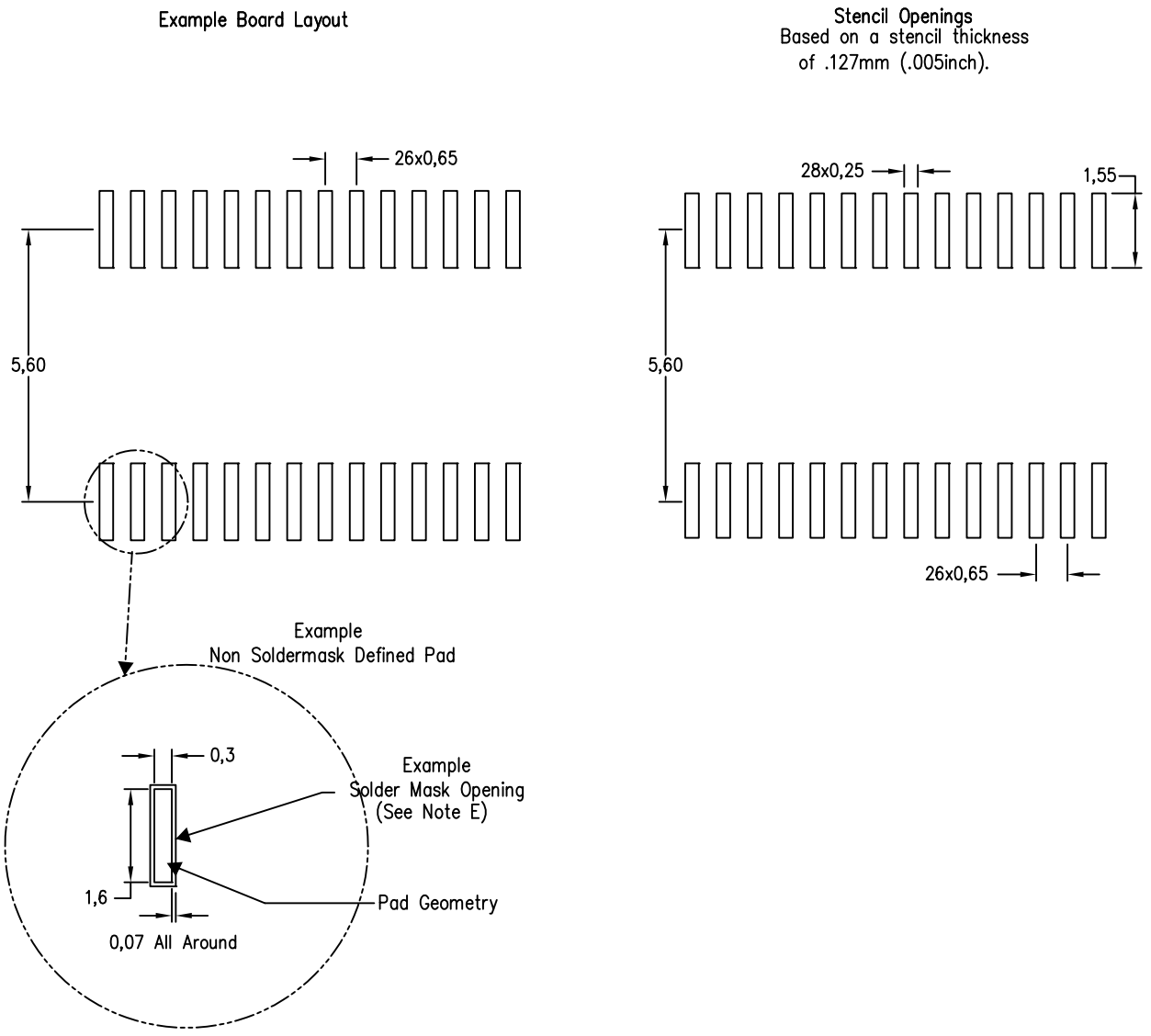
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

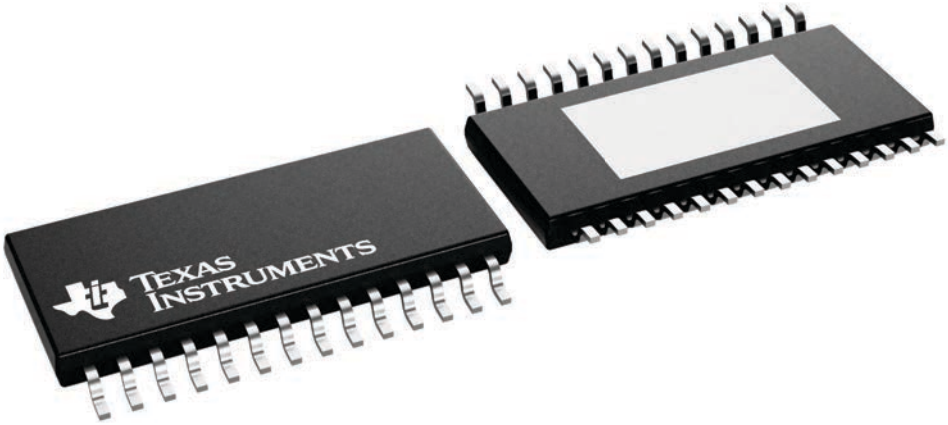
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

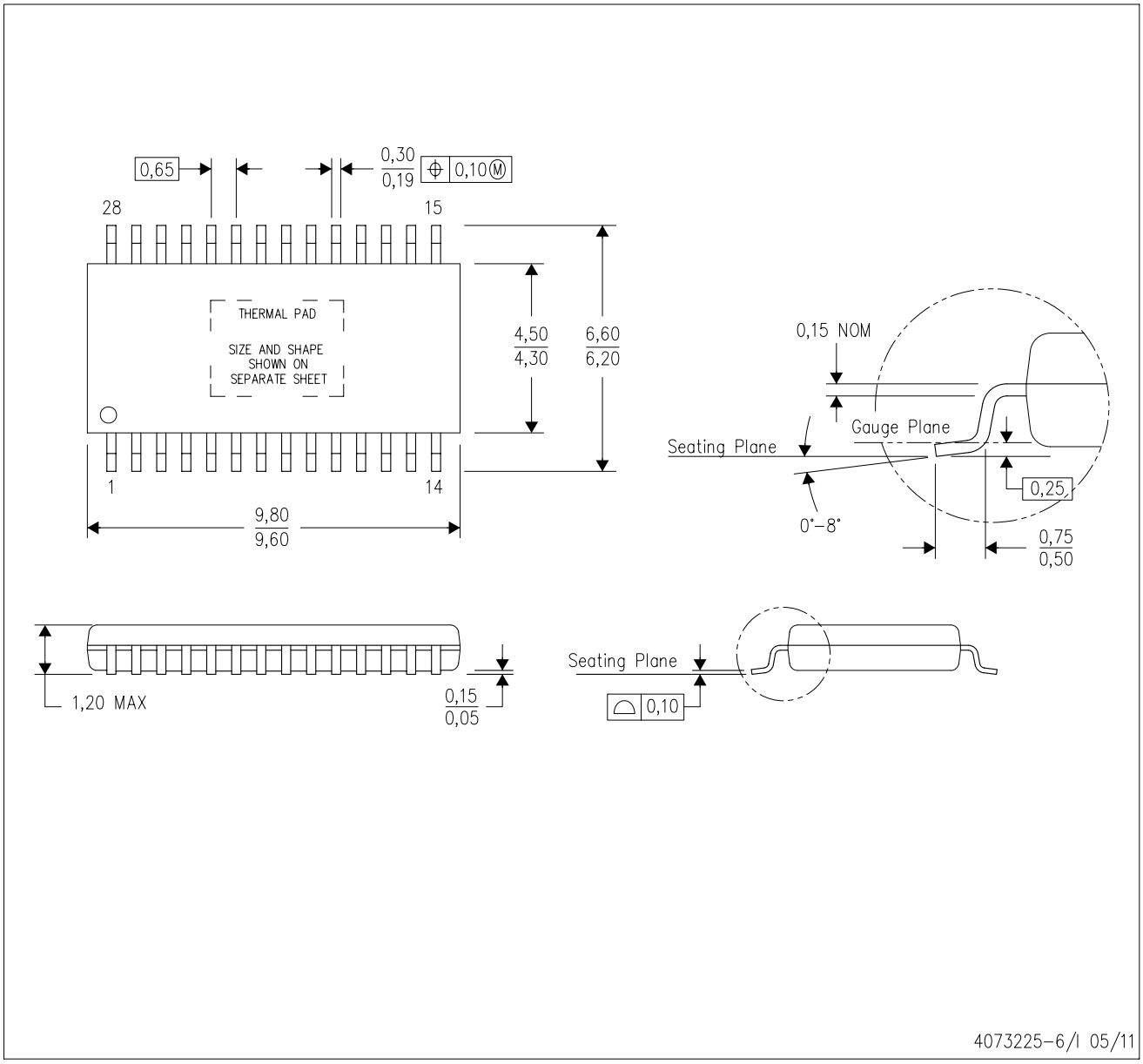
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

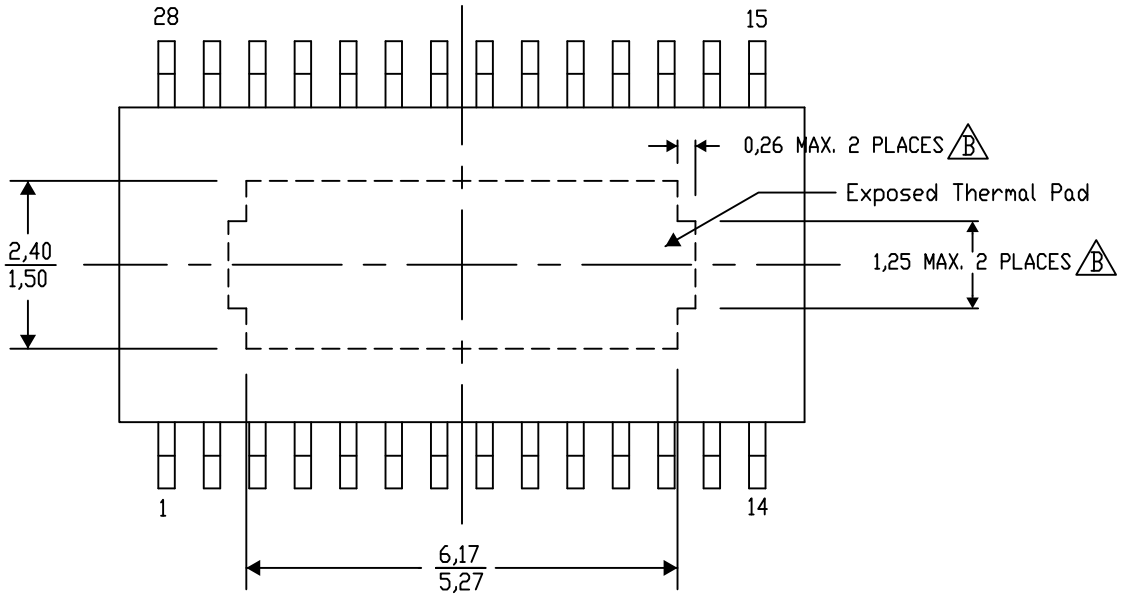
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

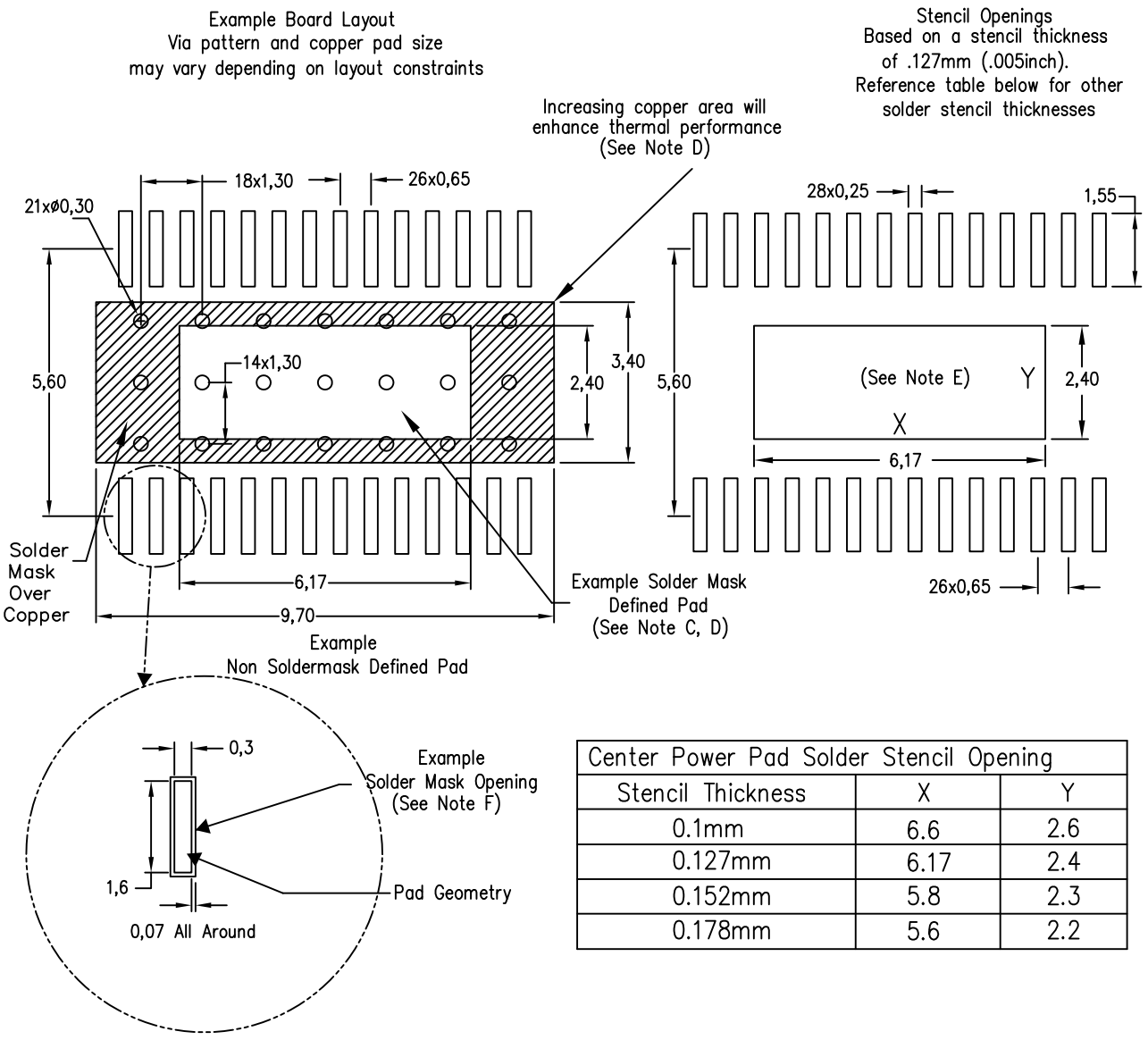
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

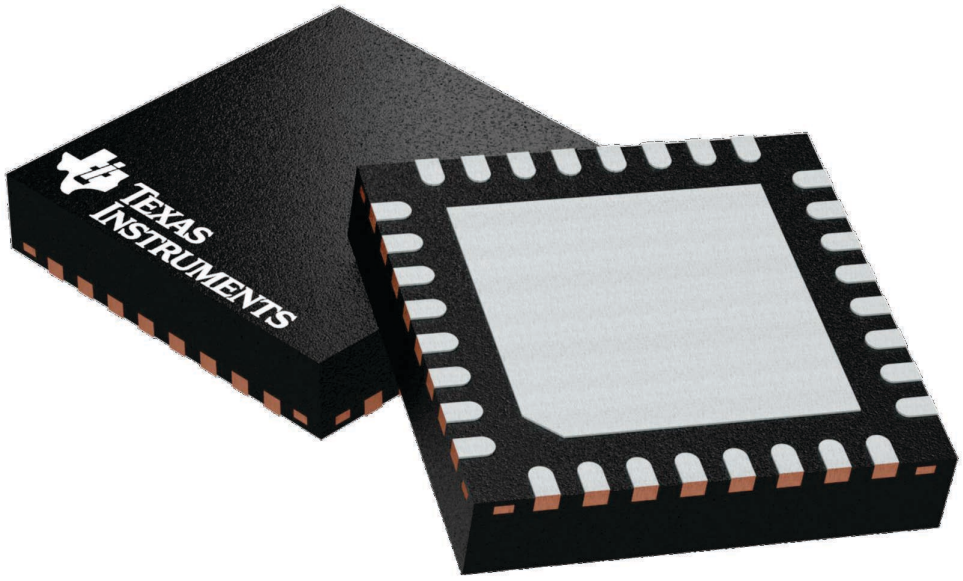
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

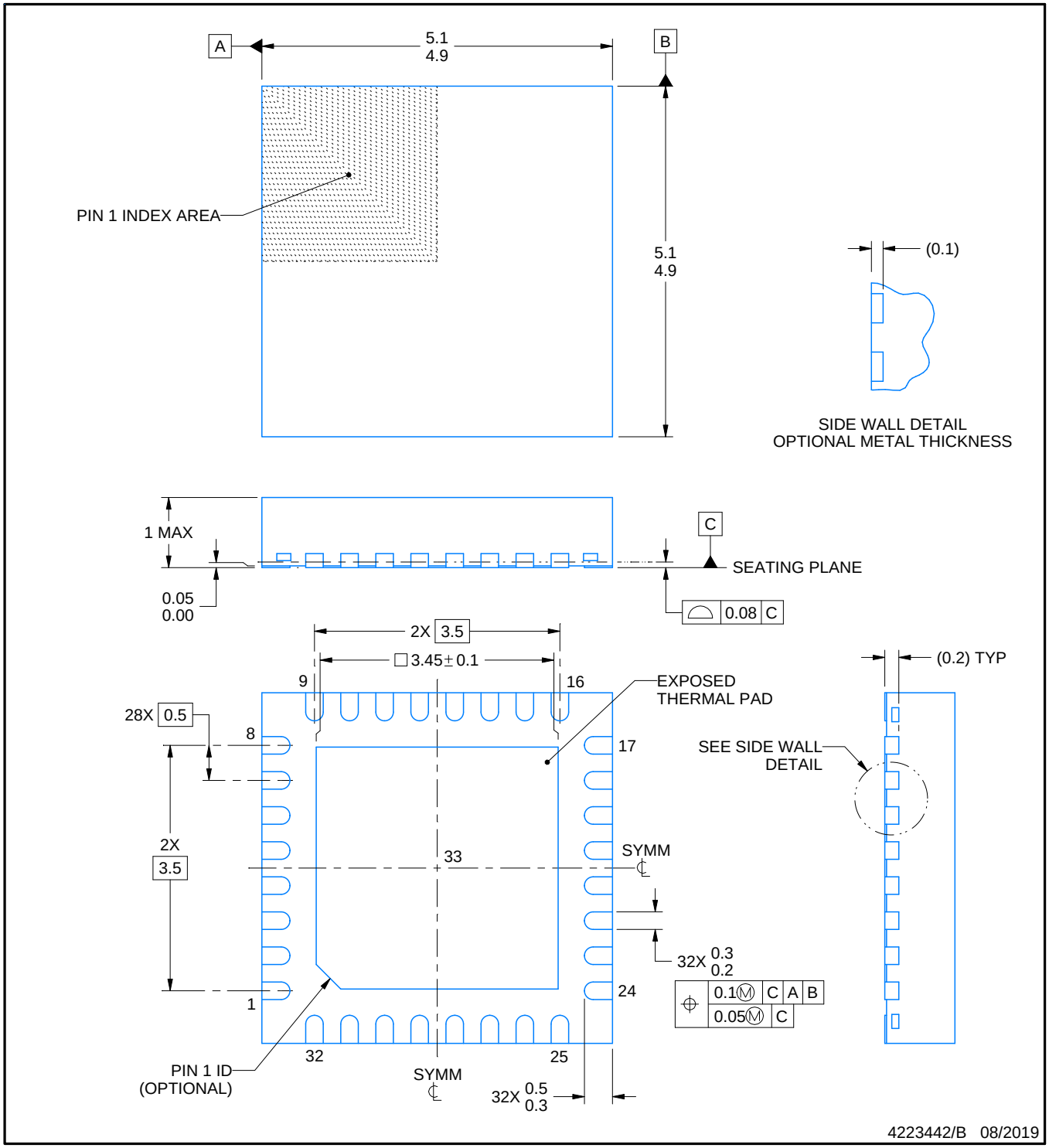
4224745/A

RHB0032E

PACKAGE OUTLINE

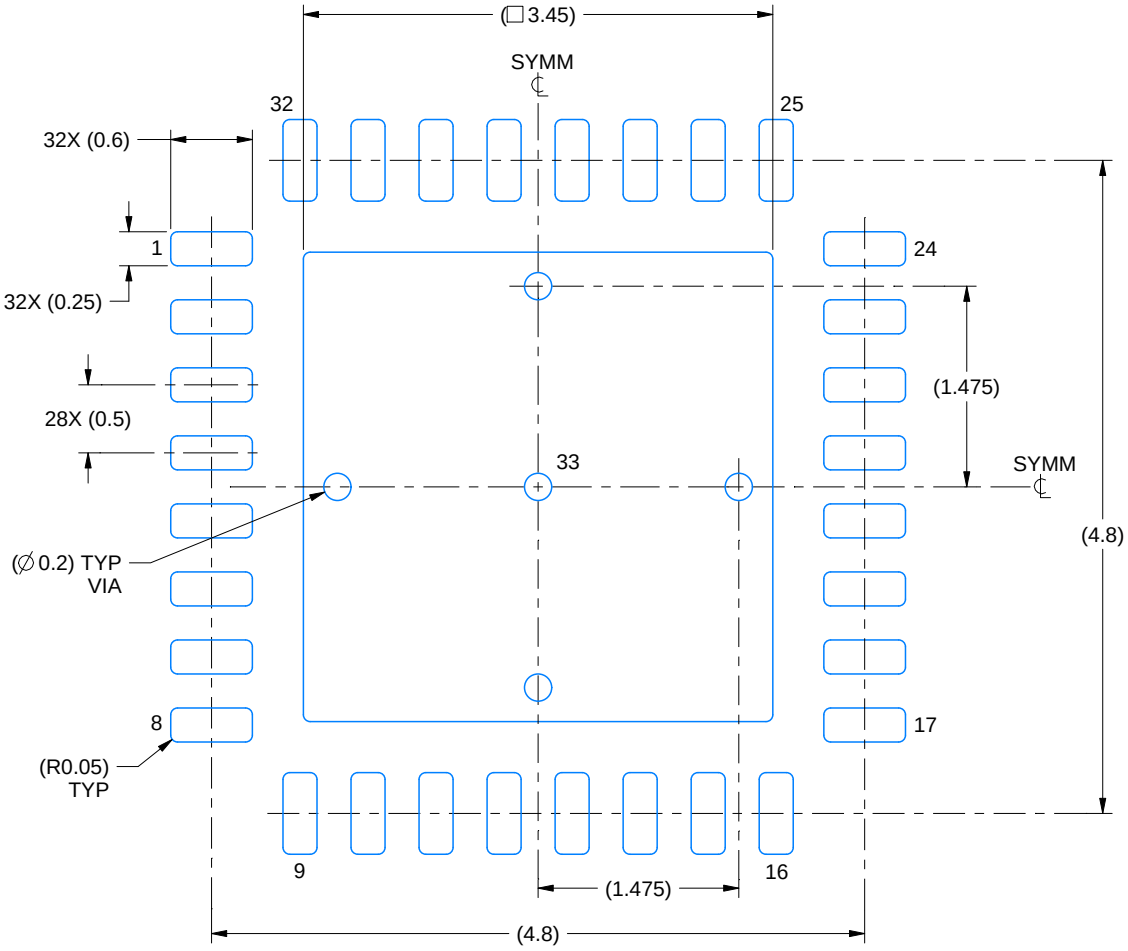
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

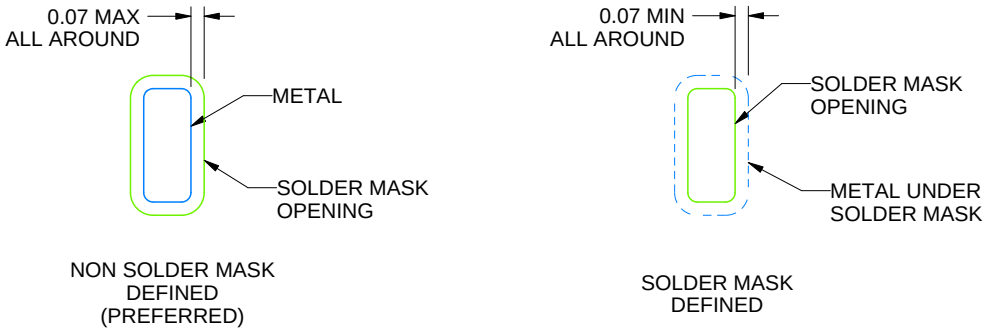


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

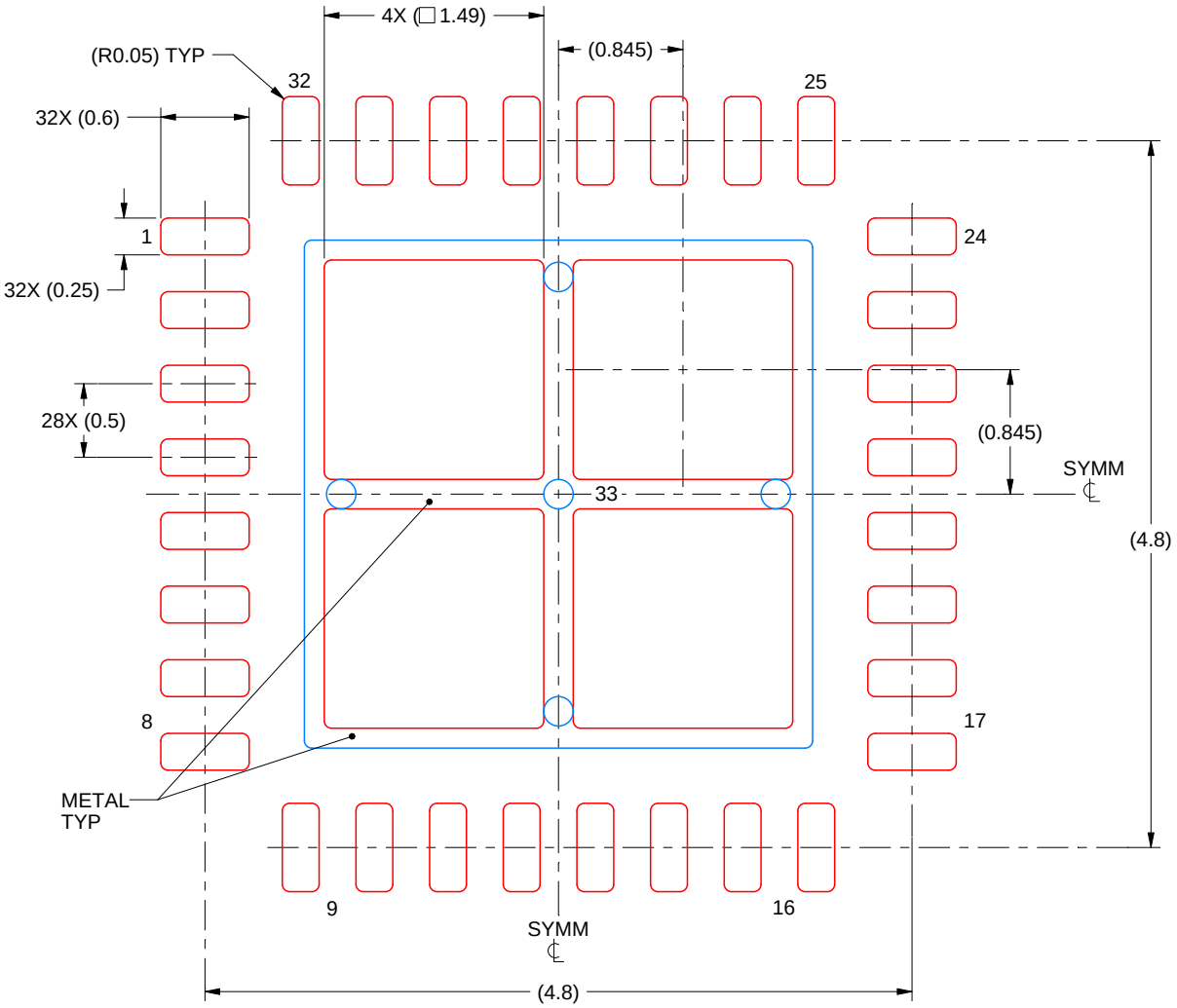


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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