具有延时时间和手动复位功能的 TPS3703-Q1 过压和欠压复位 IC

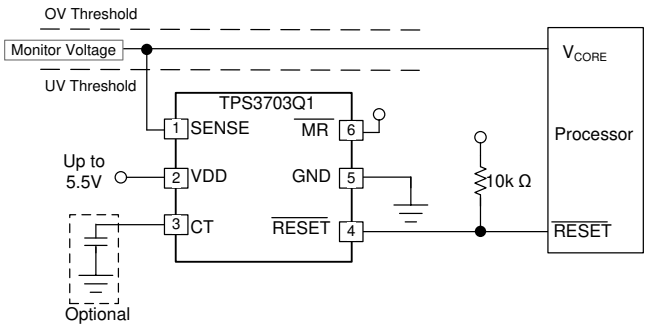
1 特性

- 符合汽车类 应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 的环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C7B
- 输入电压范围：1.7V 至 5.5V
- 欠压锁定 (UVLO)：1.7V
- 低静态电流：7μA（最大值）
- 高阈值精度：
  - ±0.25%（典型值）
  - ±0.7%（-40°C 至 +125°C）
- 固定窗口阈值电平
  - 50mV 阶跃（500mV 至 1.3V）
  - 1.5V、1.8V、2.5V、2.8V、2.9V、3.3V、5V
  - 仅使用 UV 阈值
  - 窗口公差范围为 ±3% 至 ±7%
- 用户可调的电压阈值电平
- 内部毛刺抑制和迟滞
- 固定延时时间选项：50μs、1ms、5ms、10ms、20ms、100ms、200ms
- 使用单个外部电容器的可编程延时时间选项
- 漏极开路低电平有效 UV 和 OV 监控器
- $\overline{\text{RESET}}$ 电压锁存输出模式

2 应用

- 高级驾驶员辅助系统 (ADAS)
- 摄像头
- 传感器融合
- HEV/EV
- 基于 FPGA、ASIC 和 DSP 的系统

集成式过压和欠压检测



3 说明

TPS3703-Q1 器件是一款集成式过压 (OV) 和欠压 (UV) 监控器或复位 IC，采用业界最小的 6 引脚 DSE 封装。这款高精度的电压监控器非常适合采用低电压电源轨的系统，并具有非常小的电源容差裕度。低阈值迟滞可防止在受监控的电压处于正常工作范围内时发出虚假复位信号。并且内置有毛刺抑制功能和噪声滤波器，进一步消除了错误信号所导致的错误复位。

TPS3703-Q1 不需要使用任何外部电阻器来设置过压和欠压复位阈值，因此进一步优化了整体精度、成本、解决方案大小并提高了安全系统的可靠性。电容器时间 (CT) 引脚用于在每个器件的两个可用复位延时时间之间进行选择，还可以连接一个电容器以调整复位延时时间。单独的 SENSE 输入引脚和 VDD 引脚可实现高可靠性系统所需的冗余。

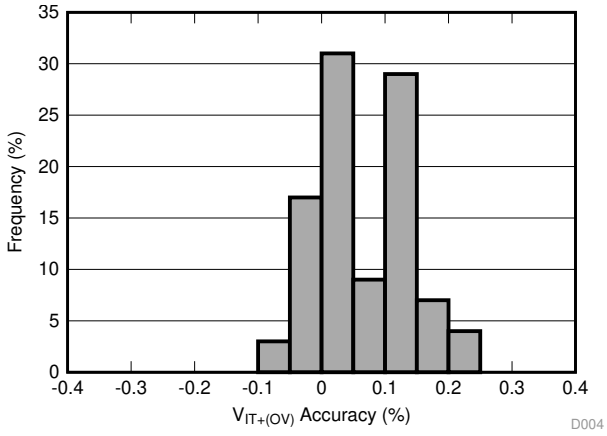
此器件的低典型静态电流规格为 4.5μA（典型值）。TPS3703-Q1 适用于汽车 应用 ，符合 AEC-Q100 1 级标准。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS3703-Q1	WSON (6)	1.50mm x 1.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型过压精度分布



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (May 2019) to Revision B — **Page**

- 已删除 仅删除了整篇文档中的 OV ... 1
- 已更改 将整个文档中的阈值公差更改为窗口公差 ... 1
- Added new voltage variants for window and UV only. ... 3
- Added pinout description for package. ... 4
- 已更改 functional block diagram for clarity between variants. ... 13
- 已添加 UV only normal operation condition. ... 15
- 已更改 equation to correctly reflect resistor divider. ... 20
- 已更改 to R_1 from R_{SENSE} ... 20

Changes from Original (November 2018) to Revision A — **Page**

- 已更改 将“预告信息”更改为“生产数据”版本 ... 1

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5 Device Comparison Table

Table 1 shows the released versions of the TPS3703-Q1, including the nominal undervoltage and overvoltage thresholds. For all possible voltages, window tolerance, time delays, and UV threshold options, see Table 7. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

Table 1. Device Comparison Table

PART NUMBER	V_{MON}	TIME DELAY (ms)			WINDOW TOLERANCE
		CT Pin = Capacitor	CT Pin= Open	CT Pin = VDD	
TPS3703B3080DSERQ1	0.80 V	Programmable	1 ms	20 ms	± 3%
TPS3703E4080DSERQ1	0.80 V	Programmable	10 ms	200 ms	– 4%
TPS3703A5090DSERQ1	0.90 V	Programmable	10 ms	200 ms	± 5%
TPS3703A7110DSERQ1	1.10 V	Programmable	10 ms	200 ms	± 7%
TPS3703A4120DSERQ1	1.20 V	Programmable	10 ms	200 ms	± 4%
TPS3703A7120DSERQ1	1.20 V	Programmable	10 ms	200 ms	± 7%
TPS3703A7125DSERQ1	1.25 V	Programmable	10 ms	200 ms	± 7%
TPS3703A4180DSERQ1	1.8 V	Programmable	10 ms	200 ms	± 4%
TPS3703B5180DSERQ1	1.8 V	Programmable	1 ms	20 ms	± 5%
TPS3703A5180DSERQ1	1.8 V	Programmable	10 ms	200 ms	± 5%
TPS3703A7180DSERQ1	1.8 V	Programmable	10 ms	200 ms	± 7%
TPS3703B4250DSERQ1	2.5 V	Programmable	1 ms	20 ms	± 4%
TPS3703A4280DSERQ1	2.8 V	Programmable	10 ms	200 ms	± 4%
TPS3703A7280DSERQ1	2.8 V	Programmable	10 ms	200 ms	± 7%
TPS3703A5290DSERQ1	2.9 V	Programmable	10 ms	200 ms	± 5%
TPS3703A4330DSERQ1	3.3 V	Programmable	10 ms	200 ms	± 4%
TPS3703A7330DSERQ1	3.3 V	Programmable	10 ms	200 ms	± 7%
TPS3703C7500DSERQ1	5 V	Programmable	5 ms	100 ms	± 7%

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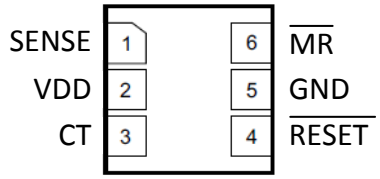
6 Pin Configuration and Functions

DSE Package
6-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SENSE	I	Input for the monitored supply voltage rail. When the SENSE voltage goes above the overvoltage threshold or below the undervoltage threshold, the $\overline{\text{RESET}}$ pin is driven low. Connect to VDD pin if monitoring VDD supply voltage.
2	VDD	I	Supply voltage input pin. Good analog design practice is to place a 0.1-μF ceramic capacitor close to this pin.
3	CT	I	Capacitor time delay pin. The CT pin offers two fixed time delays by connecting CT pin to VDD or leaving it floating. Delay time can be programmed by connecting an external capacitor reference to ground.
4	$\overline{\text{RESET}}$	O	Active-low, open-drain output. This pin goes low when the SENSE voltage rises above the internally overvoltage threshold (V_{IT+}) or below the undervoltage threshold (V_{IT-}). See the timing diagram in 图 24 for more details. Connect this pin to a pull-up resistor terminated to the desired pull-up voltage.
5	GND	—	Ground
6	$\overline{\text{MR}}$	I	Manual reset (MR), pull this pin to a logic low ($V_{\overline{MR}_L}$) to assert a reset signal . After the $\overline{\text{MR}}$ pin is deasserted the output goes high after the reset delay time(t_D) expires. $\overline{\text{MR}}$ can be left floating when not in use.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	6	V
Voltage	$V_{\overline{RESET}}$	–0.3	6	V
Voltage	V_{CT}	–0.3	6	V
Voltage	V_{SENSE}	–0.3	6	V
Voltage	$V_{\overline{MR}}$	–0.3	6	V
Current	$I_{\overline{RESET}}$		±40	mA
Temperature [2]	Continuous total power dissipation	See the Thermal Information		
	Operating junction temperature, T_J	-40	150	°C
	Operating free-air temperature, T_A	-40	150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.7		5.5	V
V_{SENSE}	Input pin voltage	0		5.5	V
V_{CT}	CT pin voltage [1] [2]			V_{DD}	V
$V_{\overline{RESET}}$	Output pin voltage	0		5.5	V
$V_{\overline{MR}}$	$\overline{MR}$ pin Voltage [3]	0		5.5	V
$I_{\overline{RESET}}$	Output pin current	0.3		10	mA
T_J	Junction temperature (free-air temperature)	-40		125	℃

(1) CT pin connected to VDD pin requires a pullup resistor; 10 kΩ is recommended.
(2) The maximum rating is V_{DD} or 5.5 V, whichever is smaller.
(3) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$.

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7.4 Thermal Information

THERMAL METRIC[1]		TPS3870-Q1 DSE (WSON) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	86.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	86.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At 1.7 V ≤ V_{DD} ≤ 5.5 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 10 kΩ to V_{DD}, $\overline{RESET}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at V_{DD} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		1.7		5.5	V
UVLO	Under Voltage Lockout[1]	V_{DD} falling below 1.7 V	1.2		1.7	V
V_{POR}	Power on reset voltage[2]	V_{OL}(max) = 0.25 V, I_{OUT} = 15 µA			1	V
$V_{IT+(OV)}$	Positive- going threshold accuracy		-0.7	±0.25	0.7	%
$V_{IT-(UV)}$	Negative-going threshold accuracy		-0.7	±0.25	0.7	%
V_{HYS}	Hysteresis Voltage[3]		0.3	0.55	0.8	%
I_{DD}	Supply current	V_{DD} ≤ 5.5 V		4.5	7	µA
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = 5 V		1	1.5	µA
V_{OL}	Low level output voltage	V_{DD} = 1.7 V, I_{OUT} = 0.4 mA			250	mV
		V_{DD} = 2 V, I_{OUT} = 3 mA			250	mV
		V_{DD} = 5 V, I_{OUT} = 5 mA			250	mV
I_{LKG}	Open drain output leakage current	V_{DD} = $V_{\overline{RESET}}$ = 5.5 V			300	nA
$V_{\overline{MR}_L}$	$\overline{MR}$ logic low input				0.3	V
$V_{\overline{MR}_H}$	$\overline{MR}$ logic high input		1.4			V
V_{CT_H}	High level CT pin voltage		1.4			V
$R_{\overline{MR}}$	Manual reset Internal pullup resistance			100		KΩ
I_{CT}	CT pin charge current		337	375	413	nA
V_{CT}	CT pin comparator threshold voltage[4]		1.133	1.15	1.167	V

(1) $\overline{RESET}$ pin is driven low when V_{DD} falls below UVLO.
(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state.
(3) Hysteresis is with respect of the tripoint ($V_{IT-(UV)}$, $V_{IT+(OV)}$).
(4) V_{CT} voltage refers to the comparator threshold voltage that measures the voltage level of the external capacitor at CT pin.

7.6 Timing Requirements

At 1.7 V ≤ V_{DD} ≤ 5.5 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 10 kΩ to V_{DD}, $\overline{RESET}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at V_{DD} = 3.3 V.

			MIN	NOM	MAX	UNIT
t_D	Reset time delay, TPS3870J	CT = Open	7	10	13	ms
t_D	Reset time delay, TPS3870J	CT = 10 kΩ to V_{DD}	140	200	260	ms
t_D	Reset time delay, TPS3870K	CT = Open	0.7	1	1.3	ms
t_D	Reset time delay, TPS3870K	CT = 10 kΩ to V_{DD}	14	20	26	ms
t_D	Reset time delay, TPS3870L	CT = Open	3.5	5	6.5	ms

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Timing Requirements (continued)

At 1.7 V ≤ V_{DD} ≤ 5.5 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 10 kΩ to V_{DD}, $\overline{RESET}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at V_{DD} = 3.3 V.

			MIN	NOM	MAX	UNIT
t_D	Reset time delay, TPS3870L	CT = 10 kΩ to V_{DD}	70	100	130	ms
t_D	Reset time delay, TPS3870M	CT = 10 kΩ to V_{DD} CT = Open		50		µs
t_{PD}	Propagation detect delay(1)(2)			15	30	µs
t_R	Output rise time(1)(3)			2.2		µs
t_F	Output fall time(1)(3)			0.2		µs
t_{SD}	Startup delay(4)			300		µs
$t_{GI\ (VIT-)}$	Glitch Immunity undervoltage $V_{IT-(UV)}$, 5% Overdrive(1)			3.5		µs
$t_{GI\ (VIT+)}$	Glitch Immunity overvoltage $V_{IT+(OV)}$, 5% Overdrive(1)			3.5		µs
$t_{GI\ (\overline{MR})}$	Glitch Immunity $\overline{MR}$ pin				25	ns
$t_{PD\ (\overline{MR})}$	Propagation delay from $\overline{MR}$ low to assert $\overline{RESET}$			500		ns
$t_{\overline{MR}_W}$	$\overline{MR}$ pin pulse width duration to assert $\overline{RESET}$		1			µs
$t_{D\ (\overline{MR})}$	$\overline{MR}$ reset time delay			t_D		ms

(1) 5% Overdrive from threshold. Overdrive % = [V_{SENSE} - V_{IT}] / V_{IT}; Where V_{IT} stands for $V_{IT-(UV)}$ or $V_{IT+(OV)}$
(2) t_{PD} measured from threhold trip point ($V_{IT-(UV)}$ or $V_{IT+(OV)}$) to $\overline{RESET}$ V_{OL} voltage
(3) Output transitions from V_{OL} to 90% for rise times and 90% to V_{OL} for fall times.
(4) During the power-on sequence, V_{DD} must be at or above $V_{DD\ (MIN)}$ for at least t_{SD} + t_D before the output is in the correct state.

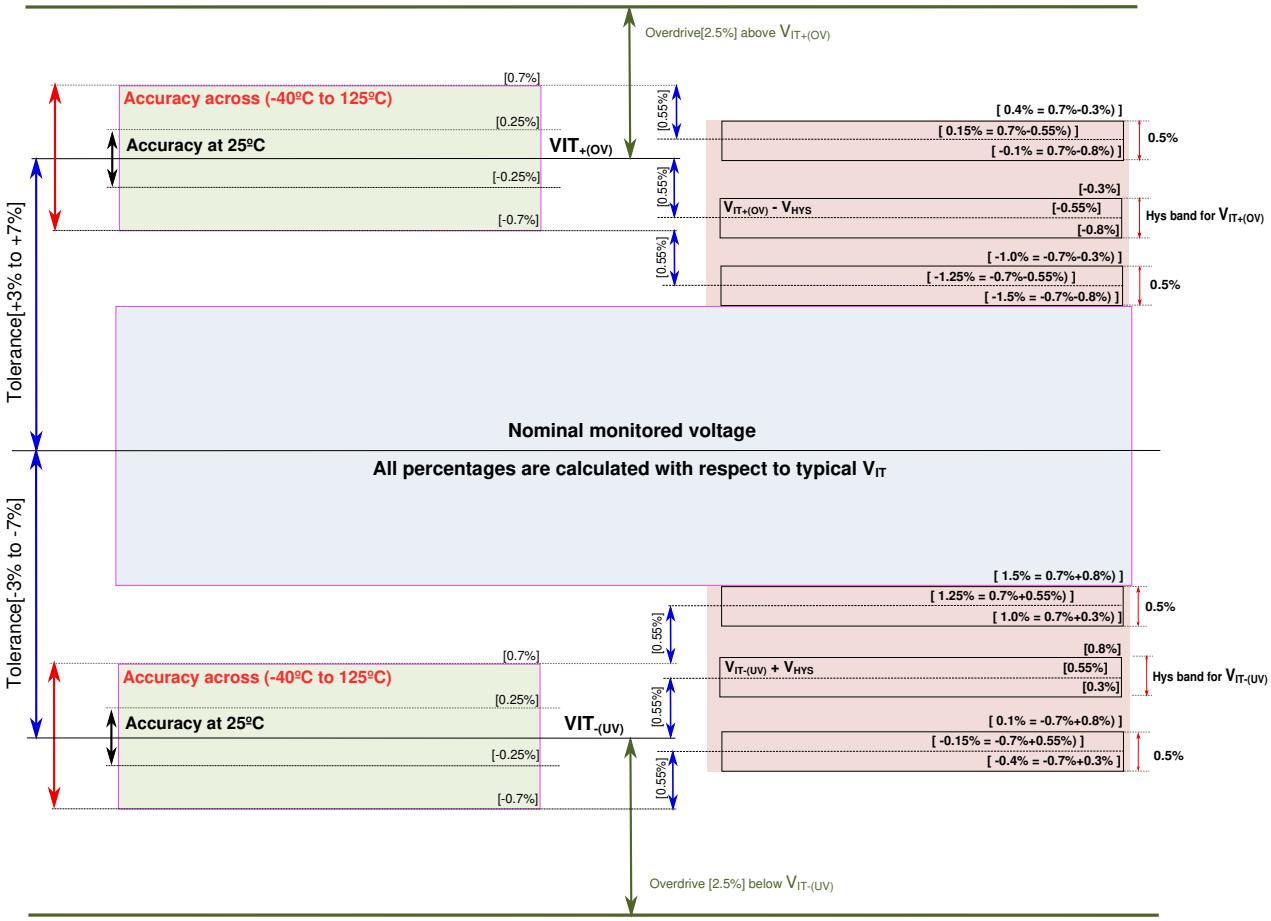
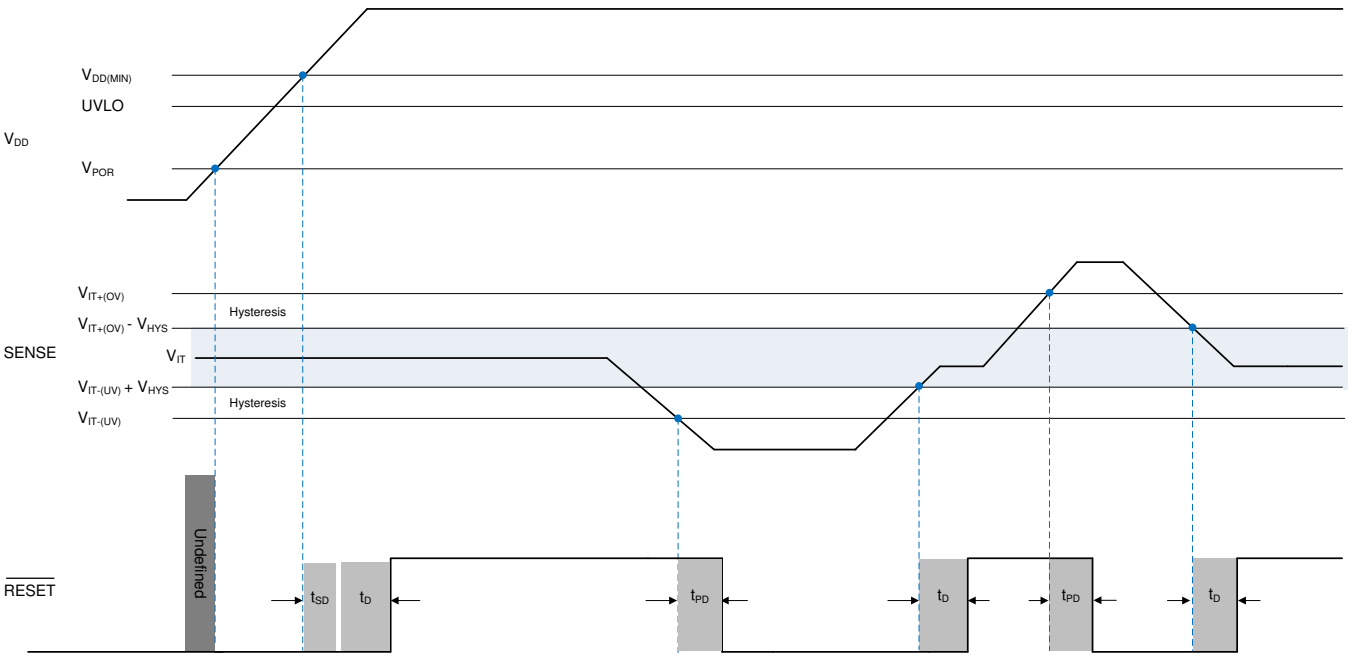


图 1. Voltage Threshold and Hysteresis Accuracy



(1) V_{DD} = 2 V, R_{PU} = 10 kΩ to V_{DD}

(2) Variant D (time delay bypass) has a ~40 µs pulse at $\overline{RESET}$ pin during power up window, this is present only when the power cycle off time is longer than 10 seconds, this behavior will not occur if SENSE pin is within window of operation during V_{DD} power up.

图 2. SENSE Timing Diagram

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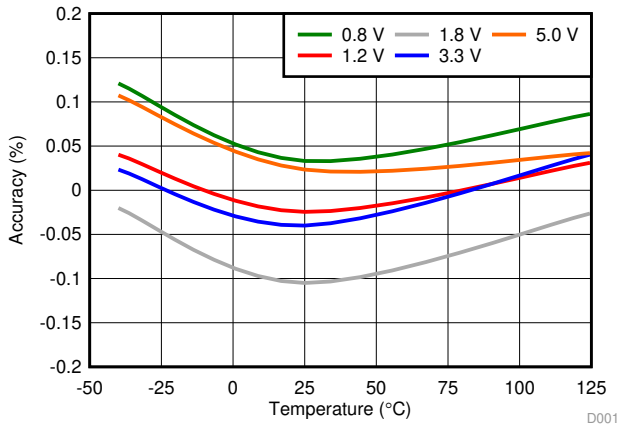
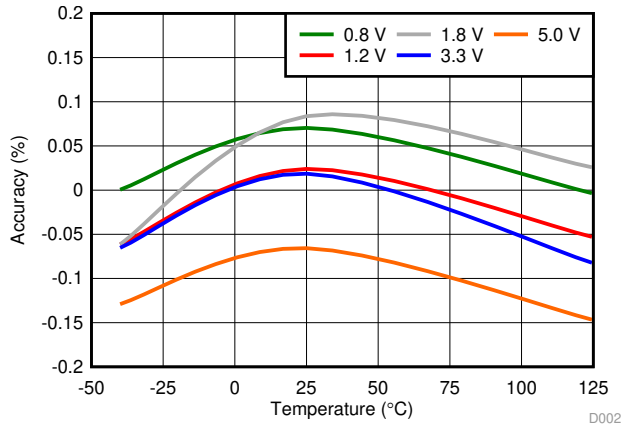
7.7 Typical Characteristics

At T_J = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.



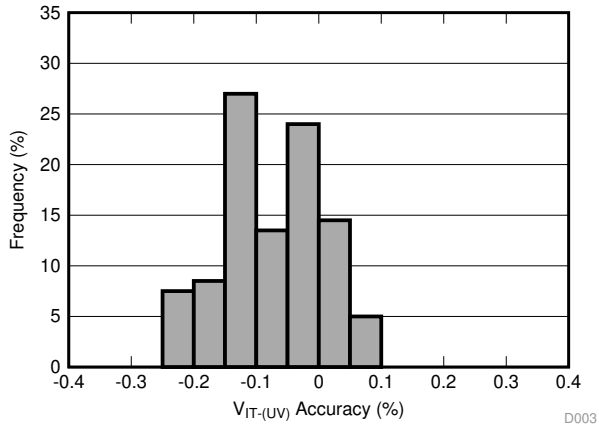
Tested across multiple voltage options

图 3. Undervoltage Accuracy vs Temperature



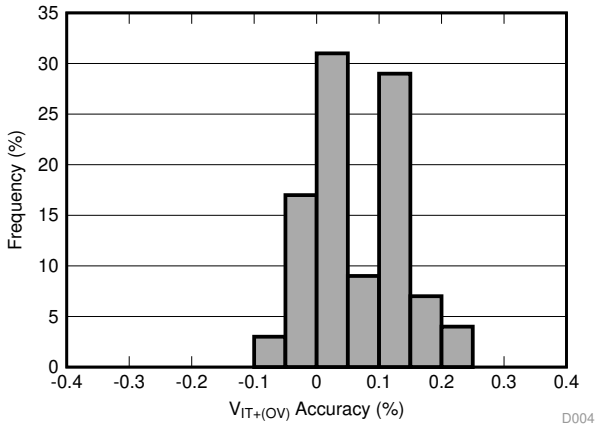
Tested across multiple voltage options

图 4. Overvoltage Accuracy vs Temperature



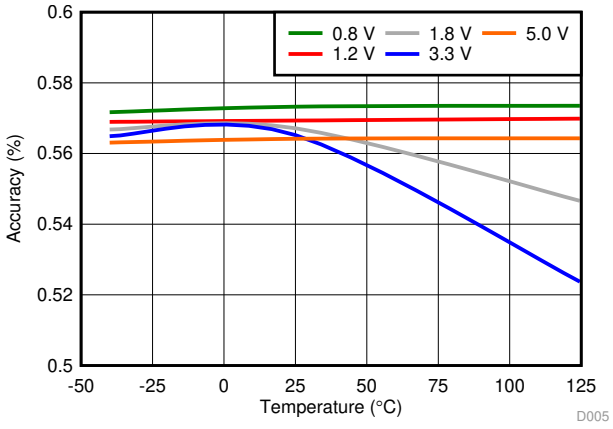
Sample Size of 100 TPS3703A7125 units

图 5. Undervoltage Accuracy Distribution



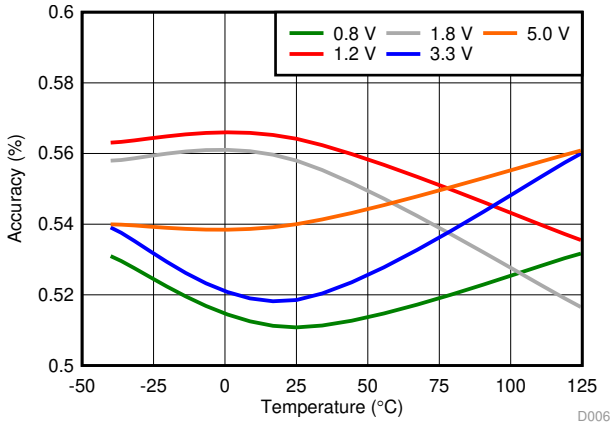
Sample Size of 100 TPS3703A7125 units

图 6. Overvoltage Accuracy Distribution



Tested across multiple voltage options

图 7. Undervoltage Hysteresis Voltage Accuracy vs Temperature

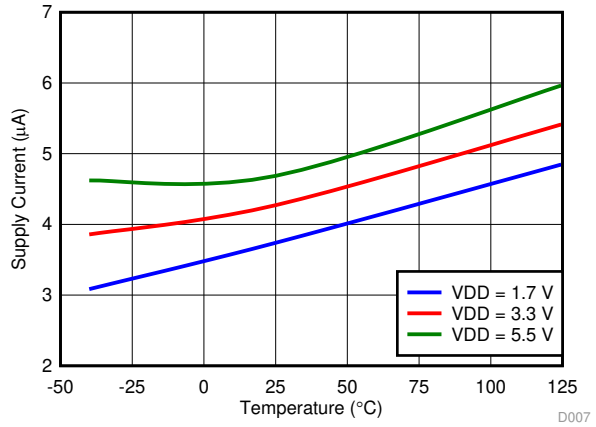


Tested across multiple voltage options

图 8. Overvoltage Hysteresis Voltage Accuracy vs Temperature

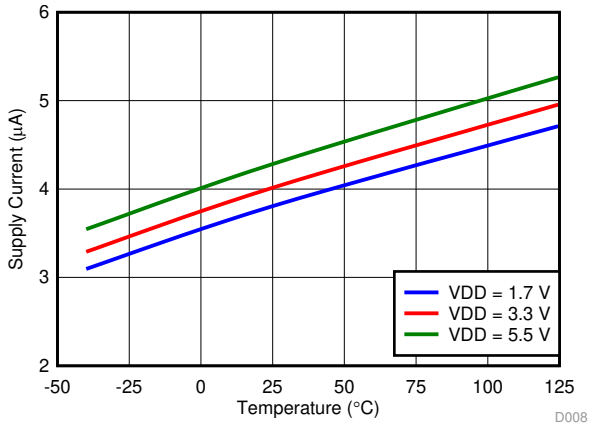
Typical Characteristics (接下页)

At T_J = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.



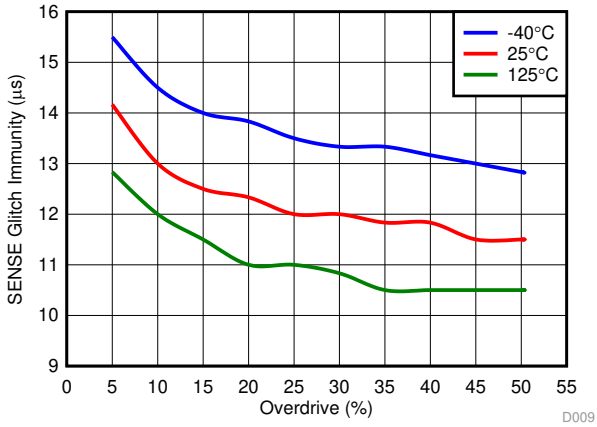
Output ($\overline{RESET}$ Pin) = High

图 9. Supply Current vs Temperature



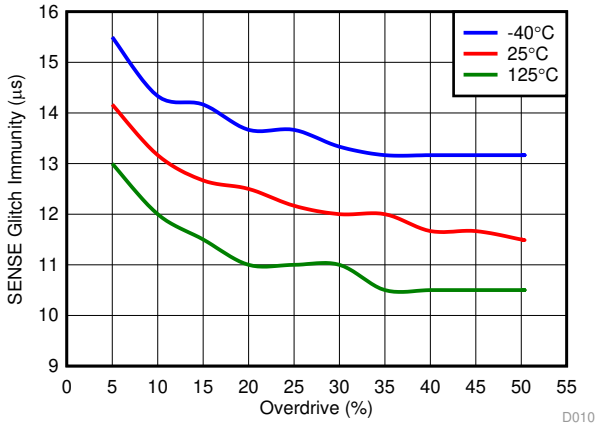
Output ($\overline{RESET}$ Pin) = Low

图 10. Supply Current vs Temperature



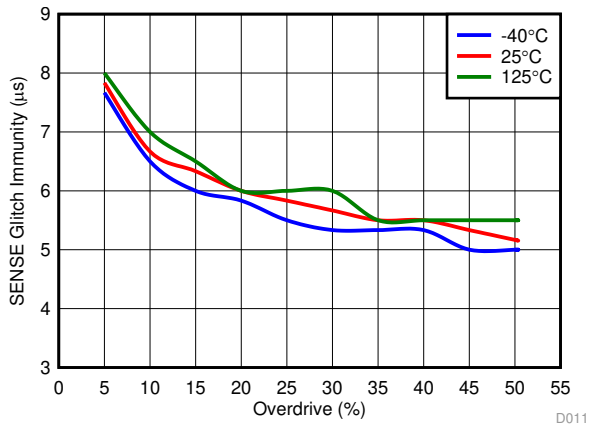
VDD = 1.7 V

图 11. SENSE Glitch Immunity (VIT-) vs Overdrive



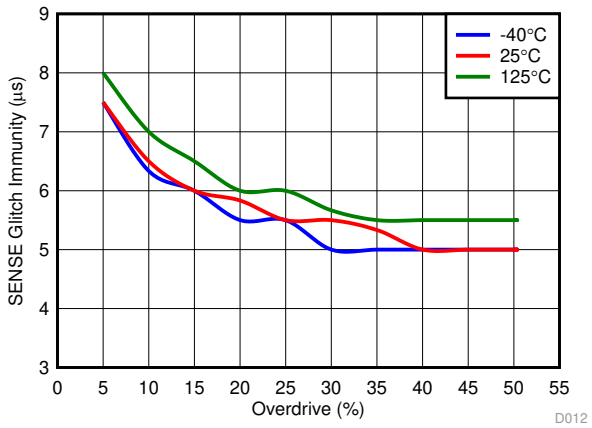
VDD = 1.7 V

图 12. SENSE Glitch Immunity (VIT+) vs Overdrive



VDD = 5.5 V

图 13. SENSE Glitch Immunity (VIT-) vs Overdrive



VDD = 5.5 V

图 14. SENSE Glitch Immunity (VIT+) vs Overdrive

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Typical Characteristics (接下页)

At T_J = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.

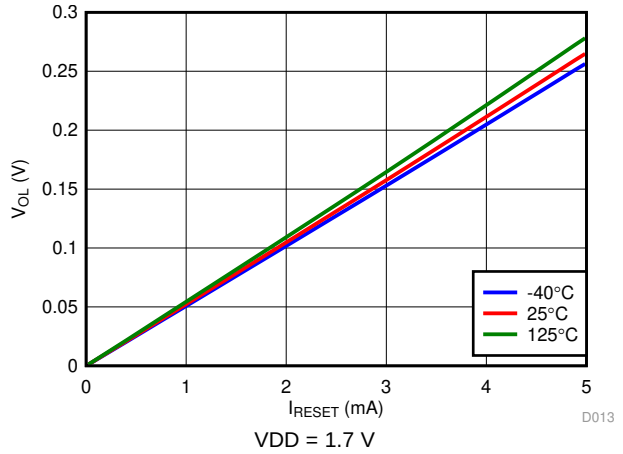

图 15. Low-Level Output Voltage vs RESET current

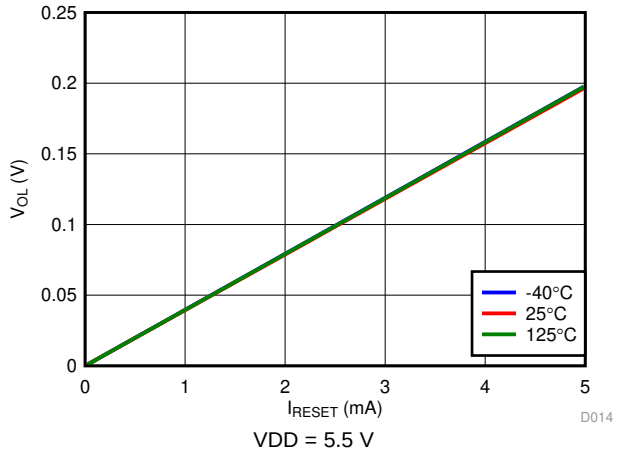

图 16. Low-Level Output Voltage vs RESET current

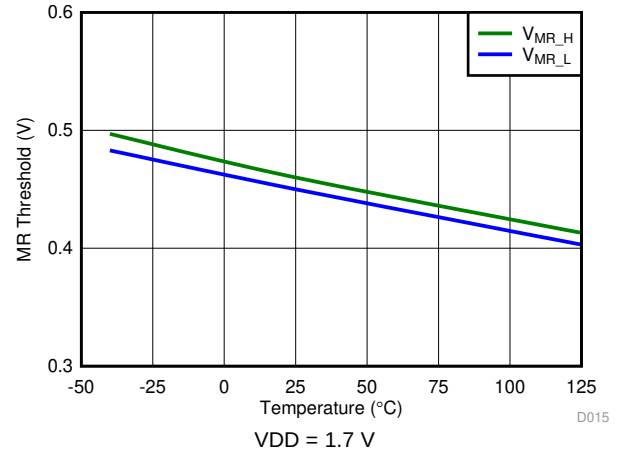

图 17. SET Threshold vs Temperature

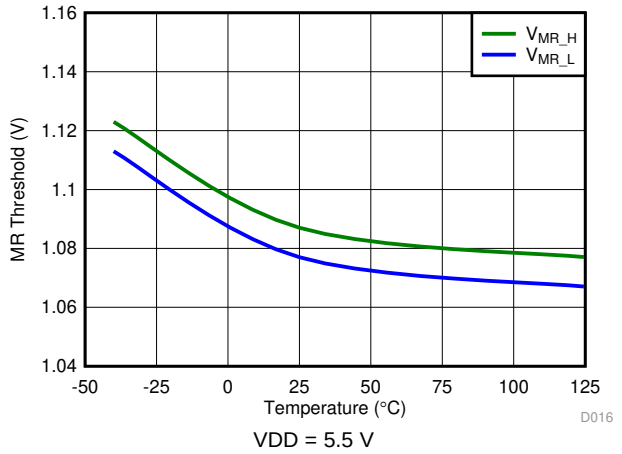

图 18. SET Threshold vs Temperature

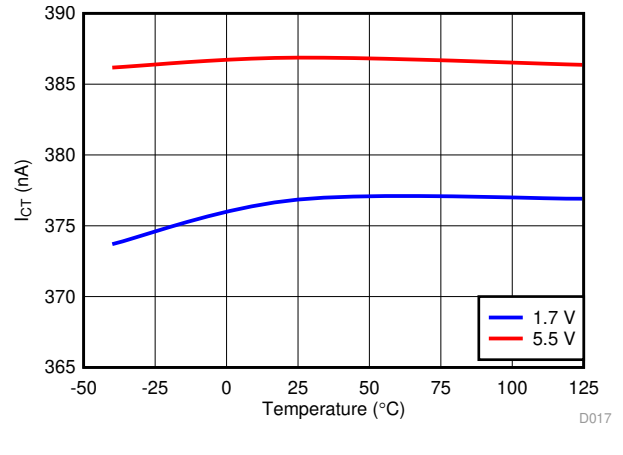

图 19. CT Current vs CT value

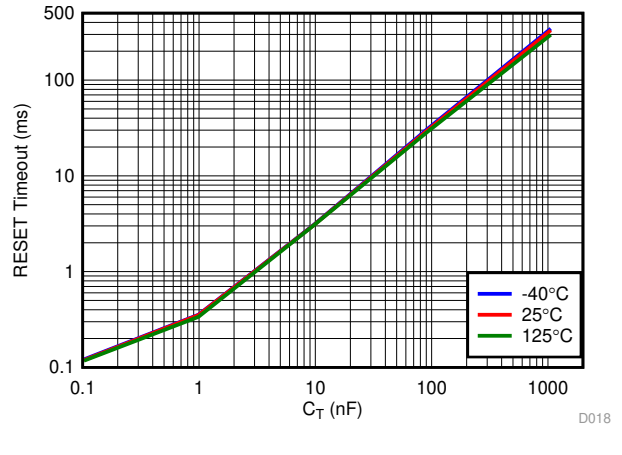

图 20. $\overline{\text{RESET}}$ Timeout vs CT Capacitor

Typical Characteristics (接下页)

At T_J = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.

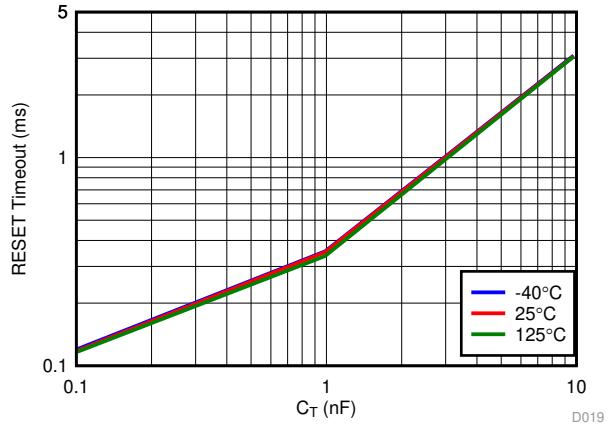

图 21. Timeout vs CT Capacitor (0.1 to 10 nF)

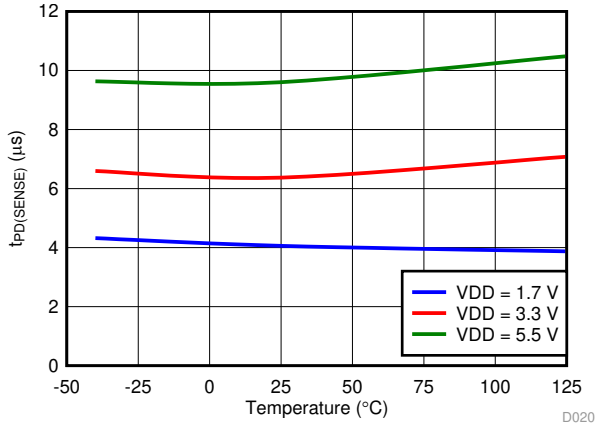

图 22. Detect Propagation Delay vs Temperature

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8 Detailed Description

8.1 Overview

The TPS3703-Q1 family of devices combines two voltage comparators and a precision voltage reference for overvoltage and undervoltage detection. The TPS3703-Q1 features a highly accurate window threshold voltages (±0.7% over temperature) and a variety voltage threshold variants.

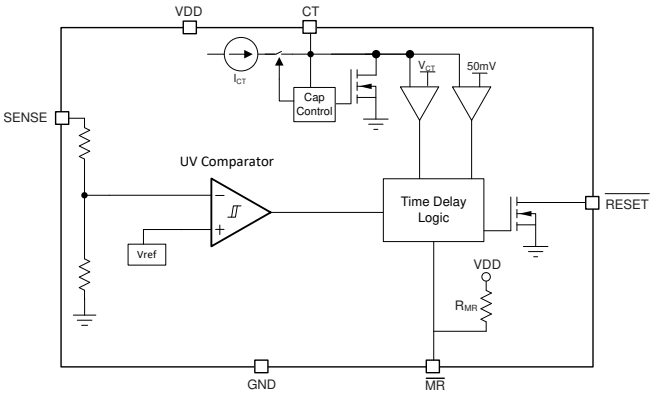
The TPS3703-Q1 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

TPS3703-Q1 version A, B and C has three time delay settings, two fixed by connecting CT pin to VDD through a resistor and leaving CT floating and a programmable time delay setting that only requires a single capacitor connected from CT pin to ground.

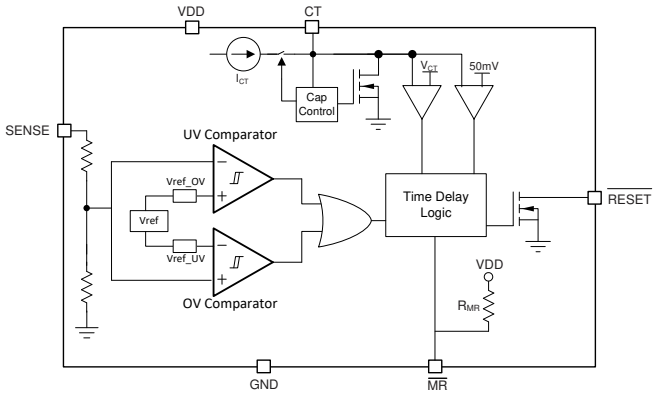
Manual Reset ($\overline{MR}$) allows for sequencing or hard reset by driving the $\overline{MR}$ pin below $V_{\overline{MR}_L}$.

The TPS3703-Q1 is designed to assert active low output signals when the monitored voltage is outside the safe window. The relationship between the monitored voltage and the states of the outputs is shown in 表 2.

8.2 Functional Block Diagram



Undervoltage Only Version



Window Version

*For all possible voltages, window tolerance, time delays, and UV threshold options, see Table 7.

8.3 Feature Description

8.3.1 VDD

The TPS3703-Q1 is designed to operate from an input voltage supply range between 1.7 V to 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 1-µF capacitor between the VDD pin and the GND pin.

V_{DD} needs to be at or above $V_{DD(MIN)}$ for at least the start-up delay (t_{SD}+ t_D) for the device to be fully functional.

8.3.2 SENSE

The TPS3703-Q1 combines two comparators with a precision reference voltage and a trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides noise immunity and ensures stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the SENSE input in order to reduce sensitivity to transient voltages on the monitored signal.

When monitoring VDD supply voltage, the SENSE pin can be connected directly to VDD. The output ($\overline{RESET}$) is high impedance when voltage at the SENSE pin is between upper and lower boundary of threshold.

Feature Description (接下页)

8.3.3 $\overline{\text{RESET}}$

In a typical TPS3703-Q1 application, the $\overline{\text{RESET}}$ output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the enable input of a voltage regulator [such as a DC-DC converter or low-dropout regulator (LDO)].

The TPS3703-Q1 has an open drain active low output that requires a pull-up resistor to hold these lines high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current. These values are specified in *Specifications*. The open drain output can be connected as a wired-OR logic with other open drain signals such as another TPS3703-Q1 $\overline{\text{RESET}}$ pin.

表 2 describes the scenarios when the output ($\overline{\text{RESET}}$) is either asserted low or high impedance.

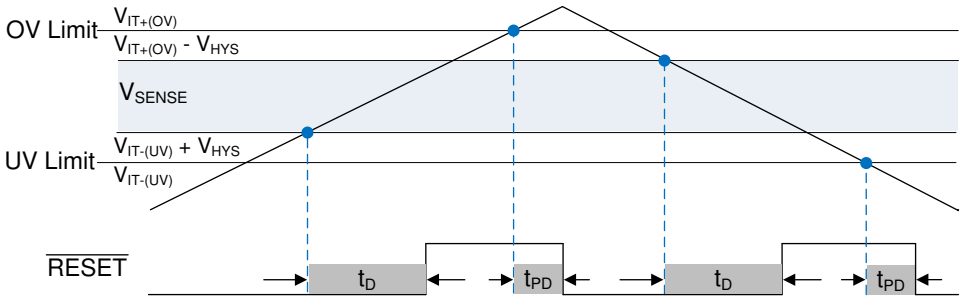


图 23. RESET output

8.3.4 Capacitor Time (CT)

The CT pin provides the user the functionality of both high-precision, factory-programmed, reset delay timing options and user-programmable, reset delay timing. The CT pin can be pulled up to V_{DD} through a resistor, have an external capacitor to ground, or can be left unconnected. The configuration of the CT pin is re-evaluated by the device every time the voltage on the SENSE line enters the valid window ($V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$). The pin evaluation is controlled by an internal state machine that determines which option is connected to the CT pin. The sequence of events takes 450 µs to determine if the CT pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CT pin is being pulled up to V_{DD}, then a pull-up resistor is required, 10 kΩ is recommended.

8.3.5 Manual Reset ($\overline{\text{MR}}$)

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and the SENSE pin voltage is within a valid window (($V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$) , $\overline{\text{RESET}}$ is deasserted after the reset delay time (t_D). If $\overline{\text{MR}}$ is not controlled externally, then $\overline{\text{MR}}$ can either be connected to V_{DD} or left floating because the $\overline{\text{MR}}$ pin is internally pulled up to V_{DD}. Figure 图 24 shows the relation between $\overline{\text{MR}}$ and $\overline{\text{RESET}}$.

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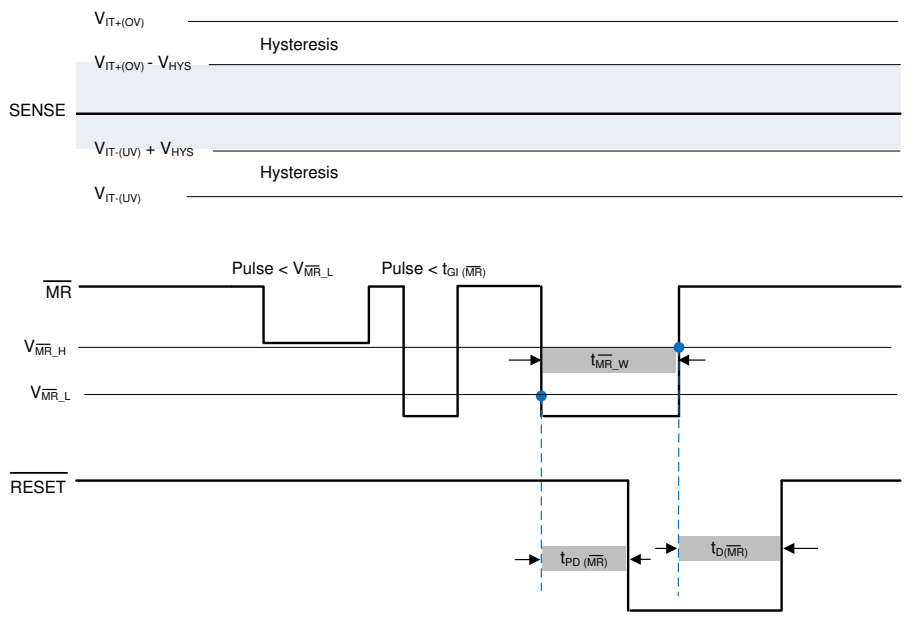
Feature Description (接下页)



(1) $\overline{RESET}$ pulls up to VDD with 10 kΩ.

(2) To initiate and continue time reset counter both conditions must be met $\overline{MR}$ pin above $V_{\overline{MR}_H}$ or floating and V_{SENSE} between $V_{IT-(UV)} + V_{HYS}$ and $V_{IT+(OV)} - V_{HYS}$

(3) $\overline{MR}$ is ignored during output $\overline{RESET}$ low event

图 24. Manual Reset Timing Diagram

8.4 Device Functional Modes

表 2. Functional Mode Truth Table

DESCRIPTION	CONDITION	$\overline{MR}$ PIN	VDD PIN	OUTPUT ($\overline{RESET}$ PIN)
Normal Operation	$V_{IT-(UV)}$ < SENSE < $V_{IT+(OV)}$	Open or above $V_{\overline{MR}_H}$	$V_{DD} > V_{DD(MIN)}$	High
Normal Operation (UV Only)	SENSE > $V_{IT-(UV)}$	Open or above $V_{\overline{MR}_H}$	$V_{DD} > V_{DD(MIN)}$	High
Over Voltage detection	SENSE > $V_{IT+(OV)}$	Open or above $V_{\overline{MR}_H}$	$V_{DD} > V_{DD(MIN)}$	Low
Under Voltage detection	SENSE < $V_{IT-(UV)}$	Open or above $V_{\overline{MR}_H}$	$V_{DD} > V_{DD(MIN)}$	Low
Manual reset	$V_{IT-(UV)}$ < SENSE < $V_{IT+(OV)}$	Below $V_{\overline{MR}_L}$	$V_{DD} > V_{DD(MIN)}$	Low
UVLO engaged	$V_{IT-(UV)}$ < SENSE < $V_{IT+(OV)}$	Open or above $V_{\overline{MR}_H}$	$V_{POR} < V_{DD}$ < UVLO	Low

8.4.1 Normal Operation ($V_{DD} > V_{DD(MIN)}$)

When the voltage on V_{DD} is greater than $V_{DD(MIN)}$ for approximately (t_{SD}+ t_D), the $\overline{RESET}$ output state will correspond to the SENSE pin voltage with respect to the threshold limits, when SENSE voltage is outside of threshold limits the $\overline{RESET}$ voltage will be low (V_{OL}).

8.4.2 Undervoltage Lockout ($V_{POR} < V_{DD}$ < UVLO)

When the voltage on V_{DD} is less than the device UVLO voltage but greater than the power-on reset voltage (V_{POR}), the $\overline{RESET}$ pin will be held low , regardless of the voltage on SENSE pin.

8.4.3 Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) to internally pull the asserted output to GND, $\overline{\text{RESET}}$ signal is undefined and is not to be relied upon for proper device function.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Voltage Threshold Accuracy

Voltage monitoring requirements vary depending on the voltage supply tolerance of the device being powered. Due to the high precision of the TPS3703-Q1 (±0.7% Max), the device allows for a wider supply voltage margins and threshold headroom for tight tolerance applications.

For example, take a DC/DC regulator providing power to a core voltage rail of an MCU. The MCU has a tolerance of ±5% of the nominal output voltage of the DC/DC. The user sets an ideal voltage threshold of ±4% which allows for ±1% of threshold accuracy. Since the TPS3703-Q1 threshold accuracy is higher than ±1%, the user has more supply voltage margin which can allow for a relaxed power supply design. This gives flexibility to the DC/DC to use a smaller output capacitor or inductor because of a larger voltage window for voltage ripple and transients. There is also headroom between the minimum system voltage and voltage tolerance of the MCU to ensure that the voltage supply will never be in the region of potential failure of malfunction without the TPS3703-Q1 asserting a reset signal.

图 25 illustrates the supply undervoltage margin and accuracy of the TPS3703-Q1 for the example explained above. Using a low accuracy supervisor will eat into the available budget for the power supply ripple and transient response. This gives less flexibility to the user and a more stringent DC/DC converter design.

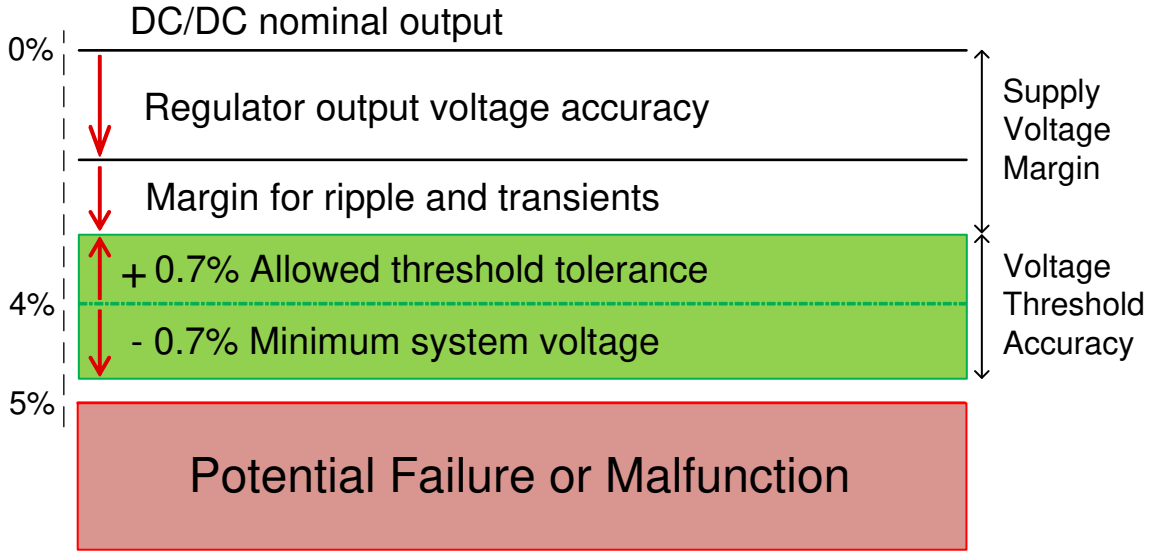

图 25. TPS3703-Q1 Voltage Threshold Accuracy

Application Information (接下页)

9.1.2 CT Reset Time Delay

The TPS3703-Q1 features three options for setting the reset delay (t_D): connecting a capacitor to the CT pin, connecting a pull-up resistor to VDD, and leaving the CT pin unconnected. 图 26 shows a schematic drawing of all three options. To determine which option is connected to the CT pin, an internal state machine controls the internal pulldown device and measures the pin voltage. This sequence of events takes 450 µs to determine which timing option is used. Every time the voltage on the SENSE line enters the valid window ($V_{IT-(UV)} + V_{HYS} < V_{SENSE} < V_{IT+(OV)} - V_{HYS}$, the state machine determines the CT option.

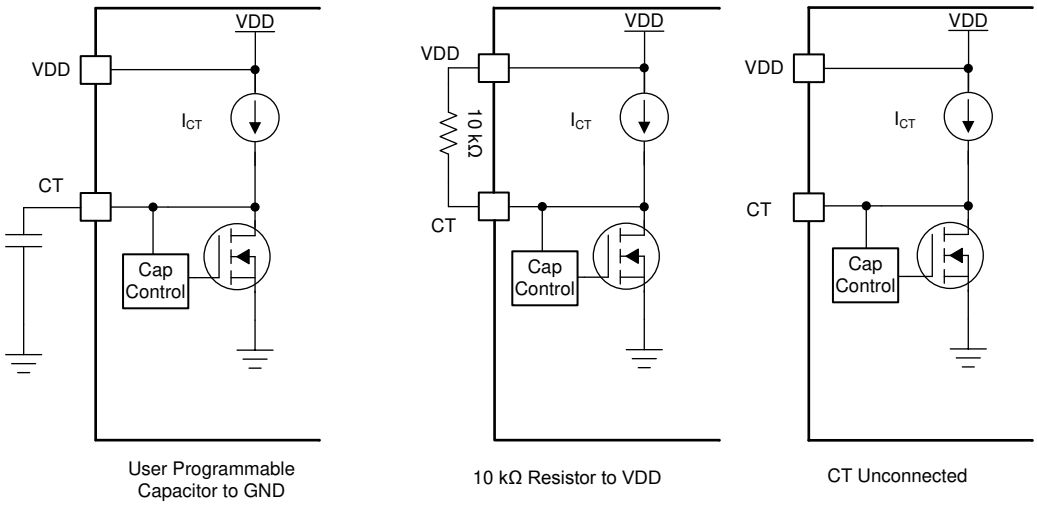

图 26. CT Charging Circuit

9.1.2.1 Factory-Programmed Reset Delay Timing

To use the factory-programmed timing options, the CT pin must either be left unconnected or pulled up to VDD through a 10 kΩ pull-up resistor. Using these options enables a high-precision reset delay timing, as shown in 表 3.

表 3. Reset Delay Time for Factory-Programmed Reset Delay Timing

VARIANT	$\overline{\text{RESET}}$ DELAY TIME (t_D)			VALUE
	CT = Capacitor to GND	CT = Floating	CT = 10 kΩ to VDD	
TPS3703A	Programmable t_D	10	200	ms
TPS3703B	Programmable t_D	1	20	ms
TPS3703C	Programmable t_D	5	100	ms
TPS3703D	N/A	50	50	µs

9.1.2.2 Programmable Reset Delay-Timing

The TPS3703 reset time delay is based on internal current source (I_{CT}) to charge external capacitor (C_{CT}) and read capacitor voltage with internal comparator. The minium value capacitor is 250 pF. There is no limitation on maximum capacitor the only constrain is imposed by the initial voltage of the capacitor, if CT cap is zero or near to zero then ideally there is no other constraint on the max capacitor. The typical ideal capacitor value needed for a given delay time can be calculated using 公式 1, where C_{CT} is in nanofarads (nF) and t_D is in ms:

$$t_D = 3.066 \times C_{CT} + 0.5 \text{ ms} \quad (1)$$

To calculate the minimum and maximum-reset delay time use 公式 2 and 公式 3, respectively.

$$t_{D(min)} = 2.7427 \times C_{CT} + 0.3 \text{ ms} \quad (2)$$

$$t_{D(max)} = 3.4636 \times C_{CT} + 0.7 \text{ ms} \quad (3)$$

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The slope of the equation is determined by the time the CT charging current (I_{CT}) takes to charge the external capacitor up to the CT comparator threshold voltage (V_{CT}). When $\overline{RESET}$ is asserted, the capacitor is discharged through the internal CT pulldown resistor. When the $\overline{RESET}$ conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor; when V_{CT} = 1.15 V, $\overline{RESET}$ is unasserted. Note that in order to minimize the difference between the calculated $\overline{RESET}$ delay time and the actual $\overline{RESET}$ delay time, use a use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. 表 4 lists the reset delay time ideal capacitor values for C_{CT}.

表 4. Reset Delay Time for Ideal Capacitor Values

C_{CT}	$\overline{RESET}$ DELAY TIME (t_D), TYPICAL
250 pF	1.27 ms
1 nF	3.57 ms
3.26 nF	10.5 ms
32.6 nF	100.45 ms
65.2 nF	200.40 ms
1uF	3066.50 ms

9.1.3 $\overline{RESET}$ Latch Mode

The TPS3703-Q1 features a voltage latch mode on the $\overline{RESET}$ pin when connecting the CT pin to common ground . A pull-down resistor is recommended to limit current consumption of the system. In latch mode, if the $\overline{RESET}$ pin is low or triggers low, the pin will stay low regardless if V_{SENSE} is within the acceptable voltage boundaries ($V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$). To unlatch the device provide a voltage to the CT pin that is greater than the CT pin comparator threshold voltage, V_{CT}. The $\overline{RESET}$ pin will trigger high instantaneously without any reset delay. A voltage greater than 1.2 V to recommended to ensure a proper unlatch. Use a series resistance to limit current when an unlatch voltage is applied. For more information, Design 2: $\overline{RESET}$ Latch Mode gives an example of a typical latch application.

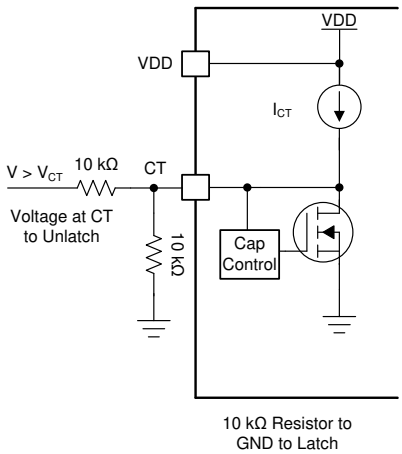

图 27. $\overline{RESET}$ Latch Circuit

9.1.4 Adjustable Voltage Thresholds

The TPS3703-Q1 0.7% maximum accuracy allows for adjustable voltage thresholds using external resistors without adding major inaccuracies to the device. In case that the desired monitored voltage is not available, external resistor dividers can be used to set the desired voltage thresholds. 图 28 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8V voltage threshold device such as the TPS3703B3080 because of the bypass mode of internal resistor ladder.

For example, consider a 2.0 V rail being monitored (V_{MON}) using the TPS3703B3080 variant. Using 公式 4, R1 = 15 kΩ given that R2 = 10 kΩ, V_{MON} = 2 V , and V_{SENSE} = 0.8 V. This device is typically meant to monitor a 0.8 V rail with ±3% voltage thresholds. This means that the device undervoltage threshold ($V_{IT-(UV)}$) and overvoltage threshold ($V_{IT-(OV)}$) is 0.776 V and 0.824 V respectively. Using 公式 4 , V_{MON} = 1.94 V when V_{SENSE} = $V_{IT-(UV)}$. This can be denoted as V_{MON-}, the monitored undervoltage threshold where the device will assert a reset signal. Using 公式 4 again, the monitored overvoltage threshold (V_{MON+}) = 2.06 V when V_{SENSE} = $V_{IT+(OV)}$. If a wider tolerance or UV only threshold is desired, use a device variant shown on Table 7 to determine what device part number matches your application.

$$V_{SENSE} = V_{MON} \times (R_2 \div (R_1 + R_2)) \quad (4)$$

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for design specifications. The internal sense resistance (R_{SENSE}) can be calculated by the sense voltage (V_{SENSE}) divided by the sense current (I_{SENSE}) as shown in 公式 6. V_{SENSE} can be calculated using 公式 4 depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using 公式 5.

$$I_{SENSE} = (V_{MON} - V_{SENSE}) \div R_1 - (V_{SENSE} \div R_2) \quad (5)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (6)$$

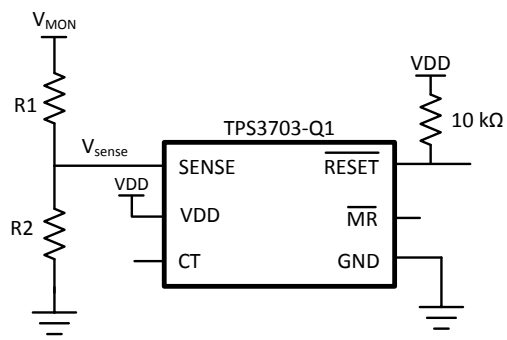

图 28. Adjustable Voltage Threshold with External Resistor Dividers

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9.1.5 Immunity to SENSE Pin Voltage Transients

The TPS3703-Q1 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient.

Overdrive is defined by how much the V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs ($\overline{RESET}$). Threshold overdrive is calculated as a percent of the threshold in question, as shown in 公式 7:

$$\text{Overdrive \%} = \left| \left(V_{SENSE} - \left(V_{IT-(UV)} \text{ or } V_{IT+(OV)}\right)\right) / V_{IT} \text{ (Nominal)} \times 100\% \right| \quad (7)$$

where:

- V_{SENSE} is the voltage at the SENSE pin
- V_{IT} (Nominal) is the nominal threshold voltage
- $V_{IT-(UV)}$ and $V_{IT+(OV)}$ represent the actual undervoltage or overvoltage tripping voltage

9.1.5.1 Hysteresis

Overvoltage and undervoltage comparators include built-in hysteresis that provides noise immunity and ensures stable operation. For example if the voltage on the SENSE pin falls below $V_{IT-(UV)}$ or above $V_{IT+(OV)}$, then $\overline{RESET}$ is asserted (driven low), then when the voltage on the SENSE pin is between the positive and negative threshold voltages, $\overline{RESET}$ deasserts after the user-defined $\overline{RESET}$ delay time. Figure 图 29 shows the relation between $V_{IT-(UV)}$,$V_{IT+(OV)}$ and hysteresis voltage (V_{HYS}).

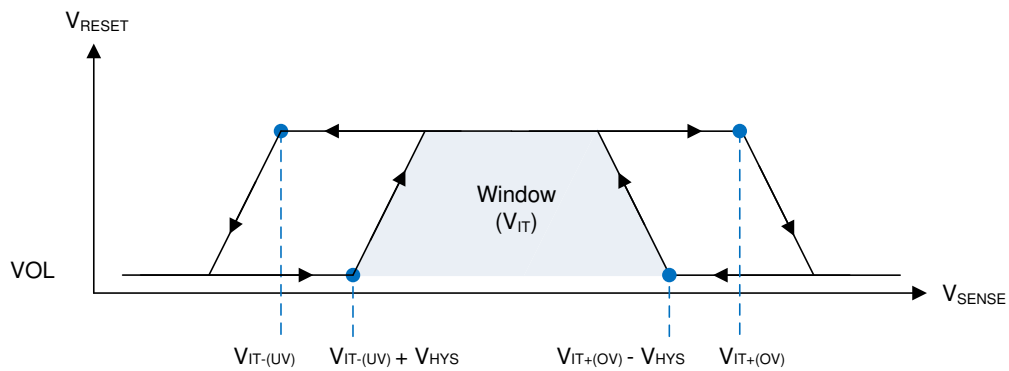

图 29. SENSE Pin Hysteresis

9.2 Typical Application

9.2.1 Design 1: Multi-Rail Window Monitoring for Microcontroller Power Rails

A typical application for the TPS3703-Q1 is shown in 图 30. The TPS3703-Q1 is used to monitor two PMIC voltage rails that powers the core and I/O voltage of the microcontroller that requires accurate reset delay and voltage supervision. Reference design TIDA-050008 is an ADAS power reference that focuses on improved voltage supervision. It utilizes the TPS3703-Q1 to monitor the core voltage rail of a MCU similar to the circuit below.

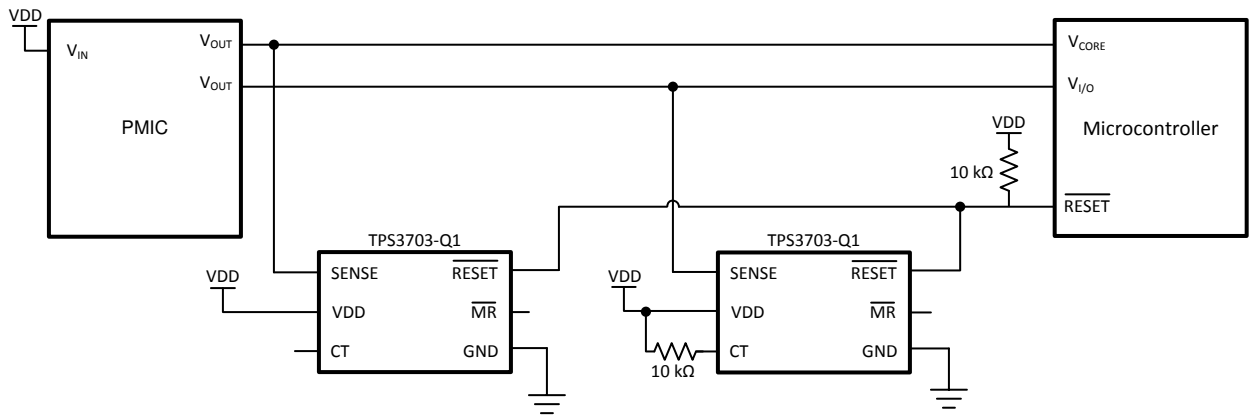

图 30. Two TPS3703-Q1 Monitoring Two Microcontroller Power Rails

9.2.1.1 Design Requirements

表 5. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored rails	3.3-$V_{I/O}$ nominal, with alerts if outside of ±8% of 3.3 V (including device accuracy), 200 ms reset delay	Worst case $V_{IT+(OV)}$ = 3.554 V (7.7%), Worst case $V_{IT-(UV)}$ = 3.046 V (-7.7%)
	1.2-V_{CORE} nominal, with alerts if outside of ±5% of 1.2 V (including device accuracy), 10 ms reset delay	Worst case $V_{IT+(OV)}$ = 1.256 V (4.7%), Worst case $V_{IT-(UV)}$ = 1.144 V (-4.7%)
Output logic voltage	5-V CMOS	5-V CMOS
Maximum system supervision current consumption	50 µA	14 µA (7 µA Max each)

9.2.1.2 Detailed Design Procedure

Determine which version of the TPS3703-Q1 best suits the monitored rail (V_{MON}) and window tolerances found on Table 7. The TPS3703-Q1 allows overvoltage and undervoltage monitoring for precise voltage supervision of common rails between 0.5 V and 5.0 V. This application calls for very tight monitoring of the rail with only ±5% of variation allowed on the 1.2V core rail. To ensure this requirement is met, the TPS3703-Q1 was chosen for its ±4% thresholds. The 3.3V I/O is more flexible and can operate up to 8% variance. Since the TPS3703-Q1 comes in various tolerance options, the ±7% thresholds can be chosen for this voltage rail. To calculate the worst-case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$, the accuracy must also be taken into account. The worst-case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$ can be calculated shown in 公式 8 and 公式 9 respectively:

$$V_{IT+(OV\text{-}Worst\ Case)} = V_{MON} \times (\%Threshold + 0.7\%) = 1.2 \times (+4.7\%) = 1.256\ V \quad (8)$$

$$V_{IT-(UV\text{-}Worst\ Case)} = V_{MON} \times (\%Threshold - 0.7\%) = 1.2 \times (-4.7\%) = 1.144V \quad (9)$$

When the outputs switch to a high impedance state, the rise time of the $\overline{RESET}$ pin depends on the pull-up resistance and the capacitance on that node. Choose pull-up resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 10 kΩ to 1 MΩ resistors are a good choice for low-capacitive loads.

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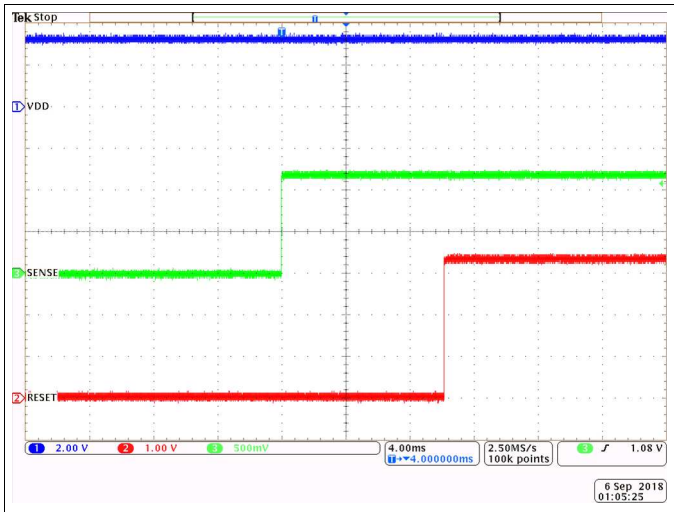
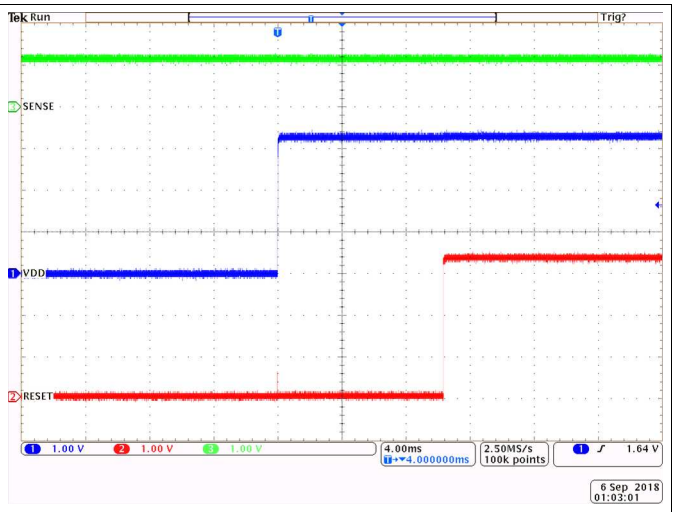
9.2.1.3 Application Curves



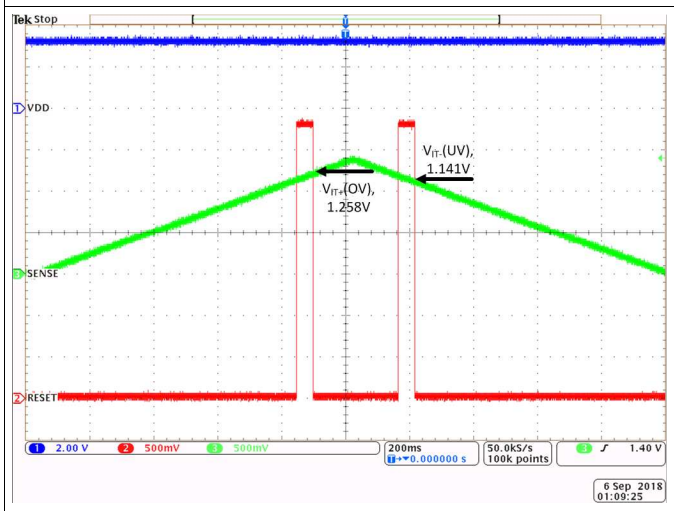
V_{SENSE} Start up from 0 V to 1.2 V, V_{DD} = 3.3 V, CT = OPEN
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

图 31. TPS3703-Q1 SENSE Start Up Function



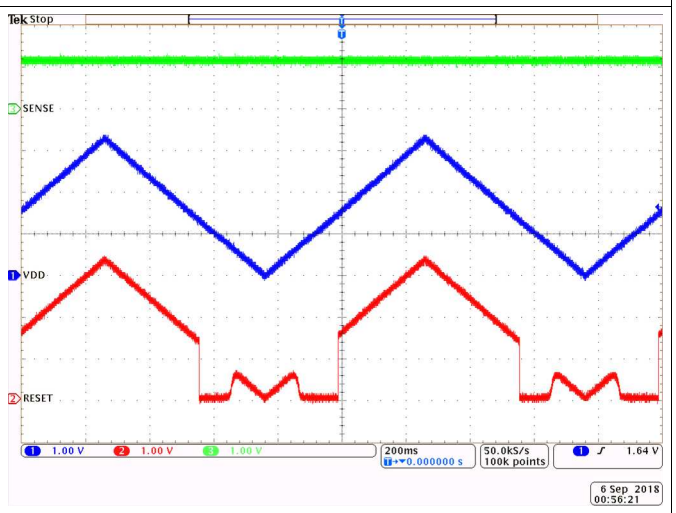
V_{DD} Start up from 0 V to 3.3 V, V_{SENSE} = 1.2 V, CT = OPEN
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

图 32. TPS3703-Q1 VDD Start Up Function



V_{SENSE} ramp from 0 V to 1.4 V, V_{DD} = 3.3 V, CT = OPEN
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

图 33. TPS3703-Q1 Overvoltage and Undervoltage Function



V_{DD} ramp from 0 V to 3.3 V, V_{SENSE} = 1.2 V, CT = OPEN
$V_{\overline{RESET}}$ = VDD = 3.3 V,TPS3703A4120

图 34. TPS3703-Q1 VDD Ramp Up Function

9.2.2 Design 2: $\overline{\text{RESET}}$ Latch Mode

Another typical application for the TPS3703-Q1 is shown in 图 30. The TPS3703-Q1 is used in a $\overline{\text{RESET}}$ latch output mode. In latch mode, once $\overline{\text{RESET}}$ driven logic low, it will stay low regardless of the sense voltage. If the $\overline{\text{RESET}}$ pin is low on start up, it will also stay low regardless of sense voltage.

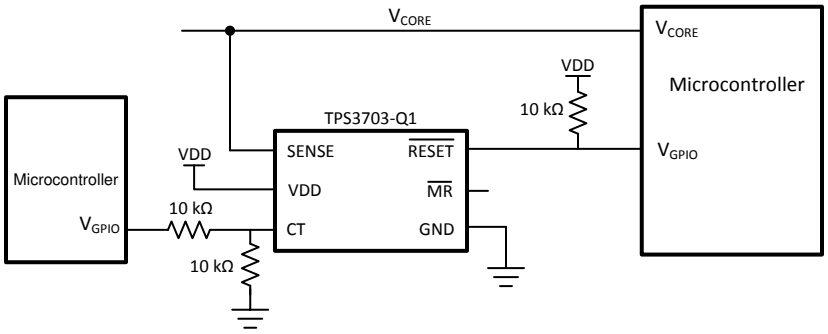


图 35. Window Voltage Monitoring with $\overline{\text{RESET}}$ Latch

9.2.2.1 Design Requirements

表 6. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored Rail	1.2-V_{CORE} nominal, with alerts if outside of ±5% of 1.2 V (including device accuracy), Latch when $\overline{\text{RESET}}$ is low, until voltage is applied on CT pin.	Worst case $V_{IT+(OV)}$ = 1.256 V (4.7%), Worst case $V_{IT-(UV)}$ = 1.144 V (-4.7%)
Output logic voltage	5-V CMOS	5-V CMOS
Maximum device current consumption	15 µA	4.5 µA (Typ), 7 µA (Max)

9.2.2.2 Detailed Design Procedure

The $\overline{\text{RESET}}$ pin can be latched when the CT pin is connected to a common ground with a pull-down resistor. A 10 kΩ resistors is recommended to limit current consumption. To unlatch the device provide a voltage to the CT pin that is greater than the CT pin comparator threshold voltage, V_{CT}. A voltage greater than 1.15 V to recommended to ensure a proper unlatch. Use a series resistance to limit current when an unlatch voltage is applied. To go back into latch operation, disconnect the voltage on the CT pin. The $\overline{\text{RESET}}$ pin will trigger high instanously without any reset delay.

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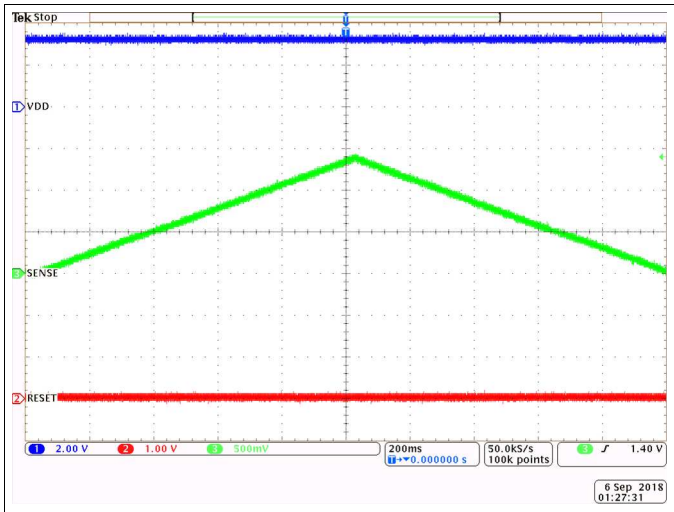
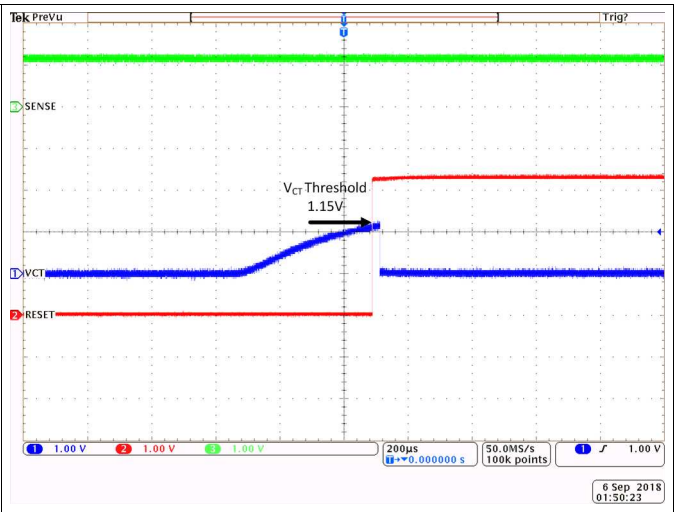
9.2.2.3 Application Curves



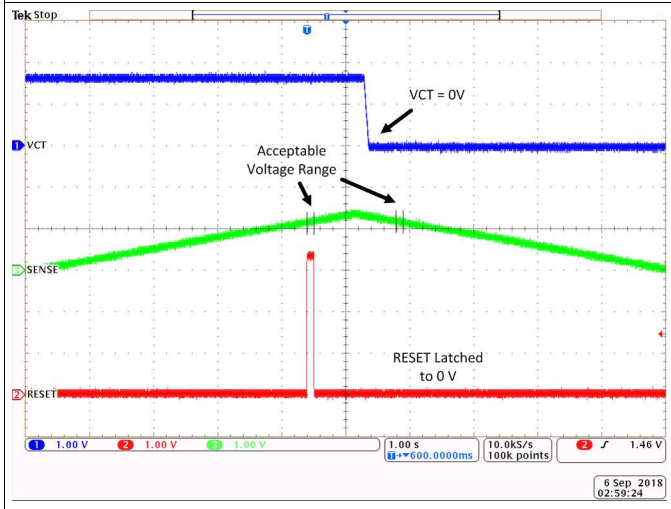
V_{SENSE} ramp from 0 V to 1.4V, V_{DD} = 3.3 V, V_{CT} = 0 V
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

图 36. TPS3703-Q1 SENSE Ramp Latch Function



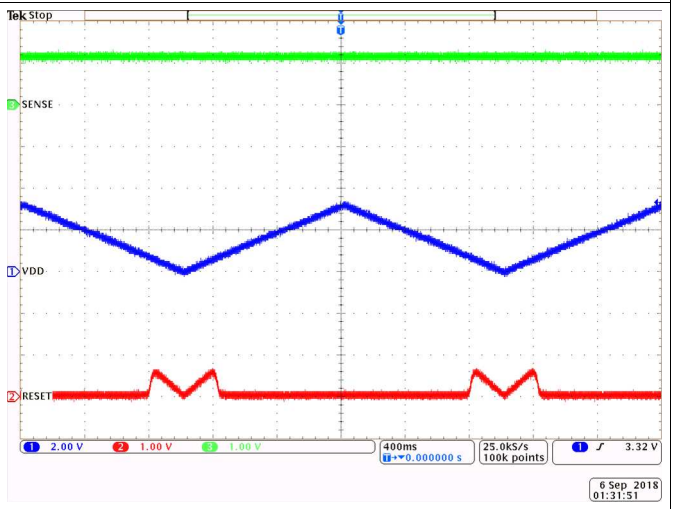
V_{CT} biased at least to 1.15 V , V_{SENSE} = 1.2 V
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

图 37. TPS3703-Q1 CT Bias Unlatch Function



V_{Sense} ramp from 0 V to 1.4 V , V_{DD} = 3.3 V, $V_{\overline{RESET}}$ = VDD
CT is pulled down after RESET is low, RESET becomes latched
TPS3703A4120

图 38. TPS3703-Q1 Overvoltage and Undervoltage Latch Function



V_{DD} ramp up from 0 V to 3.3 V , V_{SENSE} = 1.2 V, CT = 0 V
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

图 39. TPS3703-Q1 VDD Ramp Latch Function

10 Power Supply Recommendations

10.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 1.7 V to 5.5 V. It has a 6-V absolute maximum rating on the VDD pin. It is good analog practice to place a 0.1-µF to 1-µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transient that exceed maximum specifications, additional precautions must be taken. See SNVA849 for more information.

11 Layout

11.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long traces of voltage to the sense pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

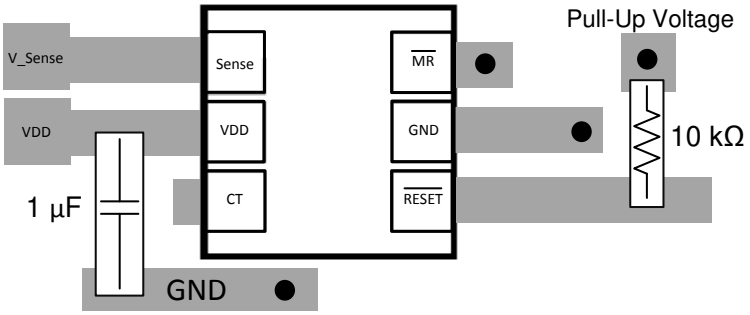


图 40. Recommended Layout

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12 器件和文档支持

12.1 器件命名规则

表 7 显示了如何根据器件型号来解译器件的功能。

表 **7.** 器件命名约定

说明		命名规则	值
		TPS3703	TPS3703
延时时间选项：每个器件都有两个固定延时时间，而且可以通过外部电容器器件型号来调节延迟选项	窗口（OV 和 UV）	A	CT 引脚断开 = 10ms，CT 引脚连接到 VDD = 200ms 可使用外部电容器对 CT 进行编程
		B	CT 引脚断开 = 1ms，CT 引脚连接到 VDD = 20ms 可使用外部电容器对 CT 进行编程
		C	CT 引脚断开 = 5ms，CT 引脚连接到 VDD = 100ms 可使用外部电容器对 CT 进行编程
		D	CT 引脚断开 = 50µs，CT 引脚连接到 VDD = 50µs 无法对 CT 进行编程
	仅 UV	E	CT 引脚断开 = 10ms，CT 引脚连接到 VDD = 200ms 可使用外部电容器对 CT 进行编程
		F	CT 引脚断开 = 1ms，CT 引脚连接到 VDD = 20ms 可使用外部电容器对 CT 进行编程
		G	CT 引脚断开 = 5ms，CT 引脚连接到 VDD = 100ms 可使用外部电容器对 CT 进行编程
		H	CT 引脚断开 = 50µs，CT 引脚连接到 VDD = 50µs 无法对 CT 进行编程
容差选项：触发电压或以上述阈值电压百分比形式表示的阈值电压		3	来自标称值的窗口阈值 = OV：3%；UV：-3%
		4	来自标称值的窗口阈值 = OV：4%；UV：-4%
		5	来自标称值的窗口阈值 = OV：5%；UV：-5%
		6	来自标称值的窗口阈值 = OV：6%；UV：-6%
		7	来自标称值的窗口阈值 = OV：7%；UV：-7%

器件命名规则 (接下页)

表 **7.** 器件命名约定
(接下页**)**

说明		命名规则	值
标称监控器阈值电压选项		050	0.50V
		055	0.55V
		060	0.60V
		065	0.65V
		070	0.70V
		075	0.75V
		080	0.80V
		085	0.85V
		090	0.90V
		095	0.95V
		100	1.00V
		105	1.05V
		110	1.10V
		115	1.15V
		120	1.20V
		125	1.25V
		130	1.30V
		150	1.50V
		180	1.80V
		250	2.50V
		280	2.80V
		290	2.90V
		330	3.30V
		500	5.00V
封装		DSE	WSON - 6 引脚 (1.5mm × 1.5mm)
卷带		R	大卷带
汽车版本		Q1	Q100 AEC

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12.2 文档支持

12.2.1 评估模块

评估模块 (EVM) 可与 TPS3703-Q1 配套使用，帮助评估初始电路性能。*TPS3703-Q1 评估模块*（和*相关的用户指南*）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 TI eStore 购买。

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3703A4085DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L8	Samples
TPS3703A4120DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AB	Samples
TPS3703A4180DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AD	Samples
TPS3703A4280DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H8	Samples
TPS3703A4330DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AE	Samples
TPS3703A5090DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GW	Samples
TPS3703A5180DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GZ	Samples
TPS3703A5290DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GT	Samples
TPS3703A7080DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LD	Samples
TPS3703A7100DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LA	Samples
TPS3703A7110DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GX	Samples
TPS3703A7120DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H1	Samples
TPS3703A7125DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AC	Samples
TPS3703A7180DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H2	Samples
TPS3703A7250DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	L9	Samples
TPS3703A7280DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H3	Samples
TPS3703A7330DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GV	Samples
TPS3703B3080DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BA	Samples
TPS3703B4250DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H6	Samples
TPS3703B5180DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GU	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3703C7500DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CF	Samples
TPS3703E4080DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3703-Q1 :

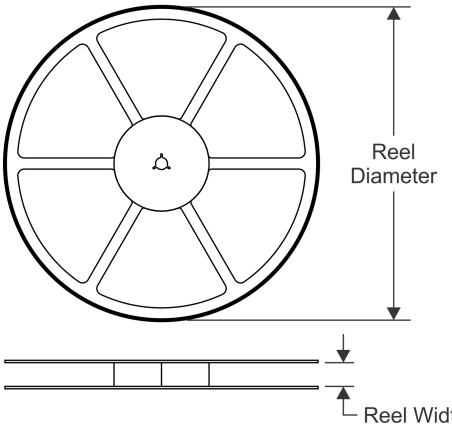
- Catalog : TPS3703

NOTE: Qualified Version Definitions:

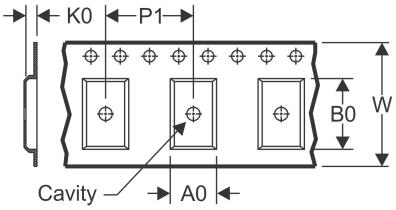
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

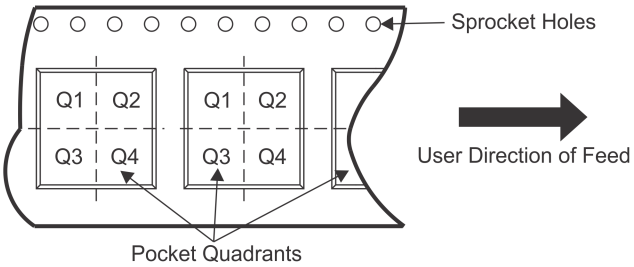


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

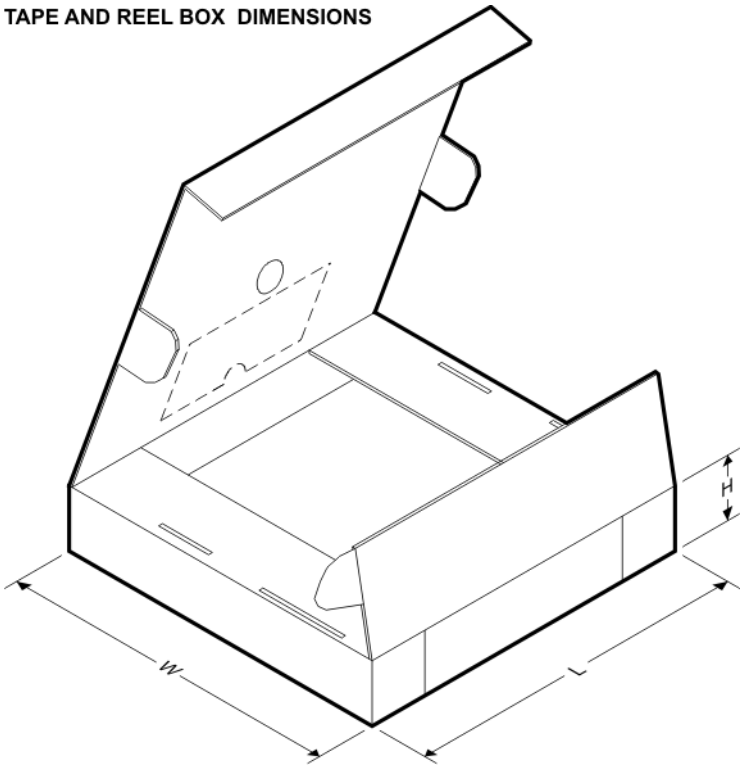


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3703A4085DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A4120DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A4180DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A4280DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A4330DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A5090DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A5180DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A5290DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7080DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7100DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7110DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7120DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7125DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7180DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7250DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7280DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7330DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703B3080DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3703B4250DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703B5180DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703C7500DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703E4080DSERQ1	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

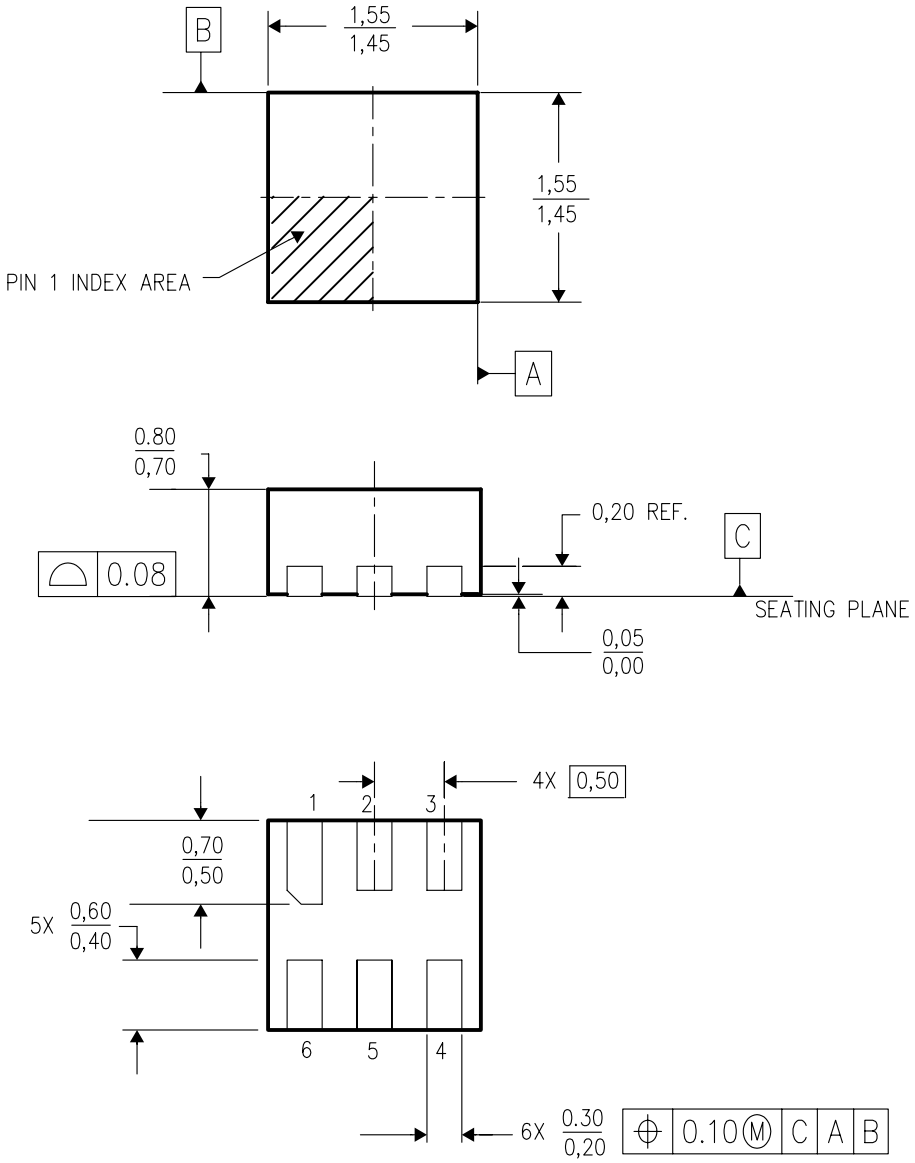


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3703A4085DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A4120DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A4180DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A4280DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A4330DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A5090DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A5180DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A5290DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A7080DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A7100DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A7110DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A7120DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A7125DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3703A7180DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A7250DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A7280DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A7330DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703B3080DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703B4250DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703B5180DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703C7500DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703E4080DSERQ1	WSON	DSE	6	3000	205.0	200.0	33.0

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

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