LM2936Q Ultralow Quiescent Current LDO Voltage Regulator

1 Features

- Qualified for Automotive Applications
- AEC Q100-Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
- Operating Input Voltage: 5.5 V to 40 V
- Ultralow Quiescent Current (I_Q ≤ 15 µA for I_{OUT} = 100 µA)
- Fixed 3-V, 3.3-V or 5-V With 50-mA Output
- ±2% Initial Output Tolerance
- ±3% Output Tolerance Over Line, Load, and Temperature
- Dropout Voltage Typically 200 mV at I_{OUT} = 50 mA
- Reverse Battery Protection
- –50-V Input Transient Protection
- Internal Short Circuit Current Limit
- Internal Thermal Shutdown Protection
- 40-V Operating Voltage Limit
- Shutdown Pin Available with LM2936QBM Package

2 Applications

Automotive

3 Description

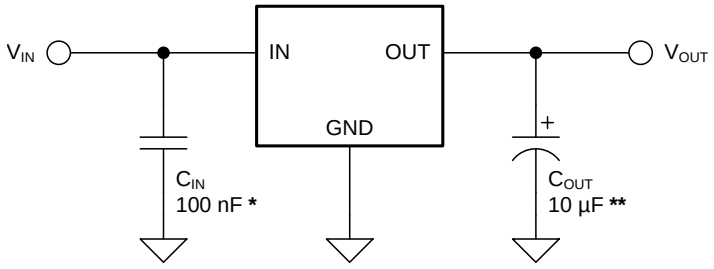
The LM2936Q ultralow quiescent-current regulator features low dropout voltage and low current in the standby mode. With less than 15-µA quiescent current at a 100-µA load, the LM2936Q is ideally suited for automotive and other battery-operated systems. The LM2936Q retains all of the features that are common to low-dropout regulators including a low dropout PNP pass device, short-circuit protection, reverse battery protection, and thermal shutdown. The LM2936Q has a 40-V maximum operating voltage limit, a −40°C to +125°C operating temperature range, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range. The LM2936Q is available in 8-pin SOIC and VSSOP packages, a 4-pin SOT–223 package, as well as a 3-pin TO-252 surface mount package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2936Q	SOIC (8)	4.90 mm × 3.91 mm
	TO-252 (3)	6.10 mm × 6.58 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOT-223 (4)	6.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



* Required if regulator is located more than 2 inches from power supply filter capacitor.
** Required for stability. See *Electrical Characteristics for 3-V LM2936Q* for required values. Must be rated over intended operating temperature range. Effective equivalent series resistance (ESR) is critical, see *Typical Characteristics*. Locate capacitor as close to the regulator output and ground pins as possible. Capacitance may be increased without bound.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D — **Page**

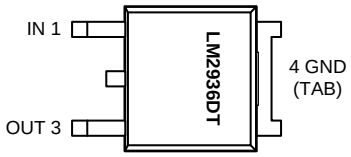
- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Thermal Information* table with updated values, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed θ_{JA} for SOIC from 140°C/W to 111.4°C/W; for TO-252 from 136°C/W to 50.5°C/W; for VSSOP from 200°C/W to 173.4°C/W; and for SOT-223 from149°C/W to 62.8°C/W ... 4
- Changed θ_{JC} for SOIC from 45°C/W to 56.3°C/W (top); TO-252 from 6°C/W to 52.6°C/W (top) and 1.6°C/W (bottom); SOT-223 from 36°C/W to 44.2°C/W (top) ... 4

Changes from Revision B (May 2012) to Revision C — **Page**

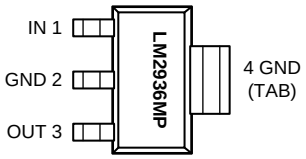
- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

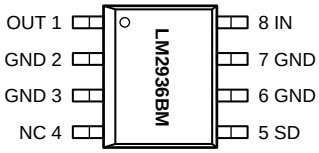
NDP Package
3-Pin TO-252
Top View



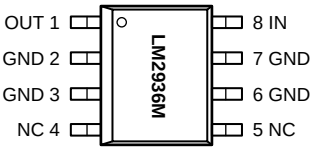
DCY Package
4-Pin SOT-223
Top View



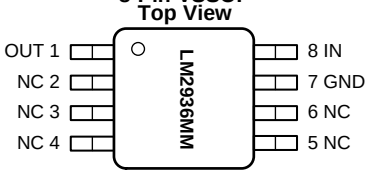
D Package (LM2936QHBM)
8-Pin SOIC
Top View



D Package (LM2936QM)
8-Pin SOIC
Top View



DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN						I/O	DESCRIPTION
NAME	D (LM2936QHBMA)	D (LM2936QM)	NDP	DGK	DCY		
IN	8	8	1	8	1	I	Unregulated input voltage.
GND	2, 3, 6, 7	2, 3, 6, 7	4	7	2, 4	—	Ground.
OUT	1	1	3	1	3	O	Regulated output voltage. Requires a minimum output capacitance, with specific ESR, on this pin to maintain stability.
SD	5	—	—	—	—	I	Shutdown (LM2936QHBMA only). Pull this pin HIGH (> 2 V) to turn the output OFF. If this pin is left open, pulled low (< 0.6 V), or connected to GND, the output will be ON by default. Avoid having any voltage from 0.6 V to 2 V on this pin as the output status may not be predicable across the operating range.
NC	4	4, 5	—	2, 3, 4, 5, 6	—	—	No internal connection, Connect to GND, or leave open.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
Input voltage (survival)	−50	60	V
Power dissipation[3]	Internally limited		
Junction temperature, T_{JMAX}		150	°C
Storage temperature, T_{stg}	−65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. If this dissipation is exceeded, the die temperature can rise above the $T_{J(MAX)}$ of 150°C, and the LM2936Q may go into thermal shutdown.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature, T_J	−40	125	°C
Input voltage, V_{IN} (LM2936Q)	5.5	40	V
Input voltage, V_{IN} (LM2936QH only)	5.5	60	V
Shutdown pin voltage, V_{SD} (LM2936QHBMA only)	0	40	V

6.4 Thermal Information

THERMAL METRIC[1]		LM2936Q				UNIT
		SOIC (D)	TO-252 (NDP)	VSSOP (DGK)	SOT-223 (DCY)	
		8 PINS	3 PINS	8 PINS	4 PINS	
$R_{\theta JA}$[2]	Junction-to-ambient thermal resistance, High-K	111.4	50.5	173.4	62.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	52.6	65.9	44.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.9	29.7	94.9	11.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	4.8	9.6	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.4	29.3	93.3	11.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	1.6	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

6.5 Electrical Characteristics for 3-V LM2936Q

V_{IN} = 14 V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
Output voltage		2.94	3	3.06	V
	4 V ≤ V_{IN} ≤ 26 V, 100 µA ≤ I_{OUT} ≤ 50 mA(2) –40°C ≤ T_J ≤ 125°C	2.91	3.000	3.09	
Quiescent current	I_{OUT} = 100 µA, 8 V ≤ V_{IN} ≤ 24 V		15	20	µA
	I_{OUT} = 10 mA, 8 V ≤ V_{IN} ≤ 24 V		0.2	0.5	mA
	I_{OUT} = 50 mA, 8 V ≤ V_{IN} ≤ 24 V		1.5	2.5	mA
Line regulation	9 V ≤ V_{IN} ≤ 16 V		5	10	mV
	6 V ≤ V_{IN} ≤ 40 V, I_{OUT} = 1 mA		10	30	
Load regulation	100 µA ≤ I_{OUT} ≤ 5 mA		10	30	mV
	5 mA ≤ I_{OUT} ≤ 50 mA		10	30	
Dropout voltage	I_{OUT} = 100 µA		0.05	0.1	V
	I_{OUT} = 50 mA		0.20	0.40	V
Short-circuit current	V_{OUT} = 0 V	65	120	250	mA
Output impedance	I_{OUT} = 30 mAdc and 10 mArms, f = 1000 Hz		450		mΩ
Output noise voltage	10 Hz–100 kHz		500		µV
Long-term stability			20		mV/1000 Hr
Ripple rejection	V_{ripple} = 1 V_{rms}, f_{ripple} = 120 Hz	−40	−60		dB
Reverse polarity transient input voltage	R_L = 500 Ω, t = 1 ms	−50	−80		V
Output voltage with reverse polarity input	V_{IN} = −15 V, R_L = 500 Ω		0	−0.3	V
Maximum line transient	R_L = 500 Ω, V_{OUT} ≤ 3.3 V, T = 40 ms	60			V
Output bypass capacitance (C_{OUT}) ESR	C_{OUT} = 22 µF, 0.1 mA ≤ I_{OUT} ≤ 50 mA	0.3		8	Ω

(1) Datasheet minimum and max specification limits are ensured by design, test, or statistical analysis.
(2) Typical limits are at 25°C (unless otherwise specified) and represent the most likely parametric norm.

6.6 Electrical Characteristics for 3.3-V LM2936Q

V_{IN} = 14 V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
Output voltage		3.234	3.300	3.366	V
	4 V ≤ V_{IN} ≤ 26 V, 100 µA ≤ I_{OUT} ≤ 50 mA(3) –40°C ≤ T_J ≤ 125°C	3.201	3.300	3.399	
Quiescent current	I_{OUT} = 100 µA, 8 V ≤ V_{IN} ≤ 24 V		15	20	µA
	I_{OUT} = 10 mA, 8 V ≤ V_{IN} ≤ 24 V		0.2	0.5	mA
	I_{OUT} = 50 mA, 8 V ≤ V_{IN} ≤ 24 V		1.5	2.5	mA
Line regulation	9 V ≤ V_{IN} ≤ 16 V		5	10	mV
	6 V ≤ V_{IN} ≤ 40 V, I_{OUT} = 1 mA		10	30	
Load regulation	100 µA ≤ I_{OUT} ≤ 5 mA		10	30	mV
	5 mA ≤ I_{OUT} ≤ 50 mA		10	30	
Dropout voltage	I_{OUT} = 100 µA		0.05	0.10	V
	I_{OUT} = 50 mA		0.2	0.4	V
Short-circuit current	V_{OUT} = 0 V	65	120	250	mA
Output impedance	I_{OUT} = 30 mAdc and 10 mArms, f = 1000 Hz		450		mΩ
Output noise voltage	10 Hz–100 kHz		500		µV
Long-term stability			20		mV/1000 Hr
Ripple rejection	V_{ripple} = 1 V_{rms}, f_{ripple} = 120 Hz	−40	−60		dB
Reverse polarity transient input voltage	R_L = 500 Ω, T = 1 ms	−50	−80		V
Output voltage with reverse polarity input	V_{IN} = −15 V, R_L = 500 Ω		0	−0.3	V
Maximum line transient	R_L = 500 Ω, V_{OUT} ≤ 3.63 V, T = 40 ms	60			V
Output bypass capacitance (C_{OUT}) ESR	C_{OUT} = 22 µF, 0.1 mA ≤ I_{OUT} ≤ 50 mA	0.3		8	Ω

(1) Datasheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.
(2) Typical limits are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

6.7 Electrical Characteristics for 5-V LM2936Q

V_{IN} = 14 V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
5-V LM2936QHBMA ONLY					
Output voltage	5.5 V ≤ V_{IN} ≤ 48 V, 100 µA ≤ I_{OUT} ≤ 50 mA(3) –40°C ≤ T_J ≤ 125°C	4.85	5	5.15	V
Line regulation	6 V ≤ V_{IN} ≤ 60 V, I_{OUT} = 1 mA		15	35	mV
ALL 5-V LM2936Q					
Output voltage		4.9	5	5.1	V
	5.5 V ≤ V_{IN} ≤ 26 V, 100 µA ≤ I_{OUT} ≤ 50 mA(3) –40°C ≤ T_J ≤ 125°C	4.85	5	5.15	
Quiescent current	I_{OUT} = 100 µA, 8 V ≤ V_{IN} ≤ 24 V		9	15	µA
	I_{OUT} = 10 mA, 8 V ≤ V_{IN} ≤ 24 V		0.2	0.5	mA
	I_{OUT} = 50 mA, 8 V ≤ V_{IN} ≤ 24 V		1.5	2.5	mA
Line regulation	9 V ≤ V_{IN} ≤ 16 V		5	10	mV
	6 V ≤ V_{IN} ≤ 40 V, I_{OUT} = 1 mA		10	30	
Load regulation	100 µA ≤ I_{OUT} ≤ 5 mA		10	30	mV
	5 mA ≤ I_{OUT} ≤ 50 mA		10	30	
Dropout voltage	I_{OUT} = 100 µA		0.05	0.1	V
	I_{OUT} = 50 mA		0.2	0.4	V
Short-circuit current	V_{OUT} = 0 V	65	120	250	mA
Output impedance	I_{OUT} = 30 mAdc and 10 mArms, f = 1000 Hz		450		mΩ
Output noise voltage	10 Hz–100 kHz		500		µV
Long-term stability			20		mV/1000 Hr
Ripple rejection	V_{ripple} = 1 V_{rms}, f_{ripple} = 120 Hz	−40	−60		dB
Reverse polarity transient input voltage	R_L = 500 Ω, T = 1 ms	−50	−80		V
Output voltage with reverse polarity input	V_{IN} = −15 V, R_L = 500 Ω		0	−0.3	V
Maximum line transient	R_L = 500 Ω, V_{OUT} ≤ 5.5 V, T = 40 ms	60			V
Output bypass capacitance (C_{OUT}) ESR	C_{OUT} = 10 µF, 0.1 mA ≤ I_{OUT} ≤ 50 mA	0.3		8	Ω
SHUTDOWN INPUT: 5-V LM2936QHBMA ONLY					
Output voltage, V_{OUT}	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500 Ω		0	0.01	V
Shutdown high threshold voltage, V_{IH}	Output off, R_{LOAD} = 500 Ω	2	1.1		V
Shutdown low threshold voltage, V_{IL}	Output on, R_{LOAD} = 500 Ω		1.1	0.6	V
Shutdown high current, I_{IH}	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500 Ω		12		µA
Quiescent current	Output off, V_{SD} = 2.4 V, R_{LOAD} = 500Ω, includes I_{IH} current		30		µA

(1) Datasheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.
(2) Typical limits are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

6.8 Typical Characteristics

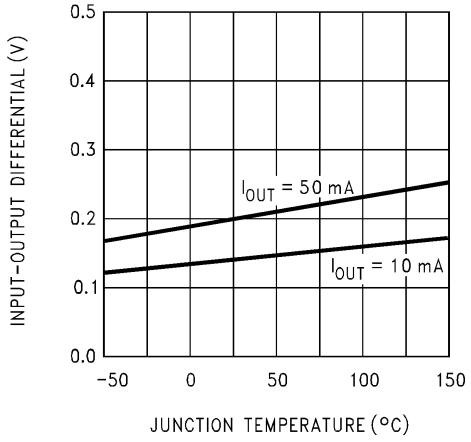


Figure 1. Dropout Voltage

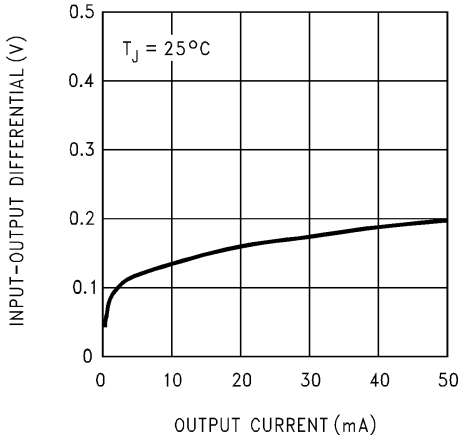


Figure 2. Dropout Voltage

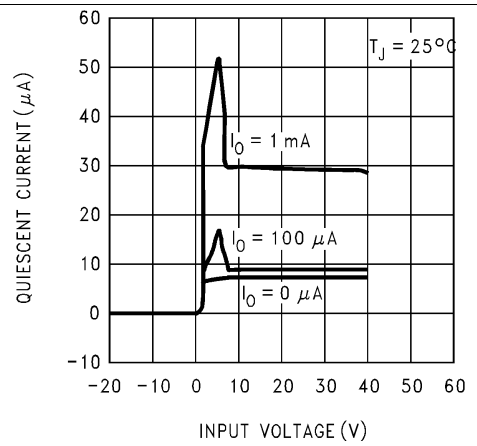


Figure 3. Quiescent Current

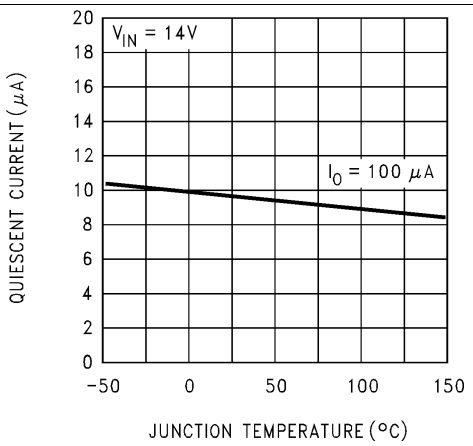


Figure 4. Quiescent Current

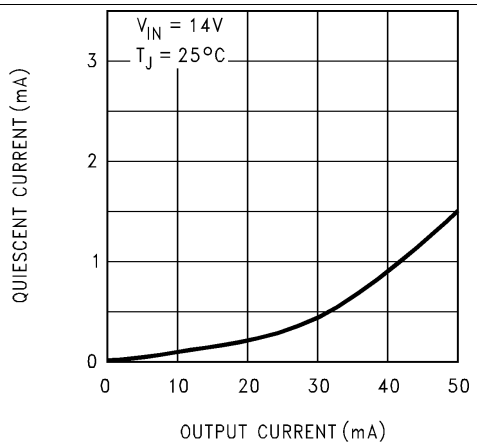


Figure 5. Quiescent Current

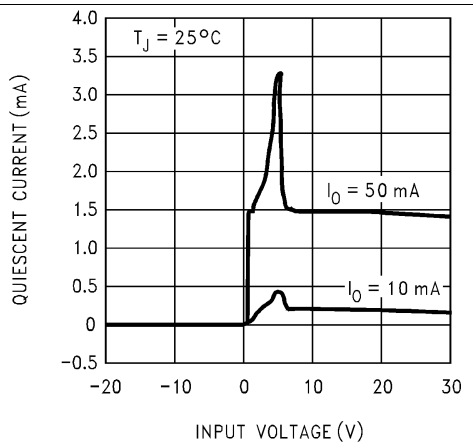


Figure 6. Quiescent Current

Typical Characteristics (continued)

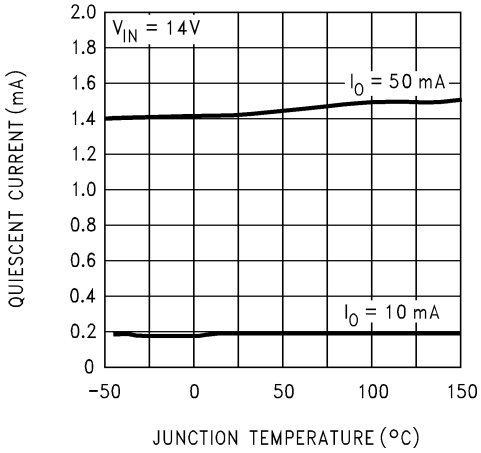


Figure 7. Quiescent Current

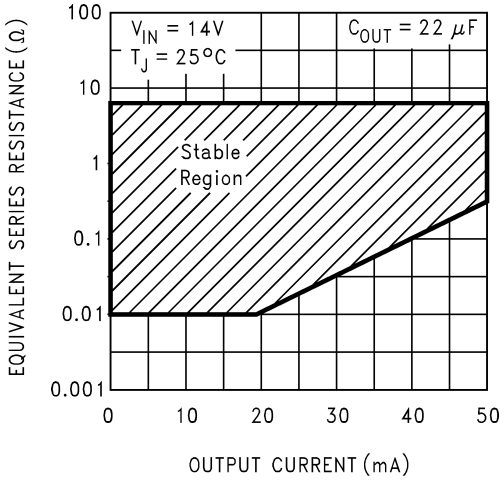


Figure 8. 3-V LM2936Q C_{OUT} ESR

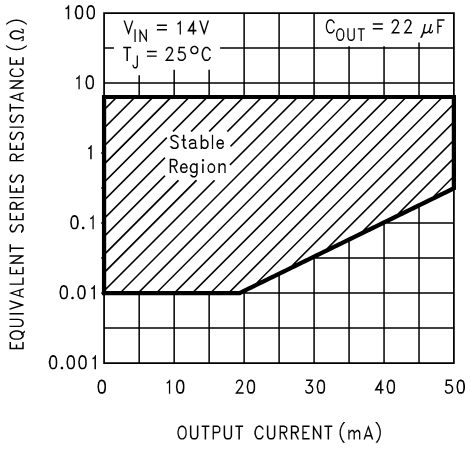


Figure 9. 3.3-V LM2936Q C_{OUT} ESR

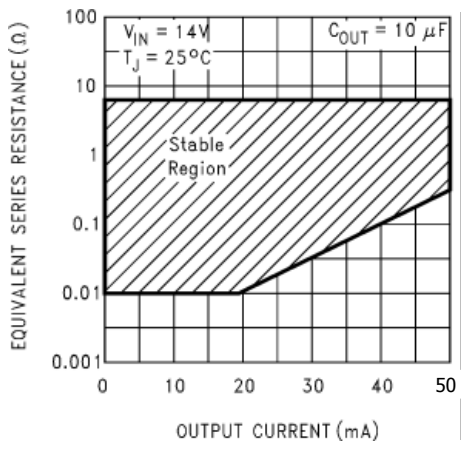


Figure 10. 5-V LM2936Q C_{OUT} ESR

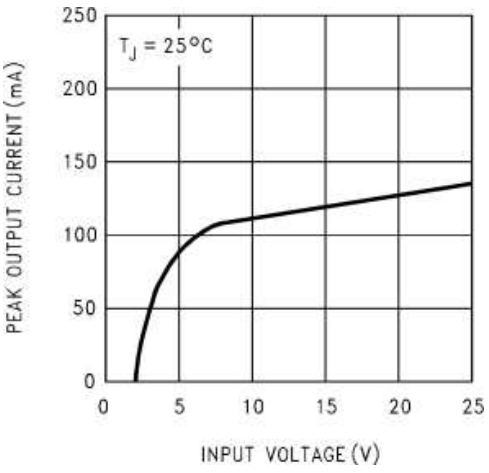


Figure 11. Peak Output Current

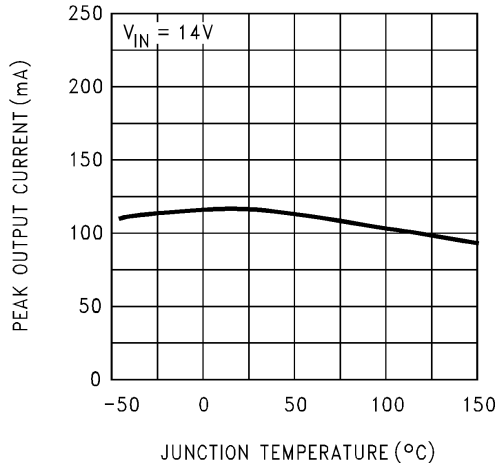


Figure 12. Peak Output Current

Typical Characteristics (continued)

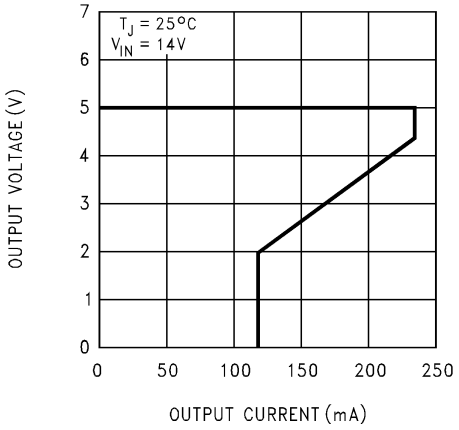


Figure 13. 5-V LM2936Q Current Limit

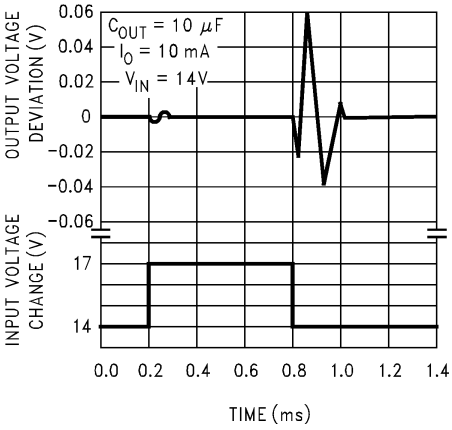


Figure 14. 5-V LM2936Q Line Transient Response

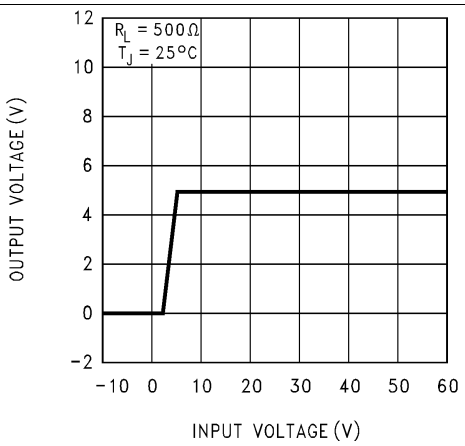


Figure 15. 5-V LM2936Q Output at Voltage Extremes

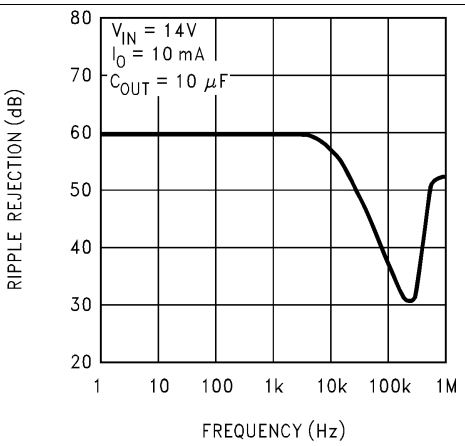


Figure 16. 5-V LM2936Q Ripple Rejection

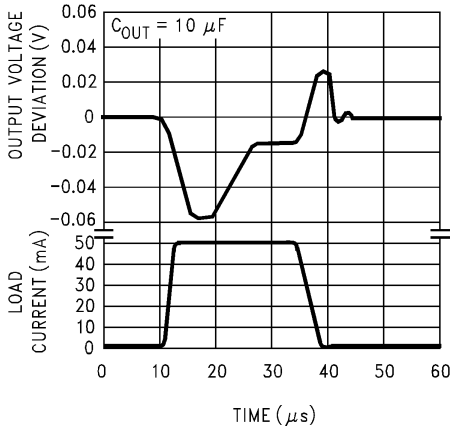


Figure 17. 5-V LM2936Q Load Transient Response

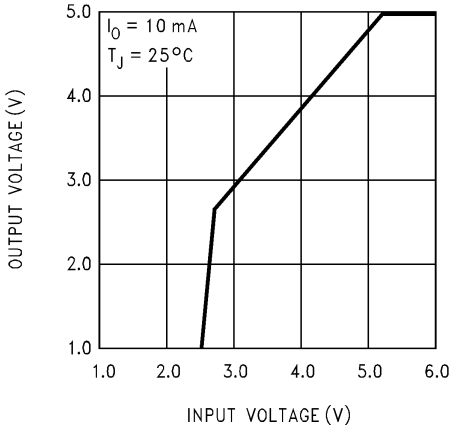


Figure 18. 5-V LM2936Q Low Voltage Behavior

Typical Characteristics (continued)

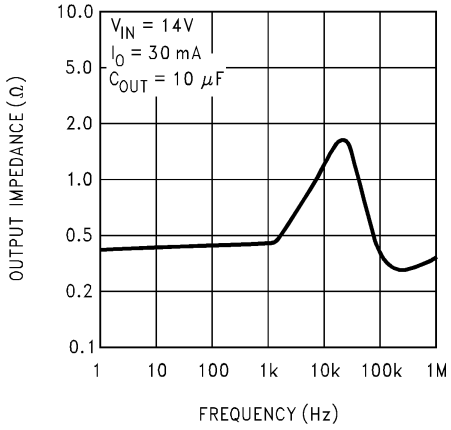


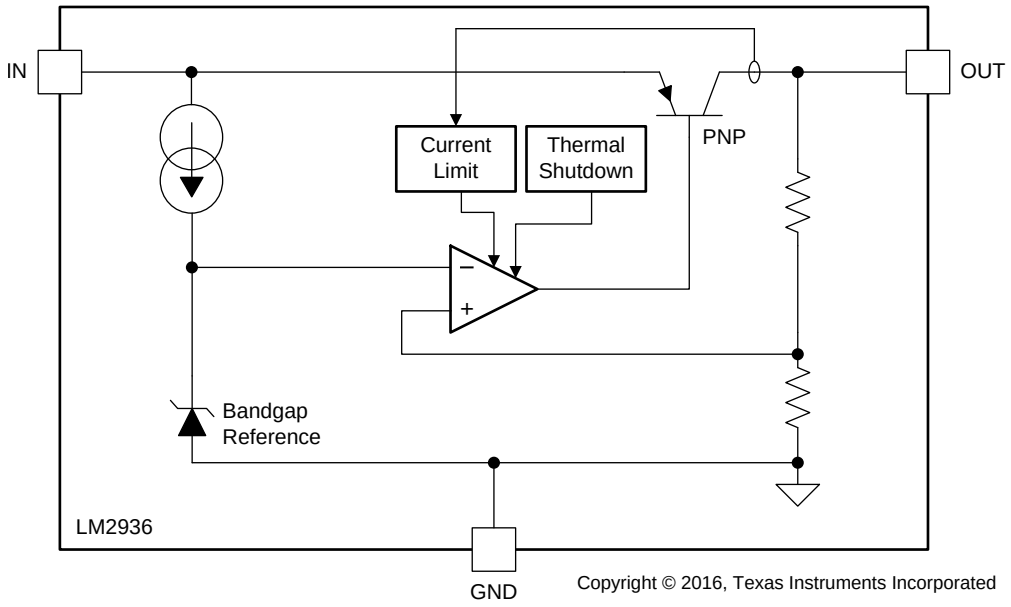
Figure 19. 5-V LM2936Q Output Impedance

7 Detailed Description

7.1 Overview

The LM2936Q ultralow quiescent current regulator is ideally suited for automotive and other battery operated systems, with less than 15 µA quiescent current at a 100-µA load. The device features low dropout voltage and low current in the standby mode and retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery input protection, and thermal shutdown. The LM2936Q has a 40-V maximum operating voltage limit and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High Input Operating Voltage

Unlike many other PNP low dropout regulators, the LM2936Q remains fully operational with V_{IN} = 40 V, and the LM2936QHBM remains fully operational with V_{IN} = 60 V. Owing to power dissipation characteristics of the available packages, full output current cannot be ensured for all combinations of ambient temperature and input voltage.

While the LM2936QHBM maintains regulation to 60 V, it does not withstand a short circuit to ground on the output when V_{IN} is above 40 V because of safe operating area limitations in the internal PNP pass device. Above 60 V the LM2936Q breaks down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40 V, or where transients are likely to exceed 60 V.

7.3.2 Thermal Shutdown (T_{SD})

The T_{SD} circuitry of the LM2936Q has been designed to protect the device against temporary thermal overload conditions. The T_{SD} circuitry is not intended to replace proper heat-sinking. Continuously running the LM2936Q device at T_{SD} may degrade device reliability as the junction temperature will be exceeding the absolute maximum junction temperature rating. If the LM2936Q goes into T_{SD} mode, the output current shuts off until the junction temperature falls approximately 10°C — the output current is then automatically restored. The LM2936Q continuously cycles in and out of T_{SD} until the condition is corrected. The LM2936Q T_{SD} junction temperature is typically 160°C.

Feature Description (continued)

7.3.3 Short-Circuit Current Limit

The output current limiting circuitry of the LM2936Q has been designed to limit the output current in cases where the load impedance is unusually low. This includes situations where the output may be shorted directly to ground. Continuous operation of the LM2936Q at the current limit typically results in the LM2936Q transitioning into T_{SD} mode.

7.3.4 Shutdown (SD) Pin

The 5-V LM2936QHBMA has a pin for shutting down the regulator output. Applying a logic level high (> 2 V) to the SD pin causes the output to turn off. Leaving the SD pin open, connecting it to ground, or applying a logic level low (< 0.6 V) allows the regulator output to turn on.

7.4 Device Functional Modes

The LM2936Q design does not include any undervoltage lockout (UVLO), or overvoltage shutdown (OVSD) functions. Generally, the output voltage tracks the input voltage until the input voltage is greater than V_{OUT} + 1 V. When the input voltage is greater than V_{OUT} + 1 V the LM2936Q is in linear operation, and the output voltage is regulated; however, the device is sensitive to any small perturbation of the input voltage. Device dynamic performance is improved when the input voltage is at least 2 V greater than the output voltage.

8 Application and Implementation

NOTE

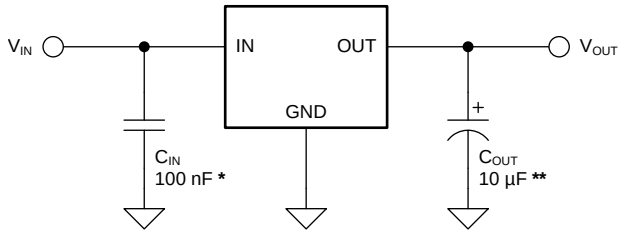
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2936Q ultralow quiescent current regulator features low dropout voltage and low current in the standby mode. The LM2936Q has a 40-V maximum operating voltage limit, a −40°C to +125°C operating temperature range, –24-V input transient protection, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range The WEBENCH® software may be used to generate complete designs. When generating a design, WEBENCH utilizes iterative design procedure and accesses comprehensive databases of components. See www.ti.com for more details.

8.2 Typical Application

Figure 20 shows the typical application circuit for the LM2936Q. For the LM2936Q 5-V option, the output capacitor, C_{OUT}, must have a capacitance value of at least 10 µF with an equivalent series resistance (ESR) of at least 0.3 Ω, but no more than 8 Ω. For the LM2936Q 3-V and 3.3-V options, the output capacitor, C_{OUT}, must have a capacitance value of at least 22 µF with an ESR of at least 0.3 Ω, but no more than 8 Ω. The minimum capacitance value and the ESR requirements apply across the entire expected operating ambient temperature range.



* C_{IN} is required only if the regulator is located more than 3 inches from the power-supply-filter capacitors.

** Required for stability. C_{OUT} must be at least 10 µF for the LM2936Q 5-V option, and at least 22 µF for the 3-V and 3.3-V options. Capacitance must be maintained over entire expected operating temperature range, and located as close as possible to the regulator. The ESR, of the C_{OUT} capacitor must at least 0.3 Ω, but no more than 8 Ω.

Figure 20. LM2936Q Typical Application

8.2.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5.5 V to 40 V
Output voltage	5 V
Output current requirement	1 mA to 50 mA
Input capacitor	0.1 µF
Output capacitance	10 µF minimum
Output capacitor ESR value	0.3 Ω to 8 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both ESR and minimum amount of capacitance.

8.2.2.1.1 Minimum Capacitance

The minimum output capacitance required to maintain stability is at least 10 µF for the LM2936Q 5-V option, and at least 22 µF for the 3-V and 3.3-V options. This value may be increased without limit. Larger values of output capacitance will give improved transient response.

8.2.2.1.2 ESR Limits

The ESR of the output capacitor causes loop instability if it is too high, or too low. The ESR of the C_{OUT} capacitor must at least 0.3 Ω, but no more than 8 Ω.

8.2.2.2 Output Capacitor ESR

It is essential that the output capacitor meet the capacitance and ESR requirements, or oscillations can result. The ESR is used with the output capacitance in order to produce a zero in the control loop frequency response. This zero increases phase margin and ensures stability of the output voltage. Refer to *ESR, Stability, and the LDO Regulator* (SLVA115) for details.

Ceramic capacitors (MLCC) can be used for C_{OUT} only if a series resistor is added to simulate the ESR requirement. The ESR is not optional — it is mandatory. Typically, a 500-mΩ to 1-Ω series resistor is used for this purpose. When using MLCCs, due diligence must be given to initial tolerances, capacitance derating due to applied DC voltage, and capacitance variations due to temperature. Dielectric types X5R and X7R are preferred.

8.2.2.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the 8-pin SOIC (D) package, the four ground pins are thermally connected to the backside of the die. Adding approximately 0.04 square inches of 2 oz. copper pad area to these four pins improves the JEDEC $R_{\theta JA}$ rating from 111.4°C/W to approximately 100°C/W. If this extra copper area is placed directly beneath the SOIC package there should not be any impact on board density.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (RθJA) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 2:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_D = T_{J(MAX)} - T_{A(MAX)} / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.4 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)}) \quad (4)$$

where

- $P_{D(MAX)}$ is explained in Equation 3
- T_{TOP} is the temperature measured at the center-top of the device package.

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)}) \quad (5)$$

where

- $P_{D(MAX)}$ is explained in Equation 3.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge.

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics* (SPRA953); for more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics* (SBVA025); and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017). These application notes are available at www.ti.com.

8.2.3 Application Curve

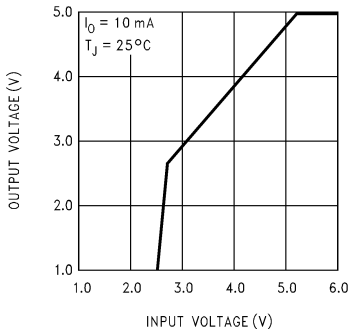


Figure 21. LM2936Q V_{OUT} vs V_{IN}

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage from at least V_{OUT} + 1 V up to a maximum of 40 V. The input supply should be well regulated and free of spurious noise. To ensure that the LM2936Q output voltage is well regulated the input supply must be at least V_{OUT} + 2 V. A capacitor at the IN pin may not be specifically required if the bulk input supply filter capacitors are within three inches of the IN pin, but adding one is not detrimental to operation.

While the LM2936Q maintains regulation to V_{IN} = 60 V, it cannot withstand a short circuit on the output with V_{IN} above 40 V because of safe operating area limitations in the internal PNP pass device. With V_{IN} above 60 V the LM2936Q breaks down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage, including transients, is likely to exceed 60 V.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LM2936Q is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LM2936Q. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LM2936Q, and as close to the packageas is practical. The ground connections for C_{IN} and C_{OUT} must be back to the LM2936Q ground pin using as wide and as short of a copper trace as possible.

Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided as these add parasitic inductances and resistances that give inferior performance, especially during transient conditions.

10.2 Layout Examples

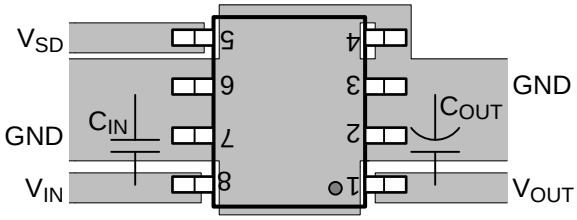


Figure 22. LM2936QHBM SOIC (D) Layout

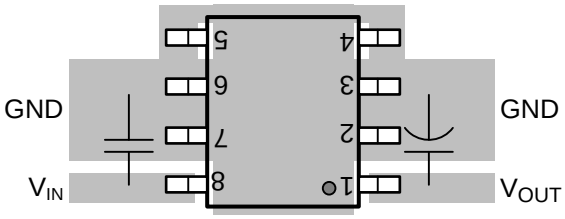


Figure 23. LM2936QM SOIC (D) Layout

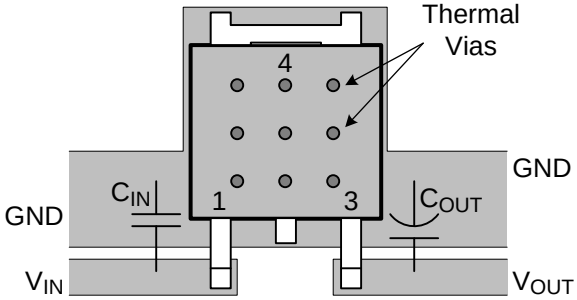


Figure 24. LM2936Q TO-252 (NDP) Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *ESR, Stability, and the LDO Regulator* (SLVA115)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Using New Thermal Metrics* (SBVA025)
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2936QDT-3.0/NOPB	ACTIVE	TO-252	NDP	3	75	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936Q DT-3.0	Samples
LM2936QDT-3.3/NOPB	ACTIVE	TO-252	NDP	3	75	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936Q DT-3.3	Samples
LM2936QDT-5.0/NOPB	ACTIVE	TO-252	NDP	3	75	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936Q DT-5.0	Samples
LM2936QDTX-3.0/NOPB	ACTIVE	TO-252	NDP	3	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936Q DT-3.0	Samples
LM2936QDTX-3.3/NOPB	ACTIVE	TO-252	NDP	3	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936Q DT-3.3	Samples
LM2936QDTX-5.0/NOPB	ACTIVE	TO-252	NDP	3	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LM2936Q DT-5.0	Samples
LM2936QHBMA-5.0/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2936H QBM5.0	Samples
LM2936QHBMAX5.0/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2936H QBM5.0	Samples
LM2936QM-3.3/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6Q-3.3	Samples
LM2936QM-5.0/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM293 6QM-5	Samples
LM2936QMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KBCQ	Samples
LM2936QMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KBBQ	Samples
LM2936QMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KBAQ	Samples
LM2936QMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KBBQ	Samples
LM2936QMMX-5.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KBAQ	Samples
LM2936QMP-3.0/NOPB	ACTIVE	SOT-223	DCY	4	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KACQ	Samples
LM2936QMP-3.3/NOPB	ACTIVE	SOT-223	DCY	4	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KABQ	Samples
LM2936QMP-5.0/NOPB	ACTIVE	SOT-223	DCY	4	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KAAQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2936QMPX-3.0/NOPB	ACTIVE	SOT-223	DCY	4	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KACQ	Samples
LM2936QMPX-3.3/NOPB	ACTIVE	SOT-223	DCY	4	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KABQ	Samples
LM2936QMPX-5.0/NOPB	ACTIVE	SOT-223	DCY	4	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KAAQ	Samples
LM2936QMX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2936Q-3.3	Samples
LM2936QMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2936QM-5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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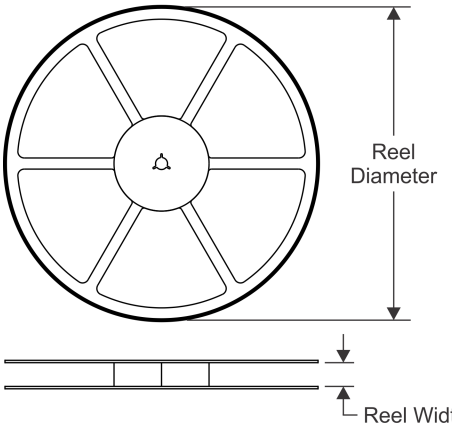
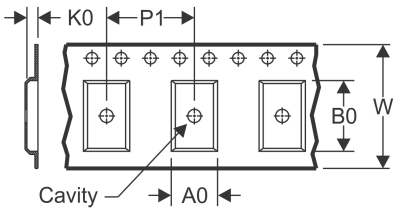
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

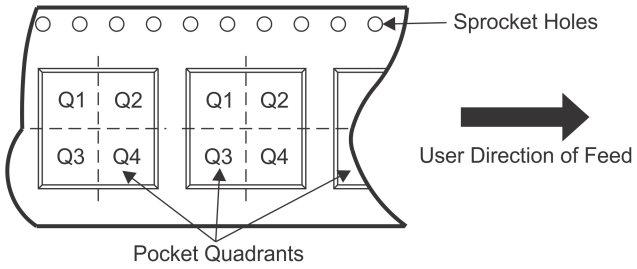


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

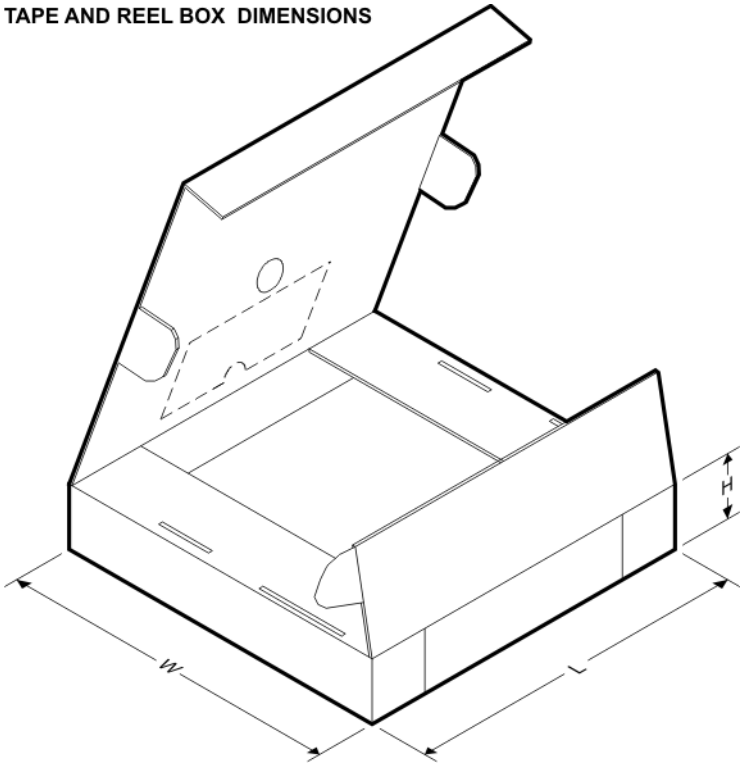
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2936QDTX-3.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM2936QDTX-3.3/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM2936QDTX-5.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM2936QHBMAX5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936QMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936QMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936QMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936QMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936QMMX-5.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2936QMP-3.0/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936QMP-3.3/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936QMP-5.0/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936QMPX-3.0/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936QMPX-3.3/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936QMPX-5.0/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2936QMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2936QMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

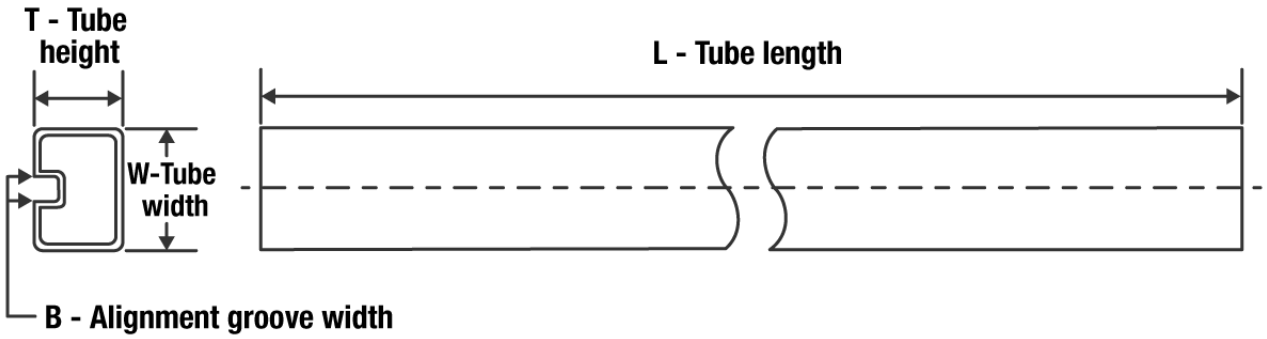
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2936QDTX-3.0/NOPB	TO-252	NDP	3	2500	853.0	449.0	35.0
LM2936QDTX-3.3/NOPB	TO-252	NDP	3	2500	853.0	449.0	35.0
LM2936QDTX-5.0/NOPB	TO-252	NDP	3	2500	853.0	449.0	35.0
LM2936QHBMAX5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2936QMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM2936QMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM2936QMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM2936QMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM2936QMMX-5.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM2936QMP-3.0/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2936QMP-3.3/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2936QMP-5.0/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2936QMPX-3.0/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM2936QMPX-3.3/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM2936QMPX-5.0/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM2936QMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2936QMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

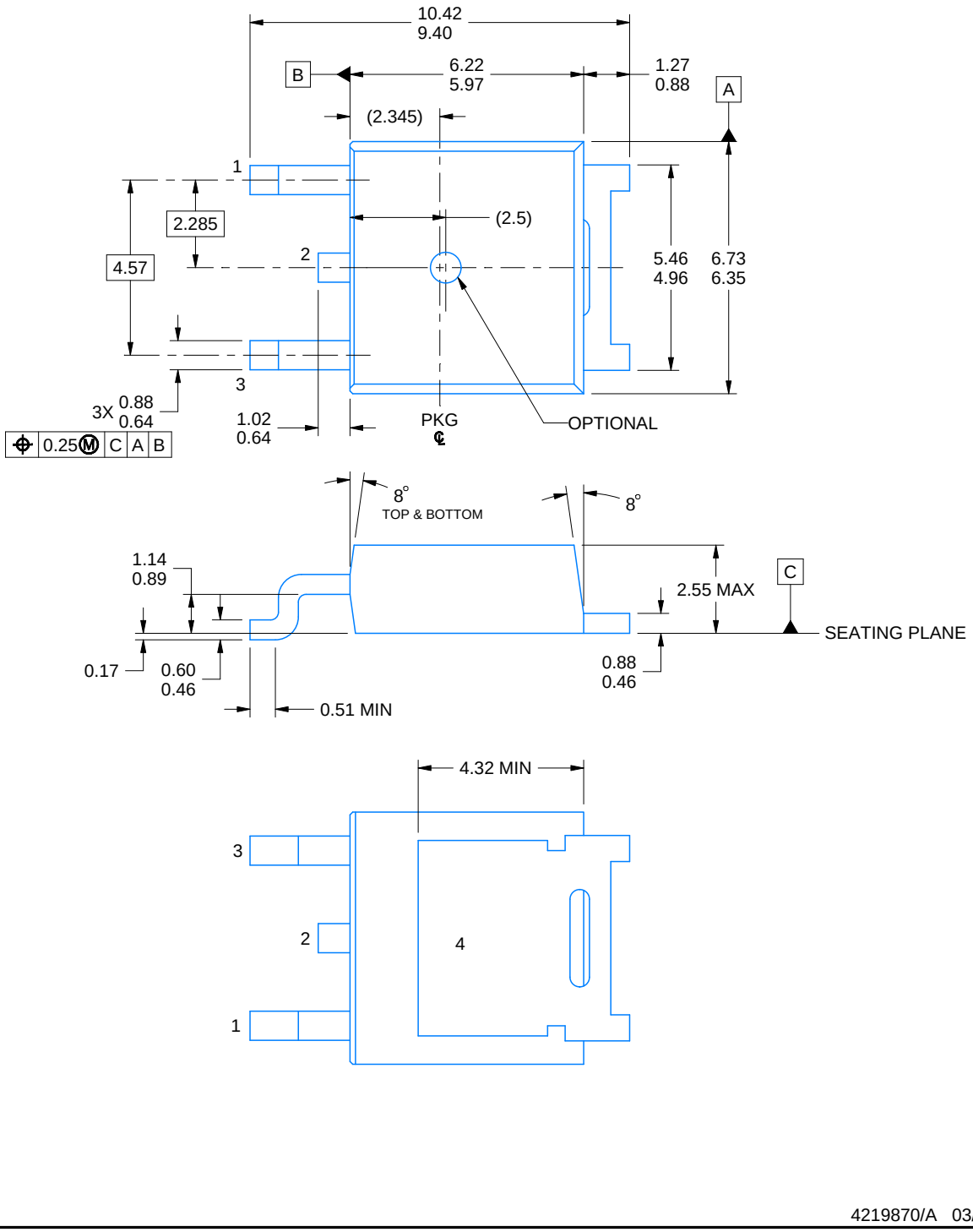
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2936QDT-3.0/NOPB	NDP	TO-252	3	75	508	20	4165.6	3.1
LM2936QDT-3.3/NOPB	NDP	TO-252	3	75	508	20	4165.6	3.1
LM2936QDT-5.0/NOPB	NDP	TO-252	3	75	508	20	4165.6	3.1
LM2936QHBMA-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM2936QM-3.3/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM2936QM-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05

NDP0003B

PACKAGE OUTLINE

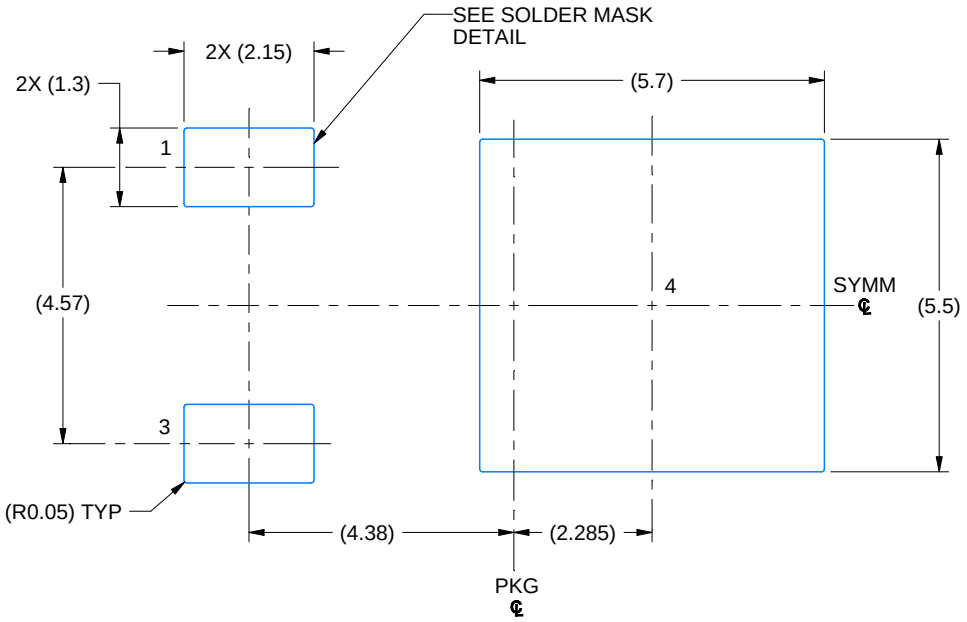
TO-252 - 2.55 mm max height

TRANSISTOR OUTLINE

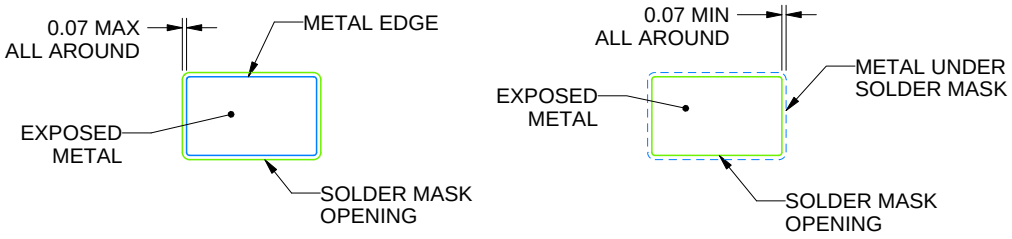


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

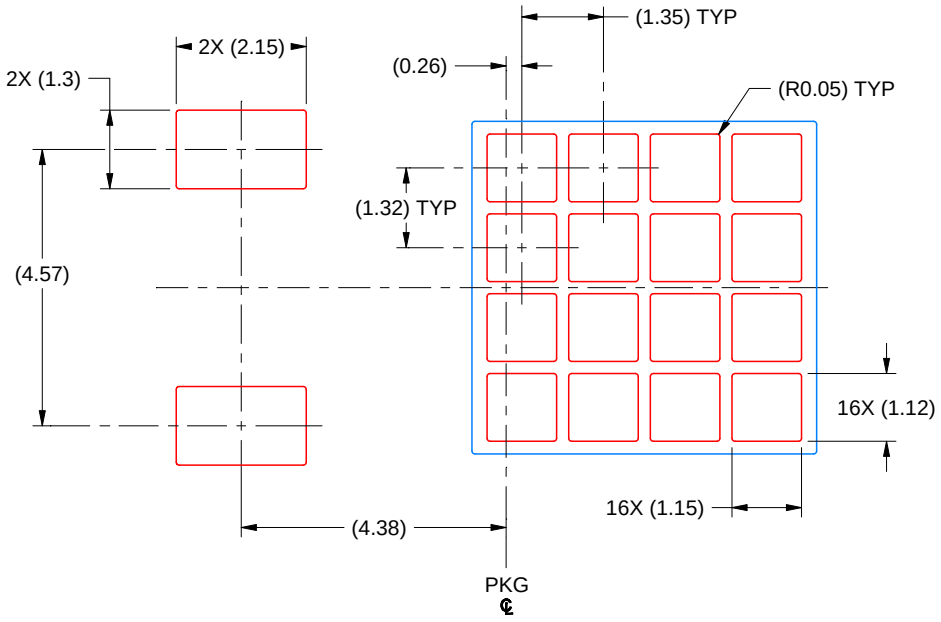


SOLDER MASK DETAIL

4219870/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



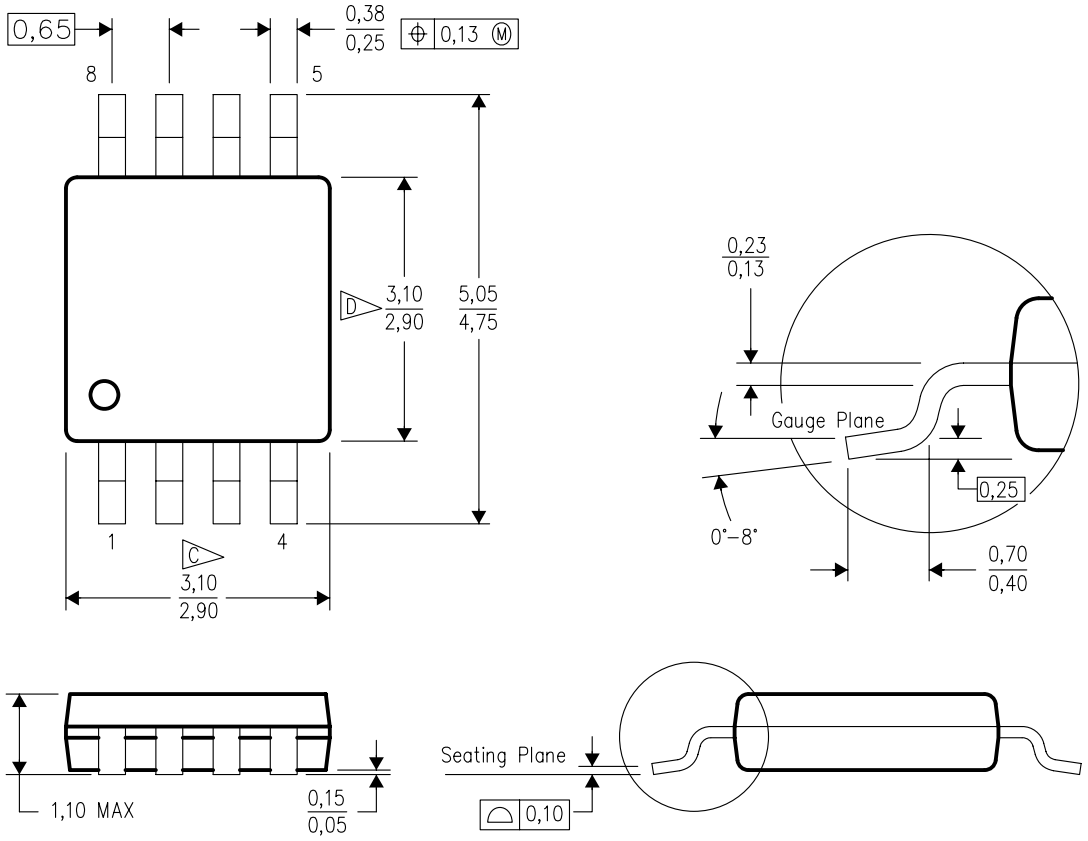
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

4219870/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

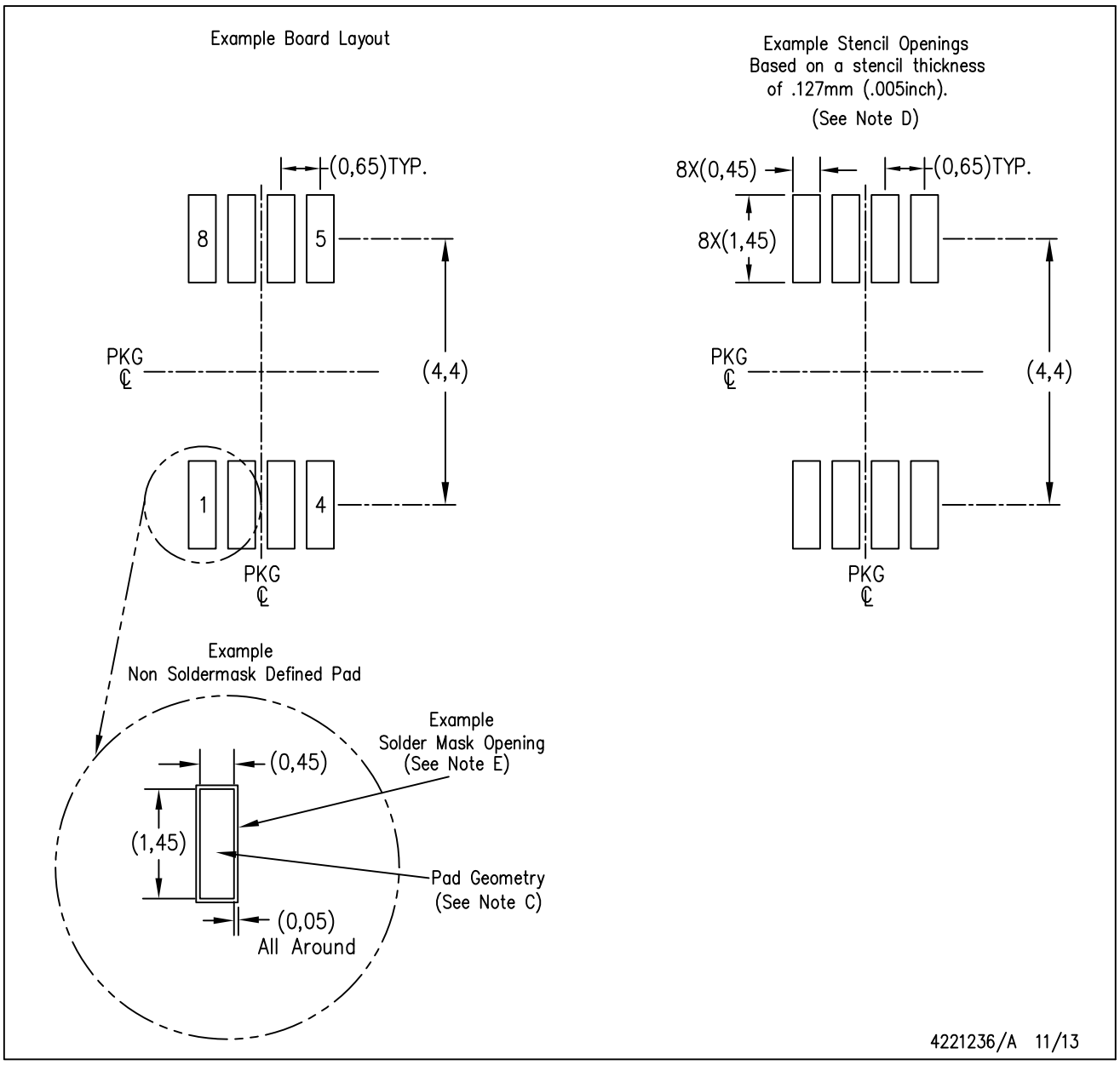
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

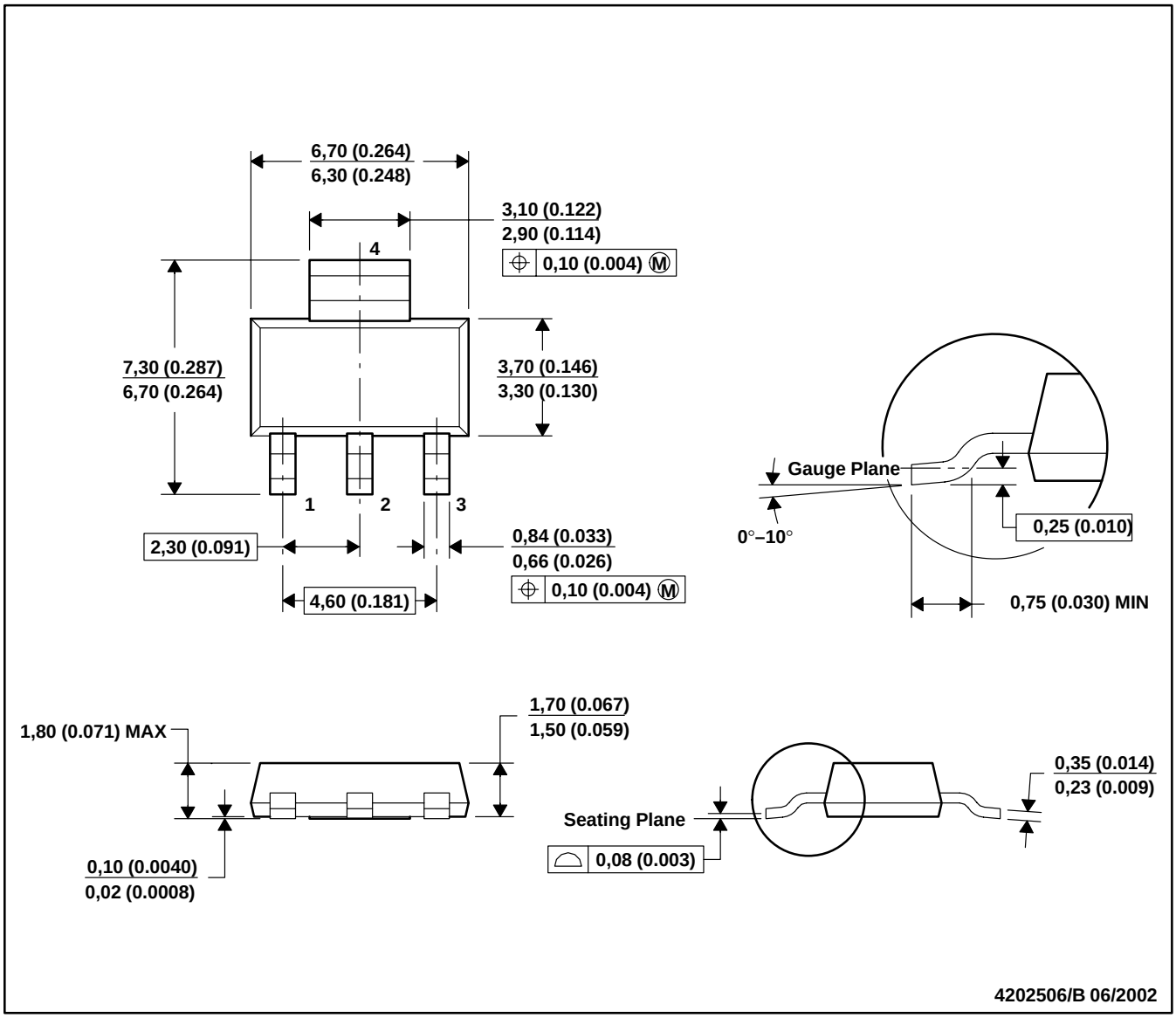
DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

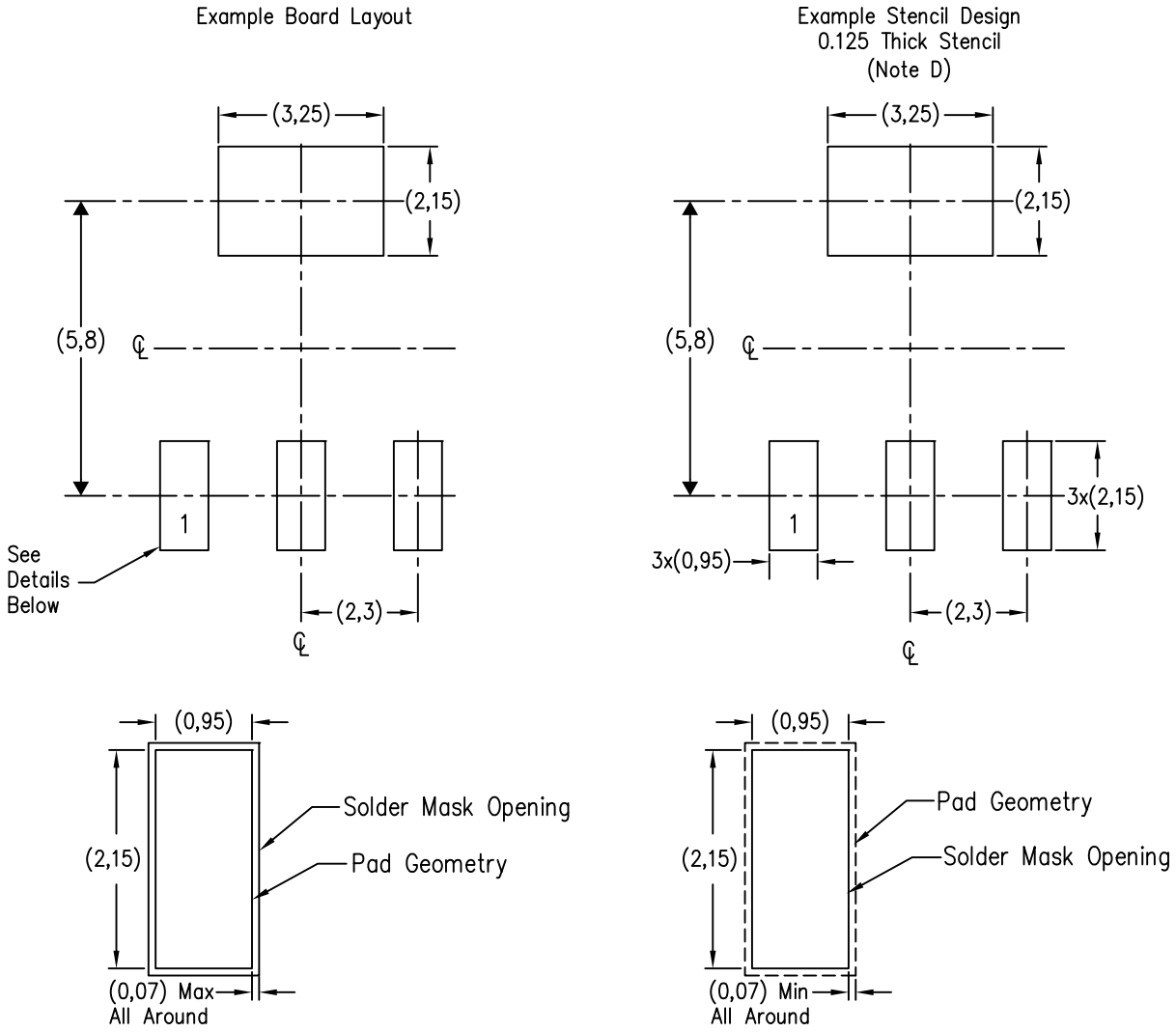
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



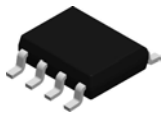
NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

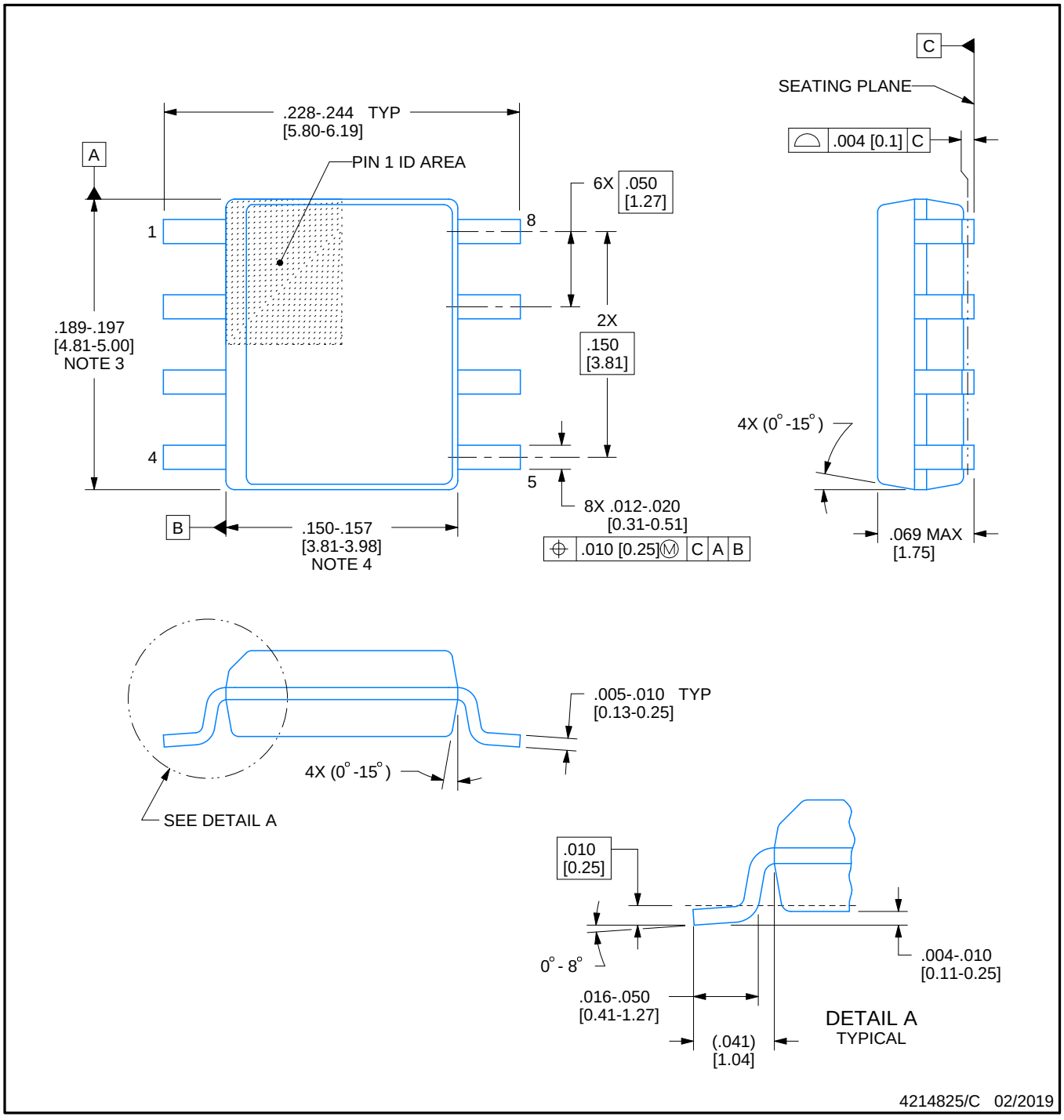


PACKAGE OUTLINE

D0008A

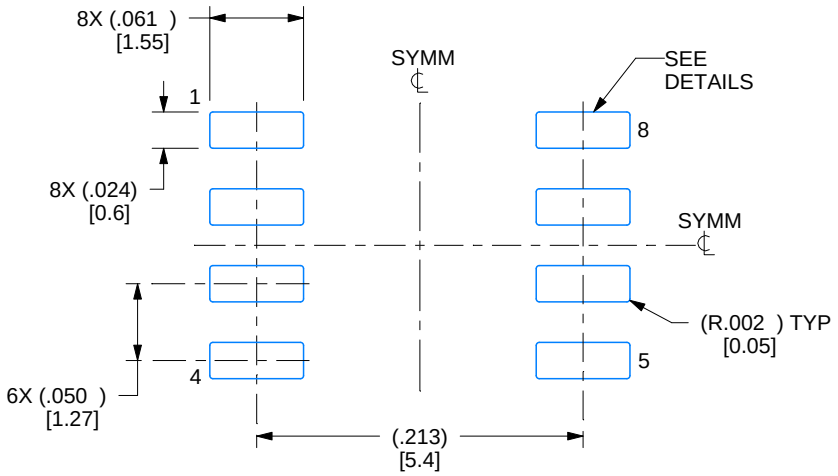
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

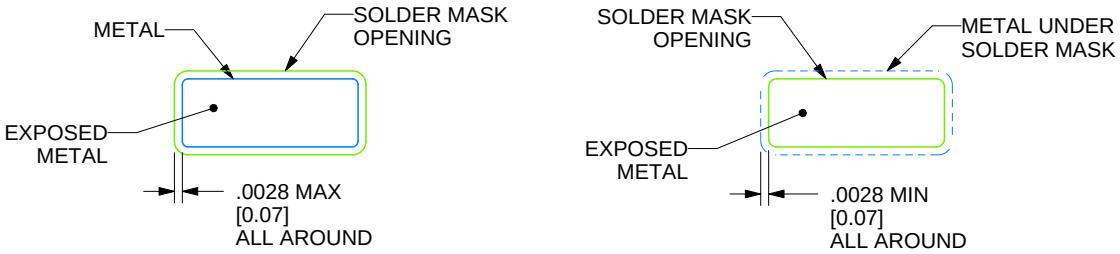


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

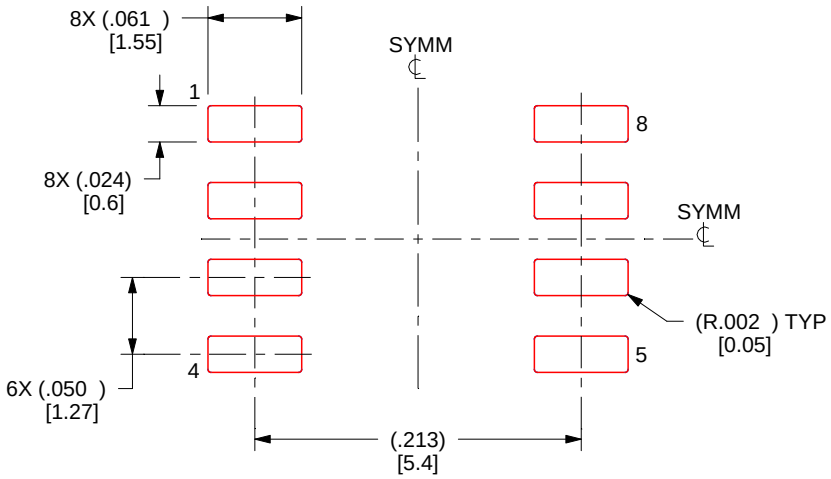
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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