TPS62230, TPS62231, TPS62232, TPS62233, TPS62234, TPS62235, TPS62236
TPS62237, TPS62238, TPS62239, TPS622310, TPS622311, TPS622312
TPS622313, TPS622314, TPS622315, TPS622316, TPS622317, TPS622318, TPS622319

SLVS941G – APRIL 2009 – REVISED AUGUST 2016

TPS6223xx 2-MHz and 3-MHz Ultra Small Step-Down Converter in 1 x 1.5 USON Package

1 Features

- 2 MHz / 3 MHz Switching Frequency
- Up to 94% Efficiency
- Output Peak Current up to 500 mA
- Operating Junction Temperature of –40°C to 125°C
- High PSRR (up to 90 dB)
- Small External Output Filter Components 1 µH and 4.7 µF
- V_{IN} range from 2.05 V to 6 V
- Optimized Power-Save Mode for Low Output Ripple Voltage
- Forced PWM Mode Operation
- Typ. 22-µA Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Small 1-mm × 1.5-mm × 0.6-mm USON Package
- 12-mm^2 Minimum Solution Size
- Supports 0.6-mm Maximum Solution Height

2 Applications

- LDO Replacement
- Portable Audio, Portable Media
- Low Power Wireless
- Low Power DSP Core Supply
- Digital Cameras

3 Description

The TPS6223x device family is a high-frequency, synchronous, step-down DC – DC converter optimized for battery powered portable applications. It supports up to 500-mA output current and allows the use of tiny and low-cost chip inductors and capacitors.

With a wide input voltage range of 2.05 V to 6 V, the device supports applications powered by Li-Ion batteries with extended voltage range. The minimum input voltage of 2.05 V allows as well the operation from Li-primary or two alkaline batteries. Different fixed output voltage versions are available from 1.0 V to 3.3 V.

The TPS6223x series features switch frequency up to 3.8 MHz. At medium to heavy loads, the converter operates in pulse width modulation (PWM) mode and automatically enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

Because of its excellent power supply rejection ratio (PSRR) and AC load regulation performance, the device is also suitable to replace linear regulators to obtain better power conversion efficiency.

The power-save mode in TPS6223x reduces the quiescent current consumption down to 22 µA during light load operation. It is optimized to achieve very low output voltage ripple even with small external component and features excellent AC load regulation.

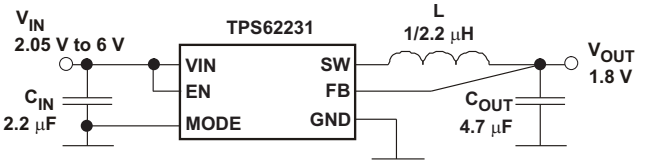
For very noise-sensitive applications, the device can be forced to PWM mode operation over the entire load range by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS6223x operates over a junction temperature range of –40°C to 125°C. It is available in a 1 mm × 1.5 mm × 0.6 mm 6-pin SON package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6223xx	USON (6)	1.45 mm x 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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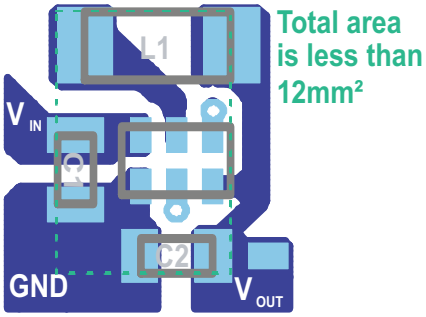
Small PCB Layout Size



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2015) to Revision G	Page
• Added device TPS622319	4
• Deleted Package information from *Device Comparison Table*, and added footnote	4
• Added *Receiving Notification of Documentation Updates* section	28

Changes from Revision E (December 2010) to Revision F	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision D (August 2010) to Revision E	Page
• Added device number TPS622318	1

Changes from Revision C (April 2010) to Revision D	Page
• Added device numbers TPS622315, TPS622316, and TPS622317	1
• Changed data sheet status from "Product Mix" to "Production Data"	1
• Deleted table footnote regarding "other voltage options"	4

Changes from Revision B (December 2009) to Revision C	Page
• Added device numbers TPS622312, TPS622313, and TPS622314	1

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Changes from Revision A (August 2009) to Revision B	Page
• Added device numbers TPS62235, TPS62236, TPS62237, TPS622311	1
• Changed the Title From: 3 MHz Ultra Small Step Down Converter in 1x1.5 SON Package To: 2 MHz / 3 MHz Ultra Small Step Down Converter in 1x1.5 SON Package	1
• Changed Feature: From: 3 MHz switch frequency To: 2 MHz / 3 MHz switch frequency	1
• Added Figure 6, Figure 7, and Figure 10	16
• Added Figure 15	17
• Added Figure 24, and Figure 25	19
• Added Figure 32	21
• Added Figure 41, and Figure 42	23

Changes from Original (April 2009) to Revision A	Page
• Added device numbers TPS62233, TPS62234, TPS62238, TPS62239, and TPS622310 to the data sheet	1

5 Device Comparison Table

PART NUMBER (1)	OUTPUT VOLTAGE	FREQUENCY [MHz]	Pulldown EN, MODE	PACKAGE MARKING
TPS62230	2.5 V	3	no	GV
TPS62231	1.8 V	3	no	GW
TPS62232	1.2 V	3	no	GX
TPS62239	1.0 V	3	no	OP
TPS622311	1.1V	2	no	PA
TPS622315	1.15V	2	no	RI
TPS62235	1.2V	2	no	OQ
TPS622318	1.25V	3	no	ST
TPS622319	1.2V	2	yes	3O
TPS622313	1.3 V	3	no	QF
TPS622314	1.5 V	3	no	QG
TPS62236	1.85V	2	no	OR
TPS622312	2.0 V	3	no	QE
TPS62234	2.1 V	3	no	OH
TPS62238	2.25 V	3	no	ON
TPS622310	2.3 V	3	no	OT
TPS622316	2.7 V	3	no	RJ
TPS622317	2.9 V	3	no	RK
TPS62233	3.0 V	3	no	OG
TPS62237	3.3 V	2	no	OS

(1) For detailed ordering information see the PACKAGE OPTION ADDENDUM at the end of this data sheet.

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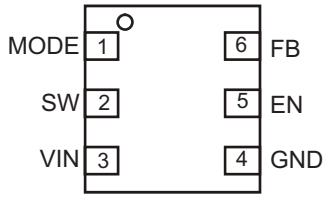
6 Pin Configuration and Functions

DRY Package
6-Pin USON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO		
VIN	3	Power	V_{IN} power supply pin
GND	4	Power	GND supply pin
EN	5	Input	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated except for the TPS622319, which has an integrated 1MΩ always active pull-down resistor.
SW	2	Output	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal
FB	6	Input	Feedback pin for the internal regulation loop. Connect this pin directly to the output capacitor.
MODE	1	Input	MODE pin = High forces the device to operate in PWM mode. Mode = Low enables the power save mode with automatic transition from pulse frequency modulation (PFM) to pulse width modulation (PWM) mode. This pin must be terminated except for the TPS622319 , which has an integrated 1MΩ always active pull-down resistor.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{IN}	Voltage at VIN and SW pin[2]	–0.3	7	V
	Voltage at EN, MODE pin[2]	–0.3	V_{IN} +0.3, ≤7	V
	Voltage at FB pin[2]	–0.3	3.6	V
	Peak output current	Internally limited		A
	Power dissipation	Internally limited		
T_J	Operating junction Temperature Range	–40	150	°C
T_{stg}	Storage Temperature Range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
	Charge- device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
Supply voltage V_{IN}[2]			2.05		6	V
Effective inductance				2.2		µH
Effective capacitance			2	4.7		µF
Recommended minimum supply voltage	$V_{OUT} \le V_{IN} - 1$ V[3]	500 mA maximum I_{OUT}[4]		3	3.6	V
		350 mA maximum I_{OUT}[4]		2.5	2.7	
	$V_{OUT} \le 1.8$ V	60 mA maximum output current[4]			2.05	
Operating junction temperature, T_J			–40		125	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$.
(2) The minimum required supply voltage for startup is 2.05 V. The part is functional down to the falling undervoltage lockout (UVL) threshold.
(3) For a voltage difference between minimum V_{IN} and V_{OUT} of ≥ 1 V
(4) Typical value applies for T_A = 25°C, maximum value applies for T_J ≤ 125°C, PCB layout must support proper thermal performance.

7.4 Thermal Information

THERMAL METRIC[1]		TPS6223x DRY (USON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	294.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	166.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	166.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	159.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, EN = V_{IN}, MODE = GND, T_J = –40°C to 125°C typical values are at T_J = 25°C (unless otherwise noted), C_{IN} = 2.2 µF, L = 2.2 µH, C_{OUT} = 4.7 µF.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage(2)			2.05		6	V
I_Q	Operating quiescent current	PFM operation (MODE = GND), I_{OUT} = 0 mA, device not switching, T_J = –40°C to 85°C			22	40	µA
		PFM operation (MODE = GND), I_{OUT} = 0 mA, device switching, V_{OUT} = 1.2 V			25		µA
		PWM operation (MODE = V_{IN}), I_{OUT} = 0 mA, device switching			3		mA
I_{SD}	Shutdown current	EN = GND, T_J = –40°C to 85°C			0.1	1	µA
V_{UVLO}	Undervoltage lockout threshold	Falling			1.8	1.9	V
		Rising			1.9	2.05	V
ENABLE, MODE THRESHOLD							
$V_{IH\ TH}$	Threshold for detecting high EN, MODE	2.05 V ≤ V_{IN} ≤ 6 V , rising edge			0.8	1	V
$V_{IL\ TH\ HYS}$	Threshold for detecting low EN, MODE	2.05 V ≤ V_{IN} ≤ 6 V , falling edge, T_J = –40°C to 85°C		0.4	0.6		V
R_{pd}	Pull-down resistor EN, MODE	TPS622319			1		MΩ
I_{IN}	Input bias current, EN, MODE	EN, MODE = GND or V_{IN}, T_J = –40°C to 85°C, except TPS622319			0.01	0.5	µA
POWER SWITCH							
$R_{DS(ON)}$	High side MOSFET ON-resistance	V_{IN} = 3.6 V, T_J = –40°C to 85°C			600	850	mΩ
	Low Side MOSFET ON-resistance				350	480	
I_{LIMF}	Forward current limit MOSFET high-side	V_{IN} = 3.6 V, open-loop		690	850	1050	mA
	Forward current limit MOSFET low-side			550	840	1220	mA
T_{JSD}	Thermal shutdown	Increasing junction temperature			150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature			20		°C
CONTROLLER							
t_{ONmin}	Minimum ON-time	MODE = V_{IN}, I_{OUT} = 0 mA			135		ns
t_{OFFmin}	Minimum OFF-time				40		ns
OUTPUT							
V_{REF}	Internal reference voltage				0.7		V
V_{OUT}	Output voltage accuracy(3)	MODE = GND, I_{OUT} = 0 mA			0%		
		MODE = V_{IN}, I_{OUT} = 0 mA	T_J = 25°C	–2%		2%	
			T_J = –40°C to 125°C	–2.5%		2.5%	
	DC output voltage load regulation	MODE = V_{IN}			0.001		%/mA
	DC output voltage line regulation	MODE = V_{IN}, I_{OUT} = 0 mA, 2.05 V ≤ V_{IN} ≤ 6 V			0		%/V
t_{Start}	Start-up time	Time from active EN to V_{OUT} = 1.8 V, 10-Ω load			100		µs
I_{LK_SW}	Leakage current into SW pin	V_{IN} = V_{OUT} = V_{SW} = 3.6 V, EN = GND(4) , T_J = –40°C to 85°C			0.1	0.5	µA

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application (PD(max)), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$.
(2) The minimum required supply voltage for startup is 2.05 V. The part is functional down to the falling under voltage lockout (UVL) threshold.
(3) $V_{IN} = V_O + 1.0$ V
(4) The internal resistor divider network is disconnected from FB pin.

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7.6 Typical Characteristics

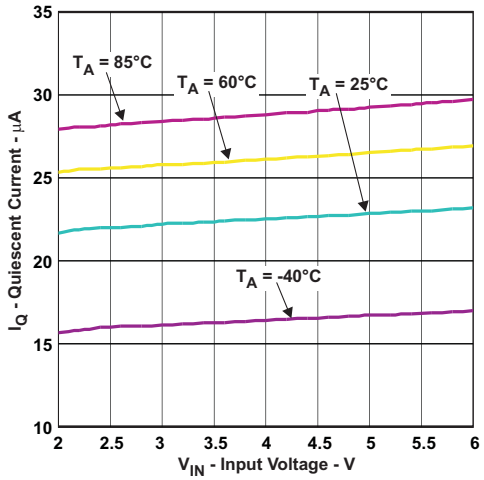

Figure 1. Quiescent Current I_Q vs Ambient Temperature T_A

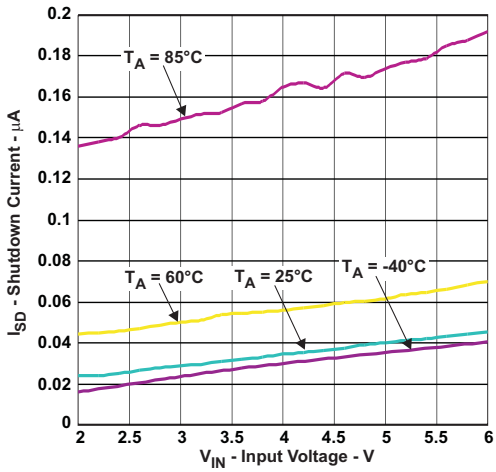

Figure 2. Shutdown Current I_{SD} vs Ambient Temperature T_A

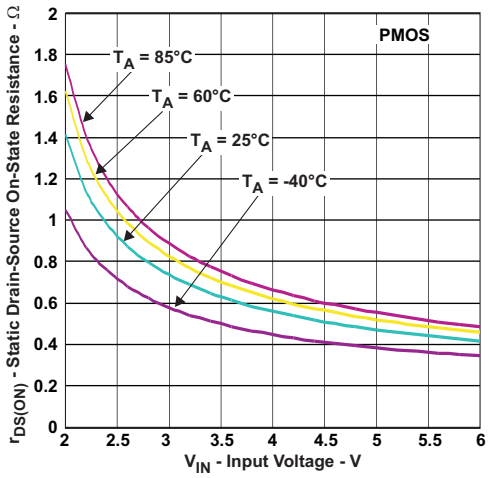

Figure 3. PMOS R_{DSON} vs Supply Voltage V_{IN} and Ambient Temperature T_A

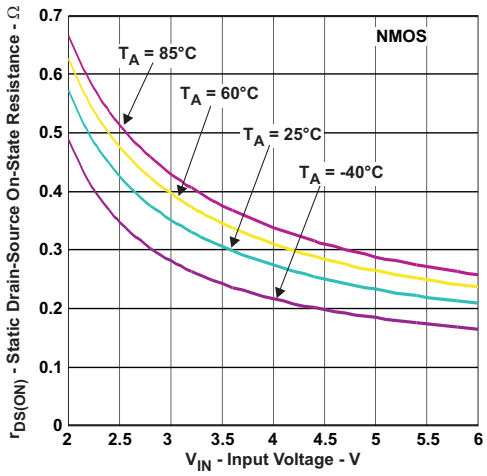

Figure 4. NMOS R_{DSON} vs Supply Voltage V_{IN} and Ambient Temperature T_A

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8 Detailed Description

8.1 Overview

The TPS6223x synchronous step-down DC – DC converter family includes a unique hysteretic PWM controller scheme which enables switch frequencies over 3 MHz, excellent transient and AC load regulation as well as operation with cost-competitive external components.

The controller topology supports forced PWM mode as well as power-save mode operation. Power-save mode operation reduces the quiescent current consumption down to 22 μA and ensures high conversion efficiency at light loads by skipping switch pulses. In forced PWM mode, the device operates on a quasi-fixed frequency, avoids pulse skipping, and allows filtering of the switch noise by external filter components.

The TPS6223x devices offer fixed output voltage options featuring smallest solution size by using only three external components.

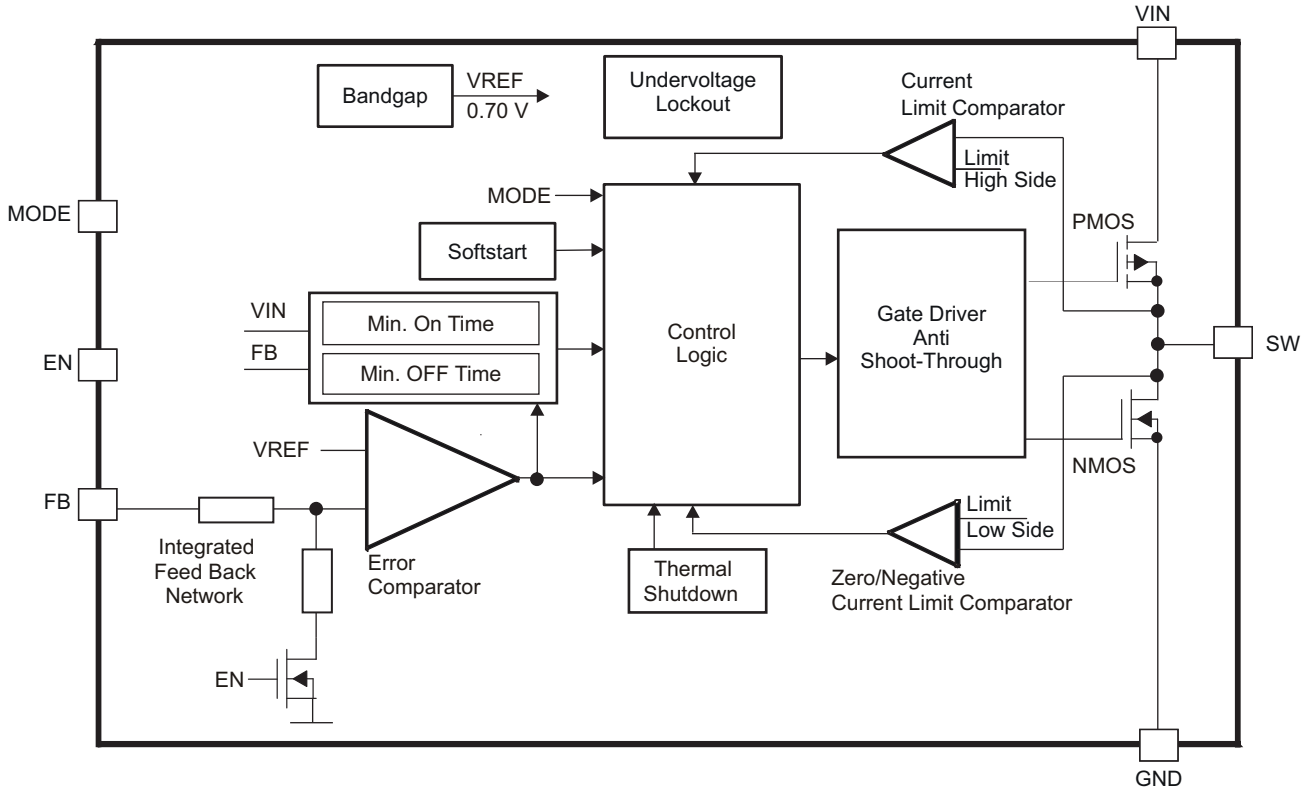
The internal switch current limit of typical 850 mA supports output currents of up to 500 mA, depending on the operating condition.

A significant advantage of TPS6223x compared to other hysteretic PWM controller topologies is its excellent DC and AC load regulation capability in combination with low-output voltage ripple over the entire load range which makes this part well suited for audio and RF applications.

Once the output voltage falls below the threshold of the error comparator, a switch pulse is initiated, and the high-side switch is turned on. It remains turned on until a minimum ON-time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high-side switch current limit. Once the high-side switch turns off, the low-side switch rectifier is turned on and the inductor current ramps down until the high-side switch turns on again or the inductor current reaches zero.

In forced PWM mode operation, negative inductor current is allowed to enable continuous conduction mode even at no load condition.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6223x devices have a UVLO threshold set to 1.8 V (typical). Fully functional operation is permitted for input voltage down to the falling UVLO threshold level. The converter starts operation again once the input voltage trips the rising UVLO threshold level.

8.3.2 Enable and Shutdown

The device starts operation when EN is set high and starts up with the soft-start as previously described. For proper operation, the EN pin must be terminated and must not be left floating, except for the TPS622319, which has an integrated 1MΩ always active pull-down resistor.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.1 μA. In this mode, the P- and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off.

The EN input can be used to control power sequencing in a system with various DC – DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails.

8.3.3 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

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8.4 Device Functional Modes

8.4.1 Soft-Start

The TPS6223x has an internal soft start circuit that controls the ramp up of the output voltage and limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system generates a monotonic ramp up of the output voltage and reaches the nominal output voltage typically 100 µs after EN pin was pulled high.

If the output voltage does not reached its target value by this time, such as in the case of heavy load, the converter then operates in a current limit mode set by its switch current limits.

TPS6223x is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.4.2 Power-Save Mode

Connecting the MODE pin to GND enables the automatic PWM and power-save mode operation. The converter operates in quasi-fixed frequency PWM mode at moderate to heavy loads and in the pulse frequency modulation (PFM) mode during light loads, which maintains high efficiency over a wide load current range. In PFM mode, the device starts to skip switch pulses and generates only single pulses with an ON-time of t_{ONmin}. The PFM mode frequency depends on the load current and the external inductor and output capacitor values. The PFM mode of TPS6223x is optimized for low-output voltage ripple if small external components are used. Even at low output currents, the PFM frequency is above the audible noise spectrum and makes this operation mode suitable for audio applications.

The ON-time t_{ONmin} can be estimated to:

$$t_{ONmin} = \frac{V_{OUT}}{V_{IN}} \times 260\ \text{ns} \tag{1}$$

Therefore, the peak inductor current in PFM mode is approximately:

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ONmin} \tag{2}$$

The transition from PFM into PWM mode and vice versa can be estimated to:

$$I_{OUT_PFM/PWM} = 0.5 \times I_{LPFMpeak}$$

where

- t_{ON}: High-side switch ON-time [ns]
- V_{IN}: Input voltage [V]
- V_{OUT}: Output voltage [V]
- L: Inductance [µH]
- $I_{LPFMpeak}$: PFM inductor peak current [mA]
- $I_{OUT_PFM/PWM}$: Output current for PFM to PWM mode transition and vice versa [mA] (3)

8.4.3 Forced PWM Mode

Pulling the MODE pin high forces the converter to operate in a continuous conduction PWM mode even at light load currents. The advantage is that the converter operates with a quasi-fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads. This pin must be terminated except for the TPS622319 , which has an integrated 1MΩ always active pull-down resistor.

For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

Device Functional Modes (continued)

8.4.4 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. To maintain the output voltage, the high side switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high-side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times \left(R_{DS(on)}max + R_L\right)$$

where

- I_{OUT}max: maximum output current plus inductor ripple current
- $R_{DS(on)}$max: maximum P-channel switch RDSon
- R_L: DC resistance of the inductor
- V_{OUT}max: nominal output voltage plus maximum output voltage tolerance (4)

8.4.5 Short Circuit Protection

The TPS6223x integrates a high-side and low-side MOSFET current limit to protect the device against heavy load or short circuit. The current in the switches is monitored by current limit comparators. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on to ramp down the current in the inductor. The high-side MOSFET switch can only turn on again, once the current in the low side MOSFET switch has decreased below the threshold of its current limit comparator.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6223x device family are high-frequency, synchronous, step-down DC-DC converters providing switch frequencies up to 3.8 MHz. Different fixed output voltage versions are available from 1.0 V to 3.3 V.

9.2 Typical Application

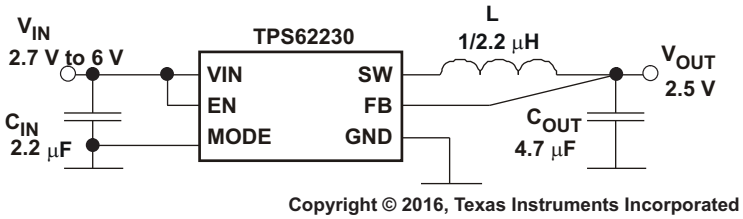

Figure 5. TPS62230 2.5-V Output

9.2.1 Design Requirements

The device operates over an input voltage range from 2.05 V to 6 V. The device family offers a broad range of internally fixed output voltage options from 1 V to 3.3 V. The TPS6223x is easy to use and needs just three external components; however, the selection of external components and PCB layout must comply with the design guidelines to achieve specified performance.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Filter Design (Inductor and Output Capacitor)

The TPS6223x is optimized to operate with effective inductance values in the range of 0.7 µH to 4.3 µH and with effective output capacitance in the range of 2.0 µF to 15 µF. The internal compensation is optimized to operate with an output filter of L = 1.0 µH/2.2 µH and C_{OUT} = 4.7 µF. Larger or smaller inductor/capacitor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *Checking Loop Stability* section.

Typical Application (continued)

9.2.2.2 Inductor Selection

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} . Equation 5 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 6. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \tag{5}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency
- L = Inductor value
- ΔI_L= Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current (6)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (that is, quality factor) and to a smaller extent by the inductor DCR value. To achieve high-efficiency operation, take care in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6223x converters.

Table 1. List of Inductors

INDUCTANCE (µH)	DIMENSIONS (mm^3)	INDUCTOR TYPE	SUPPLIER (1)
1.0 / 2.2	2.5 × 2.0 × 1.2	LQM2HPN1R0MJ0	Murata
2.2	2.0 × 1.2 × 0.55	LQM21PN2R2	Murata
1.0 / 2.2	2.0 × 1.2 × 1.0	MIPSZ2012	FDK
1.0 / 2.2	2.0 × 2.5 × 1.2	MIPSA2520	FDK
1.0 / 2.2	2.0 × 1.2 × 1.0	KSLI2012 series	Hitachi Metal

(1) See *Third-Party Products Disclaimer*

9.2.2.3 Output Capacitor Selection

The unique hysteretic PWM control scheme of the TPS62230 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operate in power save mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

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9.2.2.4 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 2.2-µF to 4.7-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering. Because ceramic capacitor loses up to 80% of its initial capacitance at 5 V, TI recommends using 4.7 µF input capacitors for input voltages > 4.5 V.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2 shows a list of tested input and output capacitors.

Table 2. List of Capacitors

CAPACITANCE [µF]	SIZE	CAPACITOR TYPE	SUPPLIER(1)
2.2	0402	GRM155R60J225	Murata
4.7	0402	AMK105BJ475MV	Taiyo Yuden
4.7	0402	GRM155R60J475	Murata
4.7	0402	CL05A475MQ5NRNC	Samsung
4.7	0603	GRM188R60J475	Murata

(1) See *Third-Party Products Disclaimer*

9.2.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

9.2.3 Application Curves

9.2.3.1 V_{OUT} = 1.1 V – TPS622311

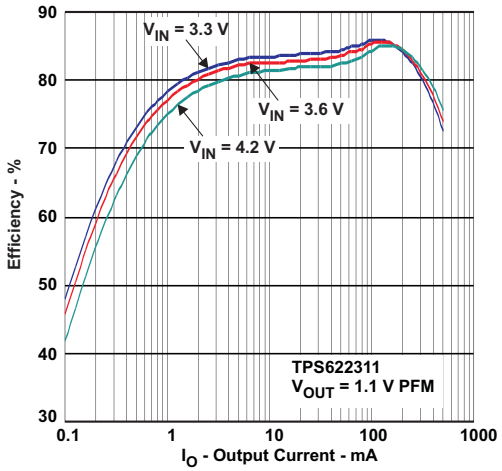

Figure 6. Efficiency vs I_{OUT}, PFM Mode – TPS622311

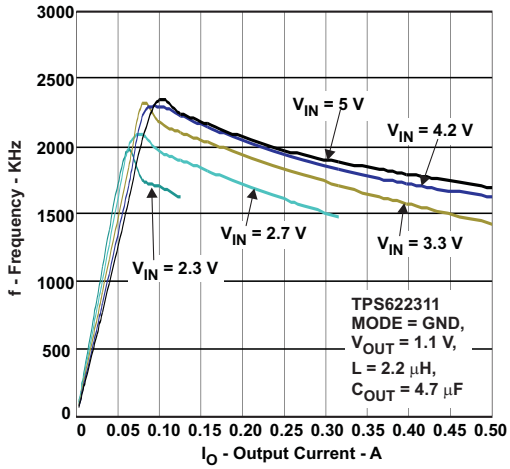

Figure 7. Switching Frequency vs Output Current, 1.1-V Output Voltage, PFM Mode – TPS622311

9.2.3.2 V_{OUT} = 1.2 V – TPS62232/TPS62235

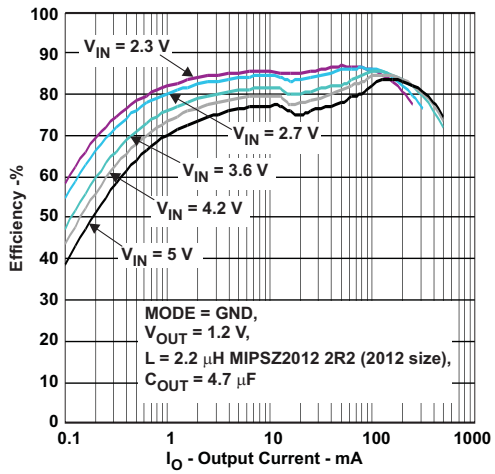

Figure 8. Efficiency PFM / PWM Mode, 1.2-V Output Voltage – TPS62232

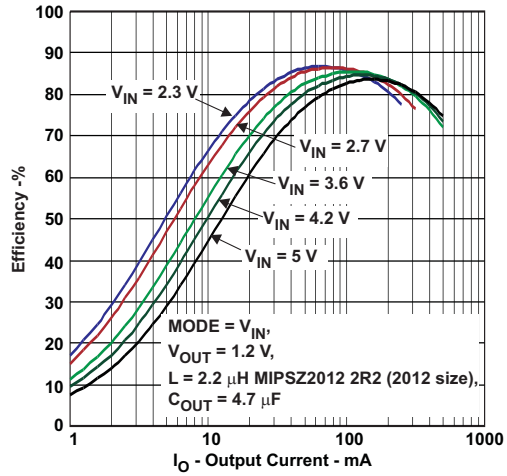

Figure 9. Efficiency Forced PWM Mode, 1.2-V Output Voltage – TPS62232

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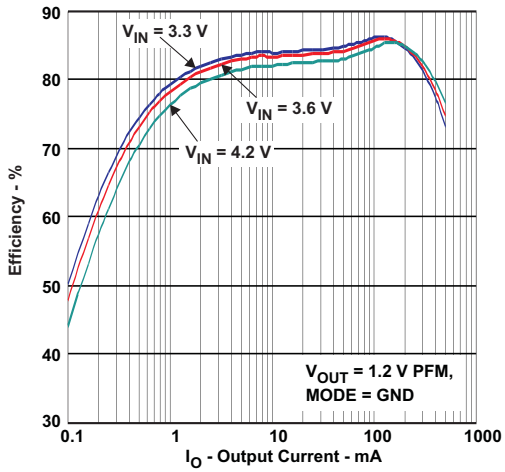

Figure 10. Efficiency vs I_{OUT}, PFM / PWM Mode – TPS62235

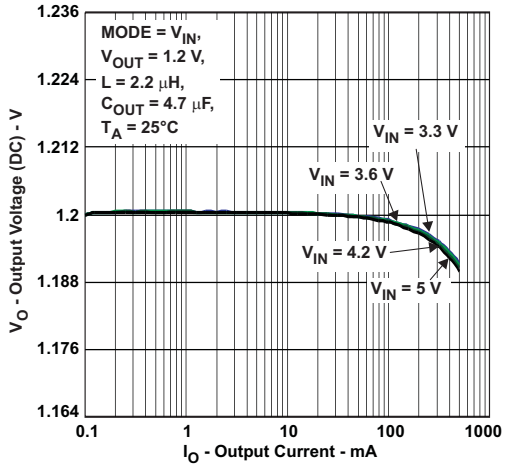

Figure 11. 1.2-V Output Voltage Accuracy Forced PWM Mode – TPS62232

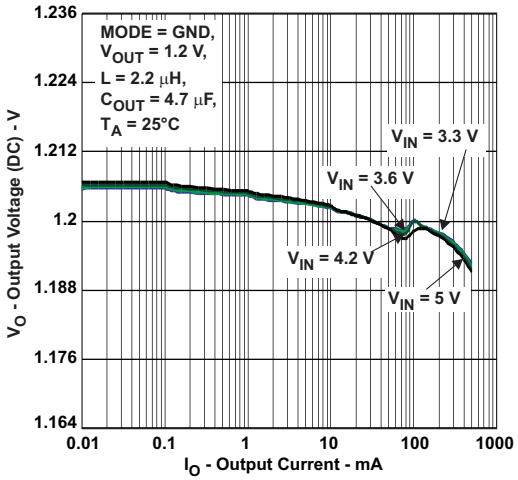

Figure 12. 1.2-V Output Voltage Accuracy PFM/PWM Mode – TPS62232

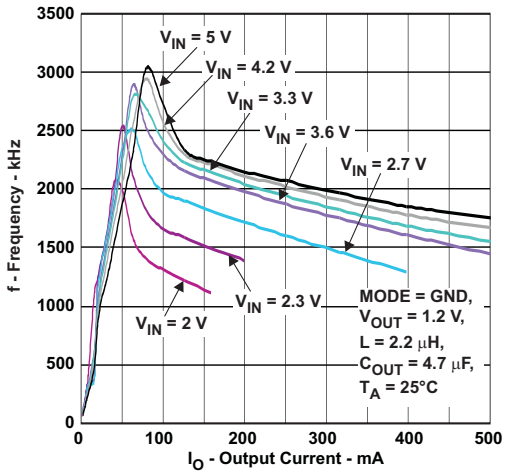

Figure 13. Switching Frequency vs Output Current, 1.2-V Output Voltage, PFM/PWM Mode – TPS62232

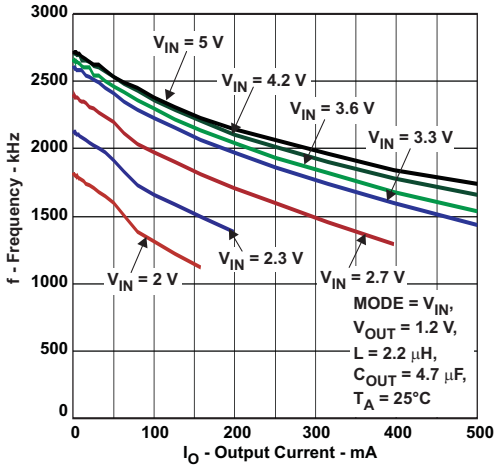

Figure 14. Switching Frequency vs Output Current, 1.2-V Output Voltage, Forced PWM Mode – TPS62232

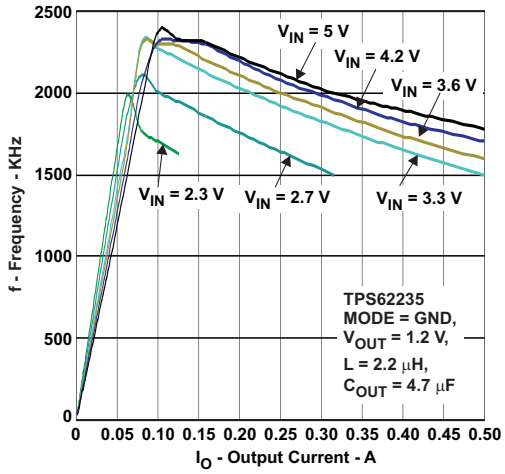

Figure 15. Switching Frequency vs Output Current, 1.2-V Output Voltage, PFM/PWM Mode – TPS62235

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9.2.3.3 V_{OUT} = 1.8 V – TPS62231

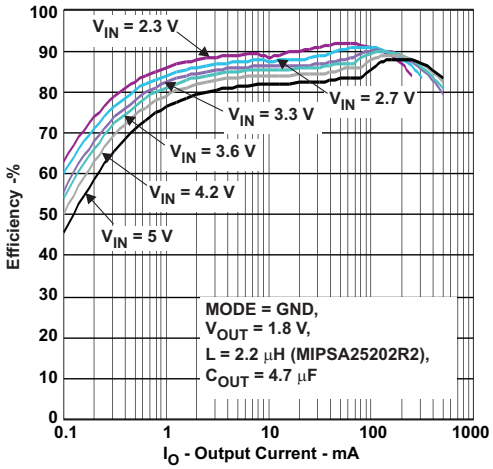

Figure 16. Efficiency PFM/PWM Mode, 1.8-V Output Voltage – TPS62231

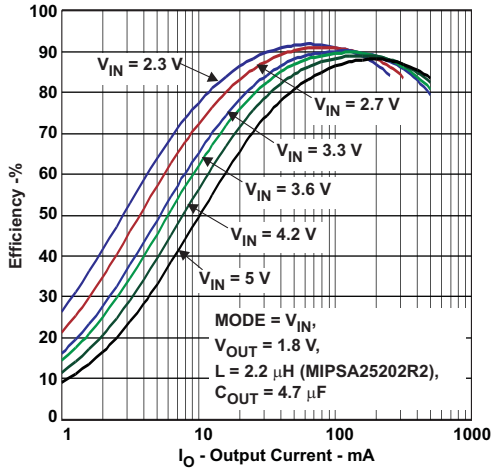

Figure 17. Efficiency Forced PWM Mode, 1.8-V Output Voltage – TPS62231

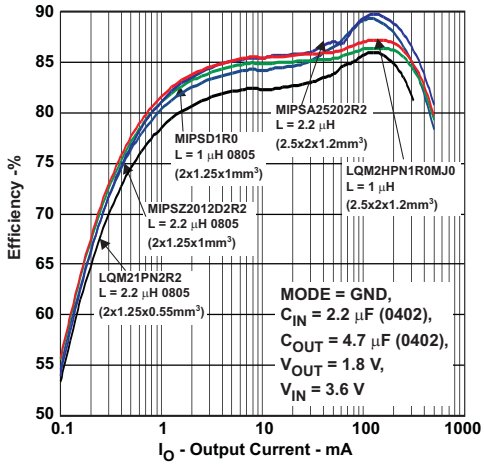

Figure 18. Comparison Efficiency vs Inductor Value and Size – TPS62231

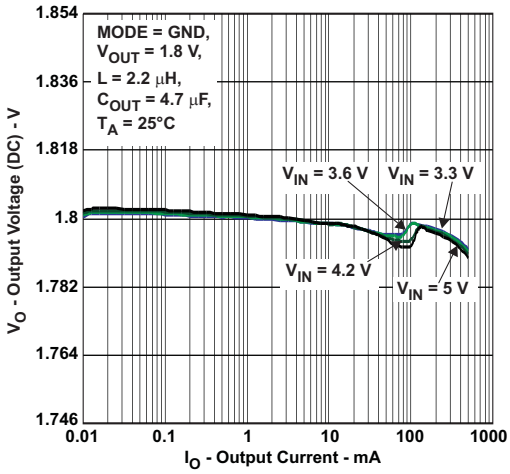

Figure 19. 1.8-V Output Voltage Accuracy PFM / PWM Mode – TPS62231

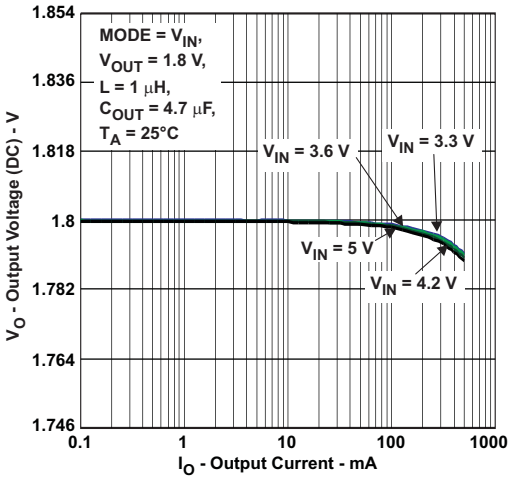

Figure 20. 1.8-V Output Voltage Accuracy Forced PWM Mode – TPS62231

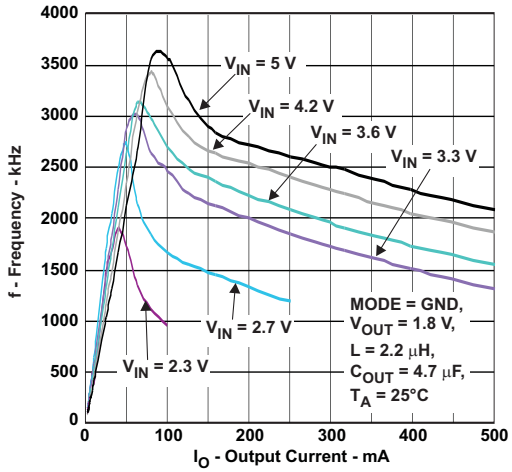

Figure 21. Switching Frequency vs Output Current, 1.8-V Output Voltage, PFM/PWM Mode – TPS62231

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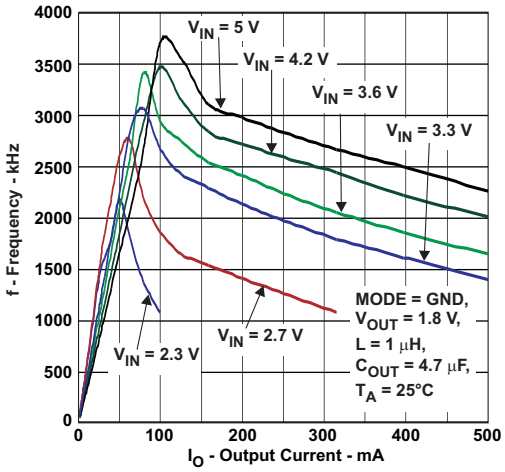

Figure 22. Switching Frequency vs Output Current, 1.8-V Output Voltage, PFM/PWM Mode – TPS62231

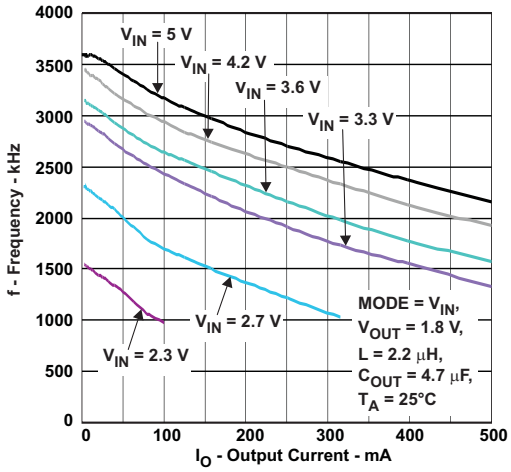

Figure 23. Switching Frequency vs Output Current, 1.8-V Output Voltage, Forced PWM Mode – TPS62231

9.2.3.4 V_{OUT} = 1.85 V – TPS62236

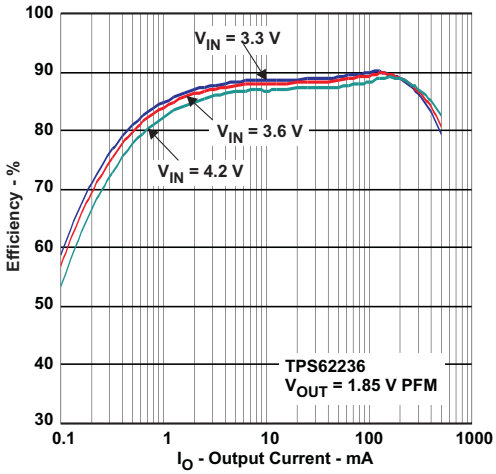

Figure 24. Efficiency vs I_{OUT}, PFM/PWM Mode – TPS62236

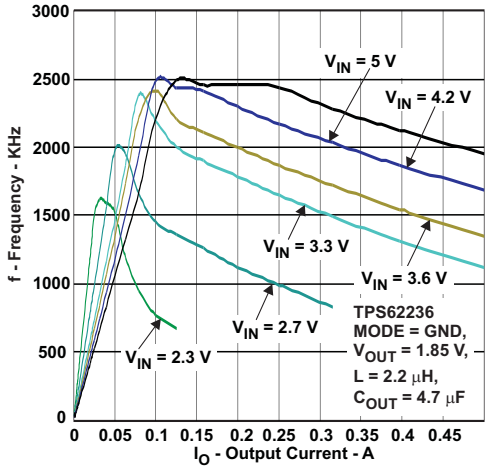

Figure 25. Switching Frequency vs Output Current, 1.85-V Output Voltage, PFM/PWM Mode – TPS62236

9.2.3.5 V_{OUT} = 2.5 V – TPS62230

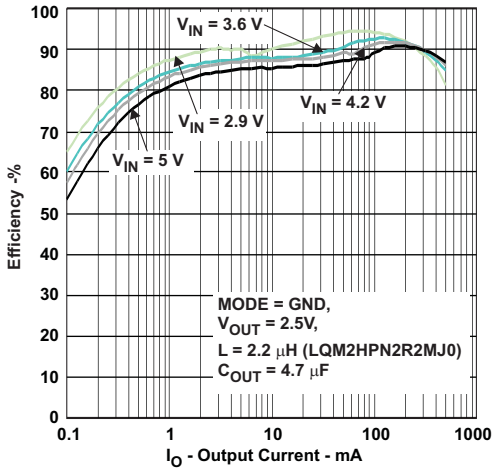

Figure 26. Efficiency PFM/PWM Mode, 2.5-V Output Voltage – TPS62230

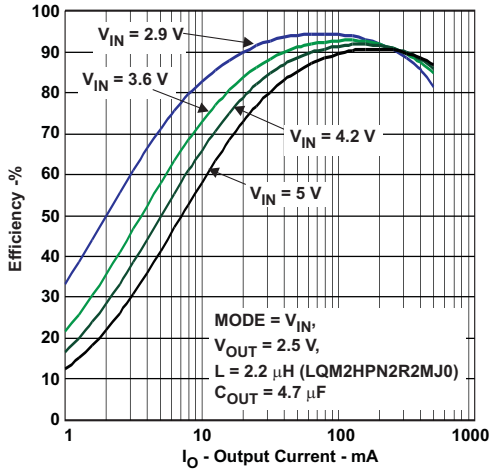

Figure 27. Efficiency Forced PWM Mode, 2.5-V Output Voltage – TPS62230

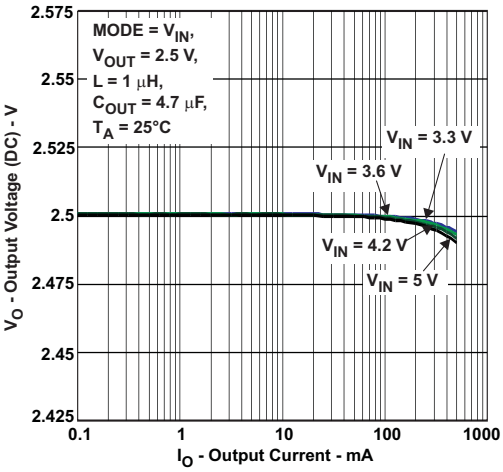

Figure 28. 2.5V Output Voltage Accuracy Forced PWM Mode – TPS62230

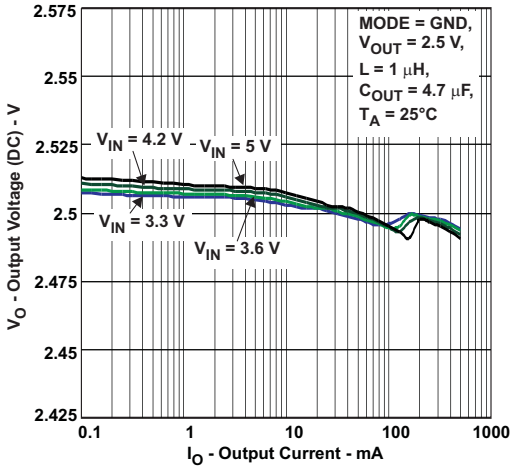

Figure 29. 2.5-V Output Voltage Accuracy PFM/PWM Mode – TPS62230

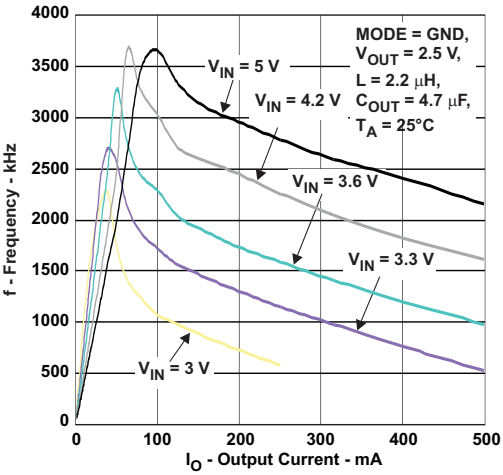

Figure 30. Switching Frequency vs Output Current, 2.5-V Output Voltage, PFM/PWM Mode – TPS62230

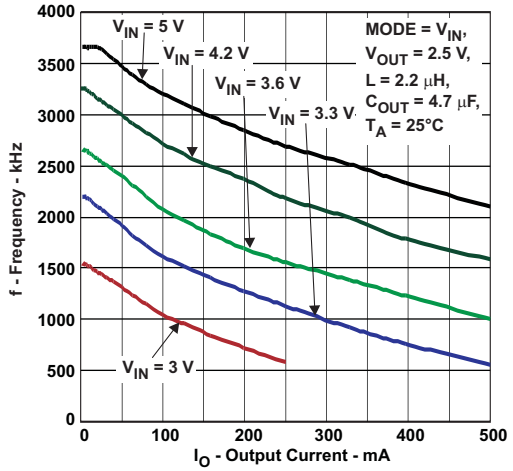

Figure 31. Switching Frequency vs Output Current, 2.5-V Output Voltage, Forced PWM Mode – TPS62230

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9.2.3.6 V_{OUT} = 3.0 V – TPS62233

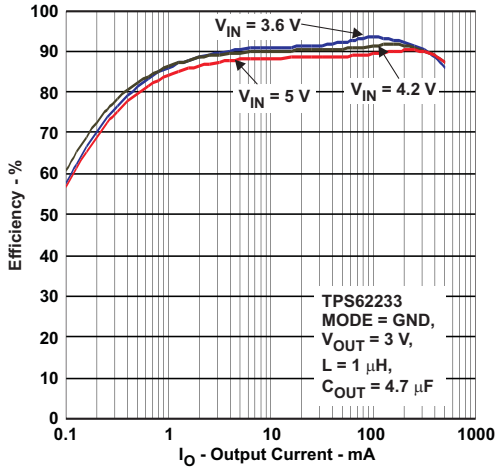

Figure 32. Efficiency vs I_{OUT} – TPS62233

9.2.3.7 Start-Up

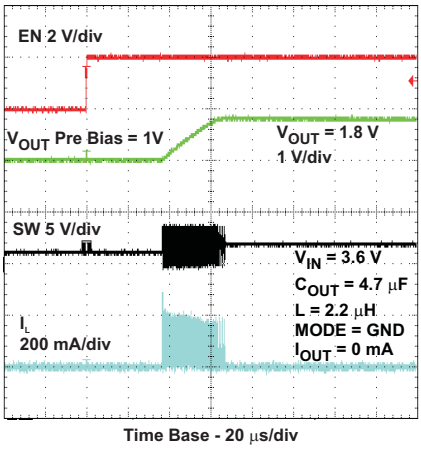

Figure 33. Start-Up in 1-V Prebiased Output – TPS62231

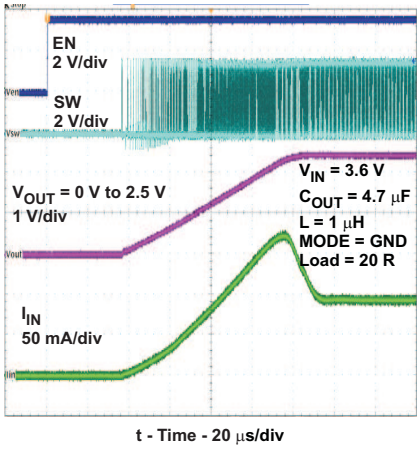

Figure 34. Start-Up into 20 Ω Load, V_{OUT} 2.5 V – TPS62230

9.2.3.8 PFM / PWM Operation

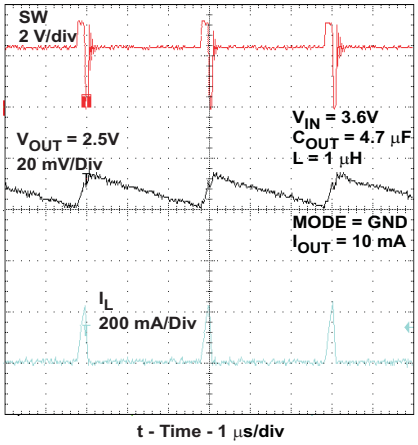

Figure 35. PFM Mode Operation, L = 1.0 µH, I_{OUT} = 10 mA – TPS62230

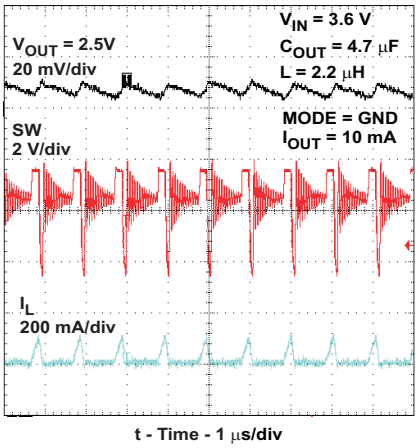

Figure 36. PFM Mode Operation, L = 2.2 µH, I_{OUT} = 10 mA – TPS62230

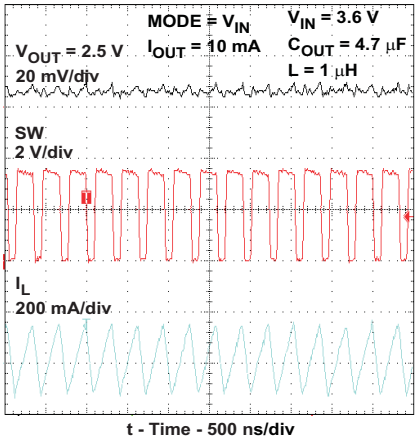

Figure 37. Forced PWM Mode Operation I_{OUT} = 10 mA – TPS62230

9.2.3.9 Peak-to-Peak Output Ripple Voltage

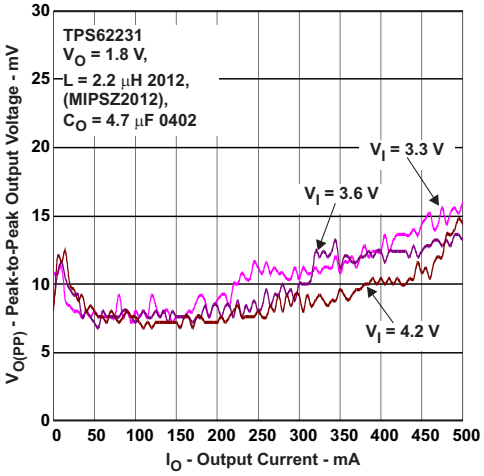

Figure 38. Output Voltage, Peak-to-Peak vs Output Current – TPS62231

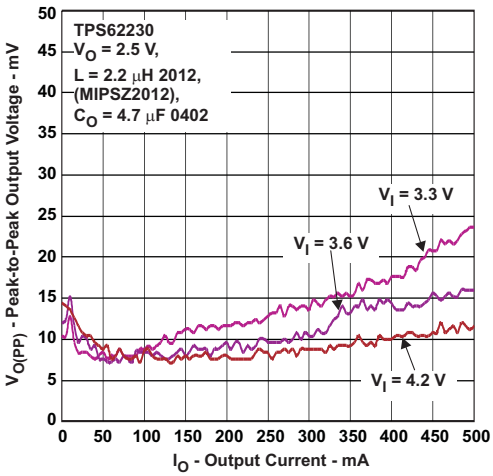

Figure 39. Output Voltage, Peak-to-Peak vs Output Current – TPS62230

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9.2.3.10 Power-Supply Rejection

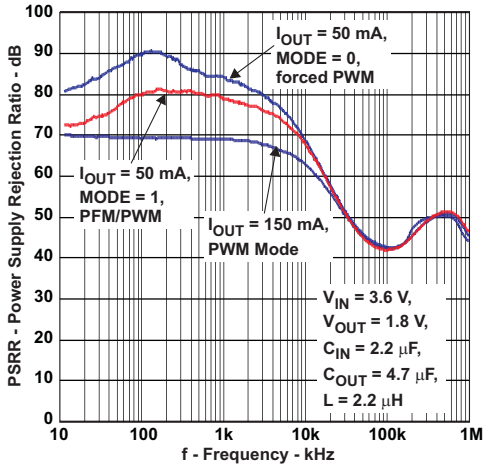

Figure 40. 1.8-V Power-Supply Rejection Ratio – TPS62231

9.2.3.11 Spurious Output Noise

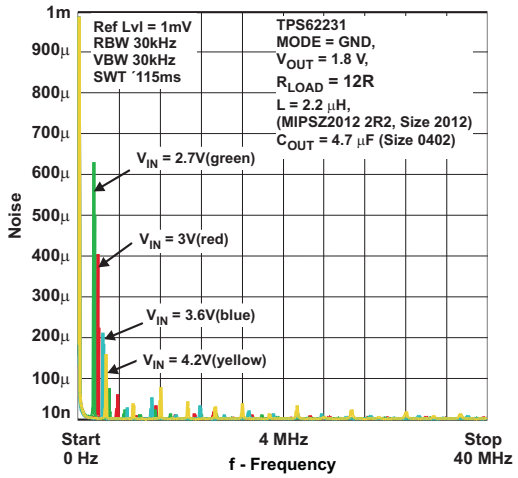

Figure 41. Spurious Output Noise, 12R Load – TPS62231

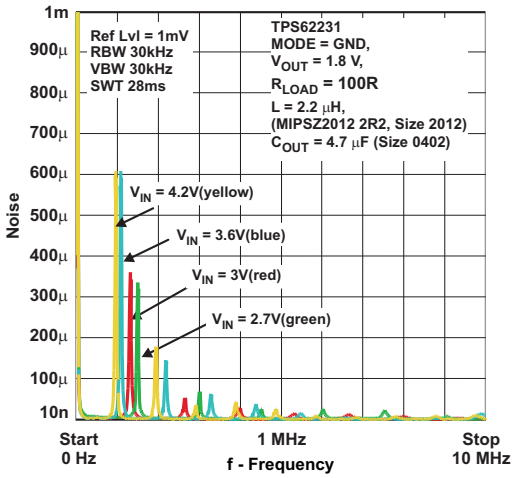

Figure 42. Spurious Output Noise, 100R Load – TPS62231

9.2.3.12 Line Transient Response

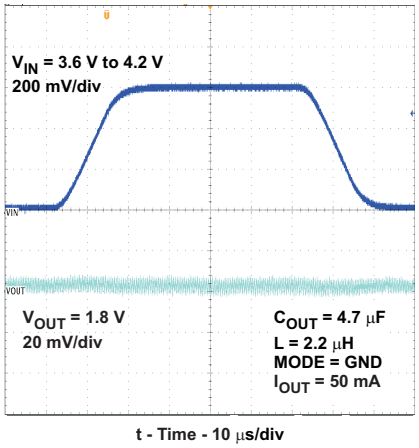

Figure 43. Line Transient Response, PFM Mode – TPS62231

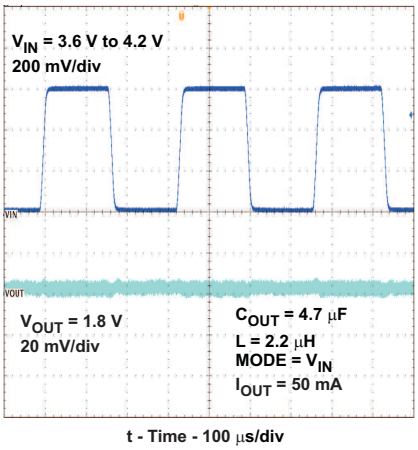

Figure 44. Line Transient Response, PWM Mode – TPS62231

9.2.3.13 Mode Transition

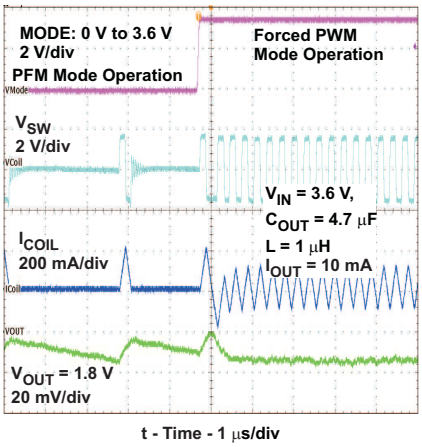

Figure 45. Mode Transition PFM / Forced PWM Mode – TPS62231

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9.2.3.14 AC-Load Regulation

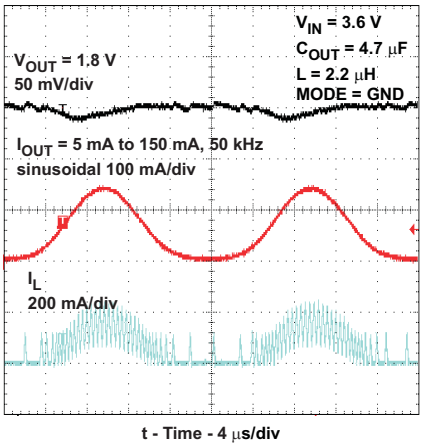

Figure 46. AC – Load Regulation Performance 1.8-V V_{OUT}, PFM Mode – TPS62231

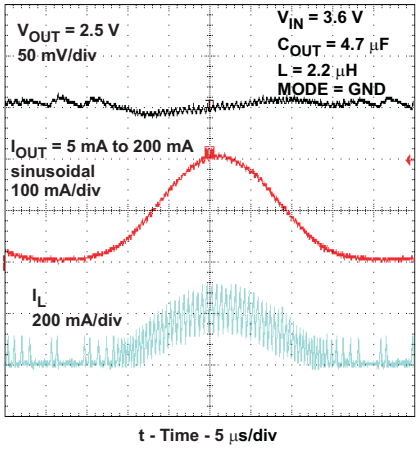

Figure 47. AC – Load Regulation Performance 2.5-V V_{OUT}, PFM Mode – TPS62230

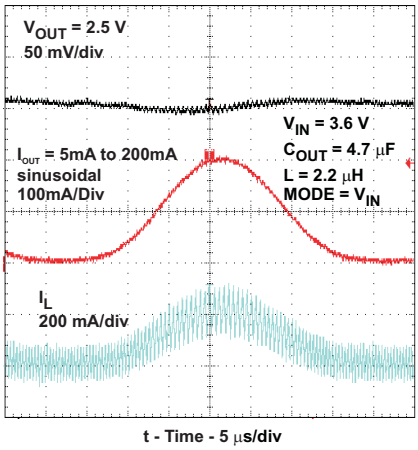

Figure 48. AC – Load Regulation Performance 2.5-V V_{OUT}, PWM Mode – TPS62230

9.2.3.15 Load Transient Response

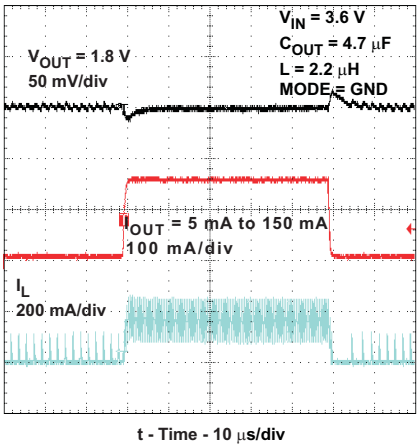

Figure 49. Load Transient Response 5 mA to 150 mA, PFM to PWM Mode, V_{OUT} 1.8 V – TPS62231

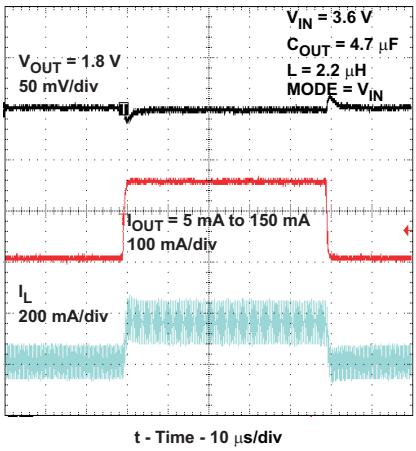

Figure 50. Load Transient Response 5 mA to 150 mA, Forced PWM Mode, V_{OUT} 1.8 V – TPS62231

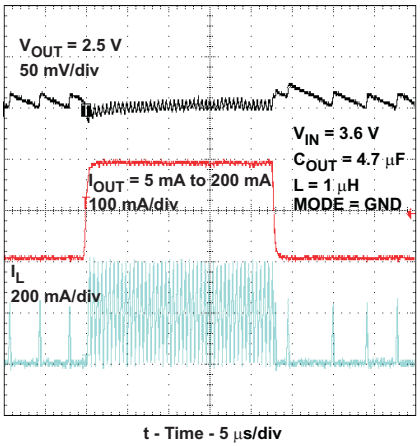

Figure 51. Load Transient Response 5 mA to 200 mA, PFM to PWM Mode, V_{OUT} 2.5 V – TPS62230

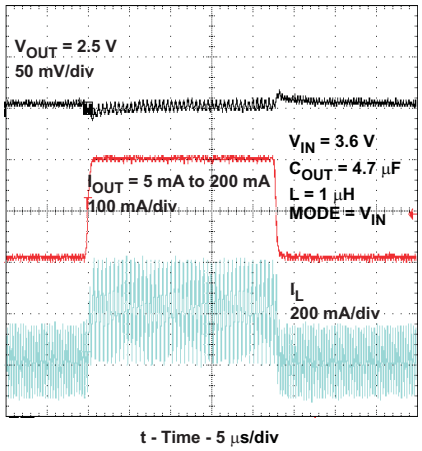

Figure 52. Load Transient Response 5 mA to 200 mA, Forced PWM Mode, V_{OUT} 2.5 V – TPS62230

9.3 System Examples

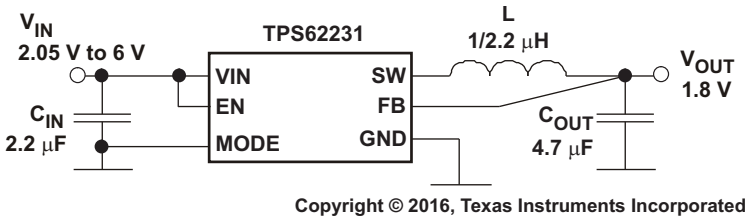

Figure 53. TPS62231 1.8-V Output

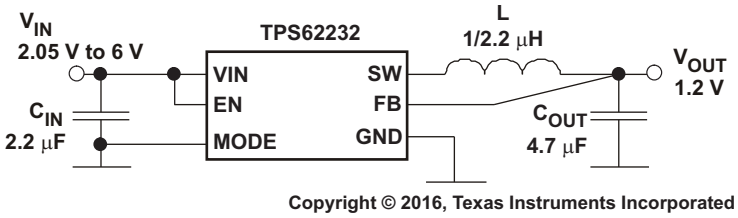

Figure 54. TPS62232 1.2-V Output

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10 Power Supply Recommendations

The TPS6223x device family has no special requirements for its input power supply. The output current of the input power supply must to be rated according to the supply voltage, output voltage and output current of the TPS6223x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in the board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, as well as EMI problems. It is critical to provide a low-inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Keep the common path to the GND pin, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line must be connected to the output capacitor and routed away from noisy components and traces (for example, SW line).

11.2 Layout Example

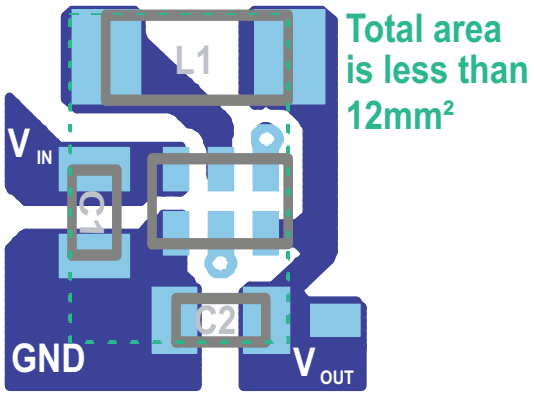

Figure 55. Recommended PCB Layout for TPS6223x

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62230	Click here	Click here	Click here	Click here	Click here
TPS62231	Click here	Click here	Click here	Click here	Click here
TPS62232	Click here	Click here	Click here	Click here	Click here
TPS62233	Click here	Click here	Click here	Click here	Click here
TPS62234	Click here	Click here	Click here	Click here	Click here
TPS62235	Click here	Click here	Click here	Click here	Click here
TPS62236	Click here	Click here	Click here	Click here	Click here
TPS62237	Click here	Click here	Click here	Click here	Click here
TPS62238	Click here	Click here	Click here	Click here	Click here
TPS62239	Click here	Click here	Click here	Click here	Click here
TPS622310	Click here	Click here	Click here	Click here	Click here
TPS622311	Click here	Click here	Click here	Click here	Click here
TPS622312	Click here	Click here	Click here	Click here	Click here
TPS622313	Click here	Click here	Click here	Click here	Click here
TPS622314	Click here	Click here	Click here	Click here	Click here
TPS622315	Click here	Click here	Click here	Click here	Click here
TPS622316	Click here	Click here	Click here	Click here	Click here
TPS622317	Click here	Click here	Click here	Click here	Click here
TPS622318	Click here	Click here	Click here	Click here	Click here
TPS622319	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62230DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GV	Samples
TPS62230DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GV	Samples
TPS622310DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OT	Samples
TPS622310DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OT	Samples
TPS622311DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PA	Samples
TPS622311DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PA	Samples
TPS622312DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QE	Samples
TPS622312DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QE	Samples
TPS622313DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QF	Samples
TPS622313DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QF	Samples
TPS622314DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QG	Samples
TPS622314DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QG	Samples
TPS622315DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RI	Samples
TPS622315DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RI	Samples
TPS622316DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RJ	Samples
TPS622316DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RJ	Samples
TPS622317DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RK	Samples
TPS622317DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RK	Samples
TPS622318DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ST	Samples
TPS622318DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ST	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS622319DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3O	Samples
TPS622319DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3O	Samples
TPS62231DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GW	Samples
TPS62231DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GW	Samples
TPS62232DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 125	GX	Samples
TPS62232DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GX	Samples
TPS62233DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OG	Samples
TPS62233DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OG	Samples
TPS62234DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OH	Samples
TPS62234DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OH	Samples
TPS62235DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OQ	Samples
TPS62235DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OQ	Samples
TPS62236DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OR	Samples
TPS62236DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OR	Samples
TPS62237DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OS	Samples
TPS62237DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OS	Samples
TPS62238DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ON	Samples
TPS62238DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ON	Samples
TPS62239DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OP	Samples
TPS62239DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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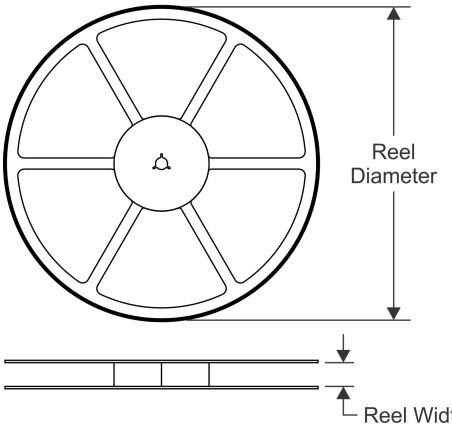
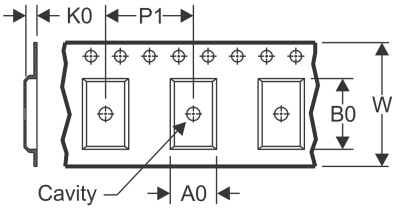
TAPE AND REEL INFORMATION

REEL DIMENSIONS

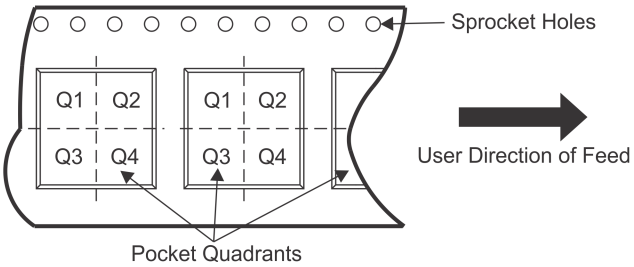


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

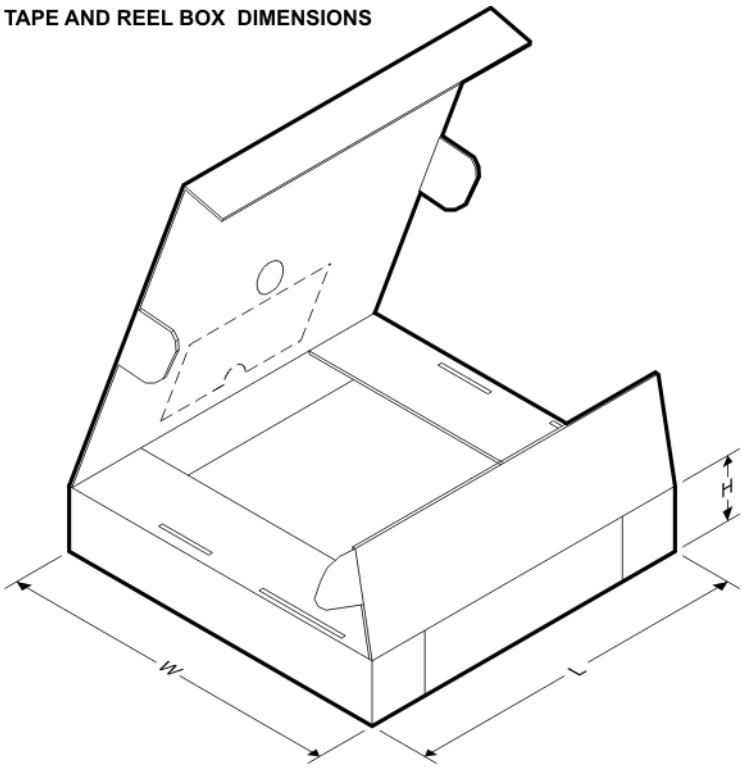


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62230DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62230DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622310DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622310DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622311DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS622312DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622312DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622313DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622313DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622314DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622314DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622315DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622315DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622316DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622316DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622317DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622317DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622318DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS622318DRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS622318DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622319DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS622319DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62231DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62231DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS62231DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62233DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62233DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62234DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62234DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62235DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62235DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62236DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62236DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62237DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62237DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS62237DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62238DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62238DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62239DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS62239DRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

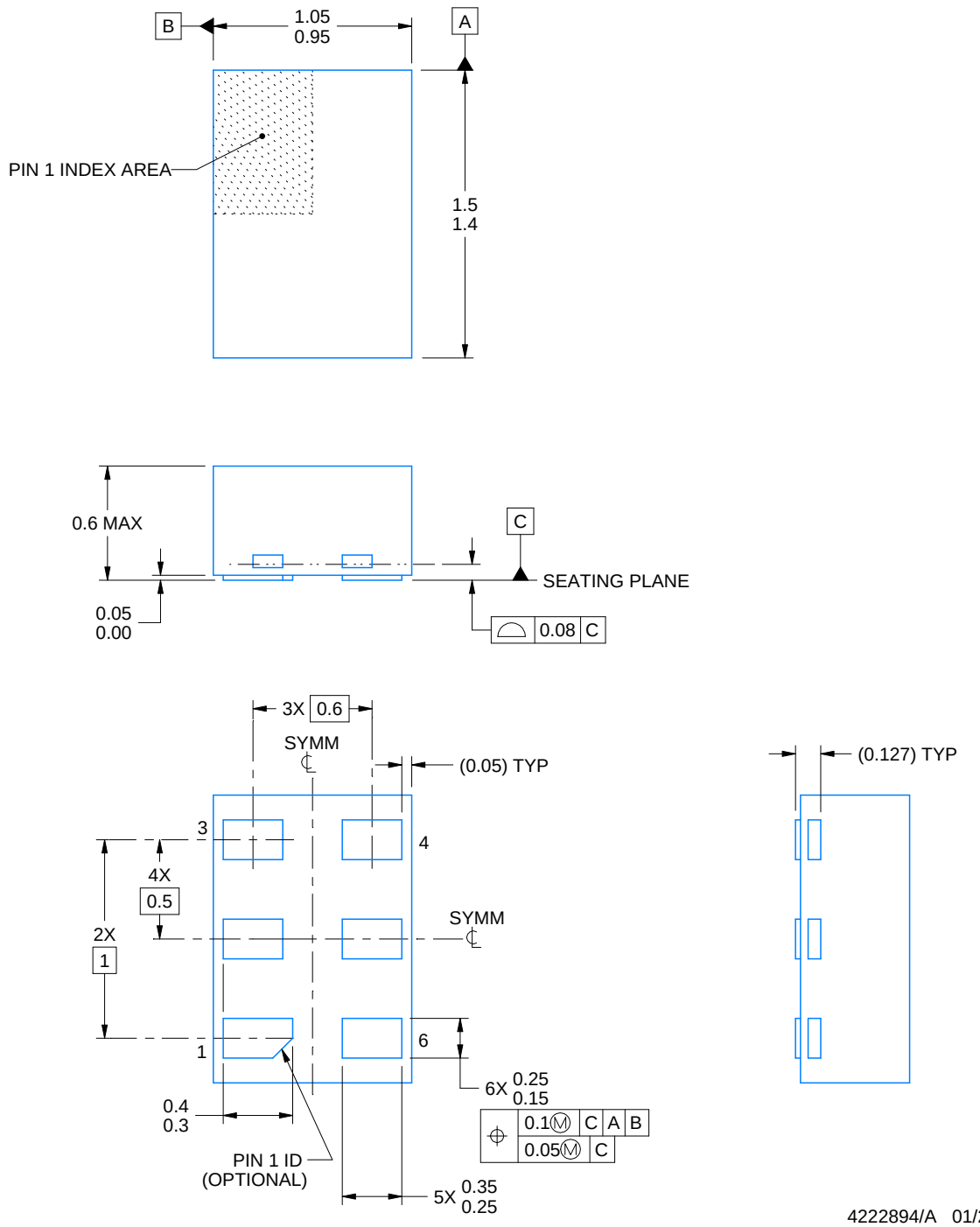


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62230DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS62230DRYT	SON	DRY	6	250	183.0	183.0	20.0
TPS622310DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS622310DRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS622311DRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS622312DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS622312DRYT	SON	DRY	6	250	183.0	183.0	20.0
TPS622313DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS622313DRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS622314DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS622314DRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS622315DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS622315DRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS622316DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS622316DRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS622317DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS622317DRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS622318DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS622318DRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS622318DRYT	SON	DRY	6	250	202.0	201.0	28.0

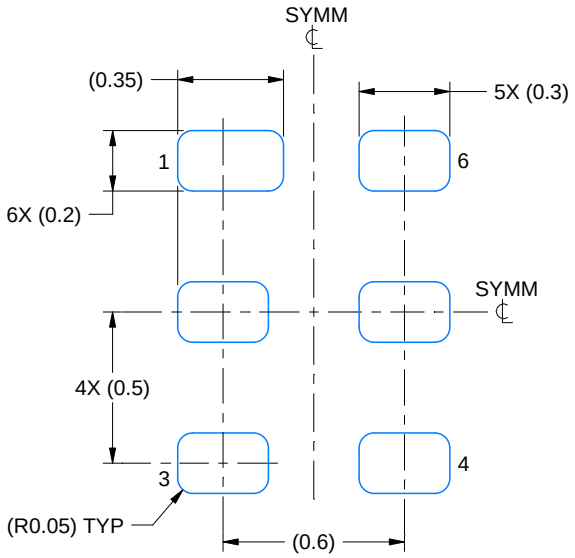
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS622319DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS622319DRYT	SON	DRY	6	250	183.0	183.0	20.0
TPS62231DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS62231DRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS62231DRYT	SON	DRY	6	250	183.0	183.0	20.0
TPS62233DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS62233DRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS62234DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS62234DRYT	SON	DRY	6	250	183.0	183.0	20.0
TPS62235DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS62235DRYT	SON	DRY	6	250	183.0	183.0	20.0
TPS62236DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS62236DRYT	SON	DRY	6	250	183.0	183.0	20.0
TPS62237DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS62237DRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS62237DRYT	SON	DRY	6	250	183.0	183.0	20.0
TPS62238DRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS62238DRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS62239DRYR	SON	DRY	6	5000	183.0	183.0	20.0
TPS62239DRYT	SON	DRY	6	250	183.0	183.0	20.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

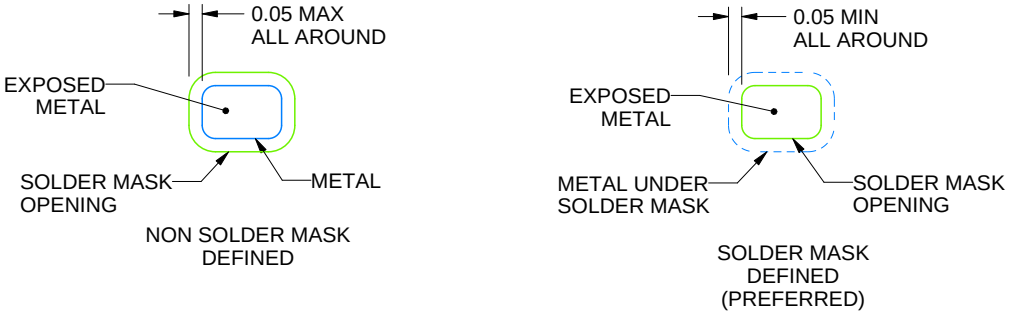


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

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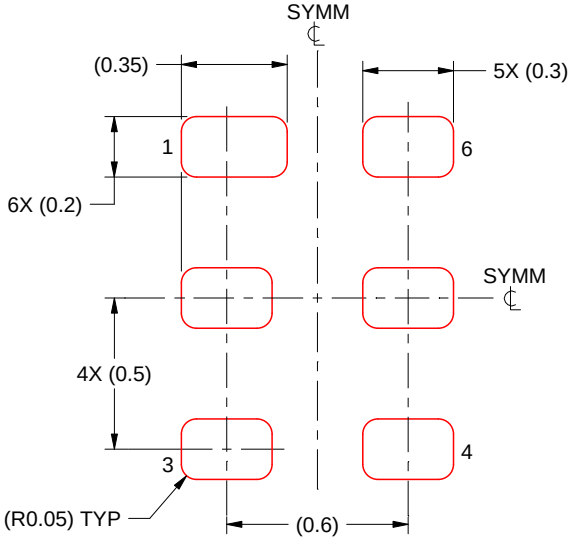
NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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