# TPS7B82-Q1 汽车类 300mA、高压、超低 $I_Q$ 低压降稳压器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C ≤ $T_A$ ≤ 125°C
  - 温度等级 0：–40°C ≤ $T_A$ ≤ 150°C
- 工作结温范围：
  - 1 级：–40°C ≤ $T_J$ ≤ 150°C
  - 0 级：–40°C ≤ $T_J$ ≤ 165°C
- 低静态电流 $I_Q$：
  - 关断模式下 $I_Q$ 为 300nA
  - 轻负载时典型值为 2.7µA
  - 轻负载时最大值为 5µA
- 3V 至 40V 宽 $V_{IN}$ 输入电压范围，瞬态电压高达 45V
- 最大输出电流：300mA
- 输出电压精度为 2%
- 最大压降电压：对于固定 5V 输出版本，200mA 负载电流下为 700mV
- 与低 ESR（0.001Ω 至 5Ω）陶瓷输出稳定电容器（1µF 至 200µF）搭配使用时可保持稳定
- 2.5V、3.3V 和 5V 固定输出电压
- 封装：
  - 8 引脚 HVSSOP，$R_{\theta JA}$ = 63.9°C/W
  - 6 引脚 WSON，$R_{\theta JA}$ = 72.8°C/W
  - 5 引脚 TO-252，$R_{\theta JA}$ = 31.1°C/W
  - 14 引脚 HTSSOP，$R_{\theta JA}$ = 52.0°C/W

## 2 应用

- 汽车音响主机
- 远程信息处理控制单元
- 大灯
- 车身控制模块
- 逆变器和电机控制

## 3 说明

在汽车电池连接应用中，低静态电流 ($I_Q$) 对于省电和延长电池寿命而言至关重要。对于始终开启的系统，必须要实现超低 $I_Q$。

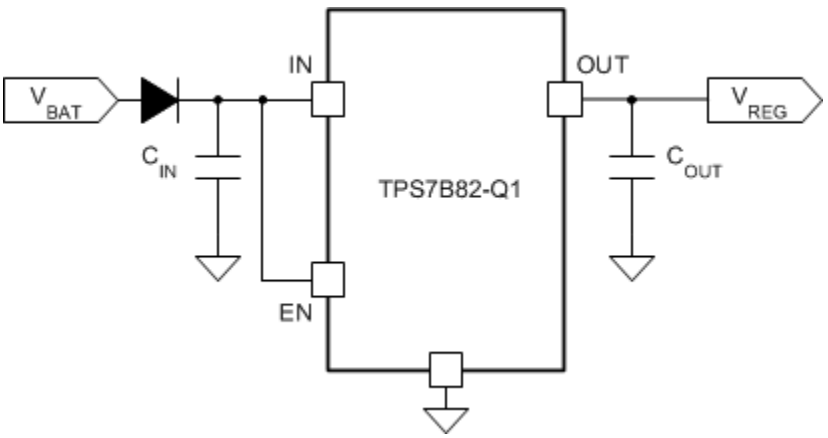
TPS7B82-Q1 是一款旨在在 3V 至 40V（45V 负载突降保护）宽输入电压范围内运行的低压降线性稳压器。TPS7B82-Q1 的工作电压低至 3V，因此可在冷启动以及启动和停止情况下继续工作。该器件在轻负载时的典型静态电流仅为 2.7µA，是用于为待机系统中的微控制器 (MCU) 和 CAN/LIN 收发器供电的理想解决方案。

这些器件具有集成的短路和过流保护功能。该器件可在 -40°C 至 +125°C 的环境温度下运行，结温范围为 -40°C 至 +150°C。此外，该器件采用了热传导封装，即使整个器件散热较多，也能实现持久运行。由于这些特性，该器件旨在用作各种汽车应用的电源。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS7B82-Q1 | HVSSOP (8) | 3.00mm × 3.00mm |
| | WSON (6) | 2.00mm × 2.00mm |
| | TO-252 (5) | 6.10mm × 6.60mm |
| | HTSSOP (14) | 5.00mm x 4.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




典型应用原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision H (March 2021) to Revision I (August 2021)** **Page**

- Changed $I_Q$ parameter maximum specifications from *3.5 μA* to *5 μA* and from *4.5 μA* to *6.5 μA* in the *Electrical Characteristics: Grade 0 Options* table ..... 6
- Changed $V_{(Load-Reg)}$ parameter maximum specification from *10 mV* to *20 mV* in the *Electrical Characteristics: Grade 0 Options* table ..... 6
- Changed $V_{OUT}$ parameter test condition from *40 V* to *14 V* in the *Electrical Characteristics: Grade 0 Options* table ..... 6

**Changes from Revision G (July 2020) to Revision H (March 2021)** **Page**

- 在文档中增加了 PWP (HTSSOP) 封装 ..... 1
- 在*特性* 部分中添加了 0 级信息 ..... 1
- 删除了*特性* 部分中的*热阻* 要点 ..... 1
- 将 TO-252 *封装* 子要点中的 $R_{\theta JA}$ 额定值从 38.8°C/W 更改为 31.1°C/W ..... 1
- Added grade 0 information to *junction temperature* parameter in *Absolute Maximum Ratings* ..... 4
- Added grade 0 information to *Recommended Operating Conditions* table ..... 4
- Added *grade 1 options* to condition statement of *Electrical Characteristics* table ..... 5
- Added *Electrical Characteristics: Grade 0 Options* table ..... 6


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## 5 Pin Configuration and Functions

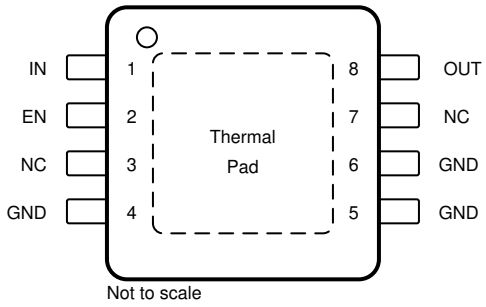



图 5-1. DGN Package, 8-Pin HVSSOP PowerPAD™, Top View

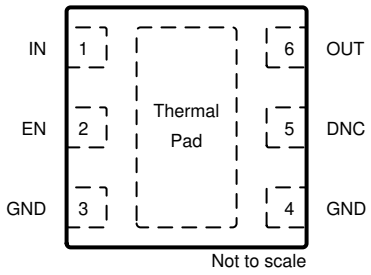



图 5-2. DRV Package, 6-Pin WSON PowerPAD™, Top View

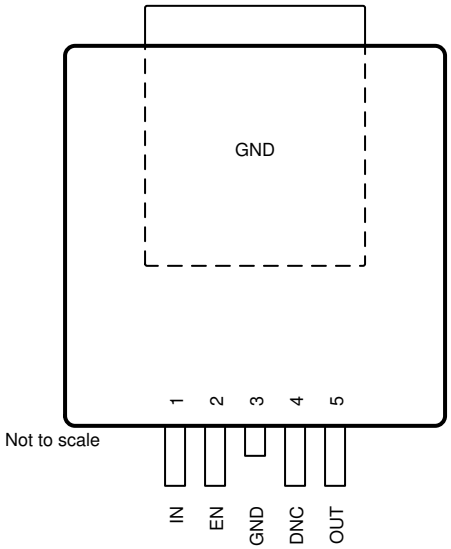



图 5-3. KVU Package, 5-Pin TO-252, Top View

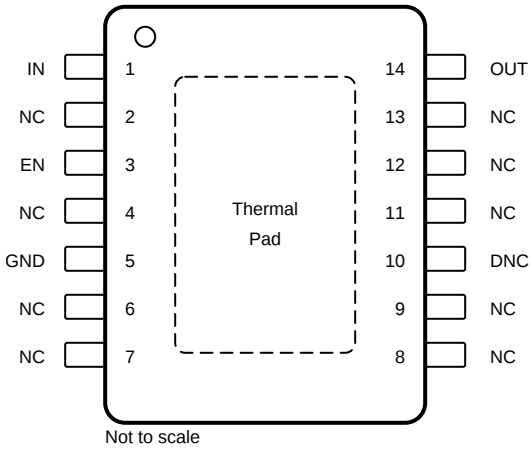



图 5-4. PWP Package, 14-Pin HTSSOP, Top View

NC – No internal connection

表 5-1. Pin Functions

| PIN | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | NO. | | | | | |
| | DGN | DRV | KVU | PWP | | |
| DNC | — | 5 | 4 | 10 | — | Do not connect to a biased voltage. Tie this pin to ground or leave floating. |
| EN | 2 | 2 | 2 | 3 | I | Enable input pin |
| GND | 4, 5, 6 | 3,4 | 3, TAB | 5 | — | Ground reference |
| IN | 1 | 1 | 1 | 1 | I | Input power-supply pin |
| NC | 3, 7 | — | — | 2, 4, 6, 7, 8, 9, 11, 12, 13 | — | Not internally connected |
| OUT | 8 | 6 | 5 | 14 | O | Regulated output voltage pin |
| Thermal pad | | | | | — | Connect the thermal pad to a large-area GND plane for improved thermal performance. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Unregulated input(3) | –0.3 | 45 | V |
| $V_{EN}$ | Enable input(3) | –0.3 | $V_{IN}$ | V |
| $V_{OUT}$ | Regulated output | –0.3 | 7 | V |
| $T_J$ | Junction temperature (grade 1) | –40 | 150 | °C |
| | Junction temperature (grade 0) | –40 | 165 | |
| $T_{stg}$ | Storage temperature range | –40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage, withstand 45 V for 200 ms.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1)<br>HBM ESD classification level H2 | | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011<br>CDM ESD classification level C3B | Corner pins (1, 4, 5, and 8) | ±750 | |
| | | | Other pins | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Unregulated input voltage | 3 | 40 | V |
| $V_{EN}$ | Enable input voltage | 0 | $V_{IN}$ | V |
| $C_{OUT}$ | Output capacitor requirements(1) | 1 | 200 | µF |
| ESR | Output capacitor ESR requirements(2) | 0.001 | 5 | Ω |
| $T_A$ | Ambient temperature (grade 1) | –40 | 125 | °C |
| | Ambient temperature (grade 0) | –40 | 150 | |
| $T_J$ | Junction temperature (grade 1) | –40 | 150 | °C |
| | Junction temperature (grade 0) | –40 | 165 | |

(1) The output capacitance range specified in the table is the effective value.
(2) Relevant equivalent series resistance (ESR) value at f = 10 kHz.


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## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS7B82-Q1 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DGN (HVSSOP) | DRV (WSON) | KVU (TO-252) | PWP (HTSSOP) | |
| | | 8 PINS | 6 PINS | 5 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 63.9 | 72.8 | 31.1 | 52.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 50.2 | 85.8 | 39.9 | 48.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 22.6 | 37.4 | 9.9 | 28.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.8 | 2.7 | 4.2 | 2.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 22.3 | 37.3 | 9.9 | 28.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 12.1 | 13.8 | 2.8 | 10.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics: Grade 1 Options

$V_{IN}$ = 14-V, 10-µF ceramic output capacitor, grade 1 options, $T_J$ = –40°C to +150°C, over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND CURRENT (IN)** | | | | | | | |
| $V_{IN}$ | Input voltage | | | $V_{OUT(NOM)}$ + $V_{(Dropout)}$ | | 40 | V |
| $I_{(SD)}$ | Shutdown current | EN = 0 V | | | 0.3 | 1 | µA |
| $I_{(Q)}$ | Quiescent current | $V_{IN}$ = 6 V to 40 V, EN ⩾ 2 V, $I_{OUT}$ = 0 mA | DRV and KVU packages | | 1.9 | 3.5 | µA |
| | | | DGN package | | 1.9 | 5 | |
| | | $V_{IN}$ = 6 V to 40 V, EN ⩾ 2 V, $I_{OUT}$ = 0.2 mA | DRV and KVU packages | | 2.7 | 4.5 | |
| | | | DGN package | | 2.7 | 6.5 | |
| $V_{(IN, UVLO)}$ | $V_{IN}$ undervoltage detection | Ramp $V_{IN}$ down until the output turns OFF | | | | 2.7 | V |
| | | Hysteresis | | | 200 | | mV |
| **ENABLE INPUT (EN)** | | | | | | | |
| $V_{IL}$ | Logic-input low level | | | | | 0.7 | V |
| $V_{IH}$ | Logic-input high level | | | 2 | | | V |
| **REGULATED OUTPUT (OUT)** | | | | | | | |
| $V_{OUT}$ | Regulated output | $V_{IN}$ = $V_{OUT}$ + $V_{(Dropout)}$ to 40 V, $I_{OUT}$ = 1 mA to 300 mA | DRV and KVU packages | –1.5% | | 1.5% | |
| | | | DGN package | –2% | | 2% | |
| $V_{(Line-Reg)}$ | Line regulation | $V_{IN}$ = 6 V to 40 V, $I_{OUT}$ = 10 mA | | | | 10 | mV |
| $V_{(Load-Reg)}$ | Load regulation | $V_{IN}$ = 14 V, $I_{OUT}$ = 1 mA to 300 mA | DRV and KVU packages | | | 10 | mV |
| | | | DGN package | | | 20 | |

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## 6.5 Electrical Characteristics: Grade 1 Options (continued)

$V_{IN}$ = 14-V, 10-µF ceramic output capacitor, grade 1 options, $T_J$ = –40°C to +150°C, over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{(Dropout)}$ | Dropout voltage(1) | $V_{OUT(NOM)}$ = 5 V | $I_{OUT}$ = 300 mA | DRV and KVU packages | | 630 | 1170 | mV |
| | | | | DGN package | | | 1000 | |
| | | | $I_{OUT}$ = 200 mA | DRV and KVU packages | | 420 | 780 | |
| | | | | DGN package | | 400 | 700 | |
| | | | $I_{OUT}$ = 100 mA | DRV and KVU packages | | 210 | 390 | |
| | | | | DGN package | | 200 | 350 | |
| | | $V_{OUT}$ = 3.3 V | $I_{OUT}$ = 300 mA | DRV and KVU packages | | 730 | 1350 | |
| | | | | DGN package | | | 1250 | |
| | | | $I_{OUT}$ = 200 mA | DRV and KVU packages | | 475 | 900 | |
| | | | | DGN package | | | 850 | |
| | | | $I_{OUT}$ = 100 mA | | | | 450 | |
| $I_{OUT}$ | Output current | $V_{OUT}$ in regulation | | | 0 | | 300 | mA |
| $I_{(CL)}$ | Output current limit | $V_{OUT}$ short to 90% × $V_{OUT}$ | | | 310 | 510 | 690 | mA |
| PSRR | Power-supply ripple rejection | $V_{(Ripple)}$ = 0.5 $V_{PP}$, $I_{OUT}$ = 10 mA, frequency = 100 Hz, $C_{OUT}$ = 2.2 µF | | | | 60 | | dB |
| **OPERATING TEMPERATURE RANGE** | | | | | | | | |
| $T_{(SD)}$ | Junction shutdown temperature | | | | | 175 | | °C |
| $T_{(HYST)}$ | Hysteresis of thermal shutdown | | | | | 20 | | °C |

(1) Dropout is not valid for the 2.5-V output because of the minimum input voltage limits.

## 6.6 Electrical Characteristics: Grade 0 Options

$V_{IN}$ = 14-V, 10-µF ceramic output capacitor, grade 0 options (PWP package), $T_J$ = –40°C to +165°C, over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND CURRENT (IN)** | | | | | | |
| $V_{IN}$ | Input voltage | | $V_{OUT(NOM)}$ + $V_{(Dropout)}$ | | 40 | V |
| $I_{(SD)}$ | Shutdown current | EN = 0 V | | 0.3 | 1 | µA |
| $I_{(Q)}$ | Quiescent current | $V_{IN}$ = 6 V to 40 V, EN ⩾ 2 V, $I_{OUT}$ = 0 mA | | 1.9 | 5 | |
| | | $V_{IN}$ = 6 V to 40 V, EN ⩾ 2 V, $I_{OUT}$ = 0.2 mA | | 2.7 | 6.5 | µA |
| $V_{(IN, UVLO)}$ | $V_{IN}$ undervoltage detection | Ramp $V_{IN}$ down until the output turns OFF | | | 2.7 | V |
| | | Hysteresis | | 200 | | mV |
| **ENABLE INPUT (EN)** | | | | | | |
| $V_{IL}$ | Logic-input low level | | | | 0.7 | V |
| $V_{IH}$ | Logic-input high level | | 2 | | | V |
| **REGULATED OUTPUT (OUT)** | | | | | | |
| $V_{OUT}$ | Regulated output | $V_{IN}$ = $V_{OUT}$ + $V_{(Dropout)}$ to 14 V, $I_{OUT}$ = 1 mA to 300 mA | –1.5% | | 1.5% | |


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## 6.6 Electrical Characteristics: Grade 0 Options (continued)

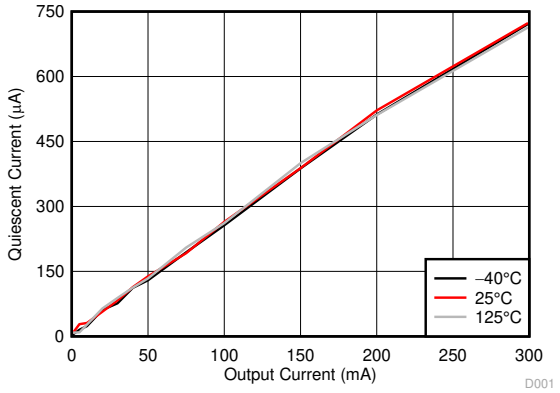
$V_{IN}$ = 14-V, 10-µF ceramic output capacitor, grade 0 options (PWP package), $T_J$ = –40°C to +165°C, over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(Line-Reg)}$ | Line regulation | $V_{IN}$ = 6 V to 40 V, $I_{OUT}$ = 10 mA | | | | 10 | mV |
| $V_{(Load-Reg)}$ | Load regulation | $V_{IN}$ = 14 V, $I_{OUT}$ = 1 mA to 300 mA | | | | 20 | mV |
| $V_{(Dropout)}$ | Dropout voltage(1) | $V_{OUT(NOM)}$ = 5 V | $I_{OUT}$ = 300 mA | | 630 | 1170 | mV |
| | | | $I_{OUT}$ = 200 mA | | 420 | 780 | |
| | | | $I_{OUT}$ = 100 mA | | 210 | 390 | |
| | | $V_{OUT}$ = 3.3 V | $I_{OUT}$ = 300 mA | | 730 | 1350 | |
| | | | $I_{OUT}$ = 200 mA | | 475 | 900 | |
| | | | $I_{OUT}$ = 100 mA | | | 450 | |
| $I_{OUT}$ | Output current | $V_{OUT}$ in regulation | | 0 | | 300 | mA |
| $I_{(CL)}$ | Output current limit | $V_{OUT}$ short to 90% × $V_{OUT}$ | | 310 | 510 | 690 | mA |
| PSRR | Power-supply ripple rejection | $V_{(Ripple)}$ = 0.5 $V_{PP}$, $I_{OUT}$ = 10 mA, frequency = 100 Hz, $C_{OUT}$ = 2.2 µF | | | 60 | | dB |
| **OPERATING TEMPERATURE RANGE** | | | | | | | |
| $T_{(SD)}$ | Junction shutdown temperature | | | | 185 | | °C |
| $T_{(HYST)}$ | Hysteresis of thermal shutdown | | | | 20 | | °C |

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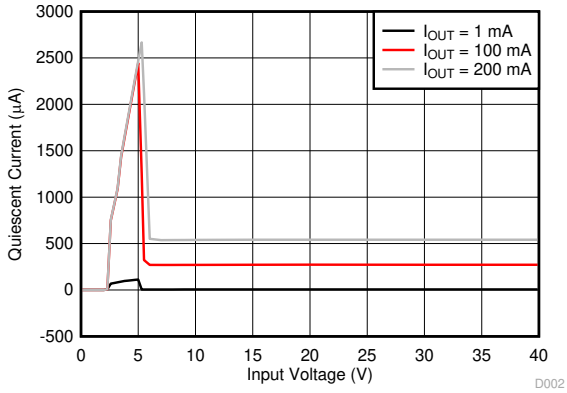
## 6.7 Typical Characteristics

$V_{IN}$ = 14 V, $V_{EN}$ ⩾ 2 V, $T_J$ = –40°C to 150°C (unless otherwise noted)



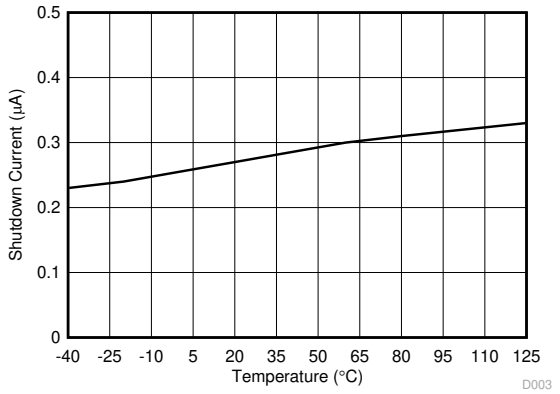

$V_{OUT}$ = 5 V

**图 6-1. Quiescent Current vs Output Current**



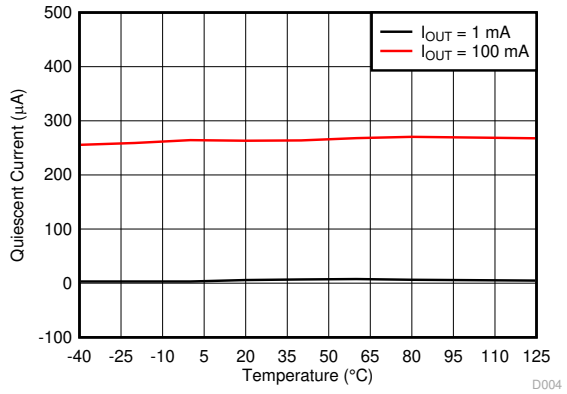

$V_{OUT}$ = 5 V

**图 6-2. Quiescent Current vs Input Voltage**



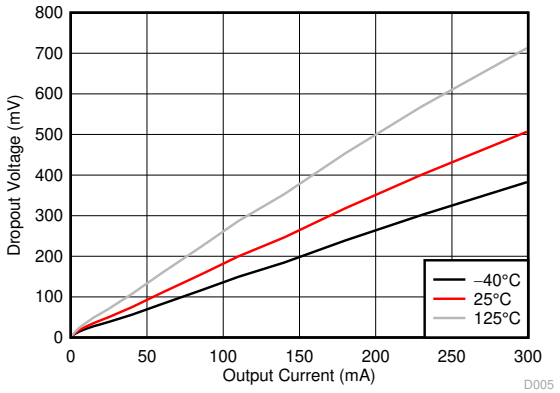

$V_{EN}$ = 0 V

**图 6-3. Shutdown Current vs Ambient Temperature**



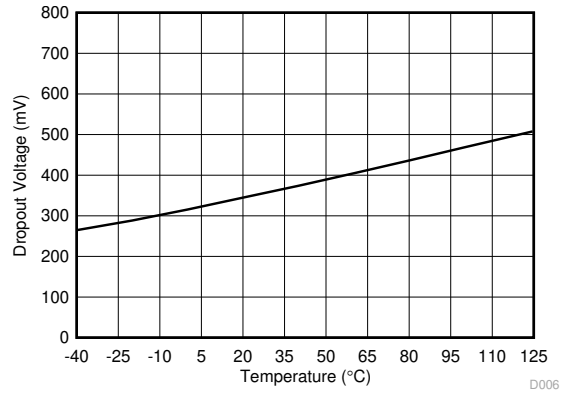

$V_{OUT}$ = 5 V

**图 6-4. Quiescent Current vs Ambient Temperature**




$V_{IN}$ = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} - V_{OUT}$

**图 6-5. Dropout Voltage vs Output Current**



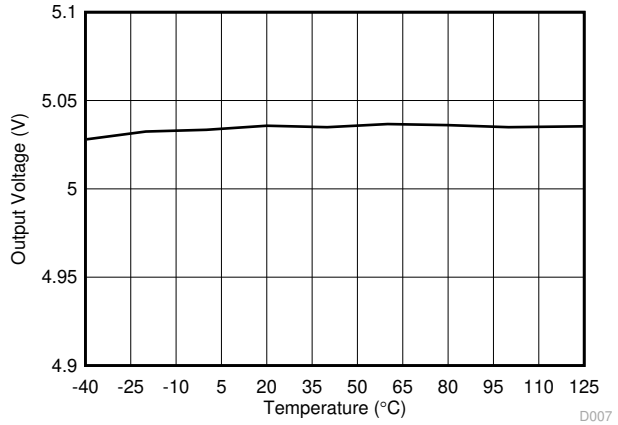

$V_{IN}$ = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} - V_{OUT}$

**图 6-6. Dropout Voltage vs Ambient Temperature**


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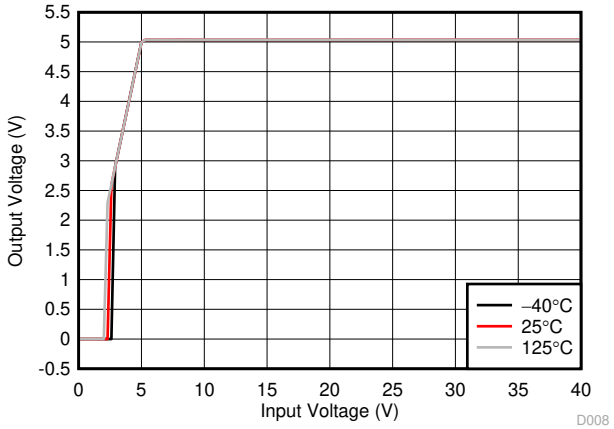
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = 14 V, $V_{EN}$ ⩾ 2 V, $T_J$ = –40°C to 150°C (unless otherwise noted)



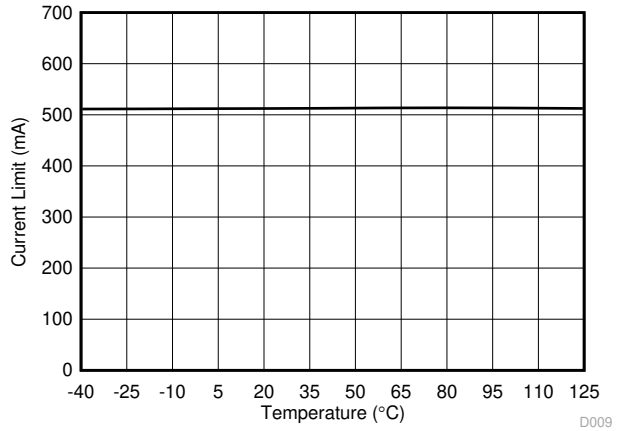

$V_{OUT}$ = 5 V

**图 6-7. Output Voltage vs Ambient Temperature**



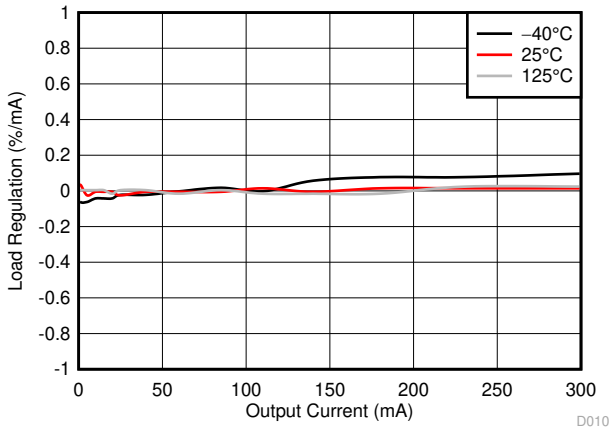

$V_{OUT}$ = 5 V, $I_{OUT}$ = 1 mA

**图 6-8. Output Voltage vs Input Voltage**



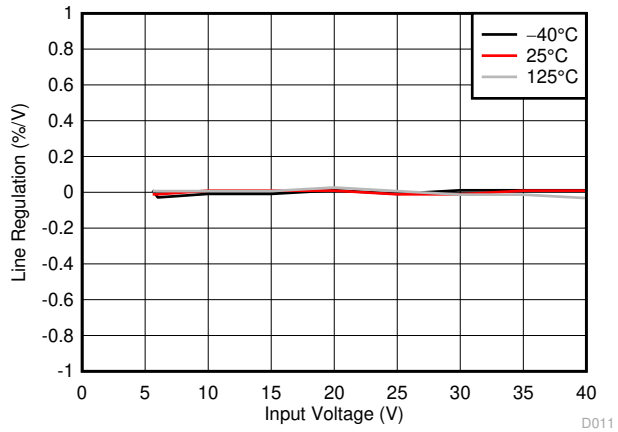

$V_{IN}$ = 14 V, $V_{OUT}$ is shorted to 90% × $V_{OUT}$

**图 6-9. Output Current Limit vs Ambient Temperature**



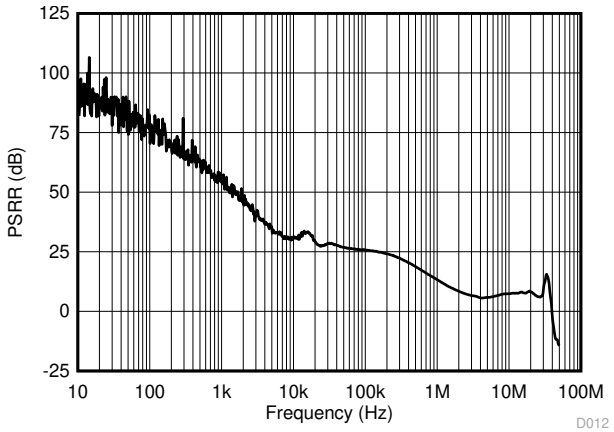

$V_{OUT}$ = 5 V

**图 6-10. Load Regulation**




$V_{OUT}$ = 5 V, $I_{OUT}$ = 10 mA

**图 6-11. Line Regulation**




$I_{OUT}$ = 10 mA

**图 6-12. PSRR vs Frequency**

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## 6.7 Typical Characteristics (continued)

$V_{IN}$ = 14 V, $V_{EN}$ ⩾ 2 V, $T_J$ = –40°C to 150°C (unless otherwise noted)

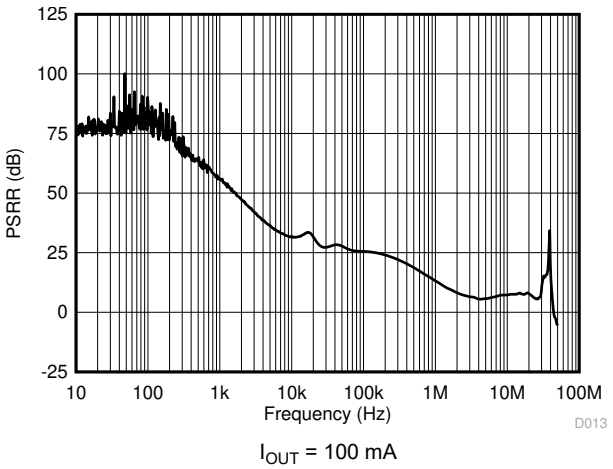



图 6-13. PSRR vs Frequency

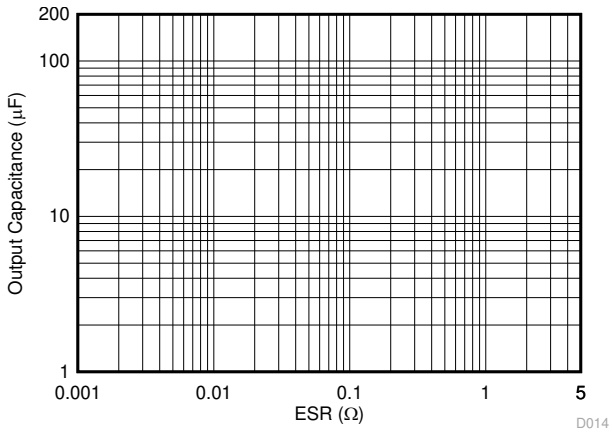



图 6-14. Output Capacitance vs ESR Stability

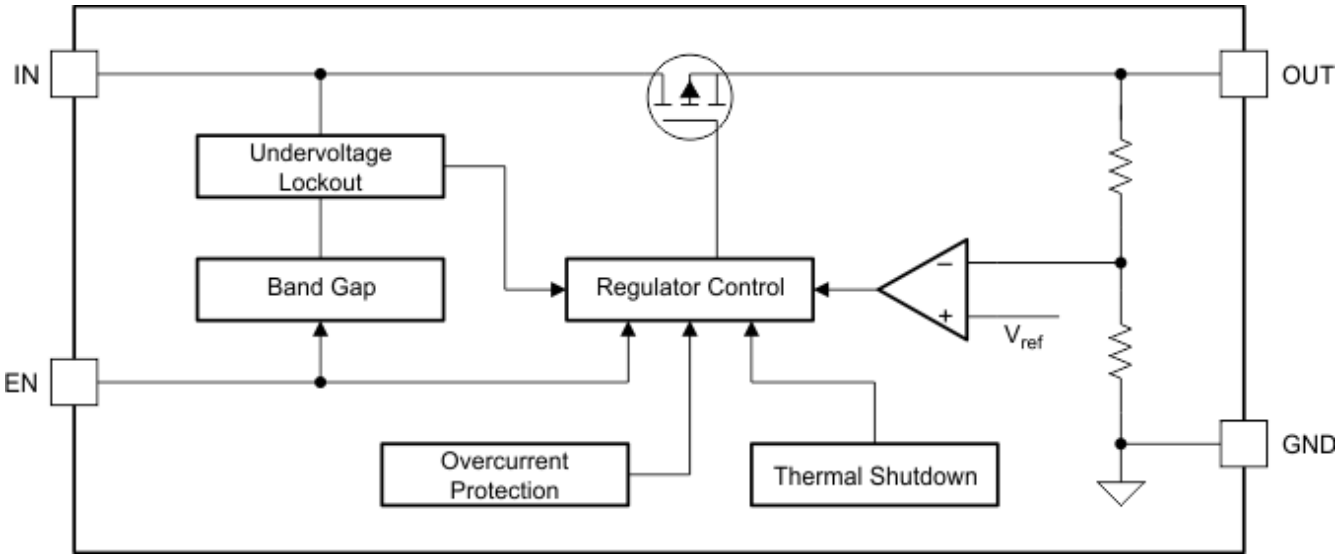

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# 7 Detailed Description

## 7.1 Overview

The TPS7B82-Q1 is a 40-V, 300-mA low-dropout (LDO) linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3 μA of quiescent current at light load, and is designed for the automotive always-on application.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation ON. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

### 7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage ($V_{IN}$) falls below an internal UVLO threshold ($V_{(UVLO)}$). This threshold limit ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

### 7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This limit protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

### 7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the TSD trip point minus thermal shutdown hysteresis, the output turns on again.

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## 7.4 Device Functional Modes

### 7.4.1 Operation With $V_{IN}$ Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. At input voltages below the actual UVLO voltage, the device does not operate.

### 7.4.2 Operation With $V_{IN}$ Larger Than 3 V

When $V_{IN}$ is greater than 3 V, if $V_{IN}$ is also higher than the output set value plus the device dropout voltage, $V_{OUT}$ is equal to the set value. Otherwise, $V_{OUT}$ is equal to $V_{IN}$ minus the dropout voltage.


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# 8 Application and Implementation

**Note**

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## 8.1 Application Information

The TPS7B82-Q1 is a 300-mA, 40-V low-dropout linear regulator with ultra-low quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

## 8.2 Typical Application

图 8-1 shows a typical application circuit for the TPS7B82-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. Use a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

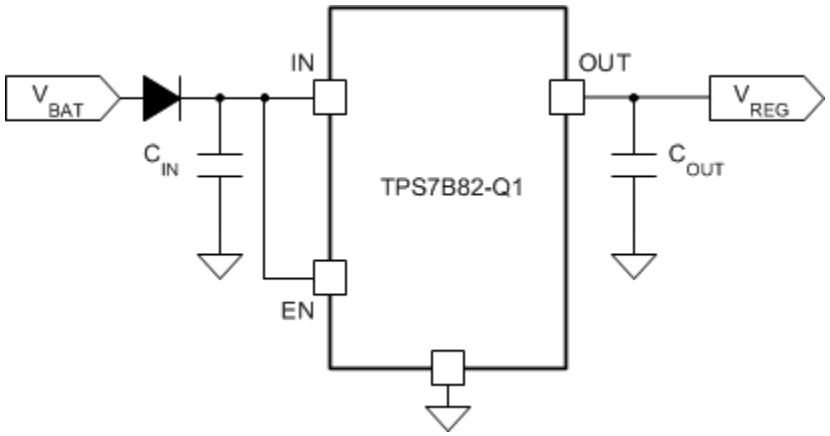



**图 8-1. TPS7B82-Q1 Typical Application Schematic**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

**表 8-1. Design Requirements Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage range | 3 V to 40 V |
| Output voltage | 5 V or 3.3 V |
| Output current | 300 mA maximum |

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

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#### 8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10-µF to 22-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

#### 8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B82-Q1, the device requires an output capacitor with a value in the range from 1 µF to 200 µF and with an ESR range between 0.001 Ω and 5 Ω. Select a ceramic capacitor with low ESR to improve the load transient response.

### 8.2.3 Application Curve

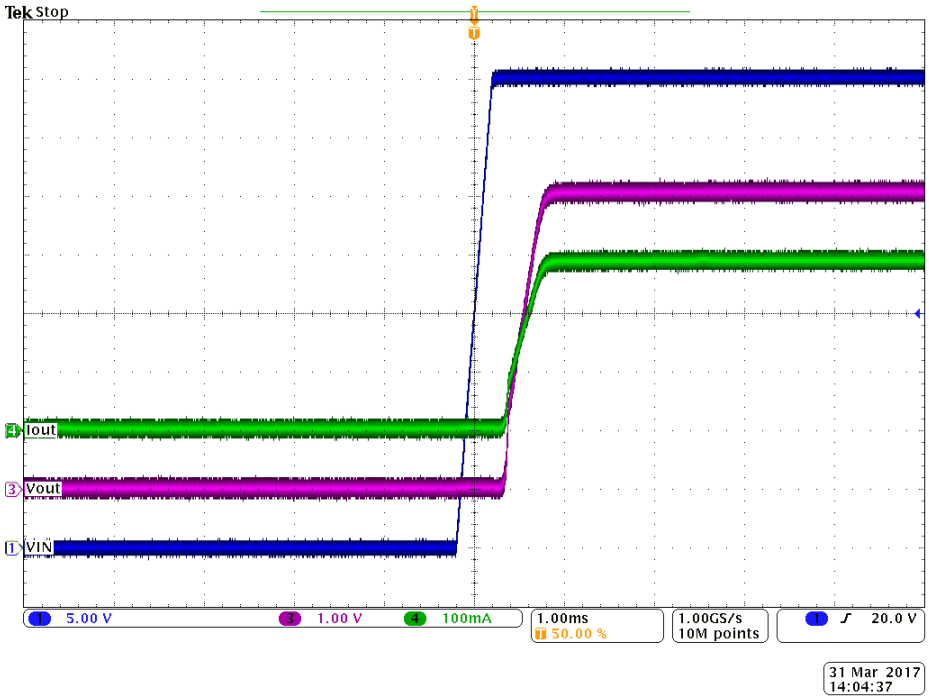



图 8-2. TPS7B82-Q1 Power-Up Waveform (5 V)


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# 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B82-Q1, add a capacitor with a value greater than or equal to 10 μF with a 0.1-μF bypass capacitor in parallel at the input.

# 10 Layout

## 10.1 Layout Guidelines

For LDO power supplies, especially high-voltage and large output current supplies, layout is an important step. If layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitation. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and place enough thermal vias on the copper under the thermal pad. 图 10-1 shows an example layout.

## 10.2 Layout Example

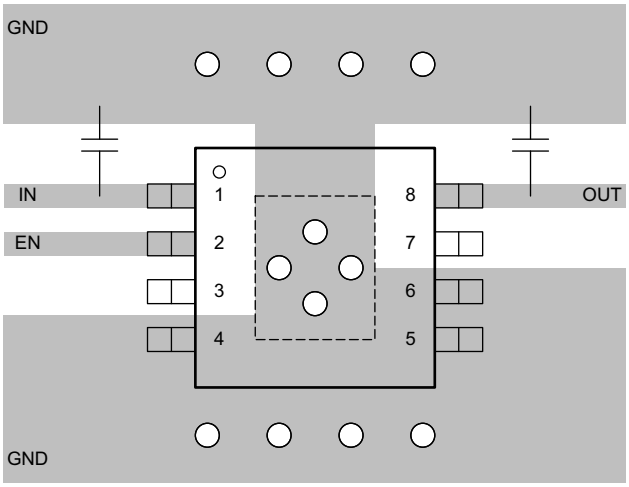



**图 10-1. TPSB82-Q1 Example Layout Diagram**

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# 11 Device and Documentation Support

## 11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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## 11.4 Electrostatic Discharge Caution



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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7B8225QDGNRQ1 | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 1QFX | Samples |
| TPS7B8233EPWPRQ1 | ACTIVE | HTSSOP | PWP | 14 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 150 | 7B8233E | Samples |
| TPS7B8233QDGNRQ1 | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 1GGX | Samples |
| TPS7B8233QDRVRQ1 | ACTIVE | WSON | DRV | 6 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1ORH | Samples |
| TPS7B8233QKVURQ1 | ACTIVE | TO-252 | KVU | 5 | 2500 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 150 | 7B8233Q1 | Samples |
| TPS7B8250EPWPRQ1 | ACTIVE | HTSSOP | PWP | 14 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 150 | 7B8250E | Samples |
| TPS7B8250QDGNRQ1 | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 19TX | Samples |
| TPS7B8250QDRVRQ1 | ACTIVE | WSON | DRV | 6 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1UFH | Samples |
| TPS7B8250QKVURQ1 | ACTIVE | TO-252 | KVU | 5 | 2500 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 150 | 7B8250Q1 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

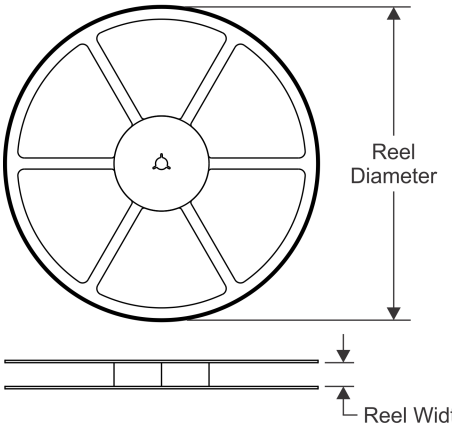
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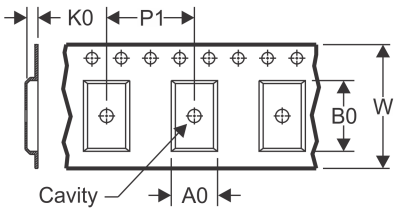
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## TAPE AND REEL INFORMATION

REEL DIMENSIONS

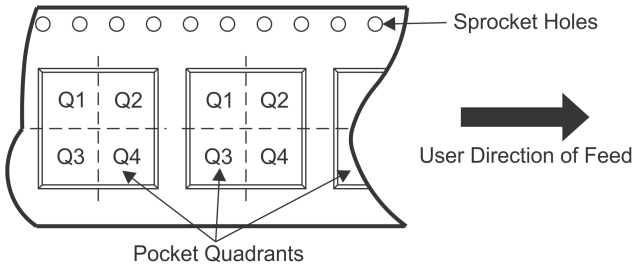



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

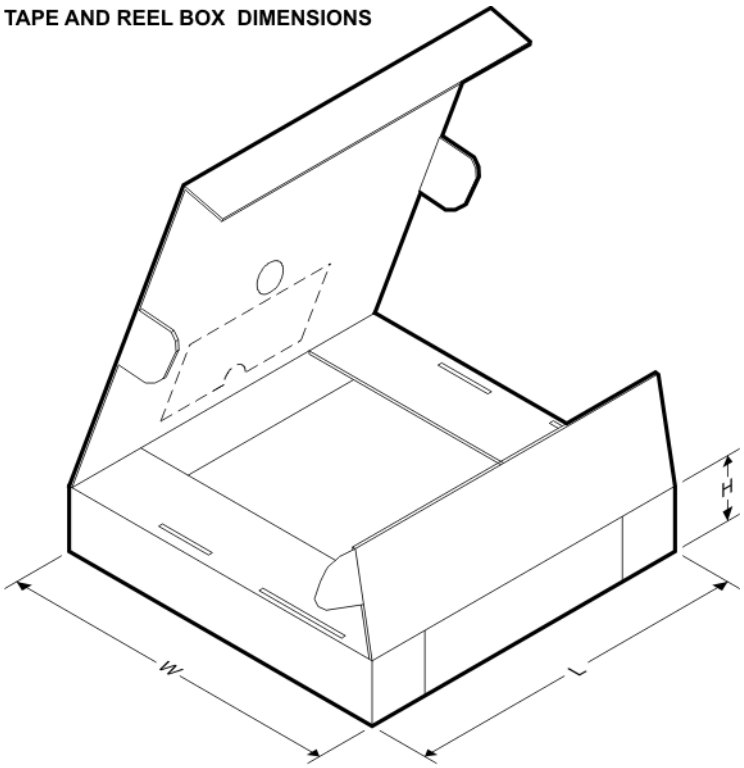
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7B8225QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS7B8233EPWPRQ1 | HTSSOP | PWP | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS7B8233QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS7B8233QDRVRQ1 | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS7B8233QKVURQ1 | TO-252 | KVU | 5 | 2500 | 330.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |
| TPS7B8250EPWPRQ1 | HTSSOP | PWP | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS7B8250QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS7B8250QDRVRQ1 | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS7B8250QKVURQ1 | TO-252 | KVU | 5 | 2500 | 330.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

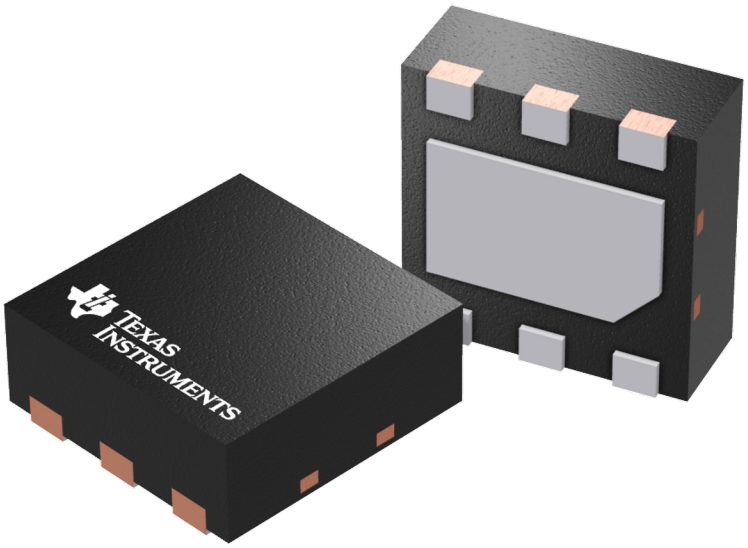



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7B8225QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS7B8233EPWPRQ1 | HTSSOP | PWP | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| TPS7B8233QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS7B8233QDRVRQ1 | WSON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7B8233QKVURQ1 | TO-252 | KVU | 5 | 2500 | 340.0 | 340.0 | 38.0 |
| TPS7B8250EPWPRQ1 | HTSSOP | PWP | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| TPS7B8250QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS7B8250QDRVRQ1 | WSON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7B8250QKVURQ1 | TO-252 | KVU | 5 | 2500 | 340.0 | 340.0 | 38.0 |

# DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



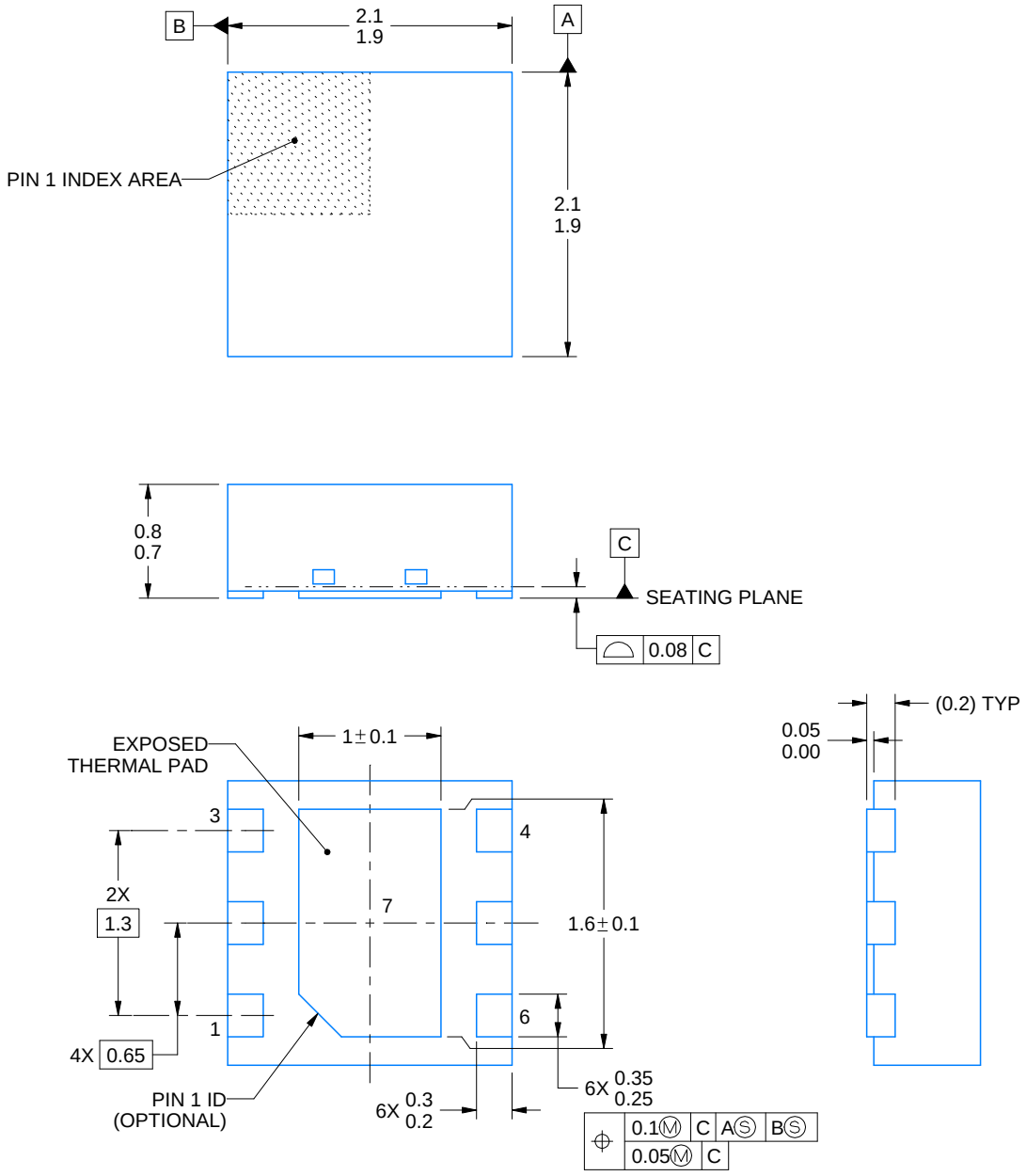

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DRV0006A

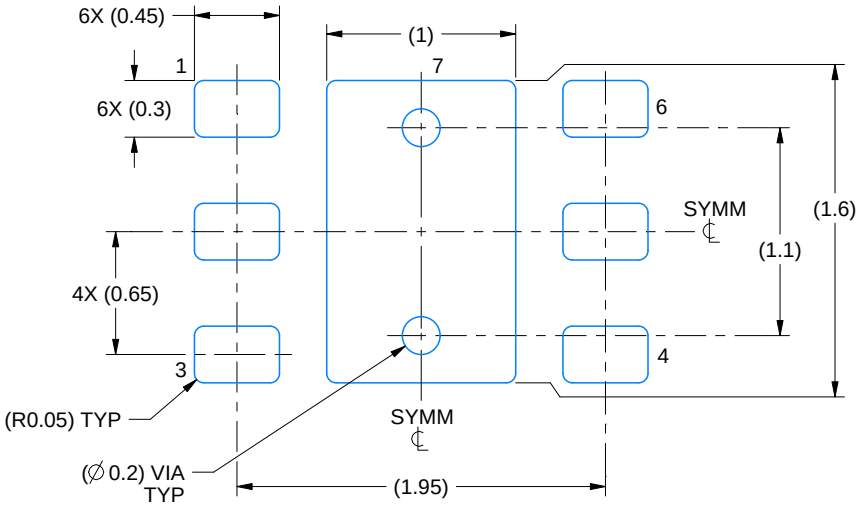
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

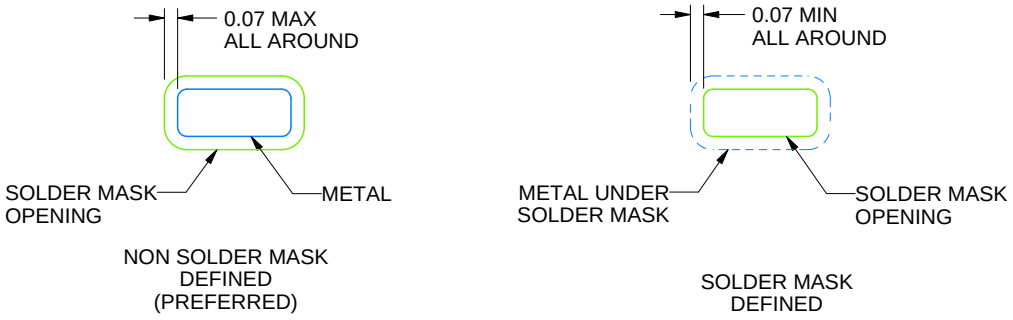



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:25X




SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

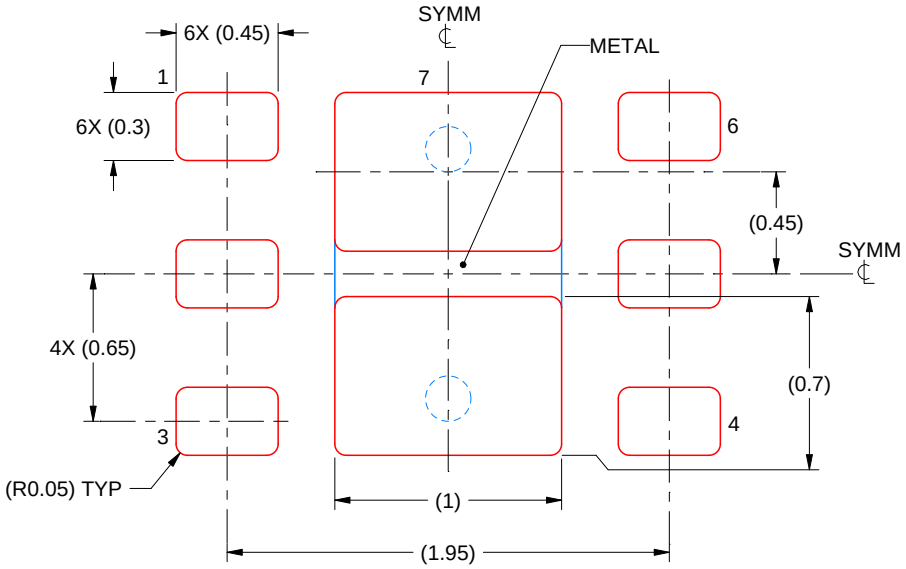
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

## DRV0006A

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

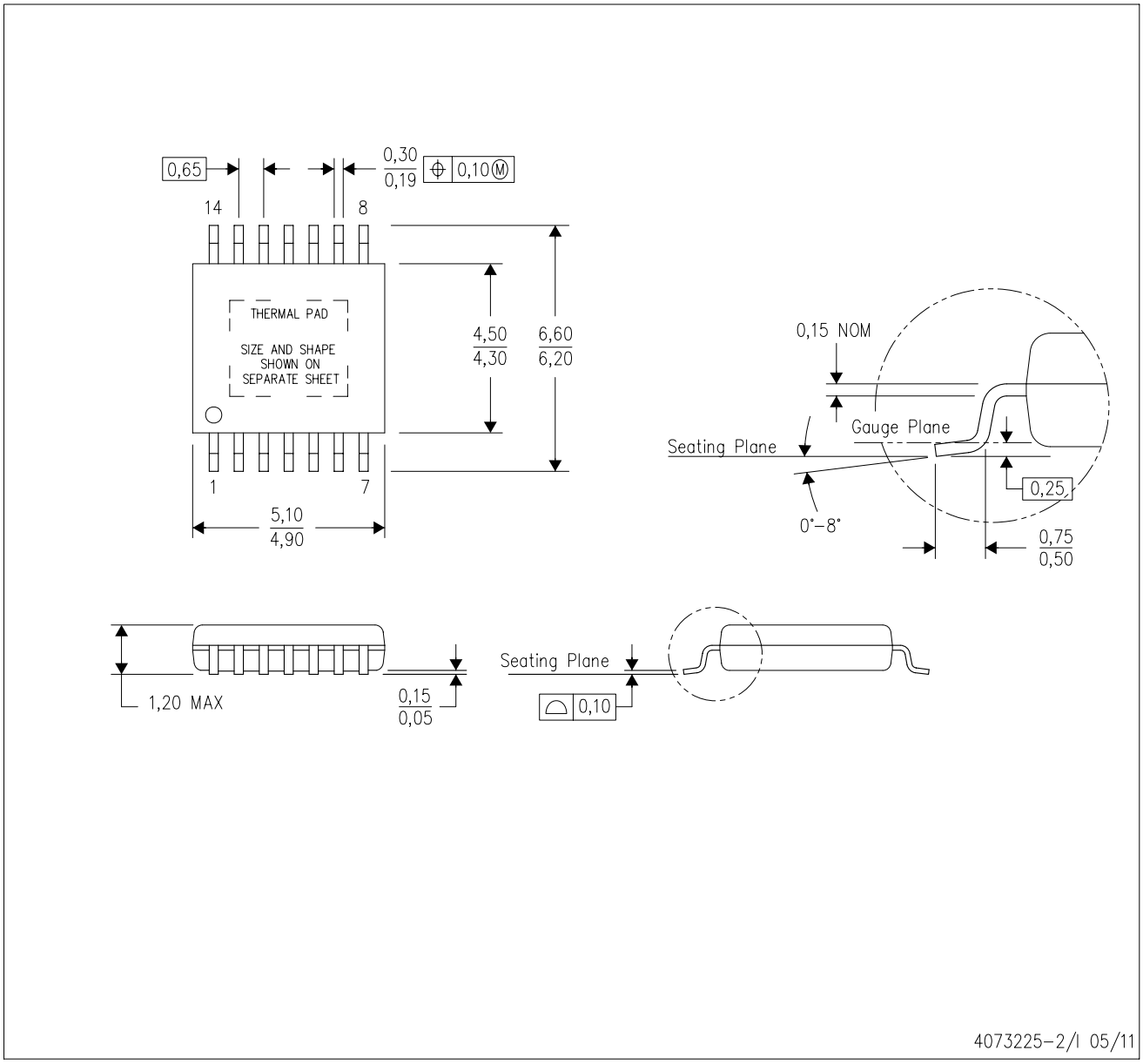
EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

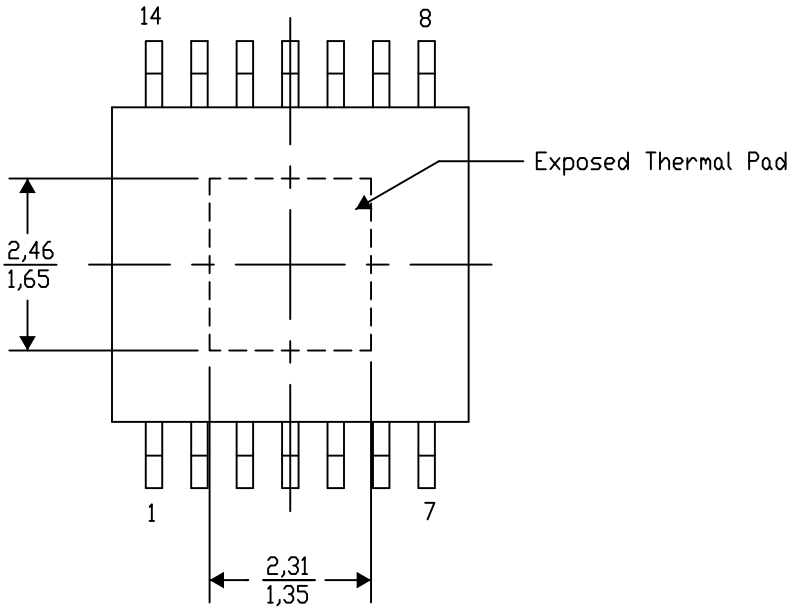
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

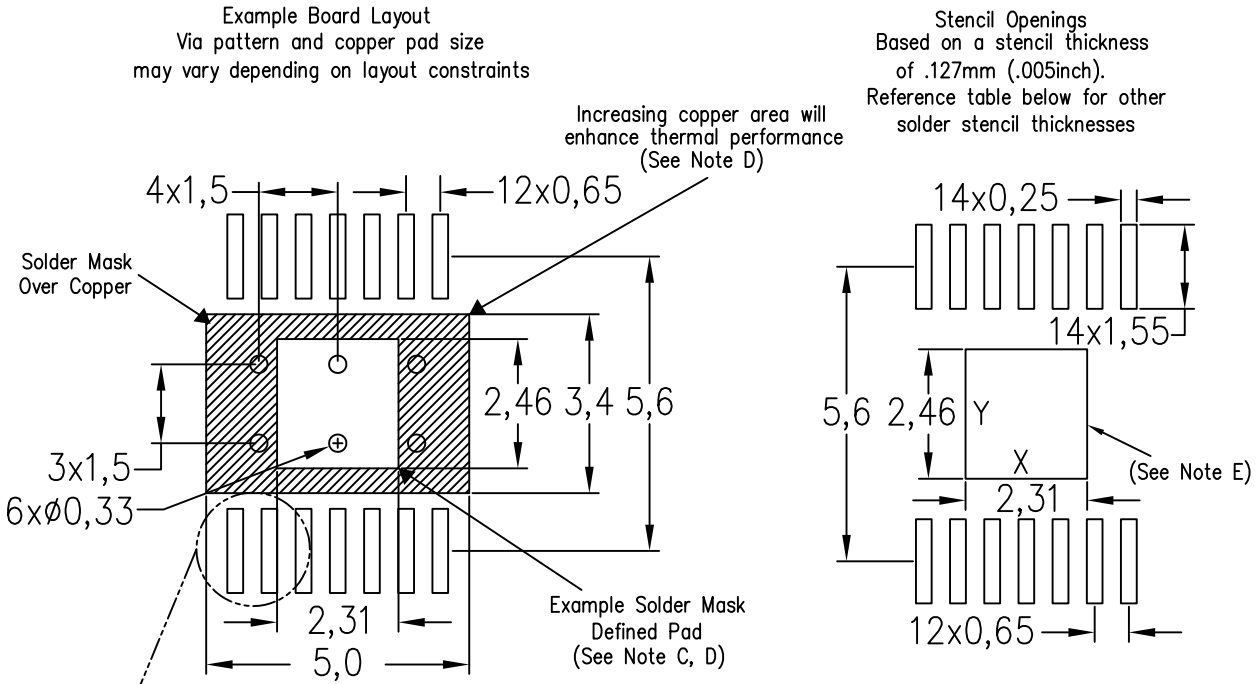
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE

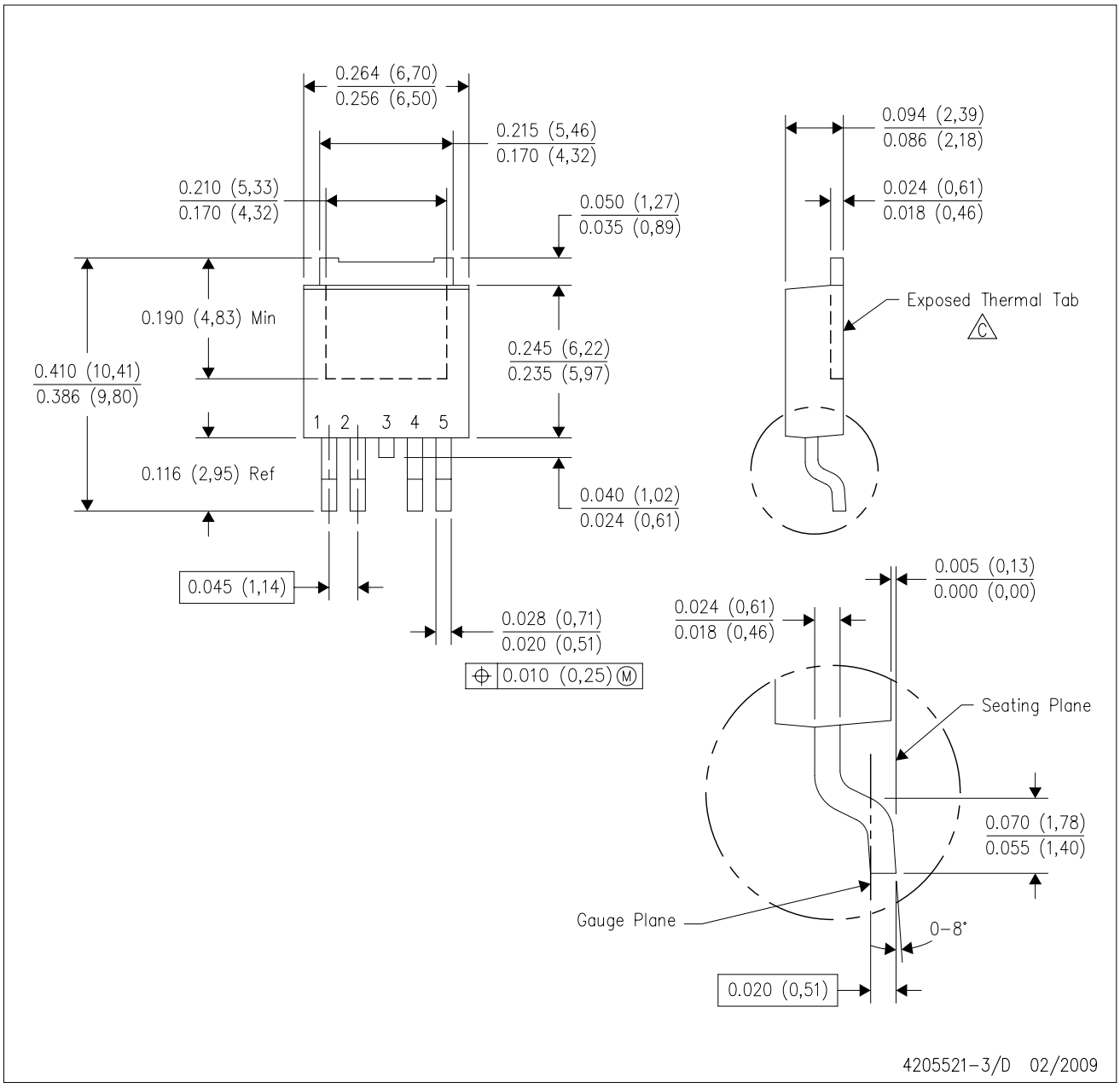



| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

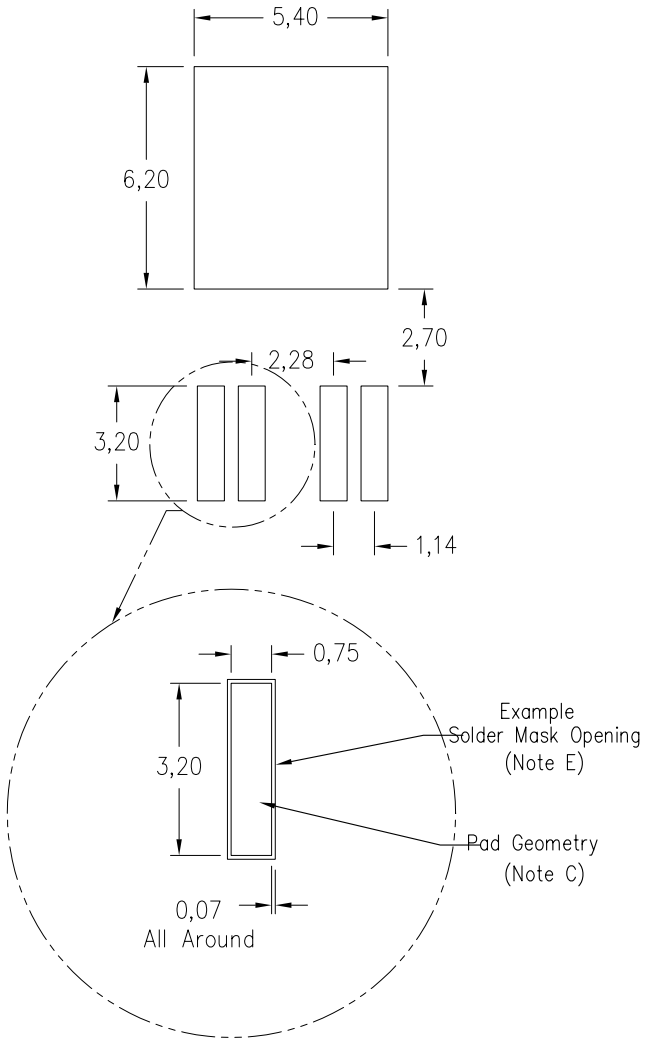
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



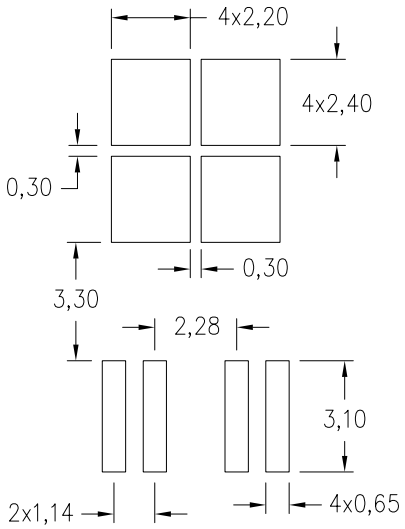

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

# KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout




Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).




63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

# GENERIC PACKAGE VIEW

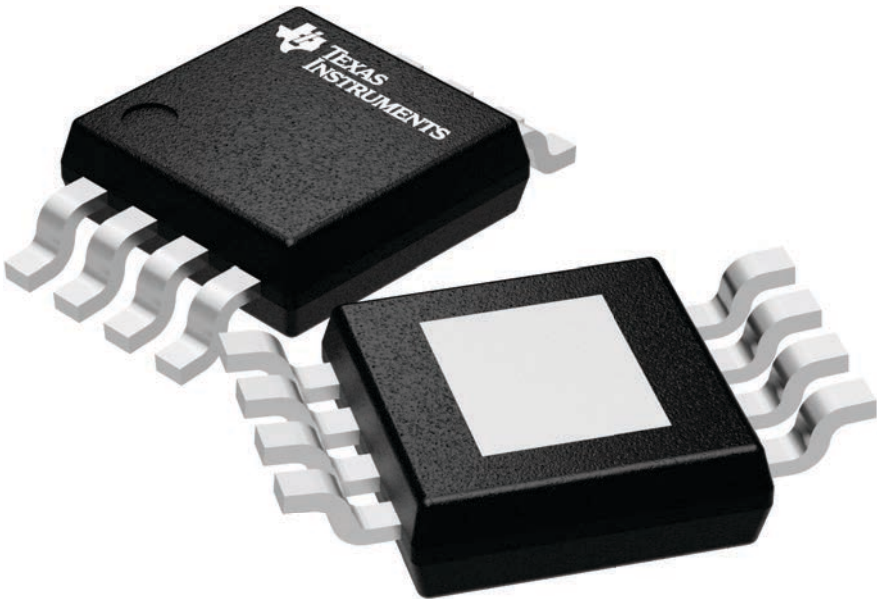
## DGN 8

## PowerPAD VSSOP - 1.1 mm max height

**3 x 3, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

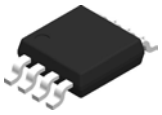
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225482/A

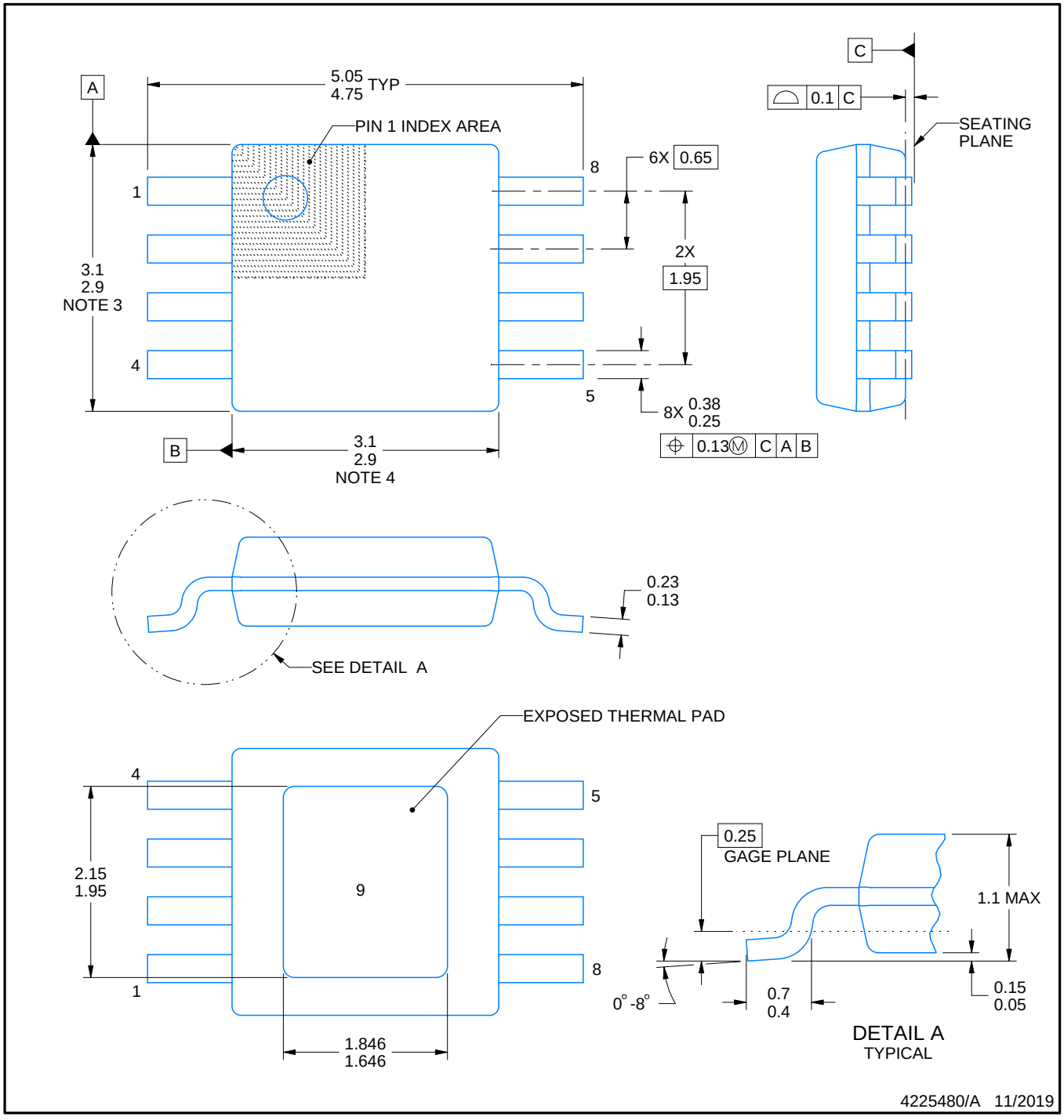
# PACKAGE OUTLINE

## DGN0008G



## PowerPAD™ VSSOP - 1.1 mm max height

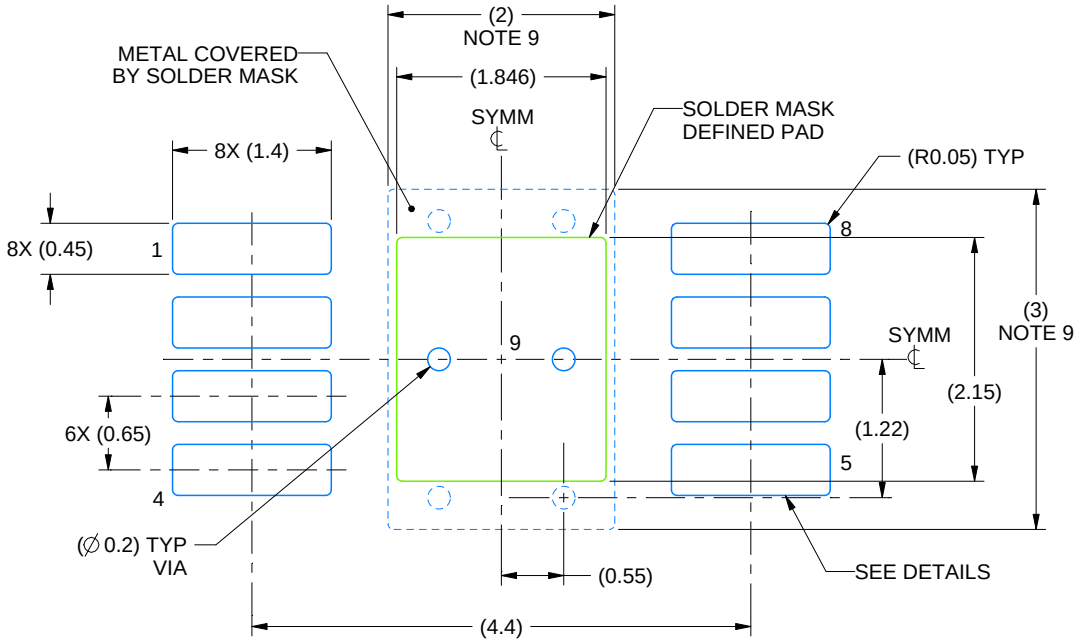
SMALL OUTLINE PACKAGE



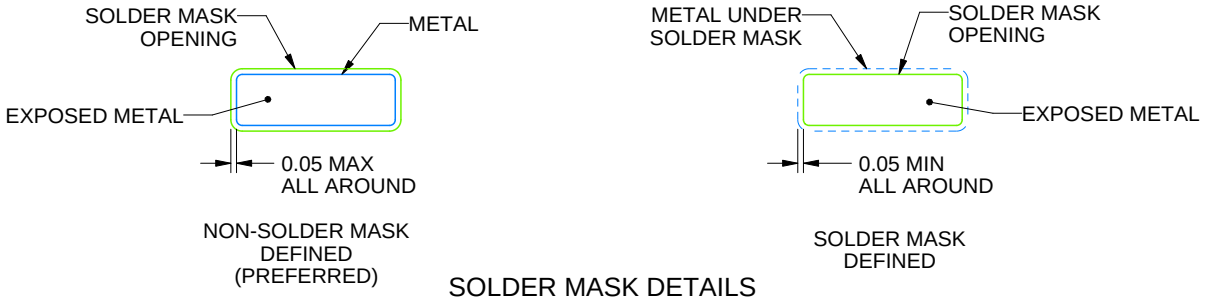

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

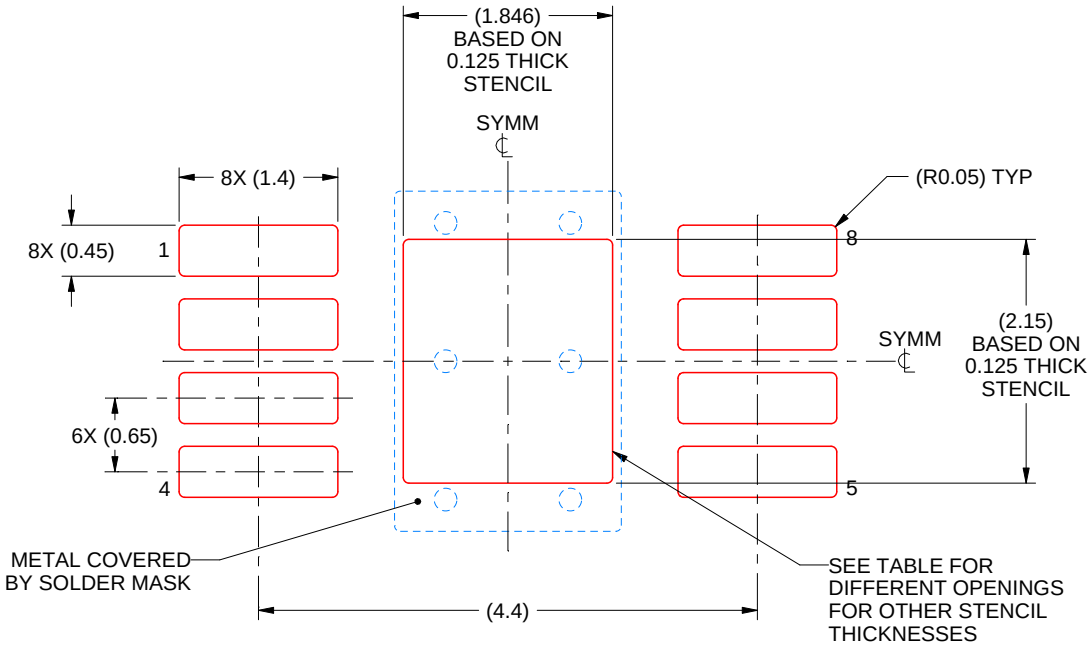



SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 2.06 X 2.40 |
| 0.125 | 1.846 X 2.15 (SHOWN) |
| 0.15 | 1.69 X 1.96 |
| 0.175 | 1.56 X 1.82 |

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

# 重要声明和免责声明

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