

# MC1458, MC1558 DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

SLOS069C – FEBRUARY 1971 – REVISED AUGUST 2010

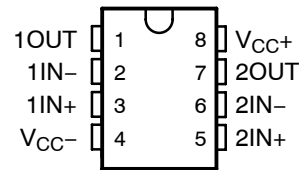
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Designed to Be Interchangeable With Motorola MC1558/MC1458 and Signetics S5558/N5558

## description/ordering information

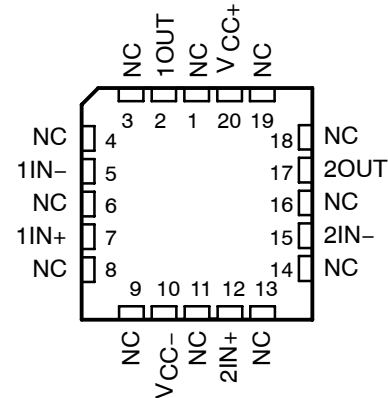
The MC1458 and MC1558 are dual general-purpose operational amplifiers, with each half electrically similar to the  $\mu$ A741, except that offset null capability is not provided.

The high-common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

MC1458 . . . D, P, OR PS PACKAGE  
MC1558 . . . JG PACKAGE  
(TOP VIEW)



MC1558 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	$V_{IOmax}$ AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (P)	Tube	MC1458P	MC1458P
		SOIC (D)	Tube	MC1458D	MC1458
			Tape and reel	MC1458DR	
		SOP (PS)	Tape and reel	MC1458PSR	M1458
-55°C to 125°C	5 mV	CDIP (JG)	Tube	MC1558JG	MC1558JG
		CDIP (JGB)	Tube	MC1558JGB	MC1558JGB
		LCCC (FK)	Tube	MC1558FK	MC1558FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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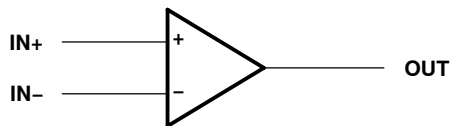
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# MC1458, MC1558 DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

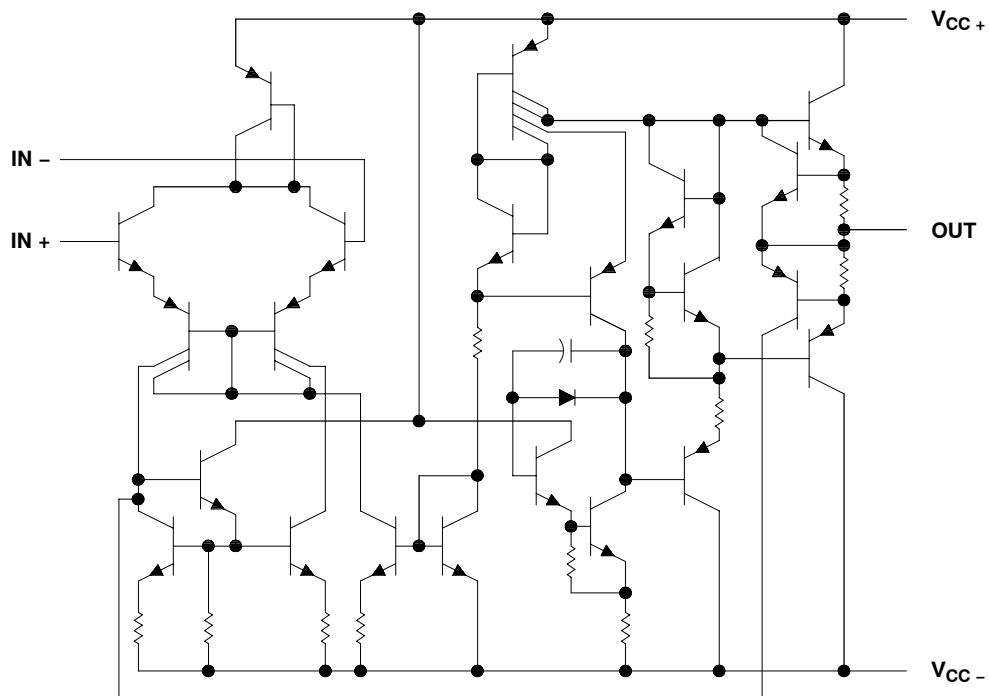
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symbol (each amplifier)



schematic (each amplifier)



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC+}$ (see Note 1):	MC1458 .....	18 V
	MC1558 .....	22 V
Supply voltage, $V_{CC-}$ (see Note 1):	MC1458 .....	-18 V
	MC1558 .....	-22 V
Differential input voltage, $V_{ID}$ (see Note 2)	.....	$\pm 30$ V
Input voltage, $V_I$ (either input, see Notes 1 and 3)	.....	$\pm 15$ V
Duration of output short circuit (see Note 4)	.....	Unlimited
Operating virtual junction temperature, $T_J$	.....	150°C
Package thermal impedance, $\theta_{JA}$ (see Notes 5 and 6):	D package .....	97°C/W
	P package .....	85°C/W
	PS package .....	95°C/W
Package thermal impedance, $\theta_{JC}$ (see Notes 7 and 8):	FK package .....	5.61°C/W
	JG package .....	14.5°C/W
Case temperature for 60 seconds: FK package	.....	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package	.....	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, P, or PS package	.....	260°C
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at  $IN+$  with respect to  $IN-$ .
  3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
  4. The output can be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 70°C free-air temperature.
  5. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  6. The package thermal impedance is calculated in accordance with JESD 51-7.
  7. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JC}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable case temperature is  $P_D = (T_J(\max) - T_C)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  8. The package thermal impedance is calculated in accordance with MIL-STD-883.

## recommended operating conditions

		MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage	±5	±15	V
$T_A$	Operating free-air temperature range	MC1458	0 70	°C
		MC1558	-55 125	



# MC1458, MC1558 DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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## electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$

PARAMETER	TEST CONDITIONS†	MC1458			MC1558			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 0$	25°C	1	6	1	5	mV	
		Full range	7.5			6		
$I_{IO}$ Input offset current	$V_O = 0$	25°C	20	200	20	200	nA	
		Full range	300			500		
$I_{IB}$ Input bias current	$V_O = 0$	25°C	80	500	80	500	nA	
		Full range	800			1500		
$V_{ICR}$ Common-mode input voltage range		25°C	±12	±13	±12	±13	V	
		Full range	±12			±12		
$V_{OM}$ Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega$	25°C	±12	±14	±12	±14	V	
	$R_L \geq 10\text{ k}\Omega$	Full range	±12			±11		
	$R_L = 2\text{ k}\Omega$	25°C	±10	±13	±10	±13		
	$R_L \geq 2\text{ k}\Omega$	Full range	±10			±10		
$A_{VD}$ Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega, V_O = \pm 10\text{ V}$	25°C	20	200	50	200	V/mV	
		Full range	15			25		
$B_{OM}$ Maximum-output-swing bandwidth (closed loop)	$R_L = 2\text{ k}\Omega, A_{VD} = 1, THD \geq 5\%$	25°C	14		14		kHz	
$B_1$ Unity-gain bandwidth		25°C	1		1		MHz	
$\phi_m$ Phase margin	$A_{VD} = 1$	25°C	65		65		deg	
		Gain margin	11		11			
$r_i$ Input resistance		25°C	0.3	2	0.3*	2	MΩ	
$r_o$ Output resistance	$V_O = 0,$ See Note 9	25°C	75		75		Ω	
$C_i$ Input capacitance		25°C	1.4		1.4		pF	
$z_{ic}$ Common-mode input impedance	$f = 20\text{ Hz}$	25°C	200		200		MΩ	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{ min}, V_O = 0$	25°C	70	90	70	90	dB	
		Full range	70			70		
$k_{SVS}$ Supply-voltage sensitivity ( $\Delta V_{IO}/\Delta V_{CC}$ )	$V_{CC} = \pm 9\text{ V to } \pm 15\text{ V}, V_O = 0$	25°C	30	150	30	150	μV/V	
		Full range	150			150		
$V_n$ Equivalent input noise voltage (closed loop)	$A_{VD} = 100, f = 1\text{ kHz}, R_S = 0, BW = 1\text{ Hz}$	25°C	45		45		nV/√Hz	
$I_{OS}$ Short-circuit output current		25°C	±25	±40	±25	±40	mA	
$I_{CC}$ Supply current (both amplifiers)	$V_O = 0, \text{ No load}$	25°C	3.4	5.6	3.4	5	mA	
		Full range	6.6			6.6		
$P_D$ Total power dissipation (both amplifiers)	$V_O = 0, \text{ No load}$	25°C	100	170	100	150	mW	
		Full range	200			200		
$V_{O1}/V_{O2}$ Crosstalk attenuation		25°C	120		120		dB	

\*On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All characteristics are specified under open-loop operating conditions with zero common-mode input voltage, unless otherwise specified. Full range for MC1458 is 0°C to 70°C and for MC1558 is -55°C to 125°C.

NOTE 9: This typical value applies only at frequencies above a few hundred hertz because of the effect of drift and thermal feedback.



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operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $C_L = 100\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 1)

PARAMETER		TEST CONDITIONS		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_r$	Rise time	$V_I = 20\text{ mV}$ ,	$R_L = 2\text{ k}\Omega$ ,	0.3			0.3			$\mu\text{s}$
	Overshoot factor	$V_I = 20\text{ mV}$ ,	$R_L = 2\text{ k}\Omega$	5			5			%
SR	Slew rate at unity gain	$V_I = 10\text{ V}$ ,	$R_L = 2\text{ k}\Omega$	0.5			0.5			$\text{V}/\mu\text{s}$

## PARAMETER MEASUREMENT INFORMATION

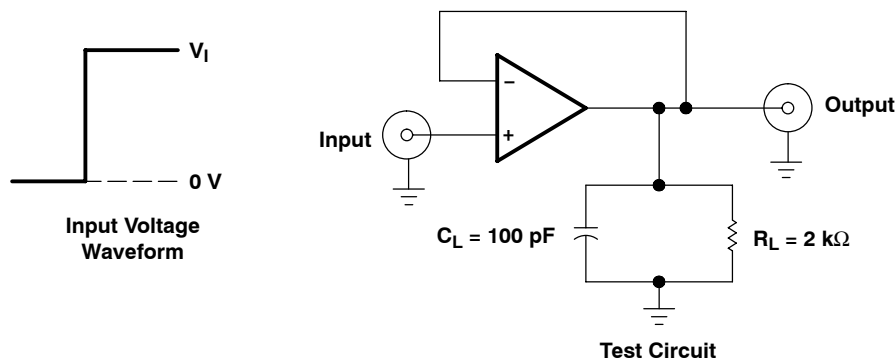


Figure 1. Rise-Time, Overshoot, and Slew-Rate Waveform and Test Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9760301Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760301Q2A MC1558FKB	Samples
5962-9760301QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9760301QPA MC1558	Samples
MC1458D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC1458	
MC1458DE4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC1458	
MC1458DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC1458	Samples
MC1458DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC1458	Samples
MC1458DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC1458	Samples
MC1458P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC1458P	Samples
MC1458PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC1458P	Samples
MC1458PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	M1458	Samples
MC1558FKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760301Q2A MC1558FKB	Samples
MC1558JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	MC1558JG	Samples
MC1558JGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9760301QPA MC1558	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

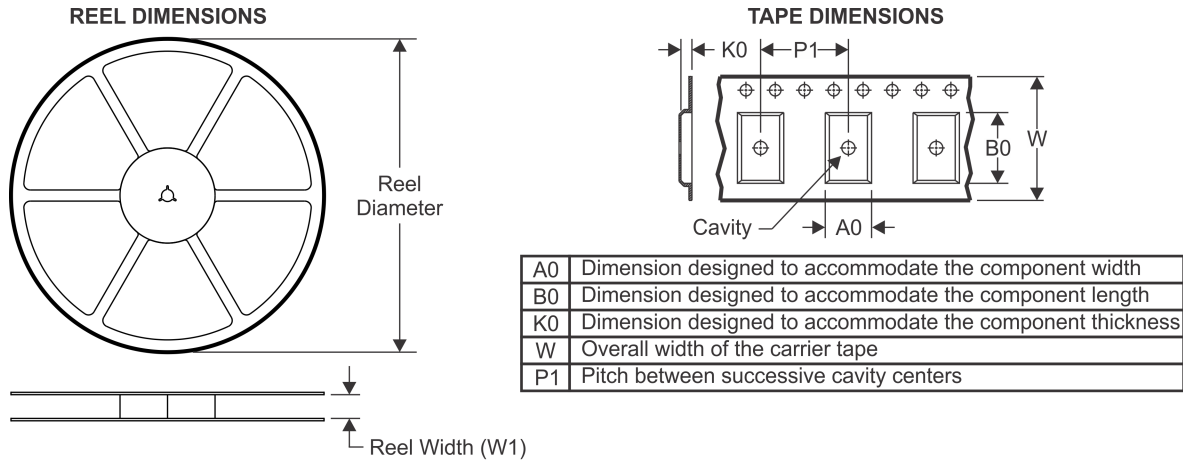
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

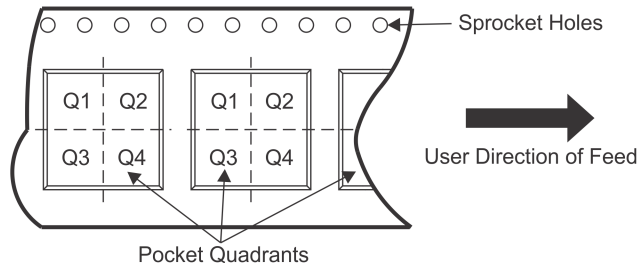
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



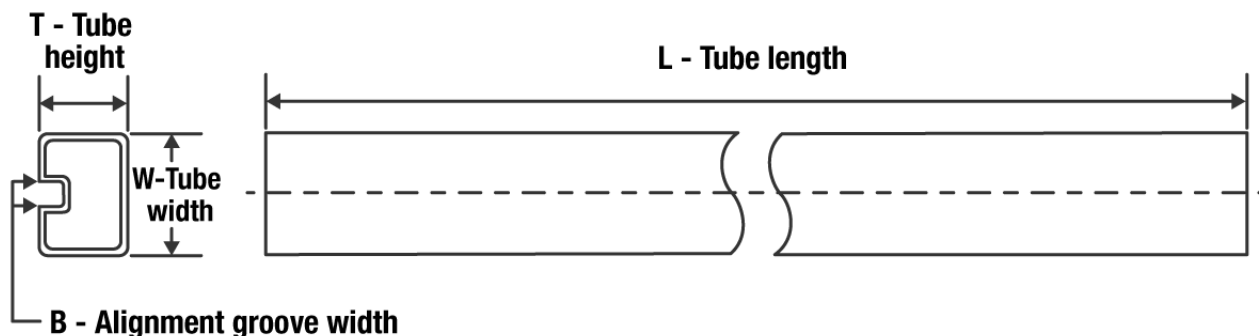
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC1458DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC1458DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC1458DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC1458DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC1458PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC1458DR	SOIC	D	8	2500	853.0	449.0	35.0
MC1458DR	SOIC	D	8	2500	853.0	449.0	35.0
MC1458DR	SOIC	D	8	2500	340.5	336.1	25.0
MC1458DR	SOIC	D	8	2500	340.5	336.1	25.0
MC1458PSR	SO	PS	8	2000	853.0	449.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9760301Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
MC1458D	D	SOIC	8	75	507	8	3940	4.32
MC1458D	D	SOIC	8	75	506.6	8	3940	4.32
MC1458DE4	D	SOIC	8	75	506.6	8	3940	4.32
MC1458DE4	D	SOIC	8	75	507	8	3940	4.32
MC1458P	P	PDIP	8	50	506	13.97	11230	4.32
MC1458PE4	P	PDIP	8	50	506	13.97	11230	4.32
MC1558FKB	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

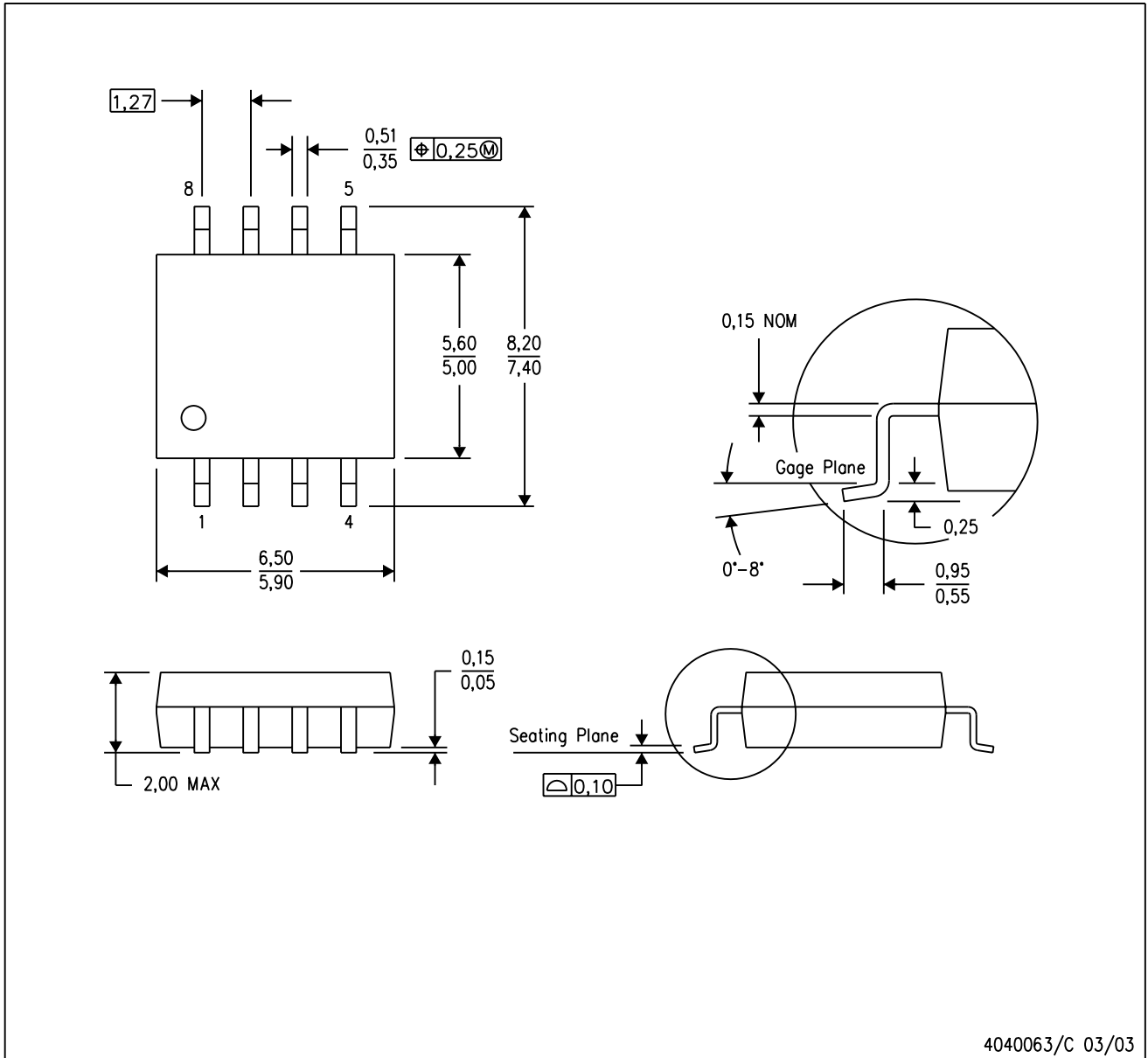
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

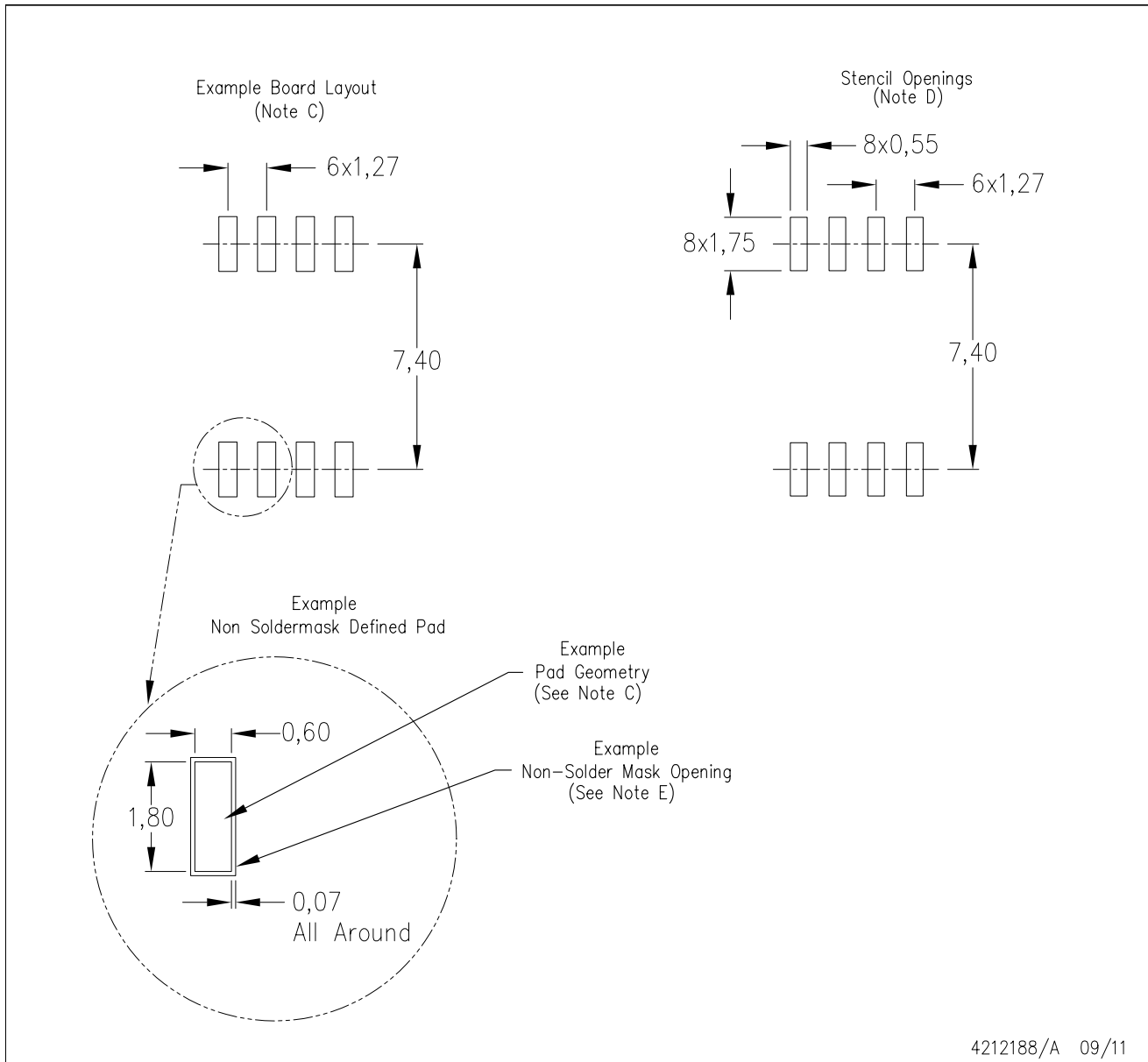
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

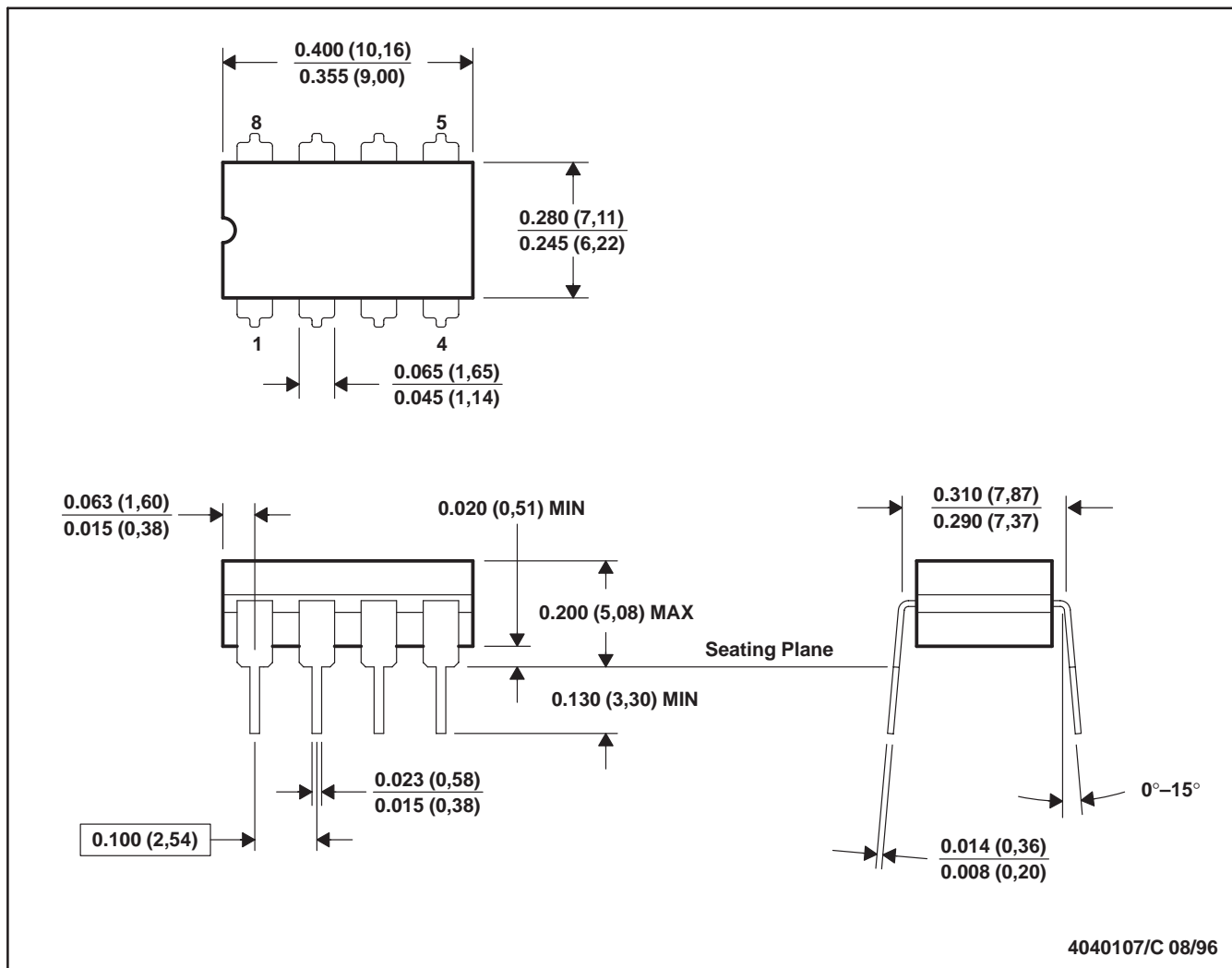
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

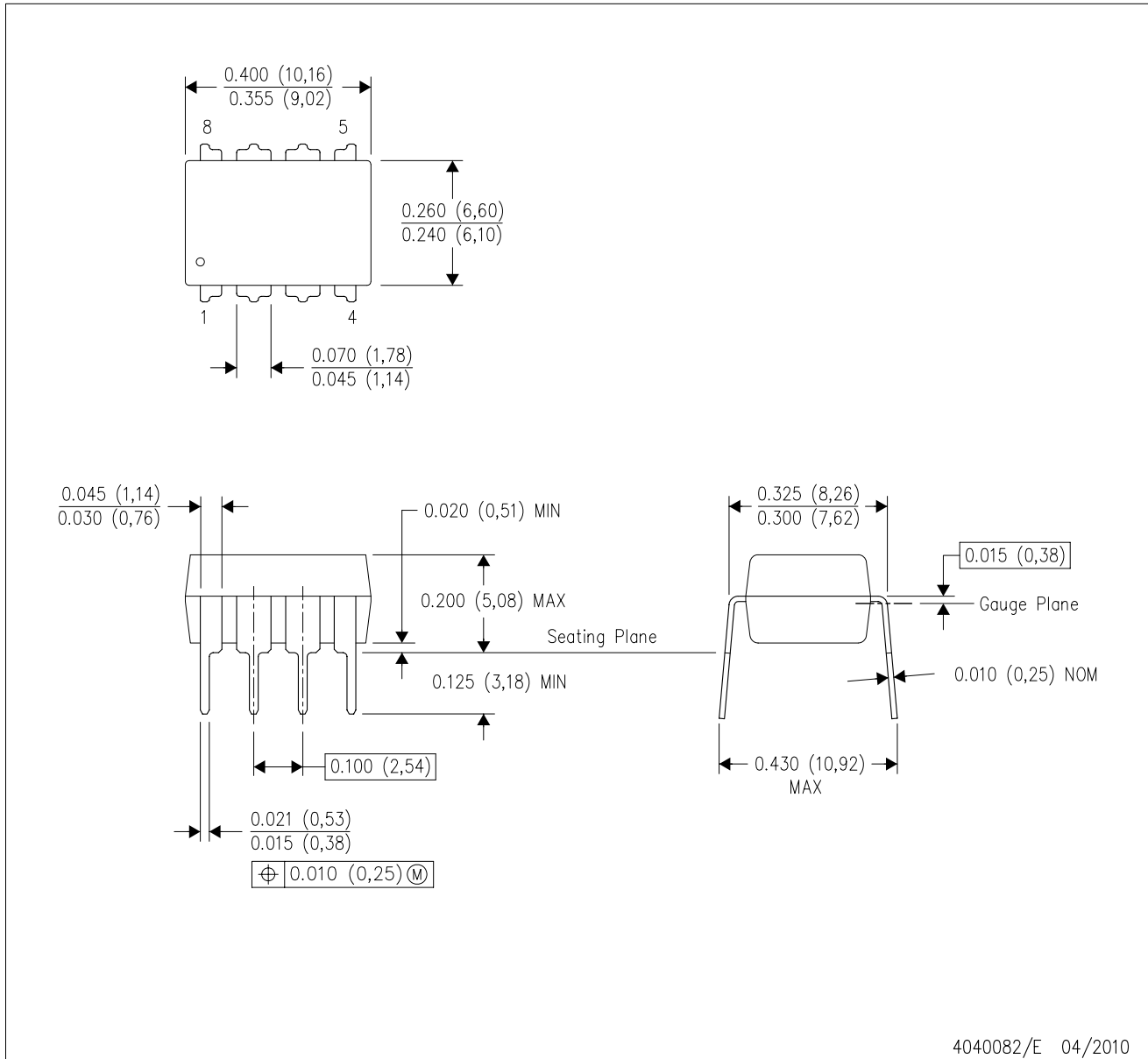
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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