TPS731xx Capacitor-Free, NMOS, 150-mA Low Dropout Regulator With Reverse Current Protection

1 Features

- Stable With or Without Capacitors of All Types
- Input Voltage Range of 1.7 V to 5.5 V
- Ultralow Dropout Voltage: 30 mV Typical (150-mA Load)
- Excellent Load Transient Response—With or Without Optional Output Capacitor
- New NMOS Topology Provides Low Reverse Leakage Current
- Low Noise: 30 μV_{RMS} Typical (10 kHz to 100 kHz)
- 0.5% Initial Accuracy
- 1% Overall Accuracy Over Line, Load, and Temperature
- Less Than 1-µA Maximum I_Q in Shutdown Mode
- Thermal Shutdown and Specified Minimum and Maximum Current Limit Protection
- Available in Multiple Output Voltage Versions
  - Fixed Outputs of 1.20 V to 5 V
  - Adjustable Outputs from 1.2 V to 5.5 V
  - Custom Outputs Available

2 Applications

- Smart Grid and Energy
- Building Automation
- Set-Top Boxes
- Medical Equipment
- Test and Measurement
- Point-of-Sale Terminals
- Wireless Infrastructure

3 Description

The TPS731xx family of low-dropout (LDO) linear voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low equivalent series resistance (ESR), and even allows operation without a capacitor. The device also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

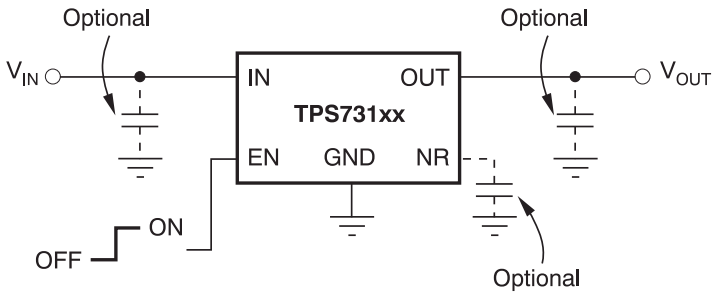
The TPS731xx uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is less than 1 µA and ideal for portable applications. The extremely low output noise (30 μV_{RMS} with 0.1-µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS731xx	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit for Fixed-Voltage Versions



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (August 2009) to Revision N — **Page**

- Changed first and third *Features* bullets ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed list of recommended *Applications* ... 1
- Changed *Pin Configuration and Functions* section; updated table format to meet new standards ... 3
- Changed free-air temperature to junction temperature in *Absolute Maximum Ratings* condition statement ... 4
- Deleted *Power Dissipation Ratings* table ... 4
- Changed *Thermal Information* table; updated thermal resistance values for all packages ... 4

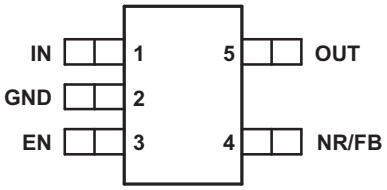
Changes from Revision L (May, 2009) to Revision M — **Page**

- Changed Figure 10 ... 6
- Added paragraph about recommended start-up sequence to *Internal Current Limit* section ... 13
- Added paragraph about current foldback and device start-up to *Enable Pin and Shutdown* section ... 13

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5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input supply.
GND	2	—	Ground.
EN	3	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to *Enable Pin and Shutdown* for more details. EN can be connected to IN if not used.
NR	4	—	Fixed-voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	4	I	Adjustable-voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	O	Output of the regulator. There are no output capacitor requirements for stability.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	6	
	V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Peak output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Power Dissipation*		
Temperature	Junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.7		5.5	V
I_{OUT}	Output current	0		150	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS731xx DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	207.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	35	
ψ_{JT}	Junction-to-top characterization parameter	13.5	
ψ_{JB}	Junction-to-board characterization parameter	34.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			1.7		5.5	V
V_{FB}	Internal reference (TPS73101)		T_J = 25°C	1.198	1.20	1.210	V
V_{OUT}	Output voltage range (TPS73101)(2)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1) (3)	Nominal	T_J = 25°C	–0.5%		0.5%	
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V; 10 mA ≤ I_{OUT} ≤ 150 mA	–1%	±0.5%	1%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		1 mA ≤ I_{OUT} ≤ 150 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 150 mA		0.0005		
V_{DO}	Dropout voltage(4) (V_{IN} = V_{OUT} (nom) – 0.1V)		I_{OUT} = 150 mA		30	100	mV
$Z_{O(DO)}$	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	150	360	500	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		200		mA
I_{REV}	Reverse leakage current(5) ($-I_{IN}$)		V_{EN} ≤ 0.5 V, 0V ≤ V_{IN} ≤ V_{OUT}		0.1	10	µA
I_{GND}	GND pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 150 mA		550	750	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_J ≤ 100°C		0.02	1	µA
I_{FB}	FB pin current (TPS73101)				0.1	0.3	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 150 mA		58		dB
			f = 10 kHz, I_{OUT} = 150 mA		37		
V_n	Output noise voltage BW = 10Hz - 100kHz		C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 3 V, R_L = 30 Ω, C_{OUT} = 1 µF, C_{NR} = 0.01 µF		600		µs
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(high)}$	EN pin current (enabled)		V_{EN} = 5.5V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature		Shutdown Temp increasing		160		°C
			Reset Temp decreasing		140		
T_J	Operating junction temperature			–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) TPS73101 is tested at V_{OUT} = 2.5 V.
(3) Tolerance of external resistors not included in this specification.
(4) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)}$ < 1.8 V because minimum V_{IN} = 1.7 V.
(5) Fixed-voltage versions only; refer to *Application Information* for more information.

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6.6 Typical Characteristics

For all voltage versions at T_J= 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

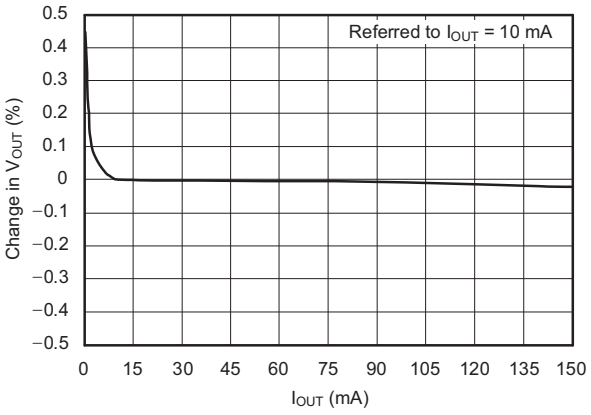


Figure 1. Load Regulation

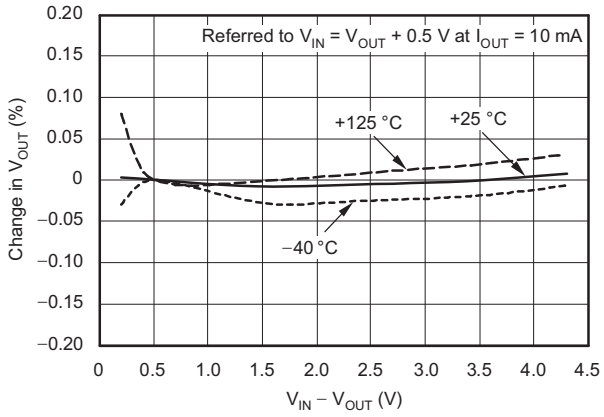


Figure 2. Line Regulation

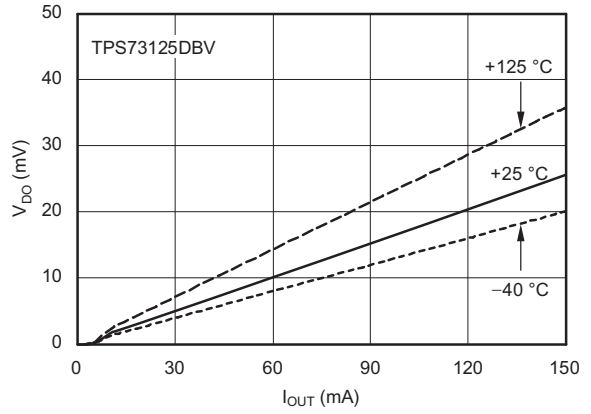


Figure 3. Dropout Voltage vs Output Current

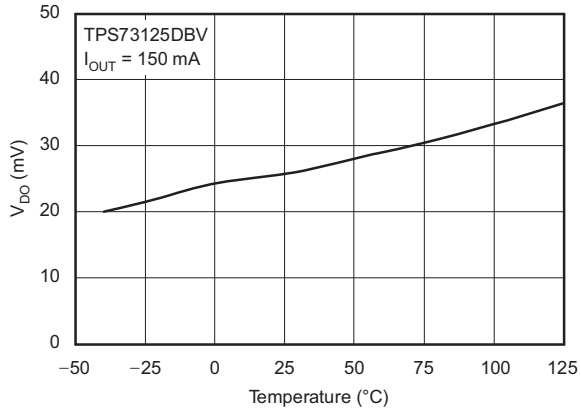


Figure 4. Dropout Voltage vs Temperature

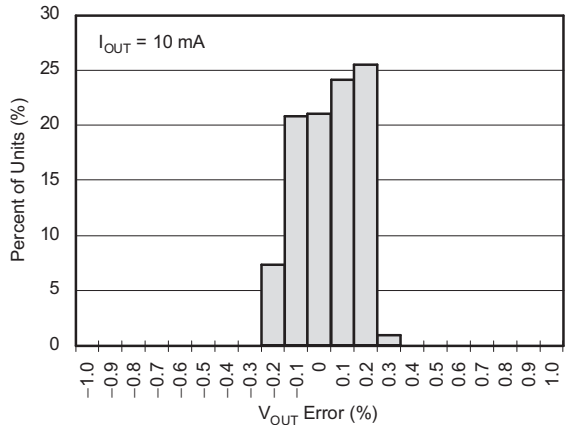


Figure 5. Output Voltage Accuracy Histogram

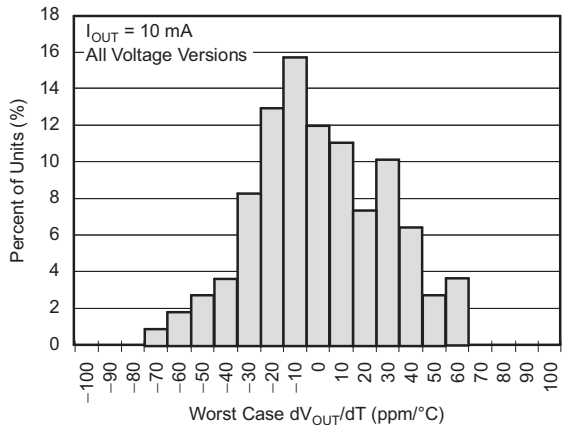


Figure 6. Output Voltage Drift Histogram

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Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

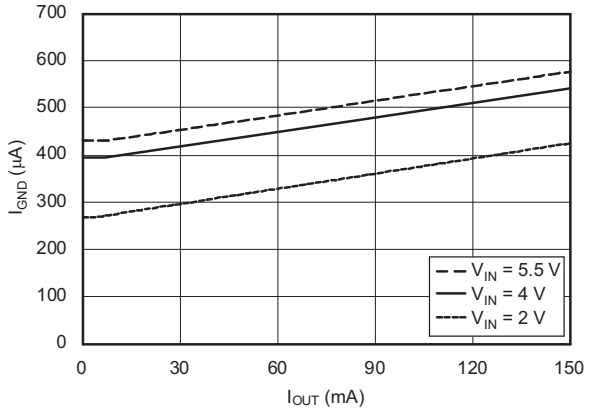


Figure 7. Ground Pin Current vs Output Current

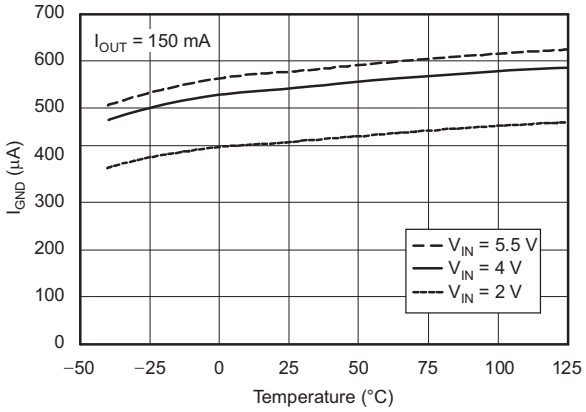


Figure 8. Ground Pin Current vs Temperature

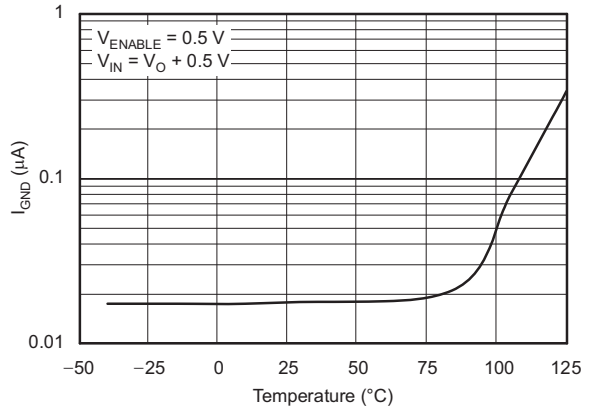


Figure 9. Ground Pin Current in Shutdown vs Temperature

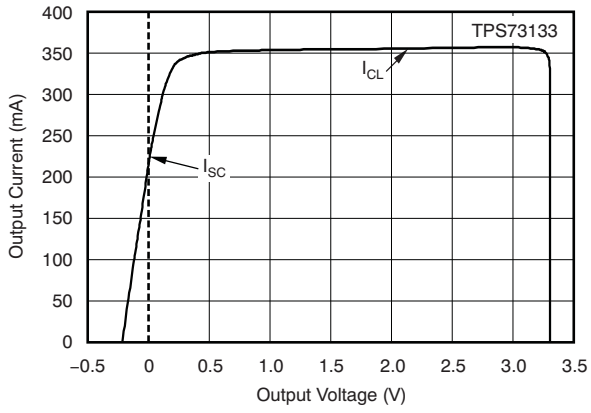


Figure 10. Current Limit vs V_{OUT} (Foldback)

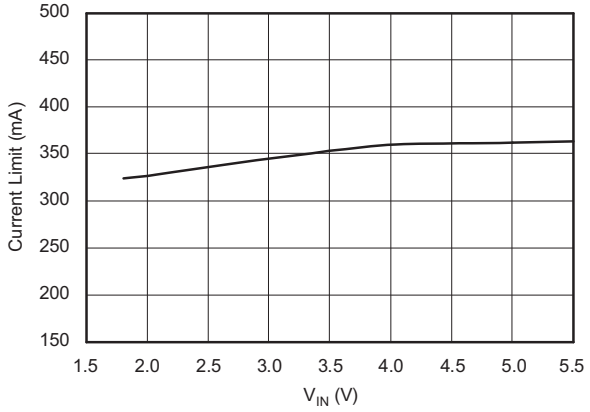


Figure 11. Current Limit vs V_{IN}

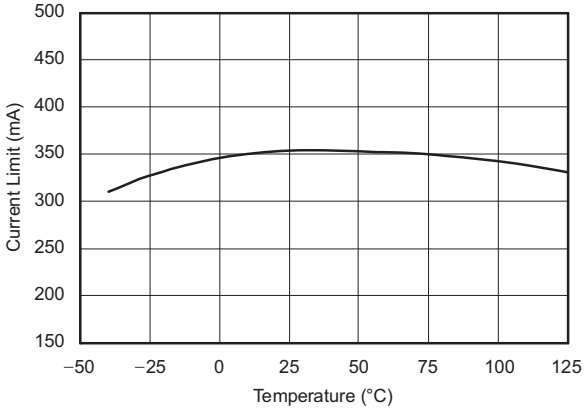


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

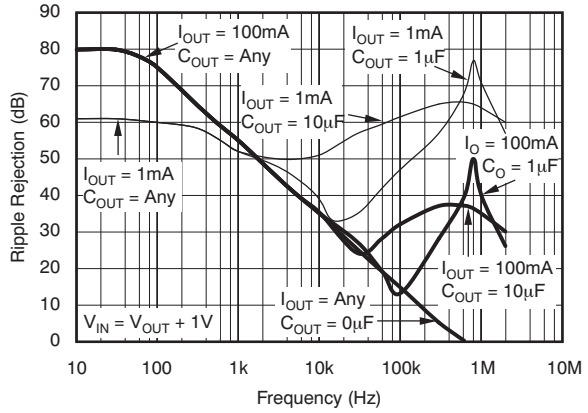


Figure 13. PSRR (Ripple Rejection) vs Frequency

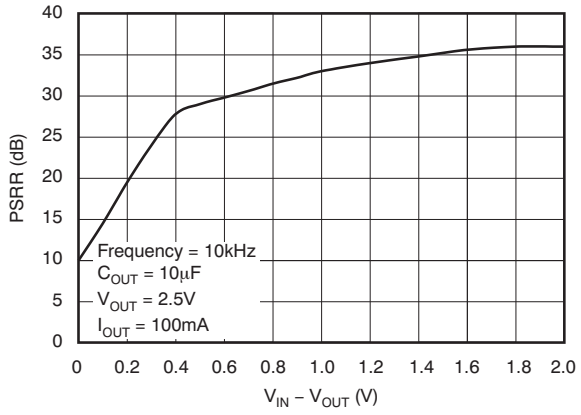


Figure 14. PSRR (Ripple Rejection) vs $V_{IN} - V_{OUT}$

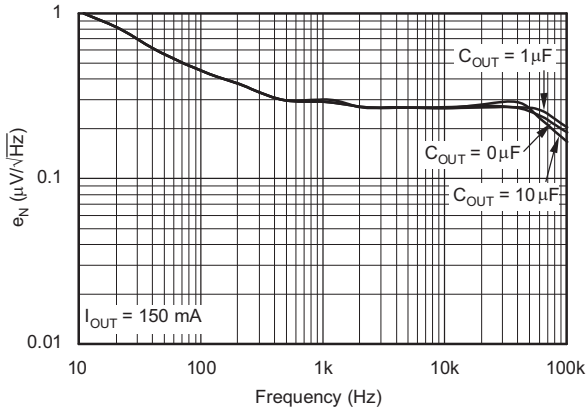


Figure 15. Noise Spectral Density C_{NR} = 0 µF

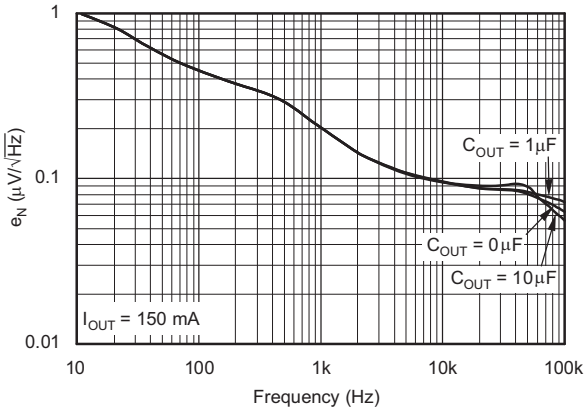


Figure 16. Noise Spectral Density C_{NR} = 0.01 µF

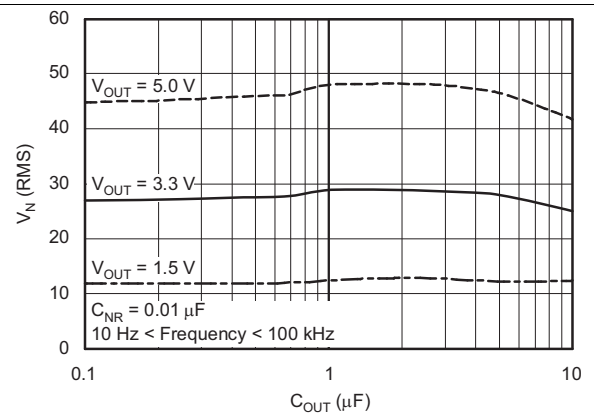


Figure 17. RMS Noise Voltage vs C_{OUT}

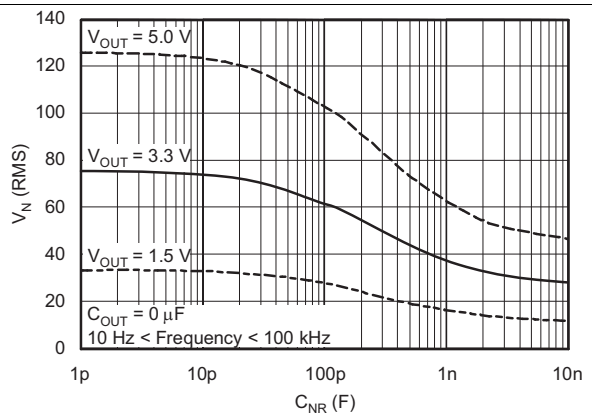


Figure 18. RMS Noise Voltage vs C_{NR}

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Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

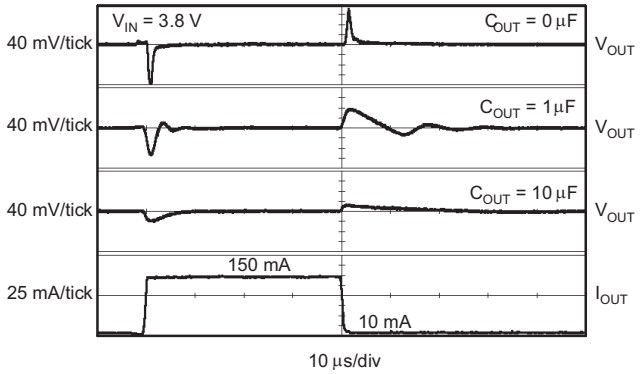


Figure 19. TPS73133 Load Transient Response

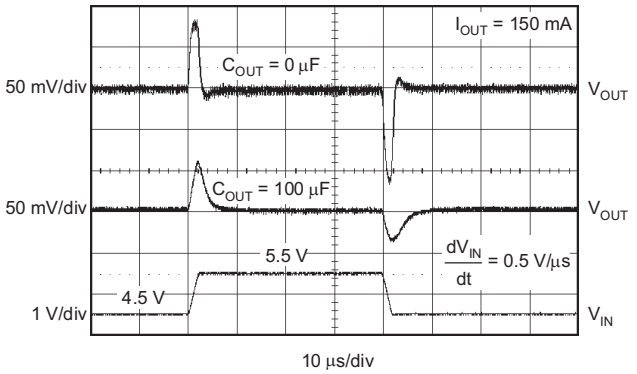


Figure 20. TPS73133 Line Transient Response

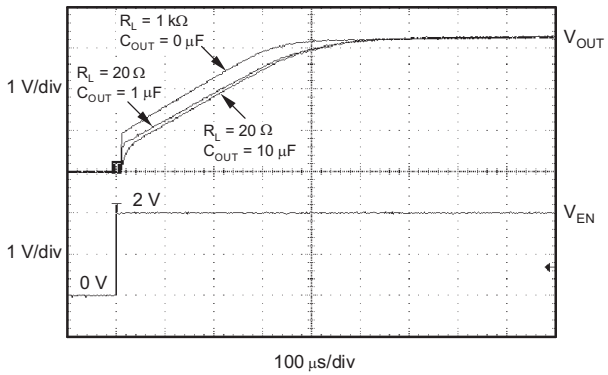


Figure 21. TPS73133 Turnon Response

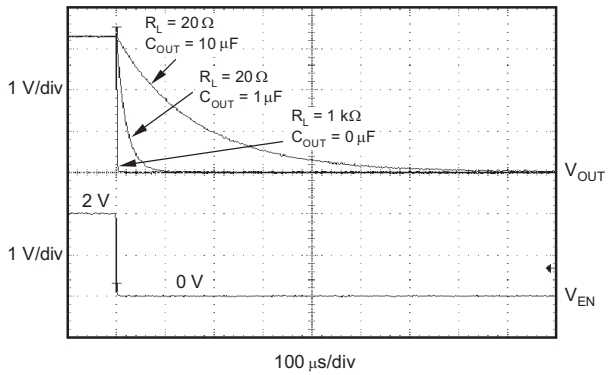


Figure 22. TPS73133 Turnoff Response

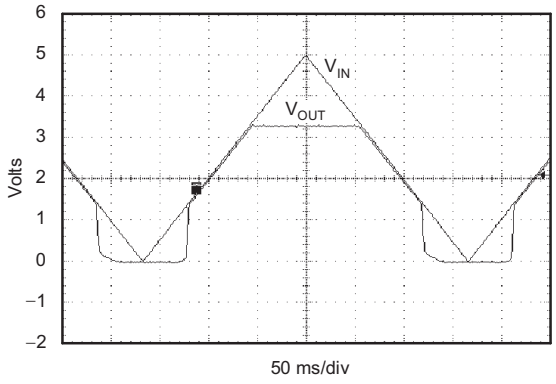


Figure 23. TPS73133 Power Up and Power Down

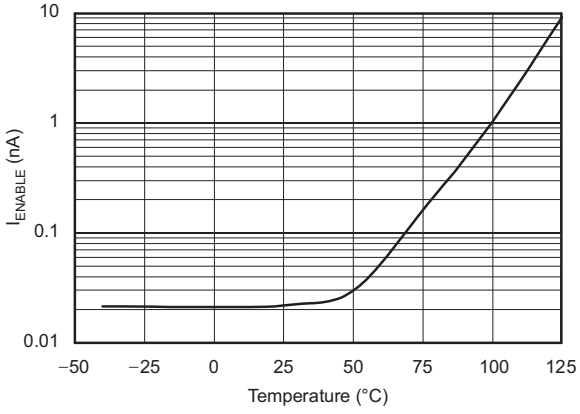


Figure 24. I_{ENABLE} vs Temperature

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Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

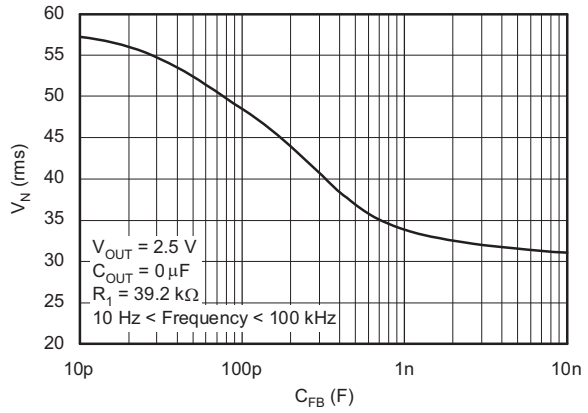


Figure 25. TPS73101 RMS Noise Voltage vs C_{FB}

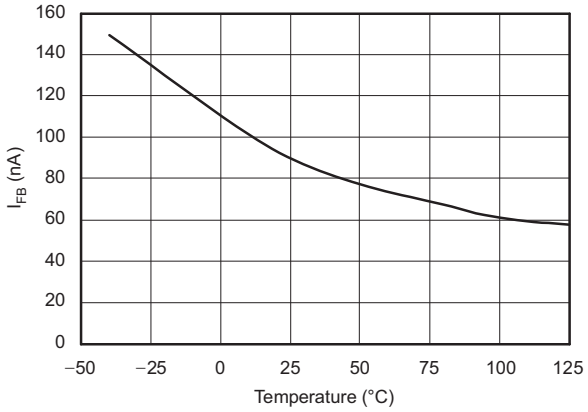


Figure 26. TPS73101 I_{FB} vs Temperature

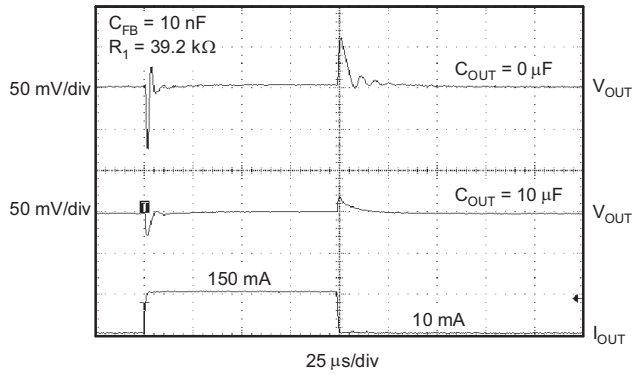


Figure 27. TPS73101 Load Transient, Adjustable Version

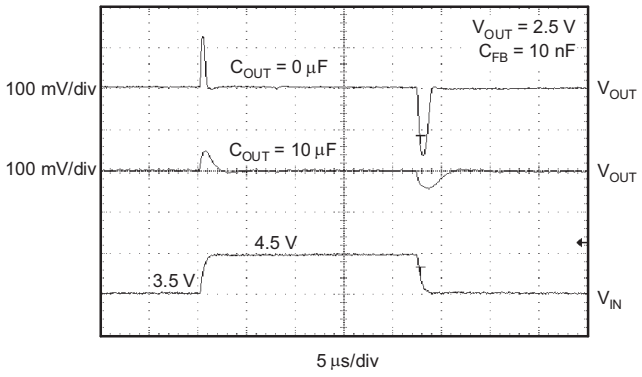


Figure 28. TPS73101 Line Transient, Adjustable Version

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7 Detailed Description

7.1 Overview

The TPS731xx family of low-dropout linear regulators operates down to an input voltage of 1.7 V and supports output voltages down to 1.2 V while sourcing up to 150 mA of load current. This linear regulator uses an NMOS pass element with an integrated 4-MHz charge pump to provide a dropout voltage of less than 100 mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS731xx family of devices does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this family of linear regulators an ideal choice when powering a load where the effective capacitance is unknown.

The TPS731xx family of devices also features a noise reduction (NR) pin that allows for additional reduction of the output noise. With a noise reduction capacitor of 0.01 µF connected from the NR pin to GND, the TPS73115 output noise can be as low as 12.75 μV_{RMS}. The low noise output featured by the TPS731xx family makes it well-suited for powering VCOs or any other noise sensitive load.

7.2 Functional Block Diagrams

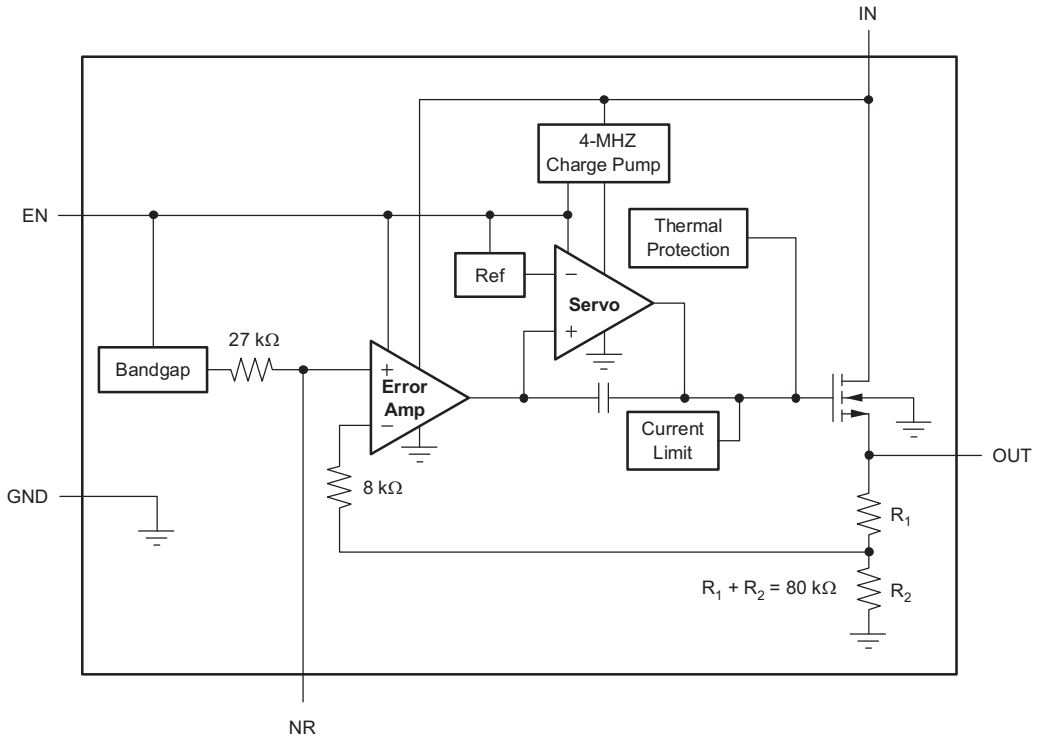
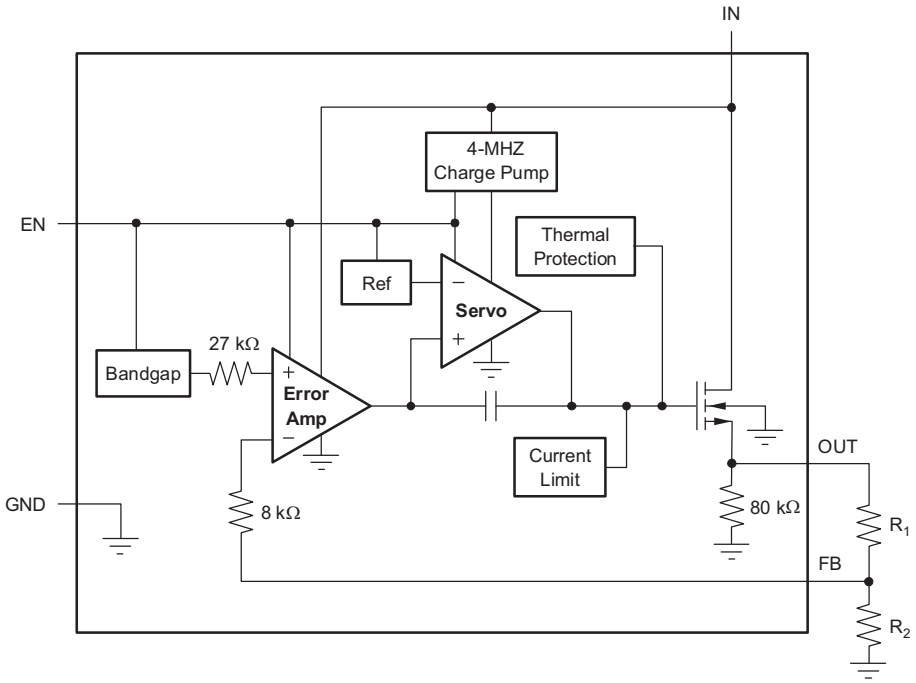


Figure 29. Fixed-Voltage Version

Functional Block Diagrams (continued)



Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3kΩ
1.8 V	28.0 kΩ	56.2 kΩ
2.5 V	39.2kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3.0 V	46.4 kΩ	30.9 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \cdot 1.204$; $R_1 \| R_2 \cong 19$ kΩ for best accuracy.

Figure 30. Adjustable-Voltage Version

7.3 Feature Description

7.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS731xx and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by Equation 1:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Because the value of V_{REF} is 1.2 V, this relationship reduces to Equation 2 for the case of no C_{NR}.

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship shown in Equation 3 for C_{NR} = 10 nF.

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in *Typical Characteristics*.

The TPS73101 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improves load transient performance.

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Feature Description (continued)

The TPS731xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250 µV of switching noise at approximately 4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

7.3.2 Internal Current Limit

The TPS731xx internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 10.

Note from Figure 10 that approximately –0.2 V of V_{OUT} results in a current limit of 0 mA. Therefore, if OUT is forced below –0.2 V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS731xx should be enabled first.

7.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5 V (maximum) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 21).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power up.

The current limit foldback can prevent device start-up under some conditions. See *Internal Current Limit*.

7.3.4 Reverse Current

The NMOS pass element of the TPS731xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. The reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80-kΩ internal resistor divider to ground (see Figure 29 and Figure 30).

For the TPS73101, reverse current may flow when V_{FB} is more than 1.0 V above V_{IN}.

7.4 Device Functional Modes

7.4.1 Normal Operation With 1.7 V ≤ V_{IN} ≤ 5.5 V and V_{EN} ≥ 1.7 V

The TPS731xx family requires an input voltage of at least 1.7 V to function properly and attempt to maintain regulation.

When operating the device near 5.5 V, take care to suppress any transient spikes that may exceed the 6.0-V absolute maximum voltage rating. The device should never operate at a DC voltage greater than 5.5 V.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS731xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS731xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

8.2 Typical Applications

Figure 31 shows the basic circuit connections for the fixed-voltage models. Figure 32 gives the connections for the adjustable output version (TPS73101).

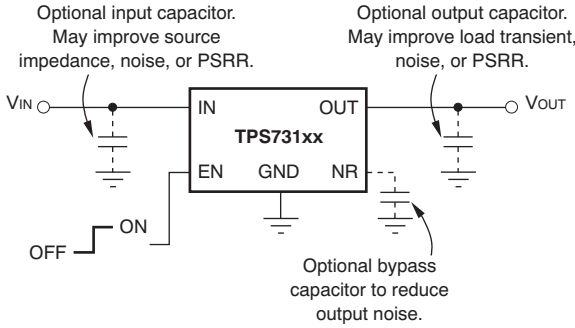


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

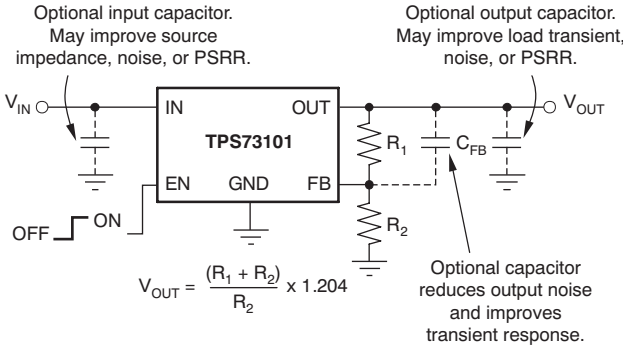


Figure 32. Typical Application Circuit for Adjustable-Voltage Version

8.2.1 Design Requirements

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 32. Sample resistor values for common output voltages are shown in Figure 30.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19 kΩ. This 19 kΩ, in addition to the internal 8-kΩ resistor, presents the same impedance to the error amp as the 27-kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

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Typical Applications (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF, low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

8.2.2.2 Dropout Voltage

The TPS731xx uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the NMOS pass element.

For large step changes in load current, the TPS731xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of V_{IN} – V_{OUT} above this line insure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to DC dropout levels], the TPS731xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

8.2.2.3 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 µF) from the output pin (OUT) to ground will reduce undershoot magnitude but increase its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin will also improve the transient response.

The TPS731xx does not have active pulldown when the output is overvoltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal and external load resistance. The rate of decay is given by Equation 4 and Equation 5:

(Fixed-voltage version)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable-voltage version)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

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Typical Applications (continued)

8.2.3 Application Curves

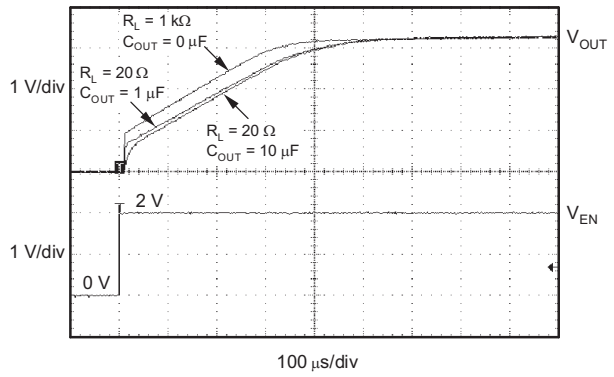


Figure 33. TPS73133 Turnon Response

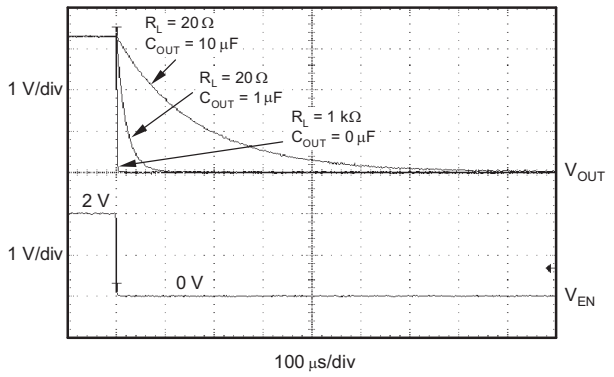


Figure 34. TPS73133 Turnoff Response

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9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.7 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin (GND) of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Solder pad footprint recommendations for the TPS731xx are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015), available from the TI website at www.ti.com.

10.2 Layout Example

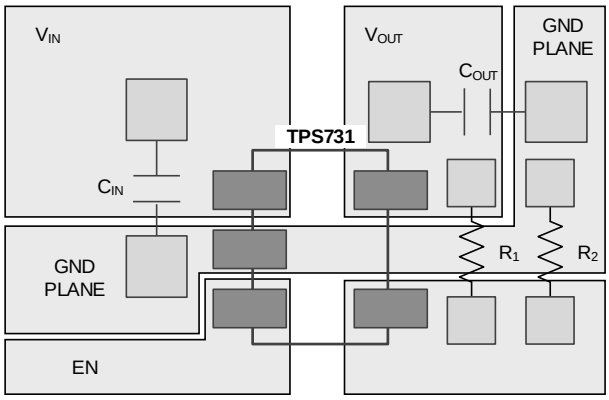


Figure 35. Example Layout (DBV Package)

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS731xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS731xx into thermal shutdown degrades device reliability.

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Thermal Considerations (continued)

10.3.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* table. Using heavier copper will increase the effectiveness in removing heat from the device.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS731 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS731**xx** ***yyy z***	**xx** is the nominal output voltage (for example, 25 = 2.5 V; 01 = Adjustable). **yyy** is the package designator. **z** is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Application report. *Solder Pad Recommendations for Surface-Mount Devices*. Literature number SBFA015.

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS73101	Click here	Click here	Click here	Click here	Click here
TPS731125	Click here	Click here	Click here	Click here	Click here
TPS73115	Click here	Click here	Click here	Click here	Click here
TPS73118	Click here	Click here	Click here	Click here	Click here
TPS73125	Click here	Click here	Click here	Click here	Click here
TPS73130	Click here	Click here	Click here	Click here	Click here
TPS73131	Click here	Click here	Click here	Click here	Click here
TPS73132	Click here	Click here	Click here	Click here	Click here
TPS73133	Click here	Click here	Click here	Click here	Click here
TPS73150	Click here	Click here	Click here	Click here	Click here

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11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73101DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PWYQ	Samples
TPS73101DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PWYQ	Samples
TPS73101DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PWYQ	Samples
TPS73101DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PWYQ	Samples
TPS731125DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYX	Samples
TPS731125DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYX	Samples
TPS73115DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T31	Samples
TPS73115DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T31	Samples
TPS73115DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T31	Samples
TPS73118DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32	Samples
TPS73118DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32	Samples
TPS73118DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32	Samples
TPS73118DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32	Samples
TPS73125DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI	Samples
TPS73125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI	Samples
TPS73125DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI	Samples
TPS73125DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI	Samples
TPS73130DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T33	Samples
TPS73130DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T33	Samples
TPS73130DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T33	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73131DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYS	Samples
TPS73131DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYS	Samples
TPS73132DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T52	Samples
TPS73132DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T52	Samples
TPS73133DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34	Samples
TPS73133DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34	Samples
TPS73133DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34	Samples
TPS73150DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35	Samples
TPS73150DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35	Samples
TPS73150DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

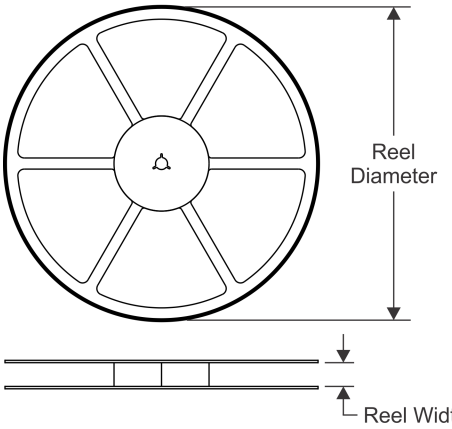
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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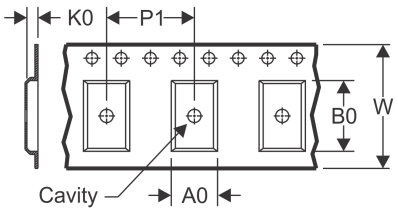
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

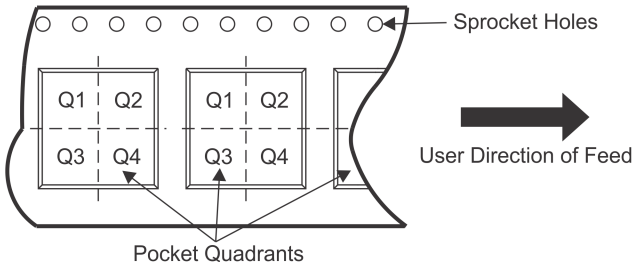


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

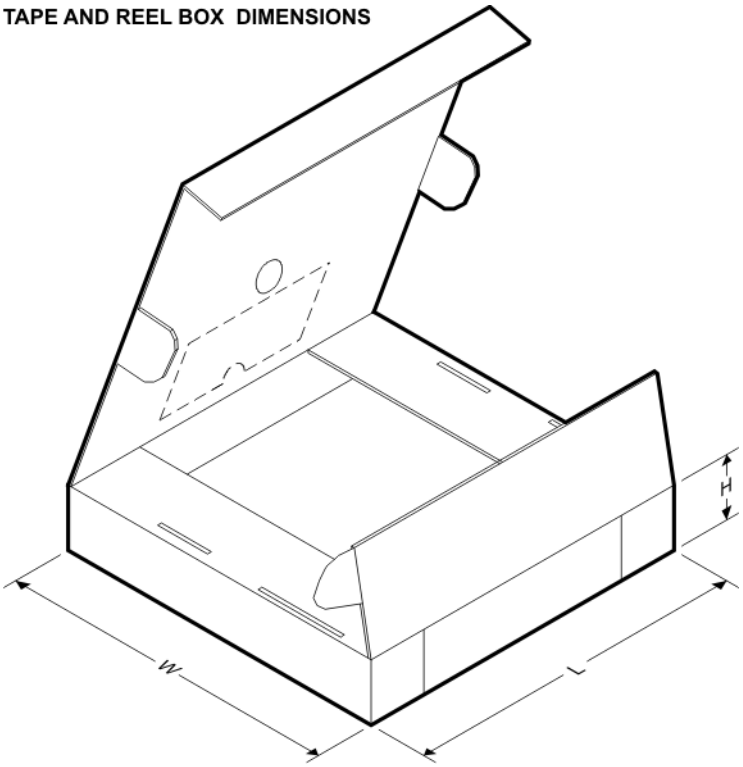


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73101DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73101DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS731125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS731125DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73115DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73115DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73118DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73118DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73125DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73130DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73130DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73131DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73131DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73132DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73132DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73133DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73133DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73150DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73150DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73101DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73101DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS731125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS731125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73115DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73115DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73118DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73118DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73130DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73130DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73131DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73131DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73132DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0

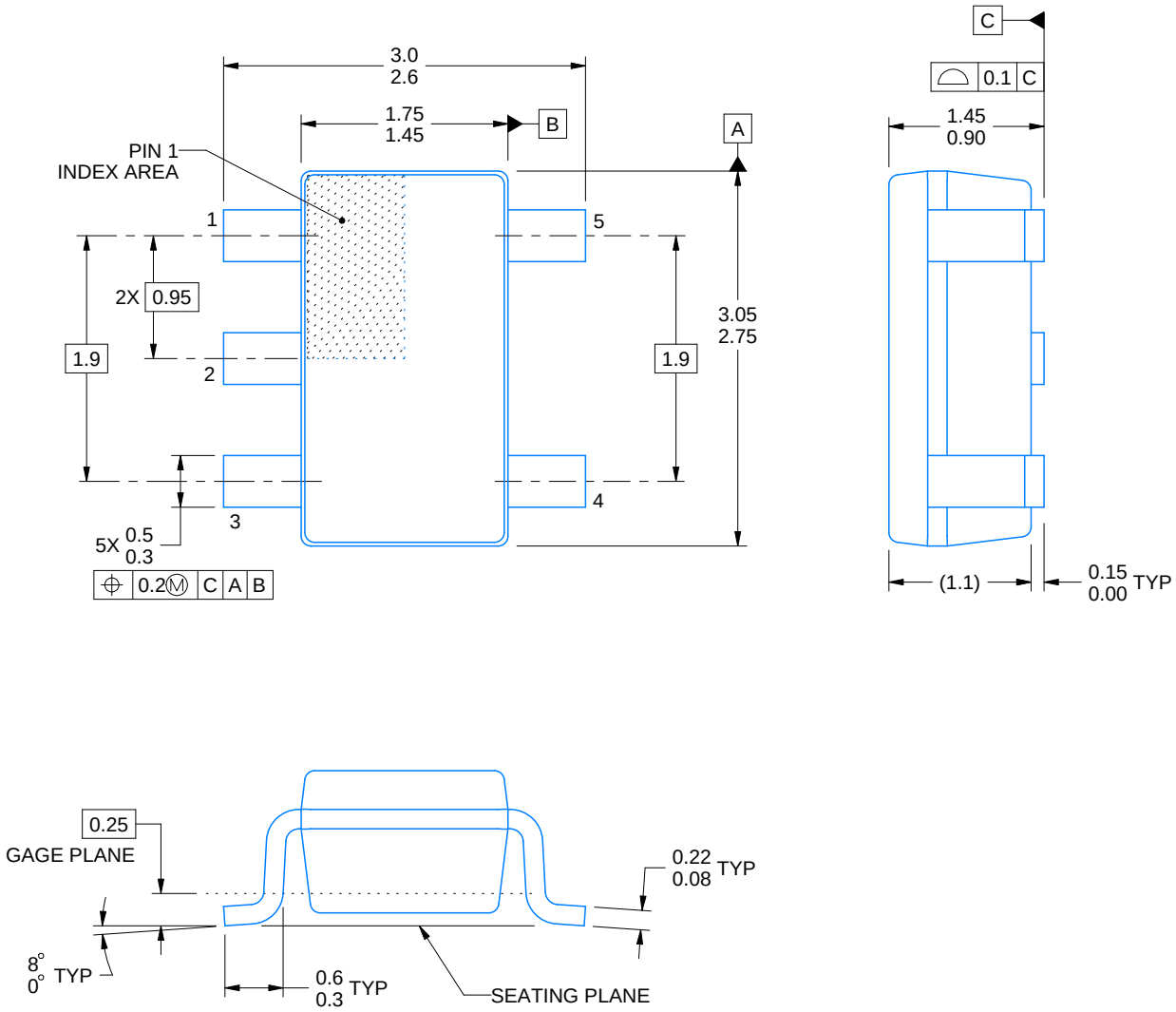
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73132DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS73133DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73133DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73150DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73150DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

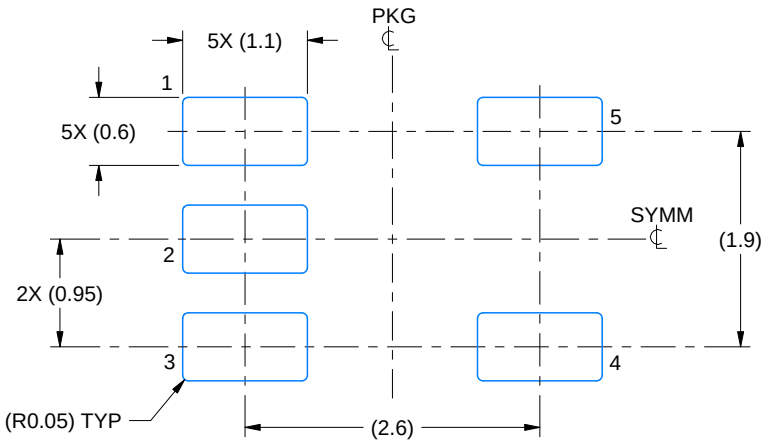
SMALL OUTLINE TRANSISTOR



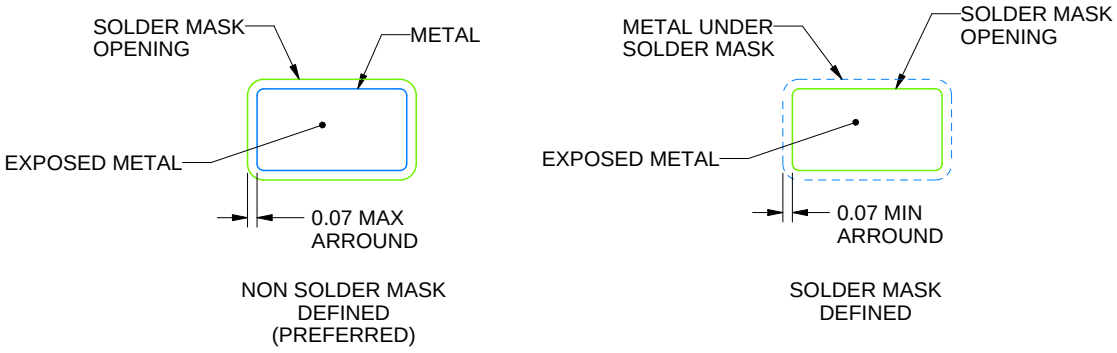
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

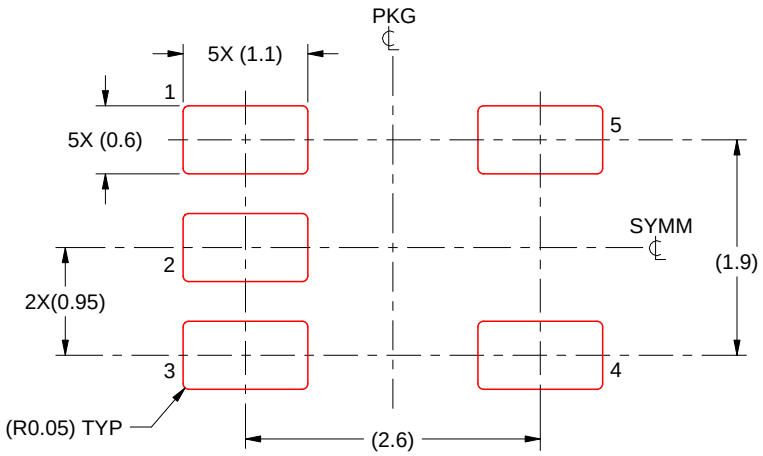


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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