SMBus/I2C Controlled WLED Driver for Medium-Sized LCD Backlight

Check for Samples: LP8543

FEATURES

- **High-Voltage DC/DC Boost Converter with Integrated FET**
- **5.5V to 22V Input Voltage Range to Support 2x, 3x and 4x Li-Ion Batteries.**
- **PWM Phase Shift Control with Adaptive Boost Output to Increase Efficiency Compared to Conventional Boost Converters Topologies**
- **PWM Brightness Control for Single Wire Control and Stand-Alone Use**
- **Digital Ambient Light Sensor Interface with User-Programmed Ambient Light to Backlight Brightness Curve**
- **Easy-to-Use EEPROM Calibration for Current, Intensity and Ambient Light Response Setting**
- **Seven LED Drivers with LED Fault (Short/open) Detection**
- **Eight-Bit LED Current Control**
- **Internal Thermal Protection and Backlight Safety Dimming Feature**
- **Two Wire, SMBus/ I^2C-Compatible Control Interface**
- **Low-Input Voltage Detection and Shutdown**
- **Minimum Number of External Components**
- **WQFN 24-Pin Package, 4 x 4 x 0.8 mm**

APPLICATIONS

- **Medium Sized (>10 inches) LCD Display Backlight**
- **LED Lighting**

DESCRIPTION

The LP8543 is a white LED driver with integrated boost converter. It has 7 adjustable current sinks which can be controlled by SMBus or I^2C-compatible serial interface, PWM input and Ambient Light Sensor (ALS).

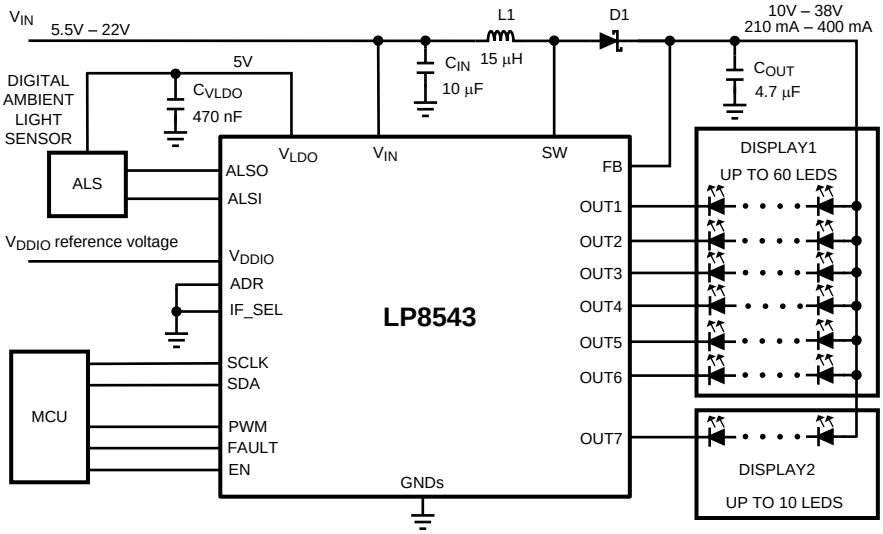
The boost converter has adaptive output voltage control based on the LED driver voltages. This feature minimizes the power consumption by adjusting the voltage to lowest sufficient level in all conditions. Phase Shift PWM dimming offers further power saving especially when there is poor matching in the forward voltages of the LED strings. Boost voltage can also be controlled through the SMBus/I^2C.

Internal EEPROM stores the data for backlight brightness and ambient light sensor calibration. Brightness can be calibrated during the backlight unit production so that all units produce the same brightness. EEPROM also stores the coefficients for the LED control equations and the default LED current value. LED current has 8–bit adjustment from 0 to 60 mA.

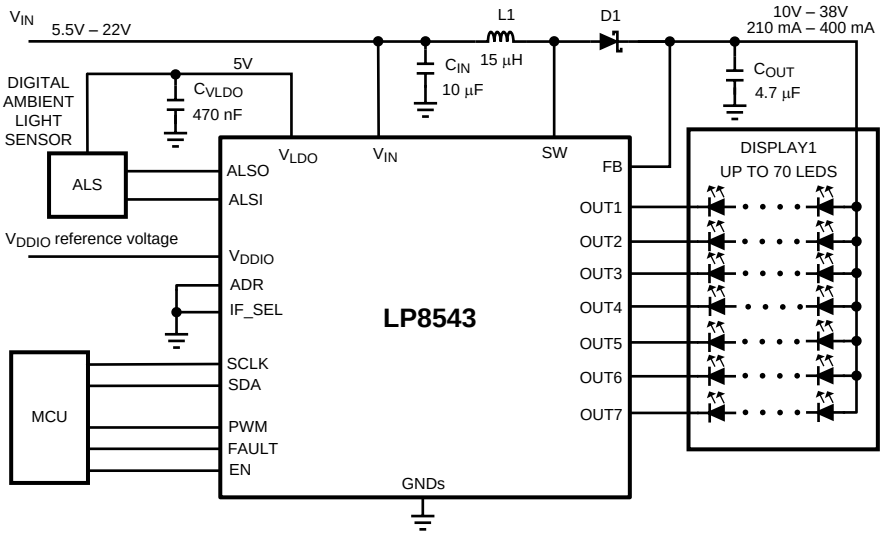
The LP8543 has several safety and diagnostic features. Low-input voltage detection turns the chip off if the system gets stuck and battery fully discharges. Input voltage detection threshold is adjustable for different battery configurations. Thermal regulation reduces backlight brightness above a set temperature. LED fault detection reports open or LED short fault. Boost over-current fault detection protects the chip in case of over-current event.

LP8543 is available in the WQFN 24-pin package.

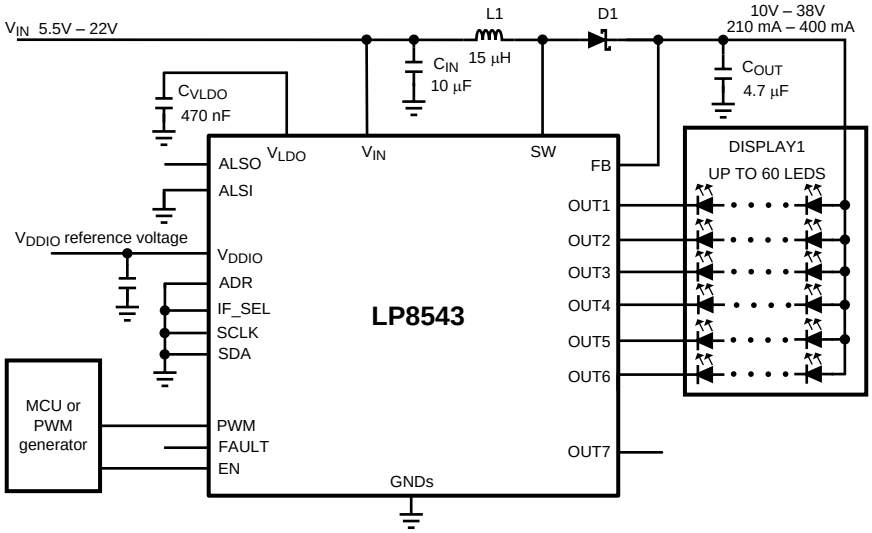
Typical Application



Typical Application, Using 7 Outputs for Display1



Typical Application, Stand-Alone Mode



Connection Diagrams

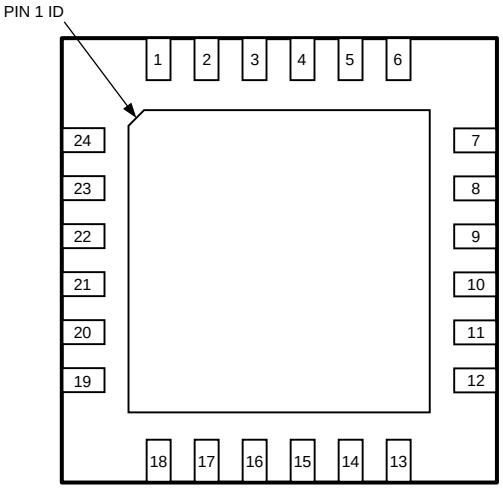


Figure 1. 24–pin WQFN Package Number RTW0024A 4.0 x 4.0 x 0.8mm, 0.5 mm pitch Bottom View

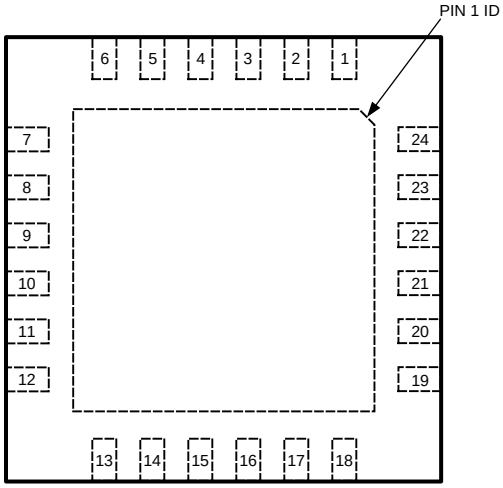


Figure 2. 24–pin WQFN Package Number RTW0024A 4.0 x 4.0 x 0.8mm, 0.5 mm pitch Top View

Pin Functions

PIN DESCRIPTIONS(1)

Pin #	Name	Type	Description
1	GND_SW	G	Boost ground
2	PWM	I	PWM dimming input. This pin must be connected to GND if not used.
3	IF_SEL	I	Serial interface mode selection: IF_SEL= Low for I^2C-compatible interface and IF_SEL=High for SMBus interface.
4	EN	I	Enable input pin

(1) **A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O: Input/Output Pin, O: Output Pin, OD: Open Drain Pin**

PIN DESCRIPTIONS(1) (continued)

Pin #	Name	Type	Description
5	ALSI	I	Ambient light sensor frequency input pin. This pin must be connected to GND if ALS is not used.
6	ALSO	O	Ambient light sensor enable output
7	FAULT	OD	Fault indication output
8	V_{DDIO}	P	Digital IO reference voltage 1.65V to 5.5V. Needed in SMBus/I^2C and stand alone mode.
9	GND_S	G	Signal ground
10	SCLK	I	Serial clock. This pin must be connected to GND if not used.
11	SDA	I/O	Serial data. This pin must be connected to GND if not used.
12	OUT1	A	Current sink output
13	OUT2	A	Current sink output
14	OUT3	A	Current sink output
15	GND_L	G	Ground for current sink outputs
16	OUT4	A	Current sink output
17	OUT5	A	Current sink output. Can be left floating if not used.
18	OUT6	A	Current sink output. Can be left floating if not used.
19	OUT7	A	Current sink output. Can be left floating if not used.
20	ADR	I	Serial interface address selection. See SMBus/I^2C Compatible Serial Bus Interface for details. This pin must be connected to GND if not used.
21	FB	A	Boost feedback input
22	V_{LDO}	A	LDO output voltage. 470 nF capacitor should be connected to this pin.
23	V_{IN}	P	Input power supply 5.5V to 22V
24	SW	A	Boost switch

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

V_{IN}	-0.3V to +24.0V
V_{DDIO}, V_{LDO}	-0.3V to +6.0V
Voltage on Logic Pins (PWM, ADR EN, IF_SEL, ALSO, ALSI)	-0.3V to +6.0V
Voltage on Logic Pins (SCLK, SDA, FAULT)	-0.3V to V_{DDIO}
V (OUT1...OUT7 SW, FB)	-0.3V to +44.0V
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T_{J-MAX})	125°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering)	(5)
ESD Rating Human Body Model: Machine Model:	(6) 2 kV OUT7: 150V All other pins : 200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pins.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(5) For detailed soldering specifications and information, please refer to Texas Instruments AN1187: *Leadless Leadframe Package (LLP).*
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1)(2)

Input Voltage Range V_{IN}	5.5 to 22.0V
V_{DDIO}	1.65 to 5V
V (OUT1...OUT7, SW, FB)	0 to 40V
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range (3)	−40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), RTW Package (1)	35 - 50°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics (1)(2)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the full operating ambient temperature range (−40°C < T_A < +85°C). Unless otherwise specified: V_{IN} = 12.0V, V_{DDIO} = 2.8V, C_{VLDO} = 470 nF, L1 = 15 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF. (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IN}	Standby supply current	Internal LDO disabled EN=L and PWM=L			**1**	µA
	Normal mode supply current	LDO enabled, boost enabled, no current going through LED outputs		3.5		mA
f_{OSC}	Internal Oscillator Frequency Accuracy		-4 **-7**		4 **7**	%
V_{LDO}	Internal LDO Voltage		**4.5**	5.0	**5.5**	V
I_{LDO}	Internal LDO External Loading				5.0	mA

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Boost Converter Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{DS-ON}	Switch ON resistance	I_{SW} = 0.5A		0.12		Ω
V_{MAX}	Boost maximum output voltage			38		V
I_{LOAD}	Maximum Continuous Load Current	V_{IN} ≥ 12V, V_{OUT} = 38V V_{IN} = 5.5V, V_{OUT} = 38V		400 180		mA
f_{SW}	Switching Frequency	BOOST_FREQ_SEL = 0 BOOST_FREQ_SEL = 1		625 1250		kHz
V_{OV}	Over-voltage protection voltage	V_{BOOST} = 38V V_{BOOST} < 38V		V_{BOOST} + 1.6V V_{BOOST} + 4V		V
t_{PULSE}	Switch pulse minimum width	no load		50		ns
t_{DELAY}	Startup delay	EN_STANDALONE = 1, PWM input active, EN is set from low to high		2		ms
$t_{STARTUP}$	Startup time	(1)		8		ms
I_{MAX}	SW pin current limit	IMAX_SEL[1:0] = 00 IMAX_SEL[1:0] = 01 IMAX_SEL[1:0] = 10 IMAX_SEL[1:0] = 11		0.9 1.4 2.0 2.5		A

(1) Start-up time is measured from the moment boost is activated until the V_{OUT} crosses 90% of its target value.

LED Driver Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LEAKAGE}$	Leakage current	Outputs OUT1 to OUT7 (Voltage on pins 40V)	**-1**		**1**	µA
I_{MAX}	Maximum Source Current	Outputs OUT1 to OUT7		60		mA
I_{OUT}	Output current accuracy (1)	Output current set to 20 mA	-3 **-4**		3 **4**	%
I_{MATCH}	Matching OUT1-7 (1)	Output current set to 20 mA		0.8	**1.5**	%
I_{MATCH}	Matching OUT1-6 (1)	Output current set to 20 mA		0.5	**1.35**	%
PWM_{RES}	PWM output resolution	f_{PWM_OUT} ≤ 4883 Hz		10		bit
		f_{PWM_OUT} = 9766Hz		9		
		f_{PWM_OUT} = 19531Hz		8		

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1 to OUT7), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN/AVG). The largest number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts. Note that some manufacturers have different definitions in use.

LED Driver Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{LED}	Min LED Switching Frequency	PWM_FREQ[2:0] = 000b PSPWM_FREQ[1:0] = 00b, PWM_MODE = 0	-4% **-7%**	229	4% **7%**	Hz
	Max LED Switching Frequency	PWM_FREQ[2:0] = 111b, PSPWM_FREQ[1:0] = 11b, PWM_MODE = 0	-4% **-7%**	19531	4% **7%**	
V_{SAT}	Saturation voltage (2)	Output current set to 20 mA		200	270 **330**	mV
		Output current set to 60 mA		300	400 **540**	

(2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 2V.

Ambient Light Sensor Interface Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{ALS}	ALS Frequency Range		0.2		2000	kHz
	ALS Duty Cycle		40		60	%
t_{CONV}	Conversion Time			500		ms

PWM Interface Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PWM}	PWM Frequency Range		0.1		25	kHz
t_{STBY}	Turn Off Delay	PWM input low time for turn off, stand-alone mode, slope disabled		50		ms
t_{PULSE}	PWM Input Pulse Width		200			ns
PWM_{RES}	PWM input resolution	f_{PWM_IN} < 4.5 kHz		10		bit
		f_{PWM_IN} = 20 kHz		8		

Under-Voltage Protection

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{UVLO}	UVLO Threshold Voltage	UVLO_THR = 1, falling	2.55	2.70	2.94	V
		UVLO_THR = 1, rising	2.62	2.76	3.00	
		UVLO_THR = 0, falling	5.11	5.40	5.68	
		UVLO_THR = 0, rising	5.38	5.70	5.98	

Logic Interface Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Logic Input PWM						
V_{IL}	Input Low Level				**0.4**	V
V_{IH}	Input High Level		**2.2**			V
I_I	Input Current		**-1.0**		**1.0**	µA
Logic Input EN						
V_{IL}	Input Low Level				**0.4**	V
V_{IH}	Input High Level		**1.2**			V
I_I	Input Current		**-1.0**		**1.0**	µA
Logic Input SCLK, SDA, ADR, ALSI, IF_SEL						
V_{IL}	Input Low Level				**$0.2xV_{DDIO}$**	V
V_{IH}	Input High Level		**$0.8xV_{DDIO}$**			V
I_I	Input Current		**-1.0**		**1.0**	µA
Logic Outputs SDA, FAULT						
V_{OL}	Output Low Level	I_{OUT} = 3 mA (pull-up current)		0.3	**0.5**	V

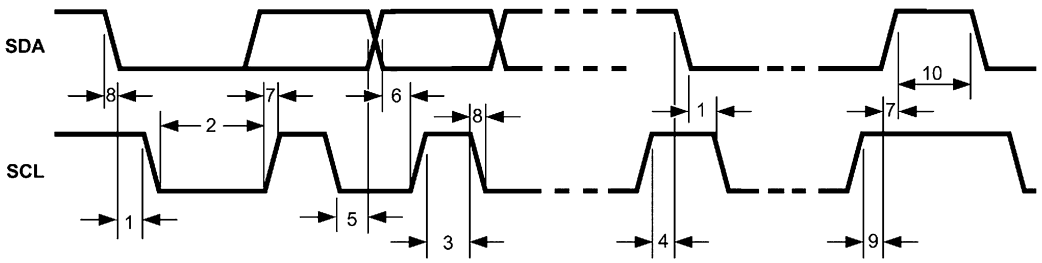
Logic Interface Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_L	Output Leakage Current	V_{OUT} = 2.8V	**-1.0**		**1.0**	µA
Logic Output ALSO						
V_{OL}	Output Low Level	I_{OUT} = 3 mA (pull-up current)		0.3	**0.5**	V
V_{OH}	Output High Level	I_{OUT} = –3 mA (pull-up current)	V_{LDO} - **0.5V**	V_{LDO} - 0.3V		V
I_L	Output Leakage Current	V_{OUT} = 2.8V	**-1.0**		**1.0**	µA

I²C Serial Bus Timing Parameters (SDA, SCLK) (1)

Symbol	Parameter	Limit		Units
		Min	Max	
f_{SCLK}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time	50		ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20+0.1C_b	300	ns
8	Fall Time of SDA and SCL	15+0.1C_b	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line Load of 1 pF corresponds to 1 ns.	10	200	ns

(1) ensured by design. V_{DDIO} = 1.65V to 5.5V.



SMBus Timing Parameters (SDA, SCLK) (1)(2)

Symbol	Parameter	Limit		Units
		Min	Max	
f_{SCLK}	Clock Frequency	10	100	kHz
1	Hold Time (repeated) START Condition	4.0		µs
2	Clock Low Time	4.7		µs
3	Clock High Time	4.0	50	µs
4	Setup Time for a Repeated START Condition	4.7		µs
5	Data Hold Time	300		ns
6	Data Setup Time	250		ns
7	Rise Time of SDA and SCL		1000	ns
8	Fall Time of SDA and SCL		300	ns
9	Set-up Time for STOP condition	4.0		µs

(1) ensured by design. V_{DDIO} = 1.65V to 5.5V.
(2) The switching characteristics of the LP8543 fully meets or exceeds the published System Management Bus (SMBus) Specification Version 2.0.

SMBus Timing Parameters (SDA, SCLK) (1)(2) (continued)

10	Bus Free Time between a STOP and a START Condition	4.7		µs
C_b	Capacitive Load for Each Bus Line Load of 1 pF corresponds to 1 ns.	10	200	ns

Typical Performance Characteristics

Unless otherwise specified: V_{BATT} = 12.0V, C_{VLDO} = 470 nF, L1 = 15 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF

LED Drive Efficiency, f_{LED} = 19.5 kHz, PSPWM enabled

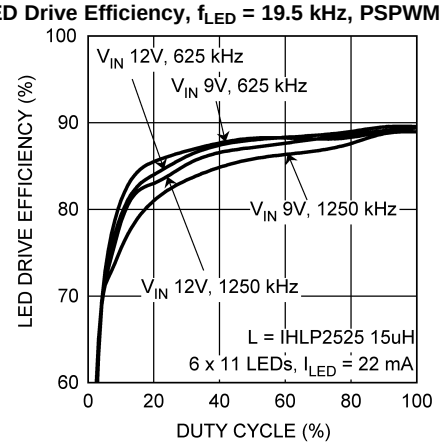


Figure 3.

Boost Converter Efficiency

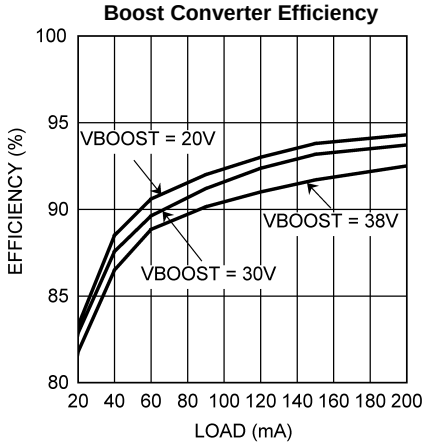


Figure 4.

Boost Maximum Output Current at V_{BOOST} = 38V

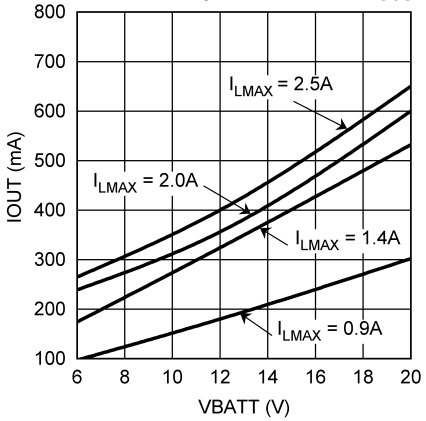


Figure 5.

Battery Current

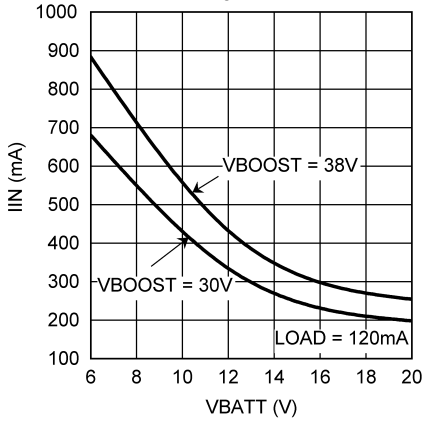


Figure 6.

Boost Converter Typical Waveforms
V_{BOOST} = 38V, I_{OUT} = 50 mA

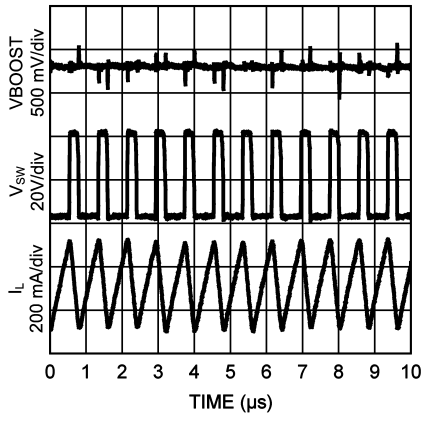


Figure 7.

Boost Line Transient Response

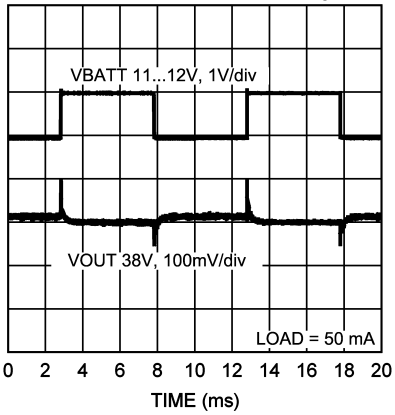


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{BATT} = 12.0V, C_{VLDO} = 470 nF, L1 = 15 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF

Typical Waveforms in PSPWM Mode, f_{LED} = 4.2 kHz

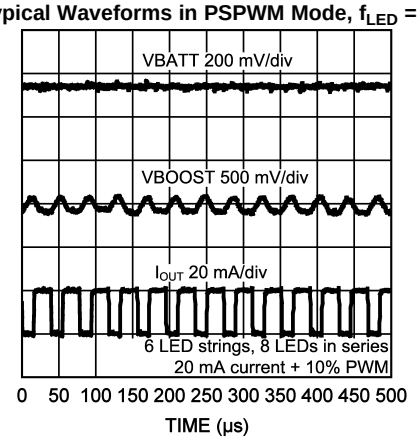


Figure 9.

Typical Waveforms in Normal PWM Mode, f_{LED} = 4.2 kHz

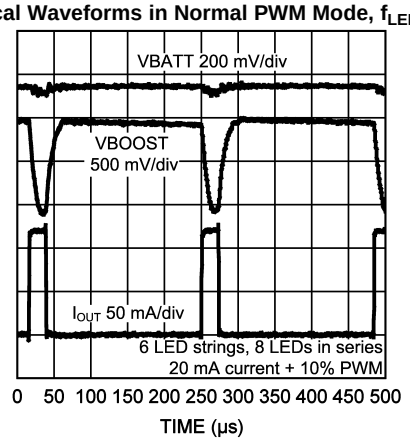


Figure 10.

FUNCTIONAL OVERVIEW

The LP8543 is a high-voltage LED driver for medium-sized LCD backlight applications. It includes 38V boost converter, 7 current sink outputs for the backlight and an interface for digital Ambient Light Sensor (ALS). LP8543 can be controlled through SMBus or I^2C serial interface or PWM input. Light-to-frequency type ambient light sensor can be directly connected to LP8543 and the sensor response vs. LED brightness curve can be programmed in the on-chip EEPROM memory.

LP8543 differs from conventional LED drivers due to following advanced features.

1. **PHASE SHIFT PWM FEATURE**
   - LP8543 supports a state-of-the-art feature called Phase Shift PWM (PSPWM). Key advantages of the PSPWM is improved power efficiency when there is variation in the forward voltages amongst the LED strings. Due to an unmatched LED V_F there is a random difference in each string forward voltage. PSPWM optimizes the boost converter output voltage by turning off LED outputs periodically. The lower the brightness, the more strings can be simultaneously off. When the strings with higher forward voltages are turned off, the boost voltage is automatically lowered thereby improving efficiency. The second benefit of PSPWM control is that it will make the boost and battery loading more constant. In other words, the peak current needed from the battery is greatly reduced beause not all LED outputs are simultaneously on.
2. **PROGRAMMABLE OUTPUT STRINGS**
   - Programmability helps display manufacturers to fit LP8543 to several sizes of displays. The number of output strings in use is a parameter in EEPROM and can be fixed during the manufacturing process of displays. Based on the configuration the device will automatically adjust the phase Shift PWM function for a given number of output strings. LP8543 supports of minimum of 4 strings and a maximum of 7 strings. In this datasheet , strings 1 through 6 are classified as Display1, and string 7 is classified as Display2.
3. **INDIVIDUALLY CONTROLLED LED STRING FOR BACKSIDE DISPLAY BACKLIGHT**
   - OUT7 string can be either used for main backlight or for possible back side sub display. Separate control allows dimming through I^2C interface and reduces extra components or ICs in display module.
4. **LED FAULT DETECTION**
   - LED fault detection enables higher yield in display manufacturing process and also makes possible to monitor backlight faults during normal operation. Fault test detects both open circuit (string with unconnected or open circuit LED) and short circuit of 2 or more shorted LEDs. Single LED short can also be detected if the amount of LEDs per string and/or the V_F variation are sufficiently low. Threshold levels are EEPROM programmable. Fault information is available in the status register and in the open drain active low FAULT output.
5. **LED PWM TEMPERATURE REGULATION**
   - This feature will decrease the effect of high temperature LED lifetime reduction. LP8543 reduces output PWM of the LEDs at high temperatures and prevents overheating of the device and LEDs. Temperature threshold can be programmed to EEPROM.
6. **AMBIENT LIGHT SENSOR INTERFACE WITH USER PROGRAMMABLE CONTROL CURVE**
   - Ambient light sensing reduces power consumption and it allows natural backlight in any ambient light condition. Programmability allows display manufacturer and even end user to control sensor to backlight control loop. By integrating this feature LP8543 reduces external component count, wiring and complexity of the design. LP8543 supports digital light-to-frequency type sensors. Prescaler and compensation curve can be programmed in to the EEPROM.

Brightness Control Methods

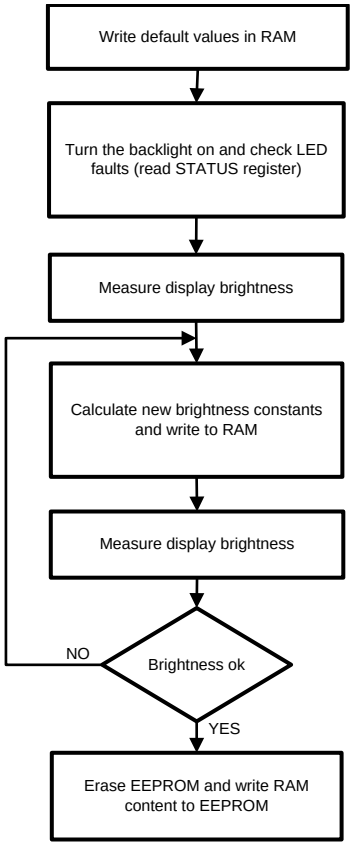
1. **CURRENT CONTROL**
   - The 8-bit LED current default value is read from EEPROM when the chip is activated. Current value can be used for fine tuning the backlight brightness between panels. This current setting can be overridden by a register write from the serial interface. Current control range is from 0 to 60 mA with 0.23 mA step. This fine grained current control gives backlight manufacturer possibility to adapt different LED bins in one product and maintain the full PWM control range. There are separate controls for both Display1 and Display2.
2. **INTERNAL PWM CONTROL**
   - The basic brightness control is register based 8-bit PWM control. There is a piecewise linear transfer curve from register value to LED PWM value and the curve coefficients are stored in the EEPROM. This makes possible to calibrate the 100% brightness and the dimming behavior. LED PWM frequency is selectable from 229 Hz to 19.5 kHz. In addition PSPWM can be used.
3. **EXTERNAL PWM CONTROL**
   - An external PWM signal can be used to set the brightness of the display. LP8543 measures the duty cycle of this input signal to calculate the output PWM value. Input PWM frequency can vary from 100 Hz to 25 kHz. Based on the configuration selected, this external PWM control can linearly reduce the brightness from the value set by the Brightness Register. This external PWM control can also be used as the only control for LP8543. In this case, when PWM input is permanently low, the chip is turned off. When there is signal in PWM input, the chip turns on and adjusts brightness according to PWM signal duty cycle. In addition, PSPWM can also be used in this mode.
4. **AMBIENT LIGHT SENSING**
   - External ambient light sensor can be used for controlling the brightness of the LEDs. Light-to- Frequency type light sensor can be connected to ALSI input in LP8543 for ambient light compensation. Transfer curve coefficients for response setting are stored in EEPROM. LP8543 has an enable output, ALSO to activate the light sensor (active high/low, programmed to EEPROM). Light sensor supply voltage can be taken from the 5V regulator in LP8543. Ambient light control is possible for Display1 (4-7 outputs).

Calibration

LP8543 has an internal EEPROM to store different control parameters which allows calibrating the backlight brightness at various brightness settings so that every display has exactly the same brightness and several LP8543 circuits can be used in the same display if needed.

Programming the EEPROM is easy. User needs to write the data in the shadow RAM memory and give the EEPROM write command. On-chip boost converter produces the needed erase and program voltages, no external voltages other than normal input voltage are required.

Calibration in backlight or display production can be done according to the flowchart below



Energy Efficiency

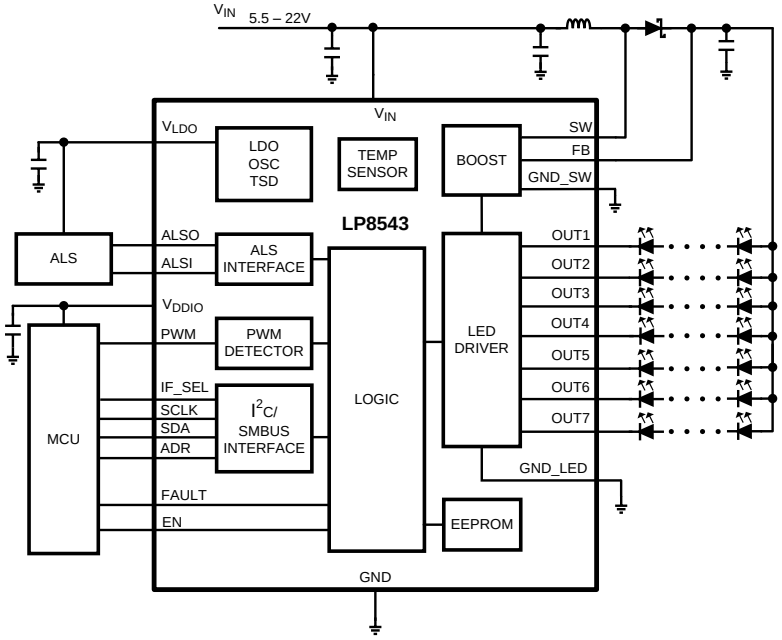
The voltage across the LED drivers is constantly monitored and boost voltage is adjusted to minimum sufficient voltage when adaptive boost mode is selected. Inductive boost converter maintains good efficiency over wide input and output operating voltage ranges. The boost output has over voltage protection limiting the maximum output to 38V. The boost is internally compensated and the output voltage can be either controlled with 5-bit register value or automatically adjusted based on the LED driver voltages.

LP8543 has an internal 5V LDO with low current consumption. The 5V LDO can supply 5 mA current for external devices like ALS (Ambient Light Sensor). LDO is switched off in standby mode. The internal LDO is used for powering internal blocks as well; therefore the 470 nF C_{VLDO} capacitor must be used even if external load is not used.

Serial Communication

LP8543 supports two serial protocols: SMBus and I^2C. IF_SEL input is used to determine the selection. SMBus interface is selected when IF_SEL is high and I^2C is selected when IF_SEL is low.

Block Diagram



LED Driver Control

Basic Operation

Principle of the LED driver control is shown in the following figure:

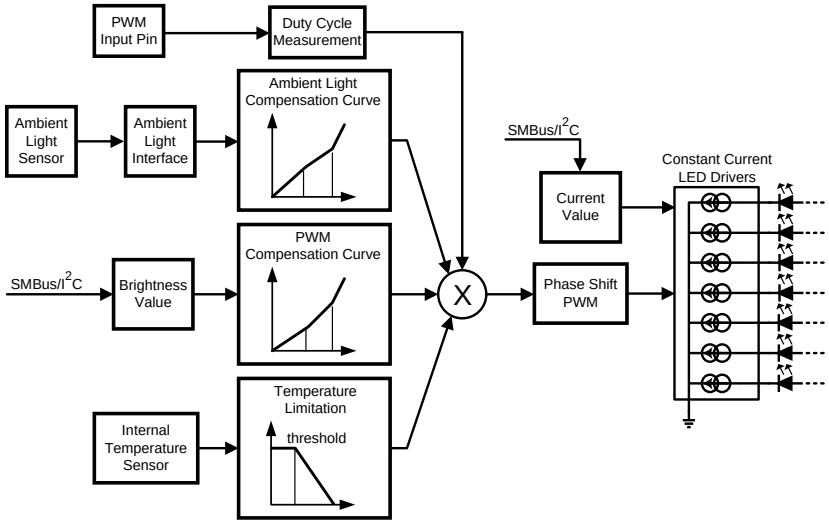


Figure 11. Principle of the LED Control Methods

LP8543 is designed to be flexible to support backlighting needs for the main display as well as lighting needs of a sub display (also for e.g. keyboard lighting or status LED) when required. In addition, a variety of PWM options are supported to drive the backlight LED strings. Various configurations that are supported using a set of programmable internal registers and EEPROM are described below. Both the register map and the EEPROM memory map are listed at the end of this datasheet.

Output Grouping

LP8543 features a total of 7 strings (OUT1-OUT7), which can be arranged into 2 groups (Display1 and Display2). Display1 refers to backlighting for main display and Display2 refers to lighting for a sub display. Number of outputs used for Display1 can be defined using EEPROM register bits, as shown in the table below. LP8543 supports a minimum of 4 strings and a maximum of 7 strings for Display1. Outputs must be used in order starting from OUT1. Unused outputs can be left open. When needed OUT7 can be configured for Display2 and it has its own current and PWM control registers for independent control. EEPROM default factory setting is 6 outputs for Display1 and OUT7 for Display2.

Table 1. Output Configurations

OUTPUT_CONF[1:0]	Outputs for Display1	Outputs for Display2
00	OUT1-OUT4	OUT7
01	OUT1-OUT5	OUT7
10	OUT1-OUT6	OUT7
11	OUT1-OUT7	-

LED Current Control

Two 8-bit EEPROM registers, **Display1 current** and **Display2 current** (addresses B0H and B1H) hold the default LED string current for the Display1 and Display2 groups respectively. The default values are read from EEPROM when the chip is activated. When required the LED current can be adjusted also in the registers **Display1** and **Display2 current** (addresses 05H and 06H). Use of this register is enabled by setting bit 1 in **Config2** register. Default value for <CURRENT SEL> bit is 0, which means that current values in EEPROM are used. Current control range is linear from 0 to 60 A with 0.23 mA step. Factory default current for Display1 and Display2 is 20 mA.

LED On/Off Control

LED strings can be activated with 100% PWM by writing <DRV[7:0]> bits high. All these controls are in **Direct control** register.

PWM Control Selection

PWM control of the LED strings can be established through 4 combinations of user configurable options as shown in the table below. <PM_MD> and <PWM_SEL> bits are part of **Config1** Register.

Default setting is external PWM input signal. Each of the option is explained in the following sections.

Table 2. PWM Control Selection

PWM_MD	PWM_SEL	PWM source
1	1	PWM input (Direct control)
0	1	PWM input pin (Duty cycle based), default
1	0	Brightness register
0	0	PWM input pin (Duty cycle based) and Brightness register

In addition Ambient light sensor (when used) and on-chip temperature regulation also influence the output PWM control. This is described later.

A. Direct PWM Input Control

Display1 group can be directly controlled with external PWM signal (bypassing all the PWM logic) by setting <PWM_MD> and <PWM_SEL> bits high. Outputs will be active when the PWM input pin is high, and when the input is low the outputs will be off. Input PWM frequency can vary from 100 Hz to 25 kHz. Display2 is not controlled with this signal.

Note: In this mode, Ambient Light sensor and PSPWM scheme do not influence the output PWM.

B. PWM Input Pin Control (Duty Cycle-based)

An external PWM signal can be used to set the brightness of the Display1 group. LP8543 measures the duty cycle of this input signal to calculate the output PWM value. Input PWM frequency can vary from 100 Hz to 25 kHz. Output PWM frequency is set by EEPROM registers.

Note: In this mode, Ambient Light compensation and PSPWM scheme can be also used.

C. PWM Control Using Brightness Register

Generation of PWM for LED strings can be based on Brightness register value. For Display1 group, this scheme is enabled when <PWM_SEL> bit is set to 0 and <PWM_MD> is set to 1. Display2 group has the brightness register control enabled by default. Two separate 8-bit registers **Displ1 brightness** and **Displ2 brightness** store the brightness values for Display1 and Display2 respectively. For Display1, this 8-bit brightness value from the register is converted to 10-bit LED PWM value using a three-part piecewise linear transfer curve as shown below. This makes it possible to calibrate the 100% brightness and the dimming behavior. The curve coefficients are stored in the EEPROM and are user programmable if needed. The LED PWM frequency is set by EEPROM register.

Note: In this mode, Ambient Light compensation and PSPWM scheme can be also used.

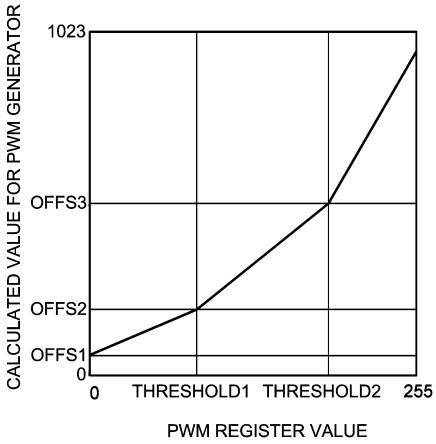


Figure 12. Three-Segment Transfer Curve Example

D. PWM Pin and Register Control

In this mode, PWM control pin can linearly reduce the brightness of Display1 from the value set by the Brightness Register and Ambient Light sensor. Same controls can be used as in brightness register based PWM control. Output PWM frequency is set by EEPROM registers. This mode is compatible with Intel DPST (Display Power Saving Technology).

Stand Alone Mode

LP8543 can be set to operate in stand alone mode, where LP8543 operates without I^2C / SMBus and EN and PWM input pins are the only controls for the device. To enable stand-alone mode, EEPROM bit <EN_STANDALONE> must be set to 1 in register B4h. In this mode PWM pin sets the brightness and with EN pin the backlight can be turned on. When PWM or EN input pin is permanently low, the chip is turned off. Turn off time is typically 50 ms. When there is signal in PWM input and EN is high, the chip turns on and adjusts brightness according to PWM signal duty cycle. All settings needed for operation like LED current, number of LEDs etc. are obtained from EEPROM. If only one signal control is needed, the EN and PWM pin can be tied together and PWM signal can be connected to this. Stand alone mode is useful in applications where I^2C or SMBus control is not possible or available to use.

Ambient Light Compensation

LP8543 supports an external ambient light sensor to control the backlight brightness (Display1) and its usage is controlled with two bits in the **Config2** register, namely <ALSO_EN> and <ALSO_CALC_EN>. <ALSO_EN> bit controls enabling/disabling of the sensor itself, and <ALSO_CALC_EN> bit determines whether the ALS measurement data will be used by an external processor (Host) or by LP8543's internal control logic to control the brightness.

If <ALSO_EN> bit is 1 the ALSO output pin is set high and the input frequency measuring is enabled. Frequency is measured for 500 ms, and the result is divided with 10-bit prescaler (defined in EEPROM), resulting in a 10-bit value. This 10-bit result can be read from **ALS MSB** and **ALS LSB** registers. **ALS MSB** register must be read first followed by **ALS LSB** register. If ALS_CALC_EN bit is set to 0, then the measurement data is not used by LP8543's internal PWM logic but left for the host to adjust the brightness.

On the other hand if the ALS_CALC_EN bit is set to 1, ALS measurement result will control backlight brightness in all but direct external PWM control mode. The measured ALS value is converted to PWM value using a three segment linear curve. The calculated PWM value is used as a multiplier for the LED PWM value obtained from brightness register, PWM input pin or combination of both depending which mode is selected. The conversion curve parameters are stored in EEPROM memory. Conversion curve is similar as in PWM control.

Smoothing filter is used to prevent rapid changes. Smoothing filter has EEPROM programmable slopes from 0 to 2s. The slope defines the time it takes to change brightness from one value to next. Slope control can be also used to smooth changes to backlight brightness caused by other PWM controls (brightness register or external PWM input).

Table 3. Slope Selections

SLOPE_SEL[1:0]	Slope
00	130 ms
01	0.5s
10	1.0s
11	2s

ALSO output can be used as GPO if not used for ALS control. ALSO pin state is then controlled with <ALSO_EN> register bit.

Phase Shift PWM (PSPWM)

PSPWM improves the system efficiency by optimizing the boost converter voltage on a cycle by cycle basis instead of maintaining a constant voltage based on the highest V_F string. PSPWM scheme can be used for Display1 group. Phase shift PWM control principle is illustrated in the picture below using an example of 6 string implementation and 41.7% brightness setting. In a 6-string implementation, each of the string supports a maximum of 16.67% (1/6) of the total backlight brightness. The brightness set value in this example is 41.7%. Hence two strings are fully on (2 x 16.67% = 33.33%) and one string is 50% on (0.5 x 16.67% = 8.34%). This pattern of two 100% and one 50% strings is then cycled through all 6 output strings. After 6 cycles the brightness value is changed to 83.33%, resulting in 5 LEDs fully on (5 x 16.67%).

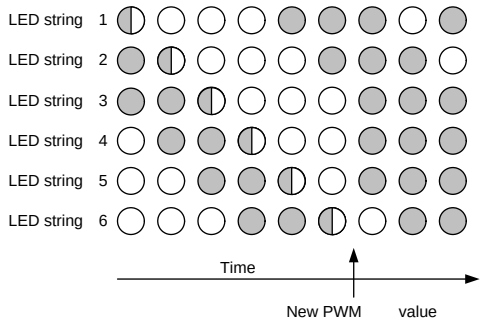


Figure 13. Principle of the PSPWM Operation

Phase shift frequency can either be the same as the PWM frequency or a lower frequency can be selected with <PHASE_SHIFT_FREQ[1:0]> EEPROM bits. At highest 19.5 kHz PSPWM frequency, the boost will use a constant voltage based on the highest V_F string because of timing constraints of the high PWM frequency. PSPWM is enabled by default, but it can be disabled by setting <DISABLE_PS> EEPROM bit to 1.

Two PSPWM modes are available. PSPWM mode is selected with <PWM_MODE> EEPROM bit. Difference between modes is in the PWM frequencies available. PWM and PSPWM frequency settings are shown in Table 4.

Number of strings simultaneously on in PSPWM mode with different PWM values and different output configurations is shown in the following diagram.

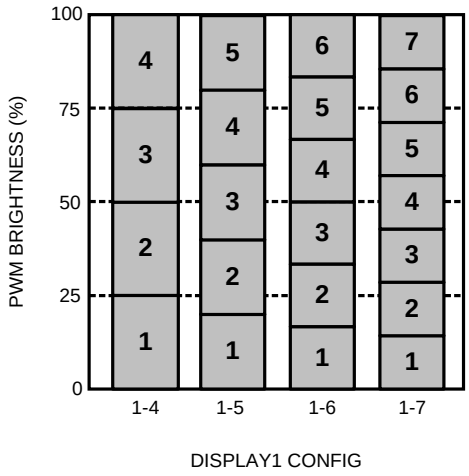


Figure 14. Number of Simultaneously Active Strings

Table 4. PSPWM Frequency Selection in EEPROM Registers (N = number of strings used)

	PWM_MODE = 0			PWM_MODE = 1	
PWM_FREQ[2:0] + PSPWM_FREQ[1:0]	PWM Frequency (Hz)	Shift Frequency (Hz)	Output Frequency (Hz)	Output Frequency (Hz)	Shift Frequency (Hz)
00000	992	992	992/N	229	229 x N
00001	992	496	496/N	305	305 x N
00010	992	248	248/N	381	381 x N
00011	992	124	124/N	458	458 x N
00100	1526	1526	1526/N	534	534 x N
00101	1526	763	763/N	610	610 x N
00110	1526	382	382/N	687	687 x N
00111	1526	191	191/N	763	763 x N
01000	1983	1983	1983/N	839	839 x N
01001	1983	993	993/N	916	916 x N
01010	1983	496	496/N	992	992 x N
01011	1983	248	248/N	1068	1068 x N
01100	2441	2441	2441/N	1144	1144 x N
01101	2441	1221	1221/N	1221	1221 x N
01110	2441	610	610/N	1297	1297 x N
01111	2441	305	305/N	1373	1373 x N
10000	2974	2974	2974/N	1450	1450 x N
10001	2974	1487	1487/N	1526	1526 x N
10010	2974	744	744/N	1602	1602 x N
10011	2974	372	372/N	1678	1678 x N

Table 4. PSPWM Frequency Selection in EEPROM Registers (N = number of strings used) (continued)

	PWM_MODE = 0			PWM_MODE = 1	
PWM_FREQ[2:0] + PSPWM_FREQ[1:0]	PWM Frequency (Hz)	Shift Frequency (Hz)	Output Frequency (Hz)	Output Frequency (Hz)	Shift Frequency (Hz)
10100	3965	3965	3965/N	1755	1755 x N
10101	3965	1983	1983/N	1831	1831 x N
10110	3965	991	991/N	1908	1908 x N
10111	3965	496	496/N	1983	1983 x N
11000	4883	4883	4883/N	2060	2060 x N
11001	4883	2441	2441/N	2671	2671 x N
11010	4883	1221	1221/N	3203	3203 x N
11011	4883	610	610/N	3737	3737 x N
11100	19531	19531	19531/N	4270	4270 x N
11101	19531	9766	9766/N	4808	4808 x N
11110	19531	4883	4883/N	9766	9766 x N
11111	19531	2441	2441/N	19531	19531 x N

Table 5. PWM Frequencies with Phase Shift Disabled

	PWM_MODE = 0	PWM_MODE = 1
PWM_FREQ[2:0] + PSPWM_FREQ[1:0]	PWM Frequency (Hz)	Output Frequency (Hz)
00000	992	229
00001	992	305
00010	992	381
00011	992	458
00100	1526	534
00101	1526	610
00110	1526	687
00111	1526	763
01000	1983	839
01001	1983	916
01010	1983	992
01011	1983	1068
01100	2441	1144
01101	2441	1221
01110	2441	1297
01111	2441	1373
10000	2974	1450
10001	2974	1526
10010	2974	1602
10011	2974	1678
10100	3965	1755
10101	3965	1831
10110	3965	1908
10111	3965	1983
11000	4883	2060
11001	4883	2671
11010	4883	3203
11011	4883	3737
11100	19531	4270

Table 5. PWM Frequencies with Phase Shift Disabled (continued)

	PWM_MODE = 0	PWM_MODE = 1
PWM_FREQ[2:0] + PSPWM_FREQ[1:0]	PWM Frequency (Hz)	Output Frequency (Hz)
11101	19531	4808
11110	19531	9766
11111	19531	19531

Device Thermal Regulation

LP8543 has an internal temperature sensor which can be used to measure the junction temperature of the device and protect the device from overheating. During thermal regulation, LED PWM is reduced by 4% of full scale per °C whenever the temperature threshold is reached. I.e., with 100% PWM value the PWM goes to 0% 25°C above threshold temperature. With lower PWM start value 0% is reached earlier. Temperature regulation is enabled automatically when the chip is enabled. 11-bit temperature value can be read from **Temp MSB** and **Temp LSB** registers, MSB should be read first. Temperature limit can be programmed in EEPROM as shown in the following table.

Table 6. Over Temperature Limit Settings

TEMP_LIM[1:0]	Over Temperature Limit (ºC)
00	100
01	110
10	120
11	130

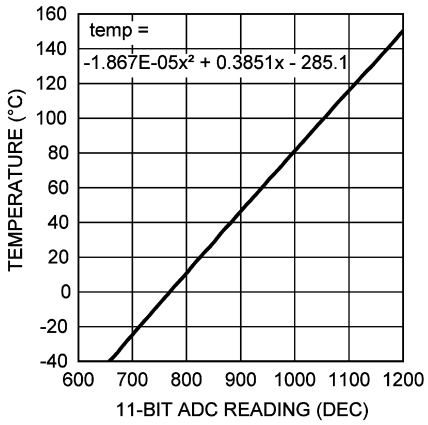


Figure 15. Internal Temperature Sensor Readings

EEPROM

EEPROM memory stores various parameters for chip control. The 256 bit EEPROM memory is organized as 32 x 8 bits. The EEPROM structure consists of a SRAM front end and the Non-volatile memory (NVM). SRAM data can be read and written through the serial interface. To erase and write NVM, separate commands need to be sent. Erase and Write voltages are generated on-chip, no other voltages than normal input voltage are required. A complete EEPROM memory map is shown in the chapter LP8543 EEPROM Memory Map.

EEPROM structure is described in the figure below. User has read and write access to SRAM part of the EEPROM directly through I^2C / SMBus when PWM calculation is not enabled; i.e., <BL_CTL> = 0 and external PWM pin = low. To see whether the EEPROM can be accessed user can read <EE_READY> bit. ALS and brightness coefficient curves (address A0h – Afh) and empty EEPROM cells (address B4h – BBh) have only NVM and SRAM. Other EEPROM cells have also EEPROM registers. For the cells which have also EEPROM registers, the changes made to SRAM does not take effect until update command is sent. This is done by setting EE_UPDATE and EE_READ bits to 1. After an update, these bits must be set back to 0. For EEPROM bits which do not have registers, changes take effect immediately.

At startup the values in NVM part of the EEPROM is loaded to SRAM and to EEPROM registers. User can also load values from NVM to SRAM and EEPROM registers by writing EE_READ to 1.

To write SRAM values to NVM user needs to first erase EEPROM and the program it. This is done by first writing EE_ERASE to 1 and then 0. At this point NVM is erased. To burn new values to NVM, user needs to write EE_PROG to 1 and then 0. The LP8543 generates the needed erase and write voltage from boost output voltage.

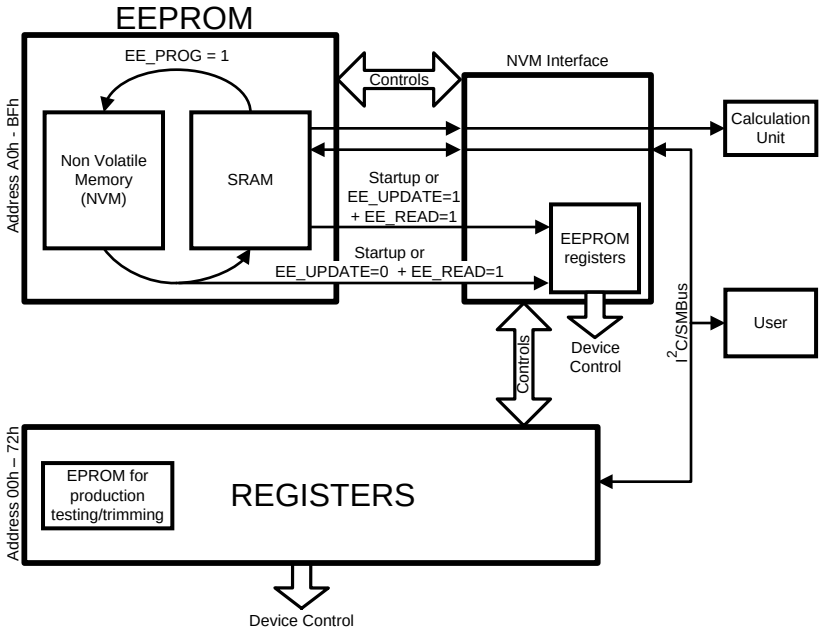


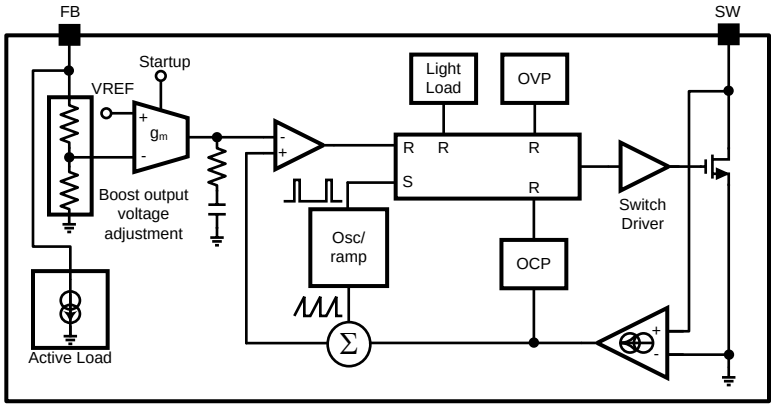
Figure 16. EEPROM Memory Control and Usage Principle

Boost Converter

Operation

The LP8543 boost DC/DC converter generates a 10…38V supply voltage for the LEDs from 5.5…22V input voltage. The output voltage is controlled with a 5-bit register in 1V steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The topology of the magnetic boost converter is called CPM (current programmed mode) control, where the inductor current is measured and controlled with the feedback. Switching frequency is selectable between 625 kHz and 1.25 MHz with EEPROM bit <BOOST_FREQ>. Boost is enabled with <EN_BOOST> bit.

User can program the output voltage of the boost converter or use adaptive mode where boost output voltage is adjusted automatically based on LED driver saturation. In adaptive mode the boost output voltage control steps are 0.25V. Enabling the adaptive mode is done with <BOOST_AUTO> bit in **Boost Control** register. If boost is started with adaptive mode enabled (default) then the initial voltage value is defined with EEPROM bits at address 29H in order to eliminate long iteration time when the chip is started. If adaptive mode is enabled after boost startup, then the boost will use register 07H values as initial voltage value. The output voltage control changes the resistor divider in the feedback loop. The following figure shows the boost topology with the protection circuitry.



Protection

Four different protection schemes are implemented:

1. Over-voltage protection limit changes dynamically based on output voltage setting
   - Over-voltage protection limit changes dynamically based on output voltage setting.
   - Keeps the output below breakdown voltage.
   - Prevents boost operation if battery voltage is much higher than desired output.
2. SW current limiting, limits the maximum inductor current.
3. Over-current protection enables fault flag and shuts down boost converter in over-current condition.
4. Duty cycle limiting.

Manual Output Voltage Control

User can control the boost output voltage with **Boost_output** (07H) register when adaptive mode is disabled; i.e., <BOOST_AUTO> = 0.

Table 7. Boost Output Voltage Controls

VPROG[4:0]		Voltage (typical)
Bin	Dec	Volts
00000	0	10
00001	1	11
00010	2	12
00011	3	13
00100	4	14
...	...	...
11011	27	37
11100	28	38

Adaptive Boost Control

Adaptive boost control function adjusts the boost voltage to the minimum sufficient voltage for proper LED driver operation. When PSPWM is used the output voltage can be adjusted for every phase shift step separately except in 19.5 kHz PSPWM mode due to timing constraints. To enable PSPWM to each phase, the <BOOST_MODE> EEPROM bit must be 0. This enables power saving when strings have mismatch in V_F voltages. The correct voltage for each string is stored and used in predicting when the boost has to start increasing voltage for the next step. The boost setup time can be defined with two EEPROM bits. Principle of the boost voltage adjustment with PSPWM is illustrated below. If higher PWM value is used then more strings are on at the same time, and voltage is adjusted based on highest V_F on simultaneously active strings.

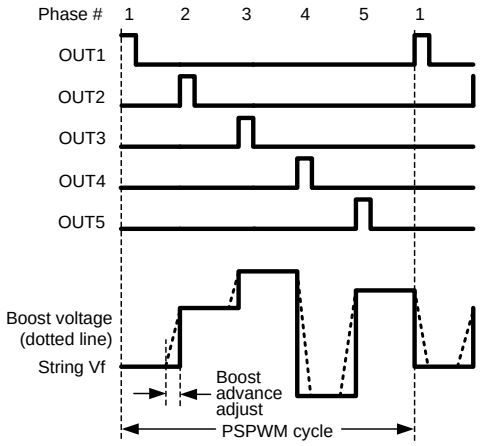


Figure 17. Boost Adaptive Voltage Control for 5–String PSPWM

When adaptive boost mode is selected the voltages across the LED drivers are constantly monitored. There are three voltage thresholds used, Low, Mid and High. Low and High thresholds are adjustable with 3 EEPROM bits. Low threshold range is from 0.5V to 2.25V and High threshold range is from 3 to 10V. Mid threshold is set 0.5V above Low threshold. Threshold levels are listed in the table below. Adjustability is provided to enable adaptation to different conditions. If there is a lot of variation between LED string V_F, then higher threshold levels must be used to avoid false fault indications. If there is low variation between LED string V_F, then lower thresholds are recommended to maintain good efficiency. Fault detection chapter describes how these thresholds are used also for fault detection.

Table 8. LED Voltage Comparator Thresholds

EEPROM bits	Threshold (V)		
LED_FAULT_THR[5:3] (HIGH comparator) DRV_HEADR_CTRL[2:0] (LOW comparator)	Low	High	Mid
000	0.50	3	Low + 0.5V
001	0.75	4	
010	1.00	5	
011	1.25	6	
100	1.50	7	
101	1.75	8	
110	2.00	9	
111	2.25	10	

If only one string is on at a time (Brightness value lower than 100% divided by number of strings) the voltage for each string is adjusted so that the voltage across the driver will fall between Low and Mid threshold. If more strings are on at the same time (high PWM value, or PSPWM not used) the situation looks like in the following diagram. In this diagram 6 outputs are on at the same time. In normal operation voltages across all LED driver outputs are between high and low threshold.

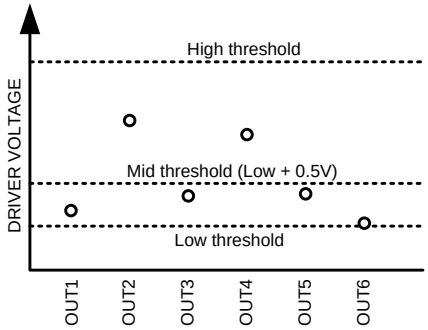


Figure 18. Normal Operation, High PWM Value

If one LED driver voltage is below Low, boost voltage will be increased. This is seen in the following figure.

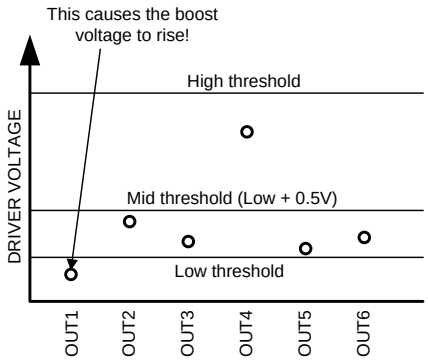


Figure 19. Boost voltage too Low

If all driver voltages are above Mid threshold (or any of the voltages in PSPWM adaptation mode and with low PWM value), boost voltage will be lowered. Decision is always based on number of strings active at the same time. In the illustrations 6 outputs are active, which basically means close to 100% PWM value with PSPWM.

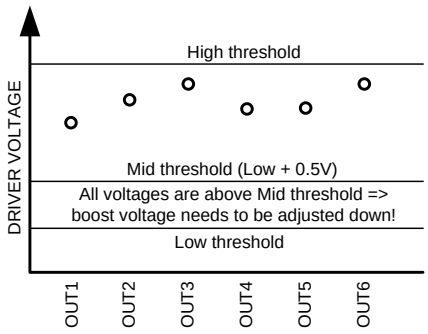


Figure 20. Boost voltage too High

Fault Detection

LP8543 has fault detection for LED fault, low-battery voltage, overcurrent and thermal shutdown. The open drain output pin (FAULT) can be used to indicate occurred fault. The cause for the fault can be read from status register. Refreshing the <BL_CTL> bit high will reset the fault register and fault pin state.

Led Fault Detection

There are two methods of detecting the LED fault. First method is based on measuring the voltage on LED driver pins (analog fault detection) and another is based on adaptive boost voltage hopping between strings (digital fault detection). The used fault detection mode is selected in EEPROM as well as the threshold levels. <FAULT_SEL[1:0]> bits selects the used mode as follows:

Table 9. LED Fault Mode Selection

FAULT_SEL[1:0]	Fault mode
00	No fault detection
01	Analog fault detection based on LED driver voltage
10	Digital fault detection based on boost voltage hopping
11	Both analog and digital fault detection

Two fault detection methods are used to detect faults in different conditions. Analog detection works better with high PWM values (in PSPWM mode) where many strings are active at a same time. It does not work when only one string is active at a time, because it is based on comparing driver voltages on strings active simultaneously. Digital fault detection is used to complement this case.

Digital fault detection works better with low PWM values, where not all strings are on at the same time. Digital short detection works only with cases where one string is active at the same time.

Analog Fault Detection

When analog fault detection mode is selected, the voltages across the LED drivers are constantly monitored. The same threshold levels (Low, Mid and High) are used for fault detection to adjust the boost voltage.

If one of the LED strings has an open fault (LED driver output pin has no contact to LED string), the output pin voltage drops to 0V. When this happens the boost voltage will be adjusted higher to get enough headroom, but at some point the voltage for all other strings will rise over the high threshold. In this case the LP8543 detects open fault, and adjusts the boost voltage based on other LED strings needs, i.e., the faulty LED string voltage is not used anymore for adjusting boost output voltage. If the LED driver output pin is shorted to GND the fault detection works exactly the same. This situation with 6 LEDs active at the same time is illustrated in the following diagram:

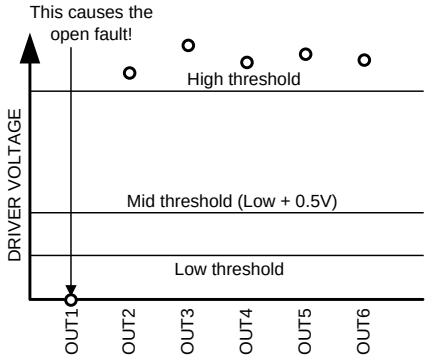


Figure 21. Open Fault

If one or more LEDs are shorted, this causes the voltage to rise in this LED driver output pin above the high threshold. This causes short fault detection as seen in the following figure:

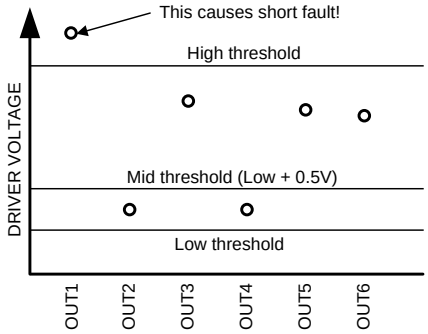


Figure 22. Short Fault

Digital Fault Detection

With digital fault detection the voltage hopping between LED strings is monitored in PSPWM mode. In normal PWM mode or with high PWM values with PSPWM mode this does not apply.

If there's open in one of the LED strings, the LED driver output pin will drop to 0V. When this happens the boost will try to increase the voltage to get enough headroom for the driver. When the voltage for one string reaches maximum voltage (38V) and the difference between consecutive LED strings is higher than set threshold level an open LED fault is detected. If all voltages are close to 38V then the threshold condition is not met and no fault is detected. If the LED output is shorted to GND it will be detected same way. Open fault detection is seen in the following figure:

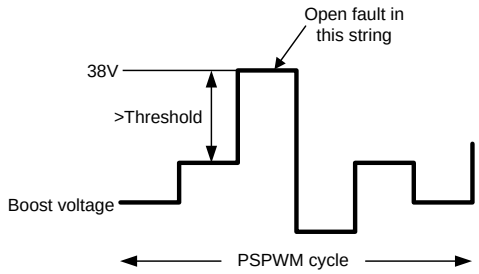


Figure 23. Digital Open Fault Detection

If there is one or more LEDs shorted in one string, the boost will drop the voltage for this string. When the difference between consecutive LED strings is higher than set threshold level a short LED fault is detected. This is described in the following figure:

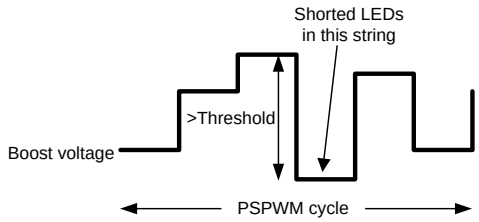


Figure 24. Digital Short Fault Detection

Threshold level is programmed to EEPROM as shown in the following table. Threshold level adjustability is provided to allow adaptation to different LED V_F used in the application.

Table 10. Digital LED Fault Detection Thresholds

DIG_COMP[1:0]	Threshold Voltage (V)
00	3
01	5
10	7
11	9

When Fault is detected the FAULT pin will be pulled down (open drain output), and corresponding status register bit is set. To clear the fault user must read the status register.

Note: LED fault output signal is generated only once for certain fault type. If, for example, open fault occurs, new open fault does not cause the FAULT pin to be pulled down uless chip is reset by setting EN pin low and high again. The faults will be seen in the register however. If LED fault is detected, the string which created the fault is no longer used for adjusting the boost voltage. Otherwise the LP8543 operates as normally.

Note: Due to the nature of fault detection it is possible to generate false faults during startup etc. conditions. Therefore when fault is detected it is recommended to read the fault/status register twice to make sure that the first fault is real. If the second reading gives the same result then the fault is real.

Under-Voltage Detection

LP8543 has detection for too low V_{IN} voltage. Threshold level for the voltage is set with EEPROM register bits as seen in the following table:

Table 11. Under-Voltage Detection Thresholds

UVLO_THR	Threshold (V)
0	6
1	3

Under voltage detection is always on. When under voltage is detected the LED outputs and boost will shutdown, Fault pin will be pulled down (open drain output) and corresponding fault bit is set in status register. Fault can be reset by reading the status register. LEDs and boost will start again when the voltage has increased above the threshold level. Hysteresis is implemented to threshold level to avoid continuous triggering of fault when threshold is reached.

Note: Due to the nature of fault detection it is possible to generate false faults during startup etc. conditions. Therefore when fault is detected it is recommended to read the fault/status register twice to make sure that the first fault is real. If the second reading gives the same result then the fault is real.

Over-Current Detection

LP8543 has detection for too high loading on the boost converter. When over current fault is detected the LP8543 will shut down and set the fault flag.

Thermal Shutdown

If the LP8543 reaches thermal shutdown temperature (150°C) the LED outputs and boost will shut down to protect it from damage. Also the fault pin will be pulled down to indicate the fault state. Device will activate again when temperature drops below 130°C.

SMBus/I^{2}C Compatible Serial Bus Interface

Interface Bus Overview

The SMBus/I^{2}C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL / SCLK). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCLK). LP8543 is always a slave device.

Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCLK and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCLK state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

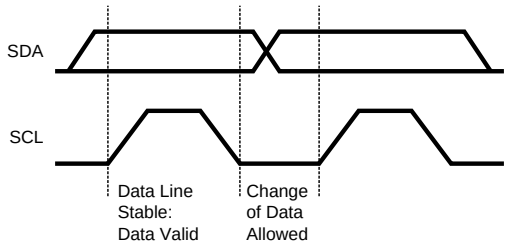


Figure 25. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

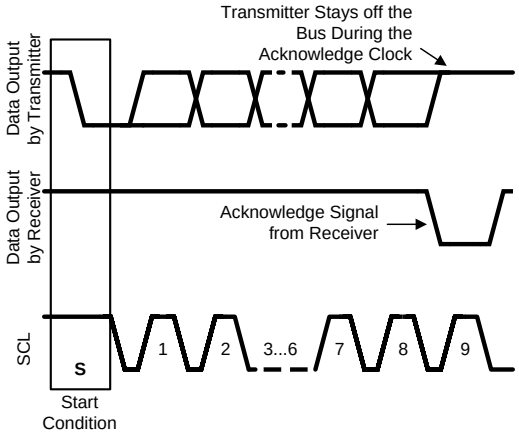


Figure 26. Start and Stop

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCLK) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCLK is high indicates a Stop Condition.

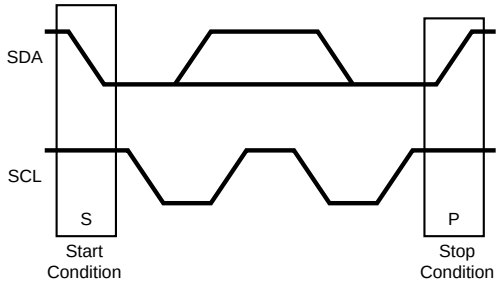


Figure 27. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

"Acknowledge After Every Byte" Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This "negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP8543 operates as a slave device with the 7-bit address combined with data direction bit. Slave address is pin-selectable as follows:

Table 12. Address Selection

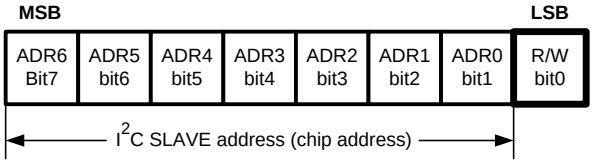
ADR	Slave Address Write (8 bits)	Slave Address Read (8 bits)
0	01011000 (58H)	01011001 (59H)
1	01011010 (5AH)	01011011 (5BH)

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

Figure 28. I²C Chip Address



Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

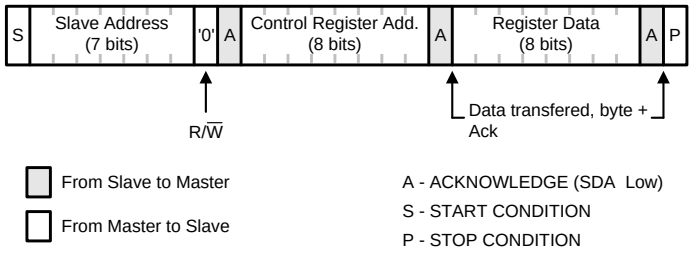
- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Table 13. Data Read and Write Cycles

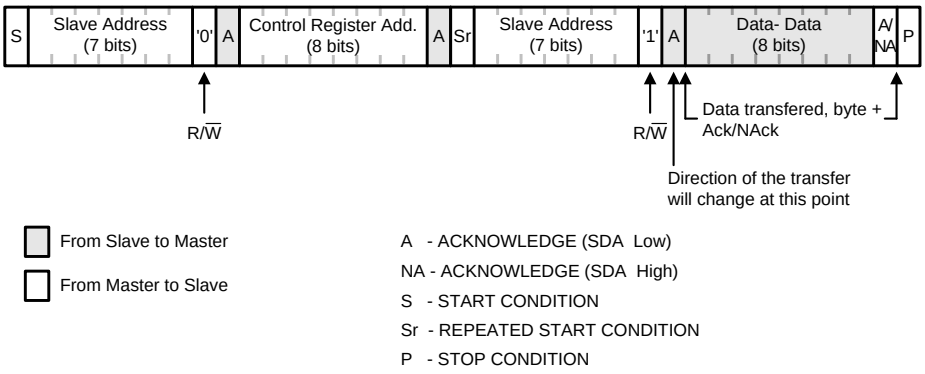
	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> … additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w='0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] … additional writes to subsequent register address possible <Stop Condition>

<>Data from master [ ] Data from slave

Register Read and Write Detail



Register Write Format



Register Read Format

Recommended External Components

Inductor Selection

A 15 µH shielded inductor is suggested for LP8543 boost converter. Inductor maximum current can be calculated from the equations below.

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1\text{-}D)$$

- I_{RIPPLE}: Average to peak inductor current
- I_{OUTMAX}: Maximum load current
- V_{IN}: Maximum input voltage in application
- L: Min inductor value including worst case tolerances
- f: Minimum switching frequency
- V_{OUT}: Output voltage

(1)

Example using above equations:

- V_{IN} = 12V
- V_{OUT} = 38V
- I_{OUT} = 400 mA
- L = 15 µH − 20% = 12 µH
- f = 1.25 MHz
- I_{SAT} = 1.6A

As a result the inductor should be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 0.9...2.5A (programmed to EEPROM). Maximum current limit needed for the application can be approximated with calculations above. A 15 µH inductor with a saturation current rating of 2.5A is recommended for most applications. The inductor's resistance should be less than 300 mΩ for good efficiency. For high efficiency choose an inductor with high frequency core material such as ferrite to reduce core losses. To minimize radiated noise, use shielded core inductor. Inductor should be placed as close to the SW pin and the IC as possible. Special care should be used when designing the PCB layout to minimize radiated noise and to get good performance from the boost converter.

Output Capacitor

A ceramic capacitor with 50V voltage rating or higher is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. For light loads (<100 mA) 4.7 µF capacitor is sufficient. For maximum output voltage/current 10 µF capacitor (4 uF effective capacitance @ 38V) is recommended to reduce the output ripple. Small 33 pF capacitor is recommended to use in parallel with the output capacitor to suppress high frequency noise.

LDO Capacitor

A 470 nF ceramic capacitor with 10V voltage rating is recommended for the LDO capacitor.

Output Diode

A schottky diode should be used for the output diode. Peak repetitive current should be greater than inductor peak current (0.9...2.5A) to ensure reliable operation. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown voltage of the Schottky diode significantly larger (~60V) than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

Ambient Light Sensor

LP8543 uses light-to-frequency type ambient light sensor. Suitable frequency range for ALS is 200 Hz to 2 MHz.

Table 14. LP8543 Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00H	Display1 PWM	DISP1_PWM[7:0]								1111 1111
01H	Config1						PWM_MD	PWM_SEL	BL_CTL	0000 0000
02H	Status			2_CH_SD	1_CH_SD	BL_STAT	OV_CUR R	THRM_SH DN	FAULT	0000 0000
03H	Identification	LED_PAN EL	MFG[3:0]				REV[2:0]			1111 1001
04H	Output Control	OUT[7:1]								0000 0000
05H	Display1 Current	DISP1_CURRENT[7:0]								0000 0000
06H	Display2 Current	DISP2_CURRENT[7:0]								0000 0000
07H	Boost Control		BOOST_A UTO	EN_BOO ST	VPROG[4:0]					0110 0000
08H	Display2 PWM	DISP2_PWM[7:0]								0000 0000

Table 14. LP8543 Register Map (continued)

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
09H	Config2					CURRENT_SEL	ALS_SEL	ALS_CALC_EN	ALS_EN	0000 0000
0AH	ALS MSB	ALS[9:2]								0000 0000
0BH	ALS LSB	ALS[1:0]								0000 0000
0CH	Fault	DISP2_FAULT	DISP1_FAULT	LED_OPEN	LED_SHORT	UVLO				0000 0000
0DH	TEMP MSB	TEMP[10:3]								0000 0000
0EH	TEMP LSB	TEMP[2:0]								0000 0000
72H	EEPROM_control	EE_READY			NSTBY	EE_UPDATE	EE_ERASE	EE_PROG	EE_READ	0000 0000

Table 15. LP8543 EEPROM Memory Map

ADDR	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
A0H	ALS A1[7:0]								3DH
A1H	ALS B1[7:0]								0AH
A2H	ALS THR[7:0]								FFH
A3H	ALS A2[7:0]								00H
A4H	ALS B2[7:0]								FFH
A5H	ALS THR2[7:0]								FFH
A6H	ALS A3[7:0]								00H
A7H	ALS B3[7:0]								FFH
A8H	PWM A1[7:0]								40H
A9H	PWM B1[7:0]								00H
AAH	PWM THR1[7:0]								FFH
ABH	PWM A2[7:0]								00H
ACH	PWM B2[7:0]								FFH
ADH	PWM THR2[7:0]								FFH
AEH	PWM A3[7:0]								00H
AFH	PWM B3[7:0]								FFH
B0H	DISP1_CURRENT[7:0]								62H
B1H	DISP2_CURRENT[7:0]								62H
B2H	SLOPE_SEL[1:0]		OUTPUT_CONF[1:0]		ALS_EN	ALSO_POLARITY	BOOST_FREQ	UVLO_THR	21H
B3H	EN_SLOPE	reserved	TEMP_LIM[1:0]		FAULT_SEL[1:0]		EN_DISP2_MON	DIS_TEMP_CALC	A4H
B4H	reserved	EN_STANDALONE	reserved		EN_AUTOLOAD	BOOST_MODE	DISABLE_PS	FILTER_TIME	45H
B5H	PWM_MODE	BOOST_UP[1:0]		PWM_FREQ[2:0]			PSPWM_FREQ[1:0]		BCH
B6H	Reserved								00H
B7H	Reserved								00H
B8H	Reserved								00H
B9H	Reserved								00H
BAH	Reserved								00H
BBH	Reserved								00H
BCH	DIG_COMP[1:0]		LED_FAULT_THR[2:0]			DRV_HEADR_CTRL[2:0]			90H
BDH	Reserved	IMAX_SEL[1:0]		VPROG[4:0]					7CH
BEH	ALS_PRESCALE[9:2]								7AH
BFH	ALS_PRESCALE[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00H

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	34

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8543SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	RoHS & Green	SN	Level-1-260C-UNLIM		L8543SQ	Samples
LP8543SQE/NOPB	ACTIVE	WQFN	RTW	24	250	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	L8543SQ	Samples
LP8543SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	L8543SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

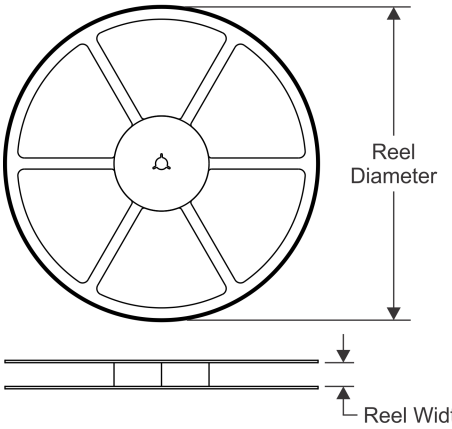
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

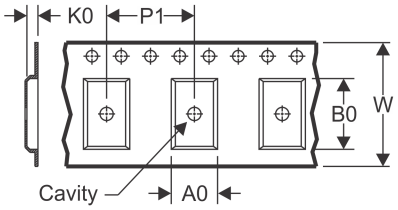
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

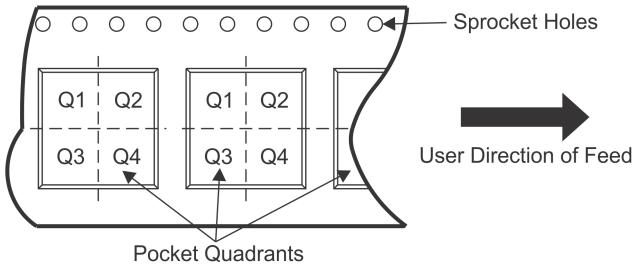


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

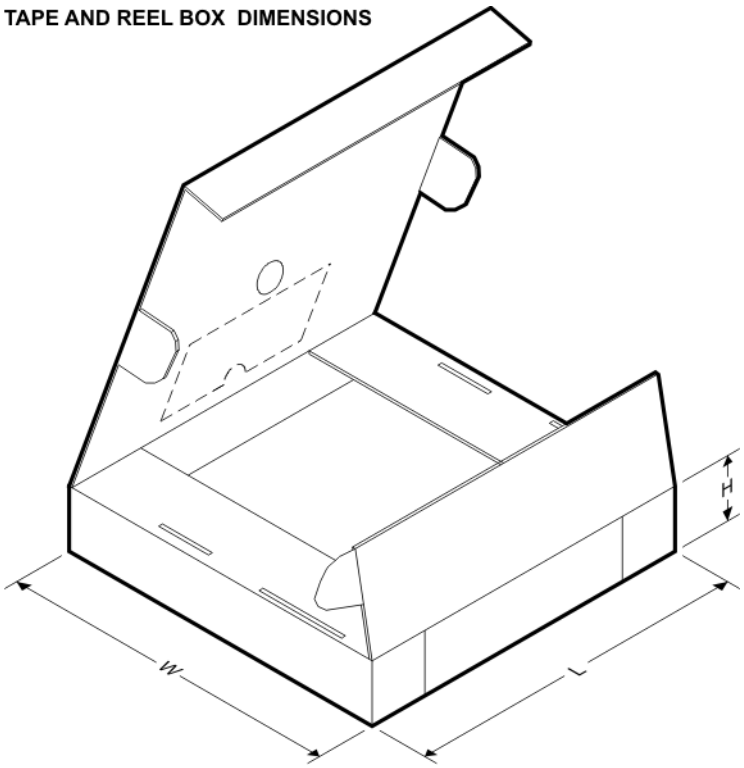
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8543SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8543SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8543SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

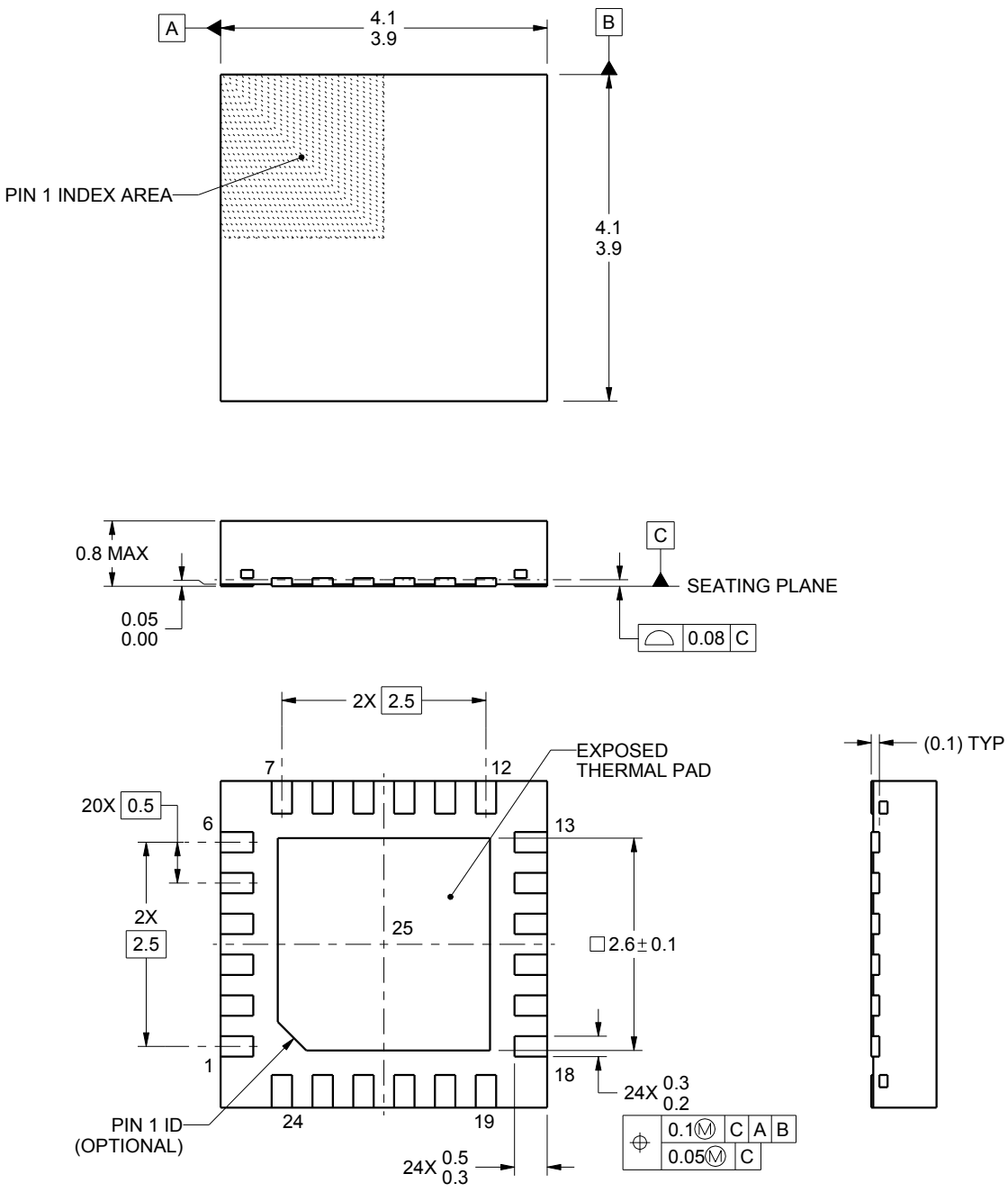
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8543SQ/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LP8543SQE/NOPB	WQFN	RTW	24	250	208.0	191.0	35.0
LP8543SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

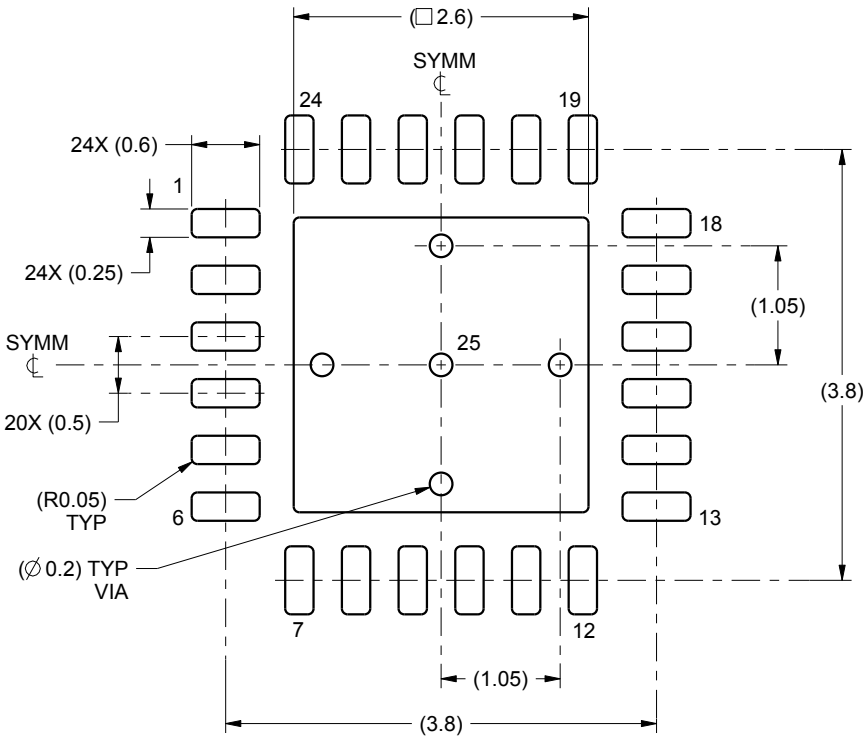
PLASTIC QUAD FLATPACK - NO LEAD



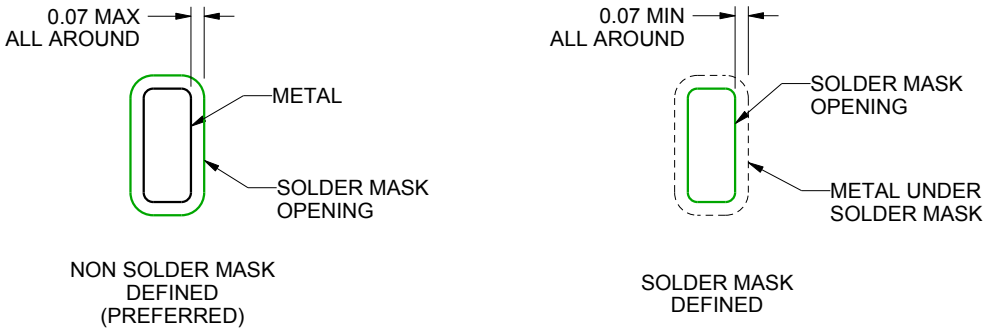
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

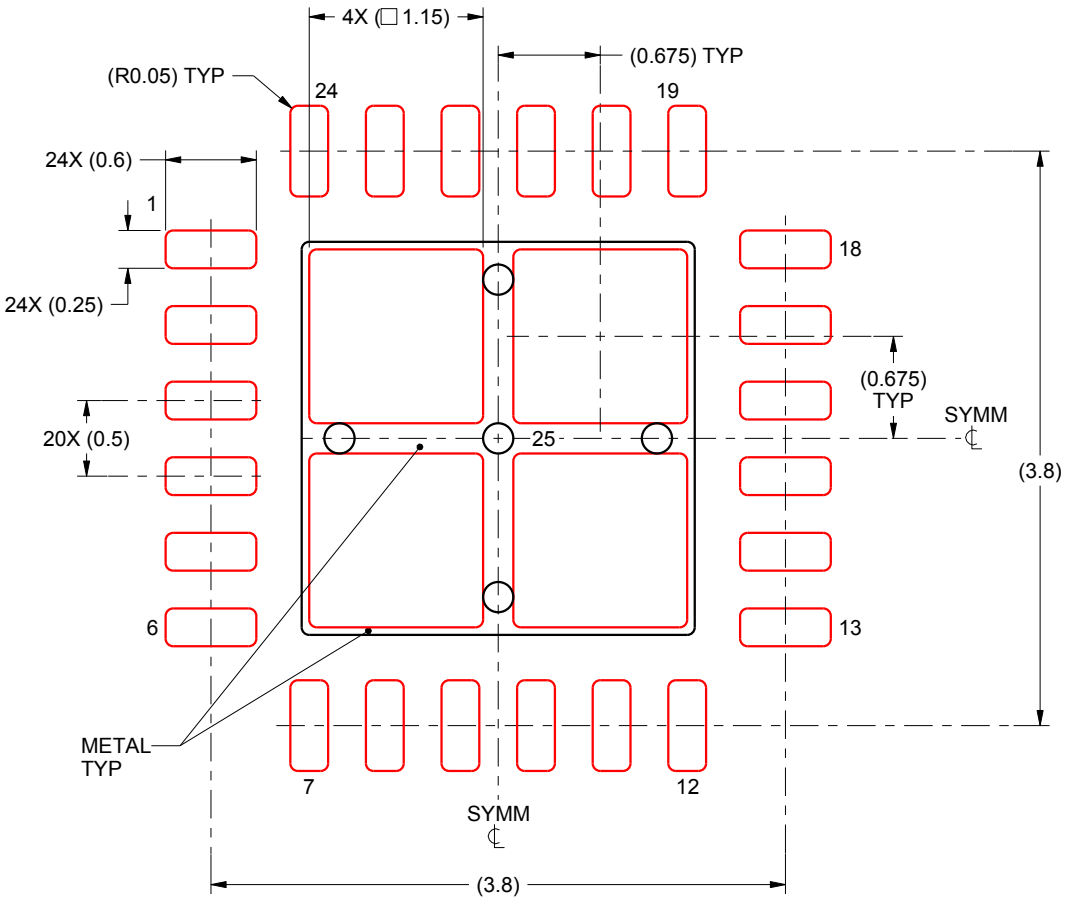


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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