具有漏极开路输出的 SN74LVC1G07 单路缓冲器/驱动器

1 特性

- 采用具有 0.5mm 间距的超小型 0.64mm^2 封装 (DPW)
- 支持 5V V_{CC} 运行
- 输入与开漏输出支持最高 5.5V 的电压
- 可进行上行或下行转换
- 电压为 3.3V 时，t_{pd} 最大值为 4.2ns
- 低功耗，10μA 最大 I_{CC}
- 电压为 3.3V 时，输出驱动为 ±24mA
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 闩锁性能超过 100mA，符合 {13}JESD 78 II 类规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器模型 (A115-A)
  - 1000V 充电器件模型 (C101)

2 应用

- AV 接收器
- 蓝光播放器与家庭影院
- DVD 录像机和播放器
- 台式机或笔记本电脑
- 数字音频广播或互联网广播播放器
- 数码摄像机 (DVC)
- 嵌入式计算机
- GPS：个人导航设备
- 移动因特网设备
- 网络投影仪前端
- 便携式媒体播放器
- 专业音频混合器
- 烟雾探测器
- 固态硬盘 (SSD): 企业
- 高清 (HDTV)
- 平板电脑：企业
- 音频接口盒：便携式
- DLP 正投影系统
- DVR 和 DVS
- 数码相框 (DPF)
- 数码相机

3 说明

此单路缓冲器/驱动器专为 1.65V 至 5.5V V_{CC} 工作电压而设计。

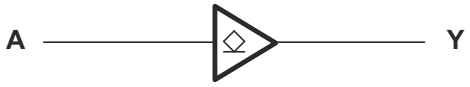
SN74LVC1G07 器件的输出为漏极开路，可连接其它开漏输出，从而实现低电平有效的连线 OR 或高电平有效的连线 AND 功能。最大灌电流为 32mA。

SN74LVC1G07 采用多种封装，包括外形尺寸为 0.8mm × 0.8mm 的超小型 DPW 封装。

器件信息

器件名称	封装(1)	封装尺寸
SN74LVC1G07DBV	SOT-23 (5)	2.9mm × 1.6mm
SN74LVC1G07DCK	SC70 (5)	2.0mm × 1.25mm
SN74LVC1G07DPW	X2SON (5)	0.8mm × 0.8mm
SN74LVC1G07DRY	SON (6)	1.45mm × 1.0mm
SN74LVC1G07DSF	SON (6)	1.0mm × 1.0mm
SN74LVC1G07DRL	SOT (5)	1.6mm x 1.2mm
SN74LVC1G07YZP	DSBGA (6)	1.38mm x 0.88mm
SN74LVC1G07YZV	DSBGA (4)	0.88mm x 0.88mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision AD (May 2016) to Revision AE (September 2020) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式。 1

Changes from Revision AC (April 2014) to Revision AD (April 2016) — **Page**

- 将*器件信息*表中 DPW 封装的 4 引脚更改为 5 引脚 1
- 向*器件信息*表添加了 DRL、YZP 和 YZV 封装信息和封装尺寸 1
- Moved "T_{stg} Storage temperature range" from *ESD Ratings* table to *Absolute Maximum Ratings* table 5
- Added "T_j Junction temperature range" to *Absolute Maximum ratings* table 5
- Split "T_A Operating free-air temperature" into package specific temperature ranges in *Recommended Operating Conditions* table 6
- Changed "H" to "Z" in Output Y column of Function Table 10

Changes from Revision AB (March 2014) to Revision AC (April 2014) — **Page**

- Updated Handling Ratings table. 5
- Added Thermal Information table. 6
- Added Typical Characteristics. 8
- Added Application and Implementation section. 11
- Added Power Supply Recommendations section. 12

Changes from Revision AA (July 2013) to Revision AB (February 2014) — **Page**

- 更新了“特性” 1
- 添加了“应用” 1
- 添加了“器件信息”表 1
- Added Pin Functions table. 4
- Moved T_{stg} to Handling Ratings table 5

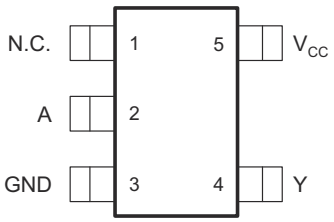
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Changes from Revision Z (November 2012) to Revision AA (July 2013) **Page**

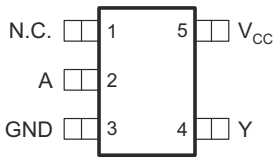
- Extended maximum temperature operating range from 85°C to 125°C..... 6

5 Pin Configuration and Functions

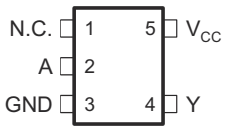
DBV PACKAGE (TOP VIEW)



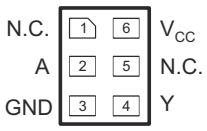
DCK PACKAGE (TOP VIEW)



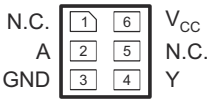
DRL PACKAGE (TOP VIEW)



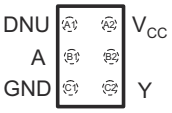
DRY PACKAGE (TOP VIEW)



DSF PACKAGE (TOP VIEW)



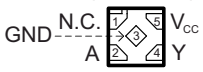
YZP PACKAGE (TOP VIEW)



YZV PACKAGE (TOP VIEW)



DPW PACKAGE (TOP VIEW)



N.C. – No internal connection
See mechanical drawings for dimensions.

Pin Functions

PIN						DESCRIPTION
NAME	DBV, DCK, DRL	DRY, DSF	DPW	YZP	YZV	
NC	1	1, 5	1	A1, B2	–	Not connected
A	2	2	2	B1	A1	Input
GND	3	3	3	C1	B1	Ground
Y	4	4	4	C2	B2	Output
V_{CC}	5	6	5	A2	A2	Power pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	6.5	V
V_I	Input voltage range(2)		– 0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		– 0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		– 0.5	6.5	V
I_{IK}	Input clamp current	V_I < 0		– 50	mA
I_{OK}	Output clamp current	V_O < 0		– 50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		– 65	150	°C
T_j	Junction temperature range			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature	DSBGA package	–40	85	°C
		All other packages	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G07						UNIT
		DBV	DCK	DRL	DRY	YZP	DPW	
		5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229	278	243	439	130	340	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164	93	78	277	54	215	
$R_{\theta JB}$	Junction-to-board thermal resistance	62	65	78	271	51	294	
ψ_{JT}	Junction-to-top characterization parameter	44	2	10	84	1	41	
ψ_{JB}	Junction-to-board characterization parameter	62	64	77	271	50	294	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	250	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	–40°C TO 85°C		–40°C TO 125°C RECOMMENDED		UNIT
					TYP(1)	MAX	TYP	MAX	
V_{OL}		I_{OL} = 100 µA		1.65 V to 5.5 V		0.1		0.1	V
		I_{OL} = 4 mA		1.65 V		0.45		0.45	
		I_{OL} = 8 mA		2.3 V		0.3		0.3	
		I_{OL} = 16 mA		3 V		0.4		0.4	
		I_{OL} = 24 mA				0.55		0.55	
		I_{OL} = 32 mA		4.5 V		0.55		0.55	
I_I	A input	V_I = 5.5 V or GND		0 to 5.5 V		±5		±5	µA
I_{off}		V_I or V_O = 5.5 V		0		±10		±10	µA
I_{CC}		V_I = 5.5 V or GND,	I_O = 0	1.65 V to 5.5 V		10		10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 5.5 V		500		500	µA
C_i		V_I = V_{CC} or GND		3.3 V	4		4		pF
C_o		V_O = V_{CC} or GND		3.3 V	5		5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2.4	8.3	1	5.5	1.5	4.2	1	3.5	ns

6.7 Switching Characteristics, –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 125°C RECOMMENDED								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2.4	8.6	1	6	1.5	4.7	1	4	ns

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF

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6.9 Typical Characteristics

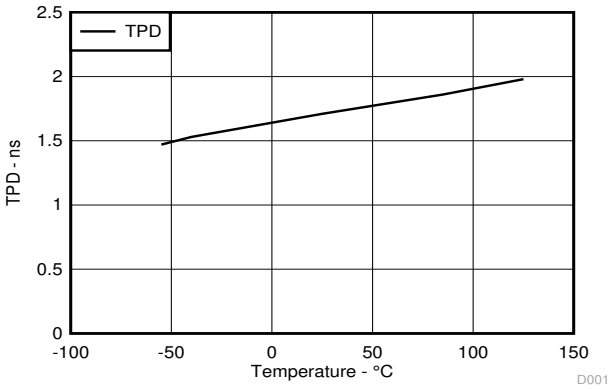


图 6-1. TPD Across Temperature at 3.3V Vcc

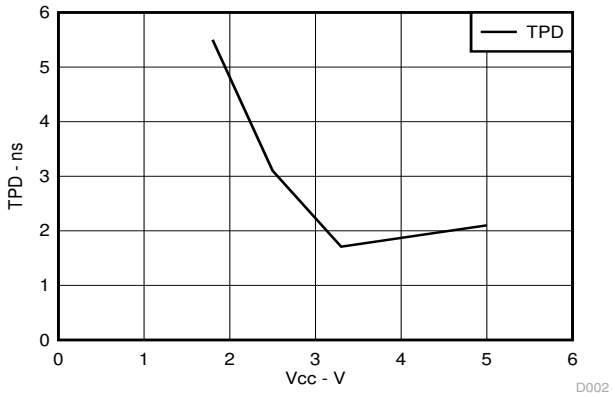
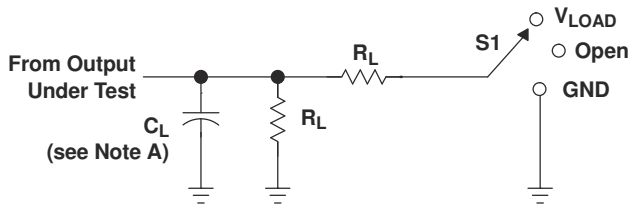


图 6-2. TPD Across Vcc at 25°C

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7 Parameter Measurement Information

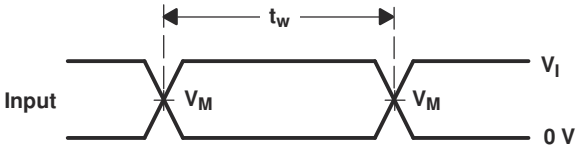
7.1 (Open Drain)



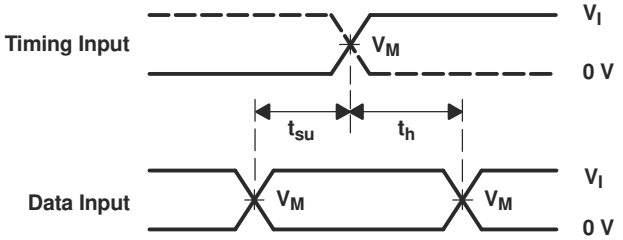
LOAD CIRCUIT

TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

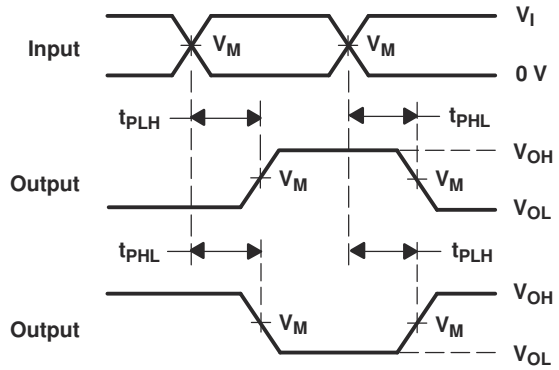
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



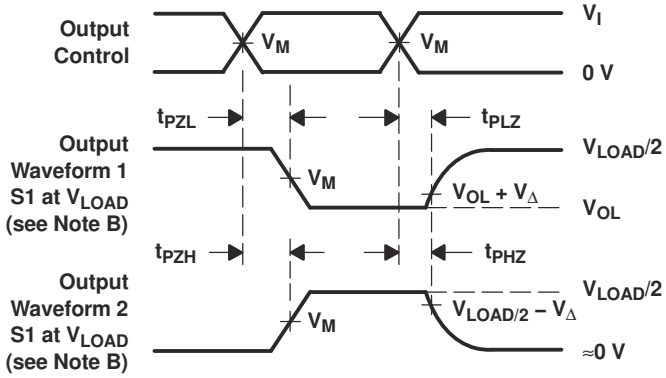
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
F. t_{PZL} is measured at V_M.
G. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

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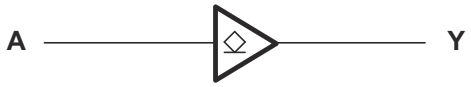
8 Detailed Description

8.1 Overview

The SN74LVC1G07 device contains one open-drain buffer with a maximum sink current of 32 mA. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. The DPW 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs and outputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

8.4 Device Functional Modes

Function Table

INPUT A	OUTPUT Y
L	L
H	Z

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9 Application and Implementation

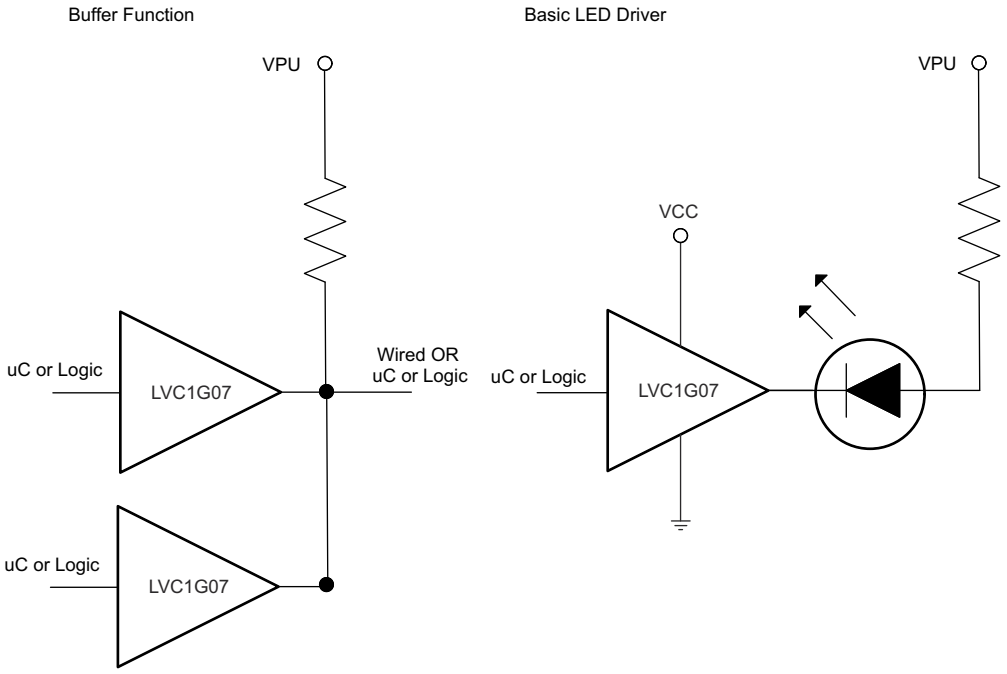
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G07 is a high drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can sink 32 mA of current at 4.5 V making it ideal for high drive and wired-OR/AND functions. It is good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate up/down to V_{CC}.

9.2 Typical Application



9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it may drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are over-voltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs should not be pulled above 5.5 V.

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9.2.3 Application Curves

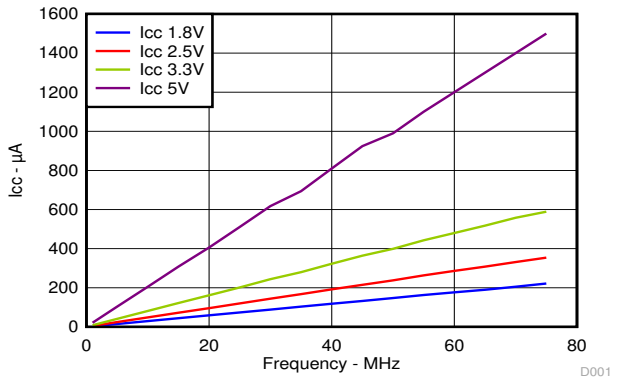


图 9-1. Icc vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

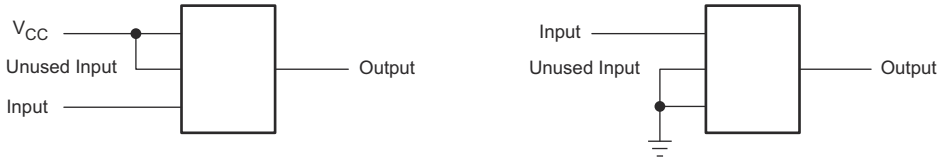
Each Vcc pin should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for devices with a single supply. If there are multiple Vcc pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to Gnd or Vcc, whichever is more convenient.

11.2 Layout Example



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12 Device and Documentation Support

12.1 Trademarks

所有商标均为其各自所有者的财产。

12.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G07DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R, C 07T) (C07H, C07P, C07S)	Samples
SN74LVC1G07DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F	Samples
SN74LVC1G07DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F	Samples
SN74LVC1G07DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R) (C07H, C07P, C07S)	Samples
SN74LVC1G07DBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F	Samples
SN74LVC1G07DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F	Samples
SN74LVC1G07DCK3	ACTIVE	SC70	DCK	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	(CVF, CVZ)	Samples
SN74LVC1G07DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) (CVH, CVP, CVS)	Samples
SN74LVC1G07DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) (CVH, CVP, CVS)	Samples
SN74LVC1G07DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) (CVH, CVP, CVS)	Samples
SN74LVC1G07DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) CVH	Samples
SN74LVC1G07DCKTE4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) CVH	Samples
SN74LVC1G07DCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										CVH	
SN74LVC1G07DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L4	Samples
SN74LVC1G07DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CV7, CVR)	Samples
SN74LVC1G07DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CV7, CVR)	Samples
SN74LVC1G07DRY2	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07DRYRG4	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07DSF2	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CV7, CVN)	Samples
SN74LVC1G07YZVR	ACTIVE	DSBGA	YZV	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CV N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G07 :

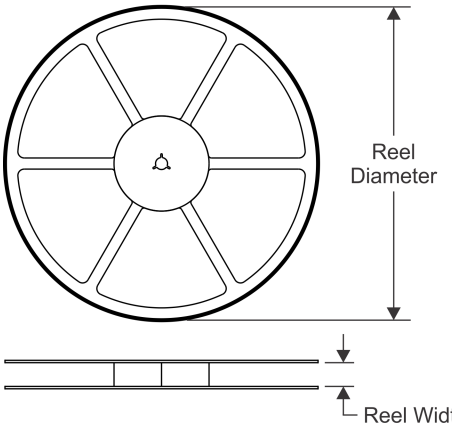
- Automotive : SN74LVC1G07-Q1
- Enhanced Product : SN74LVC1G07-EP

NOTE: Qualified Version Definitions:

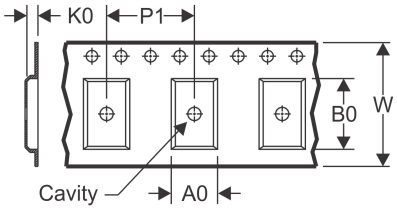
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

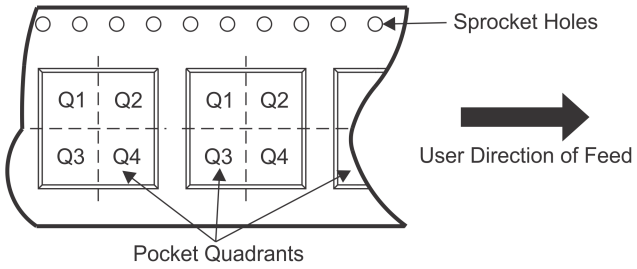


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

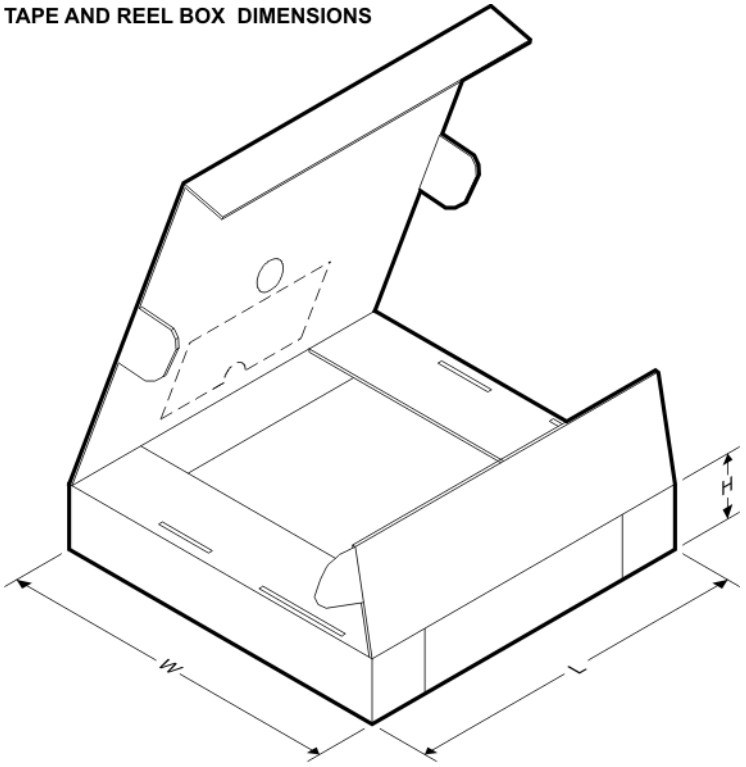


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G07DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G07DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G07DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G07DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G07DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G07DRY2	SON	DRY	6	5000	180.0	8.4	1.65	1.2	0.7	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G07DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G07DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3
SN74LVC1G07DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74LVC1G07DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G07YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G07YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G07DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LVC1G07DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

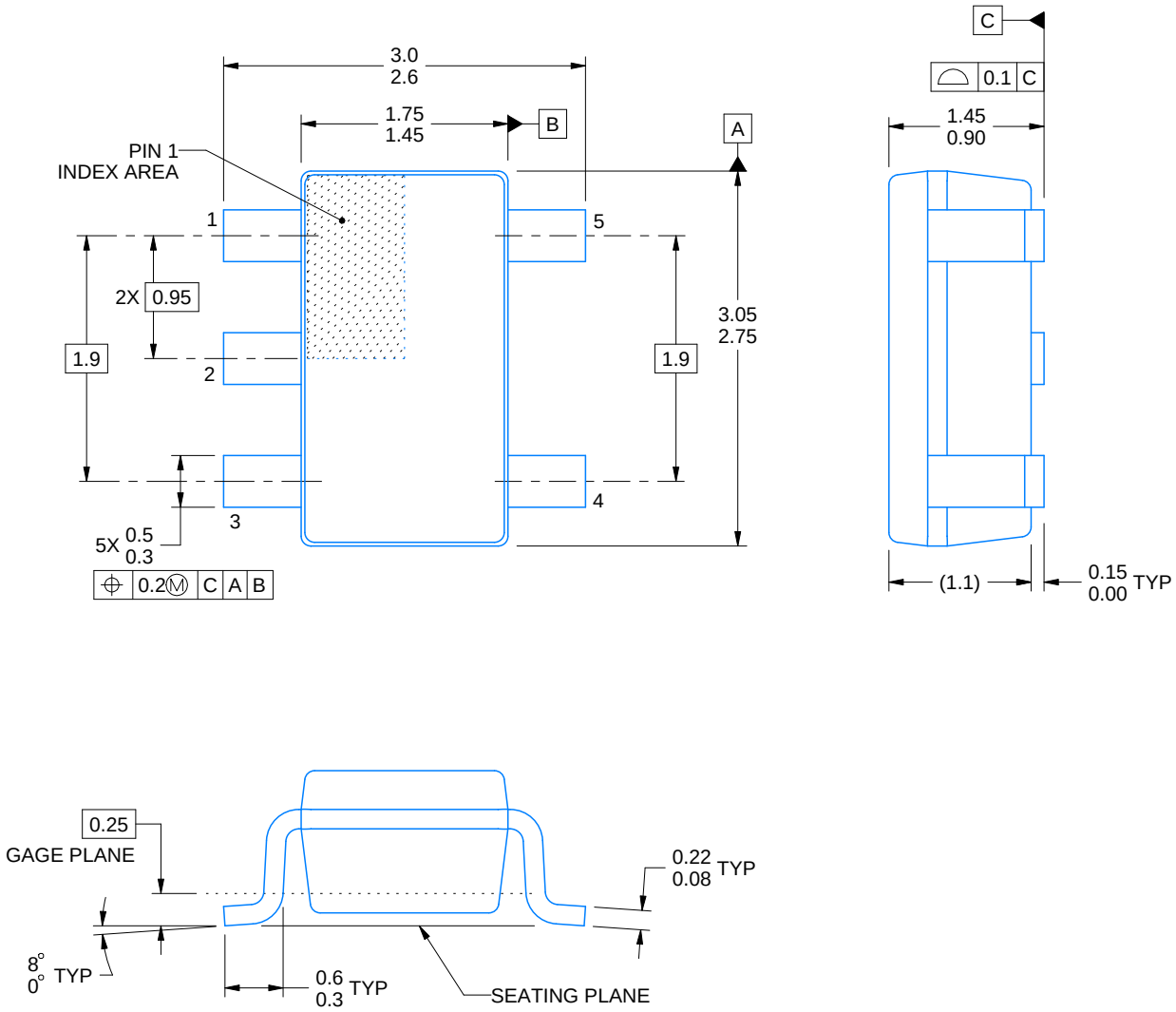
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G07DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G07DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G07DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G07DRY2	SON	DRY	6	5000	202.0	201.0	28.0
SN74LVC1G07DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G07DSF2	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G07DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G07DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G07YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G07YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

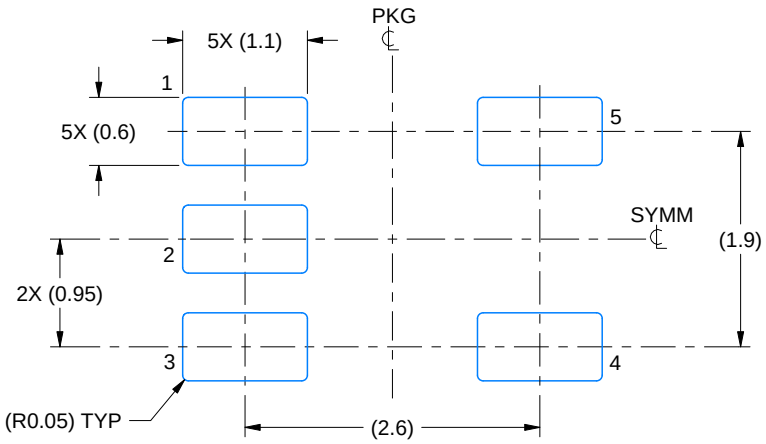
SMALL OUTLINE TRANSISTOR



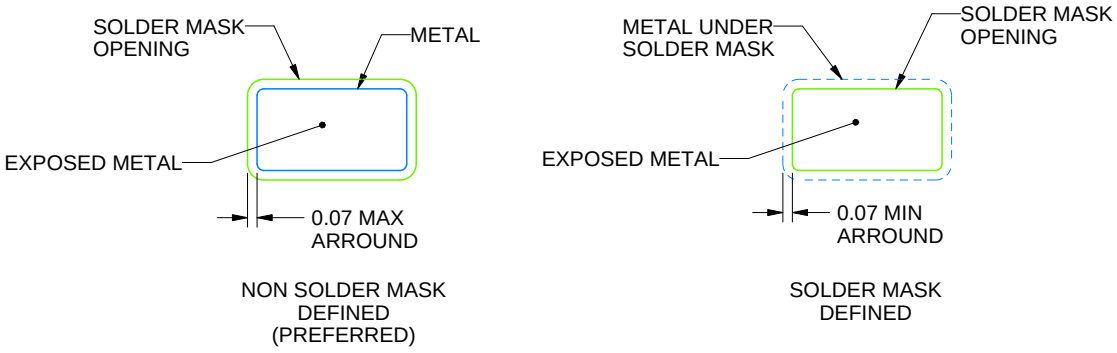
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

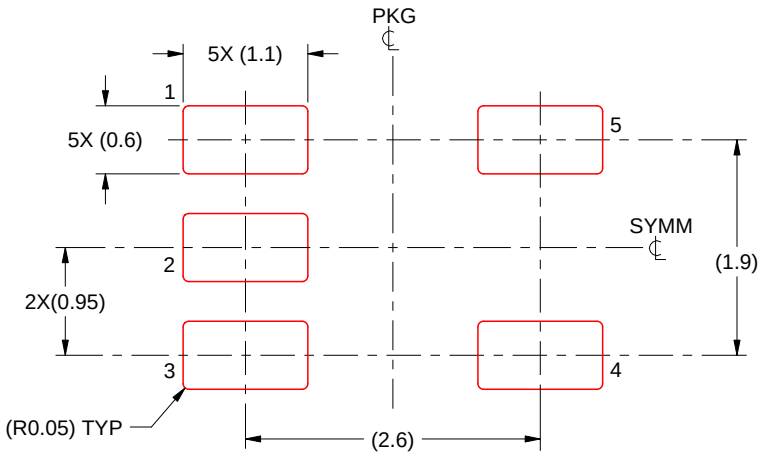


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

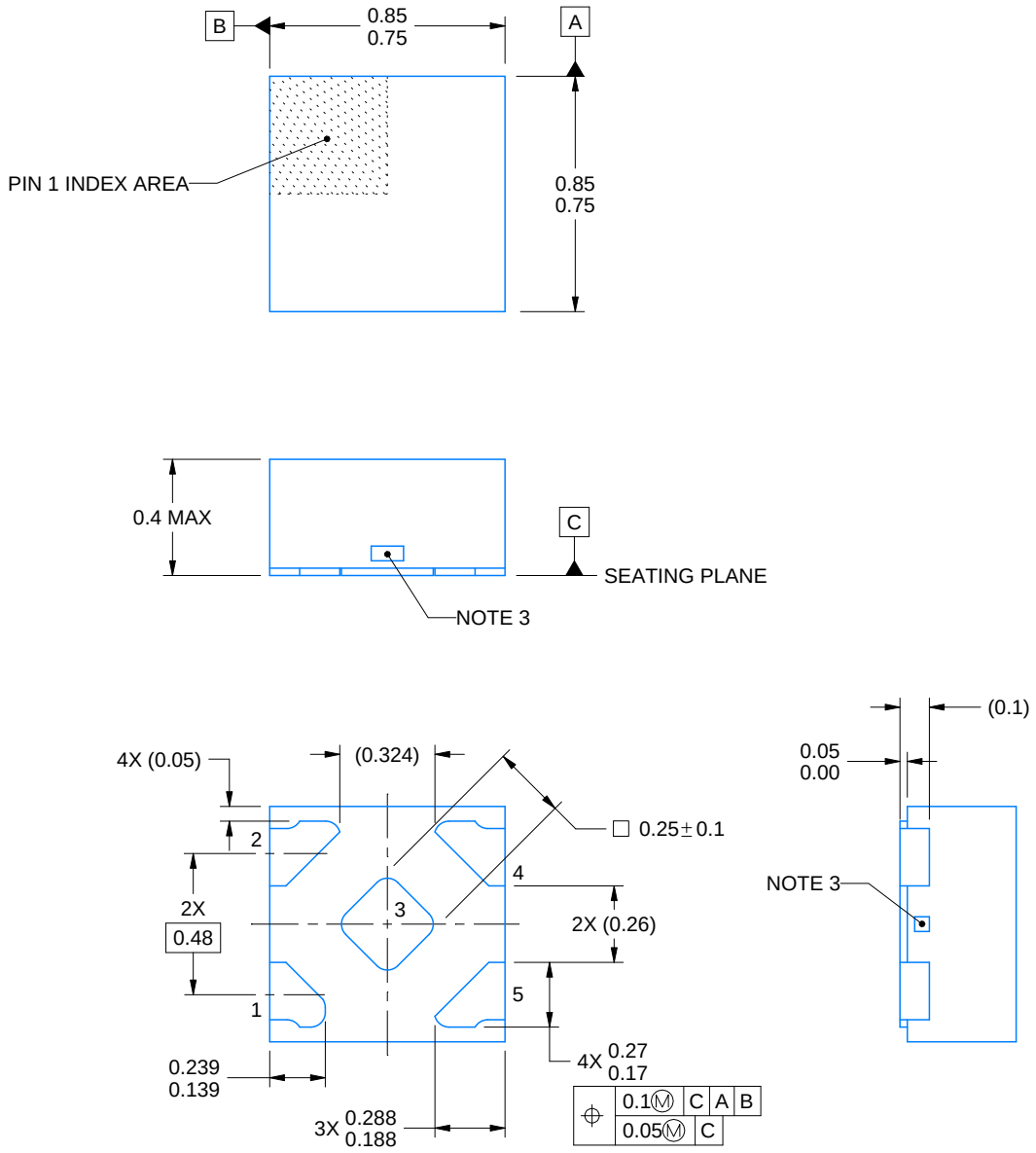
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

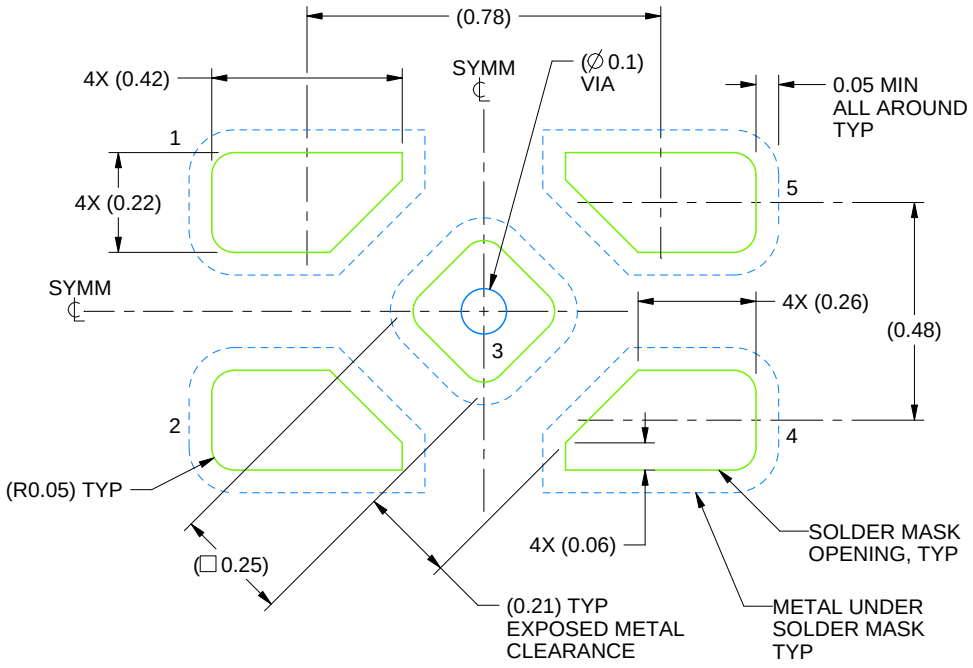
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

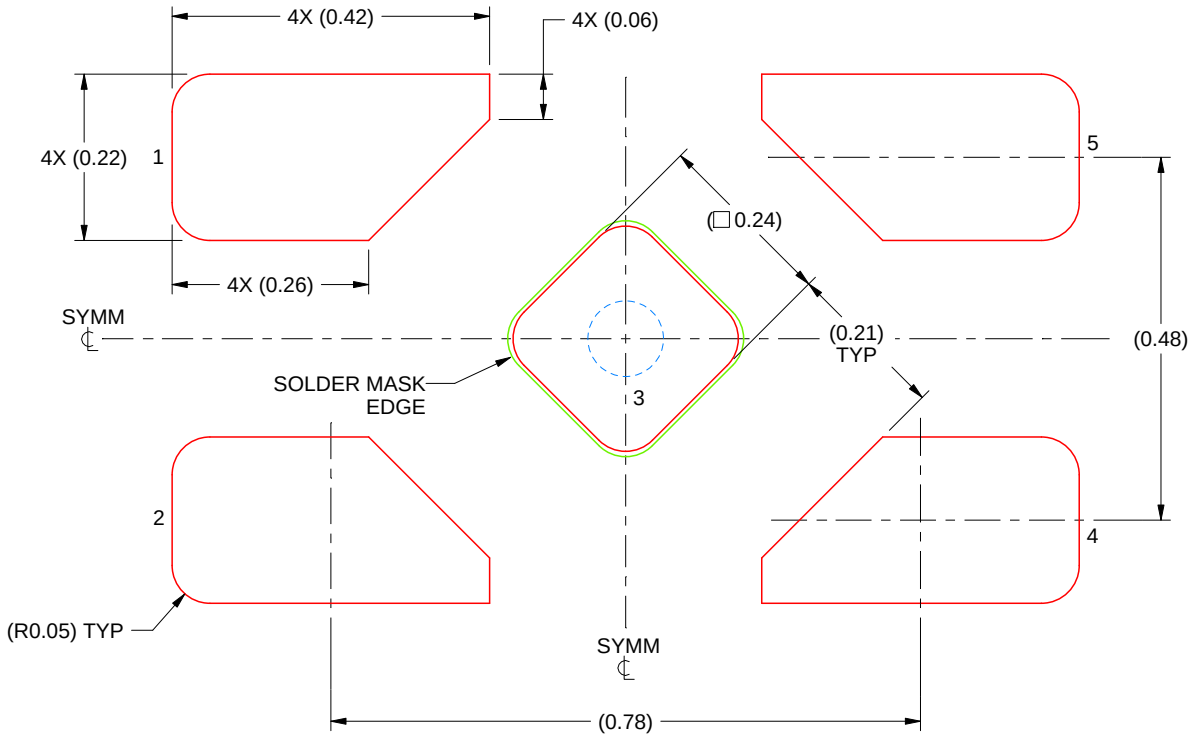
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

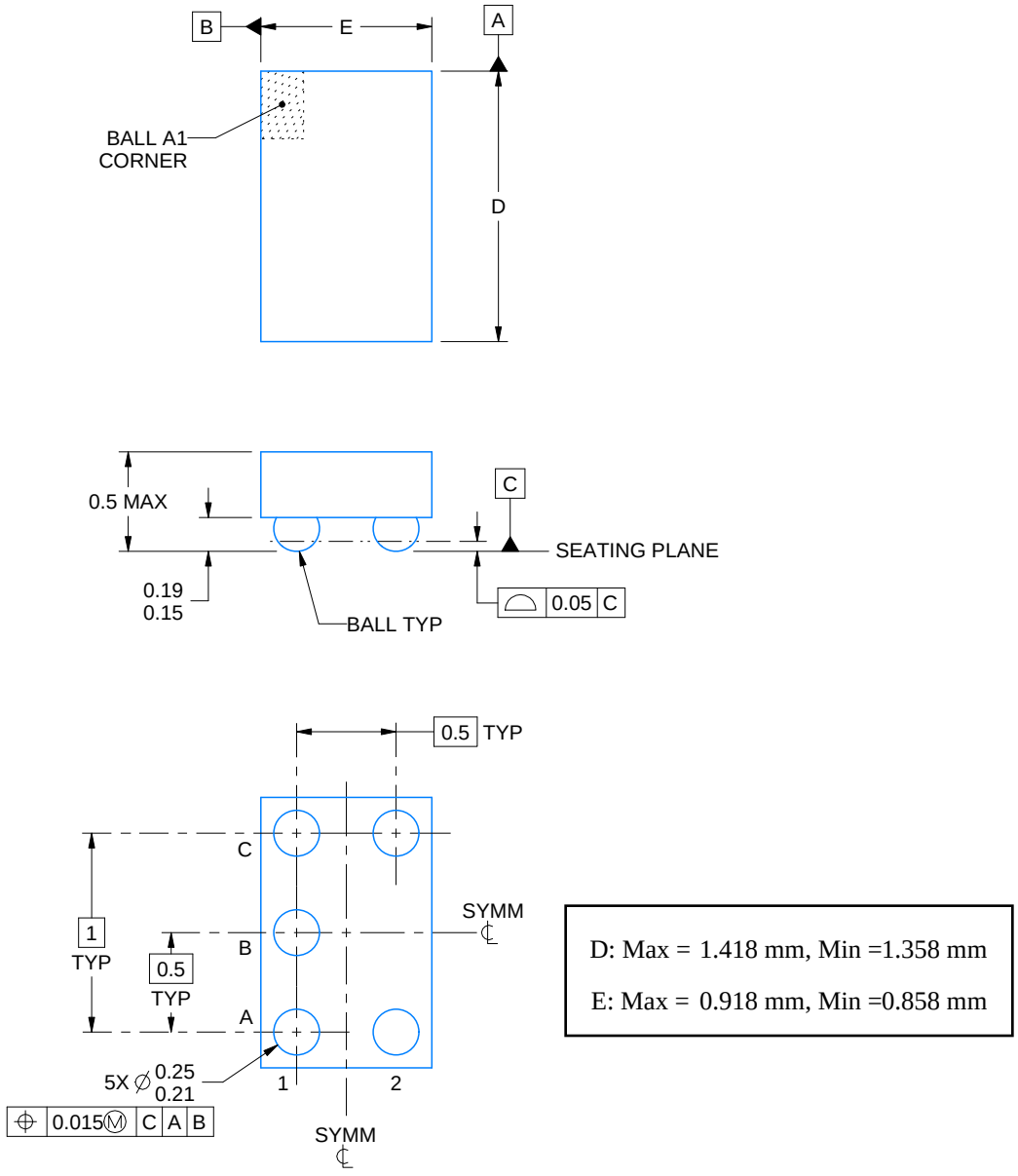
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



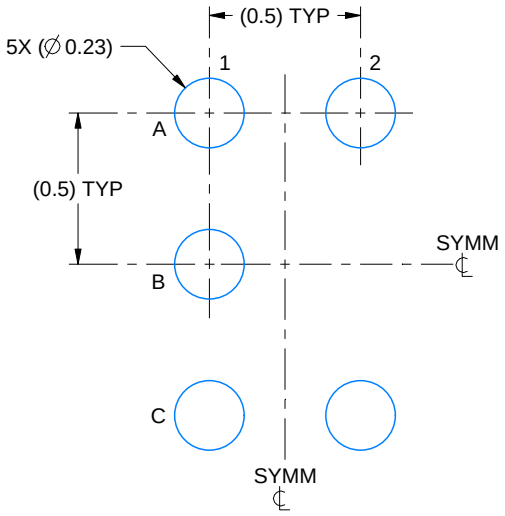
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

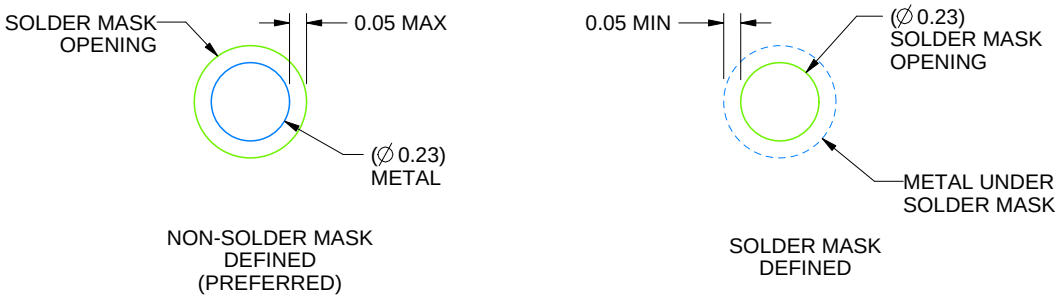
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

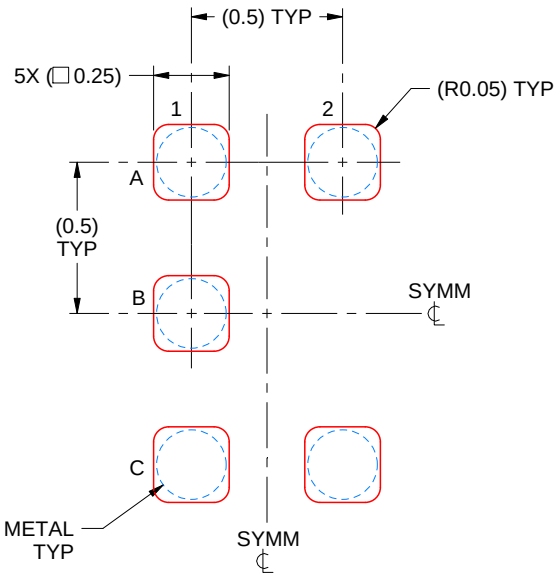


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



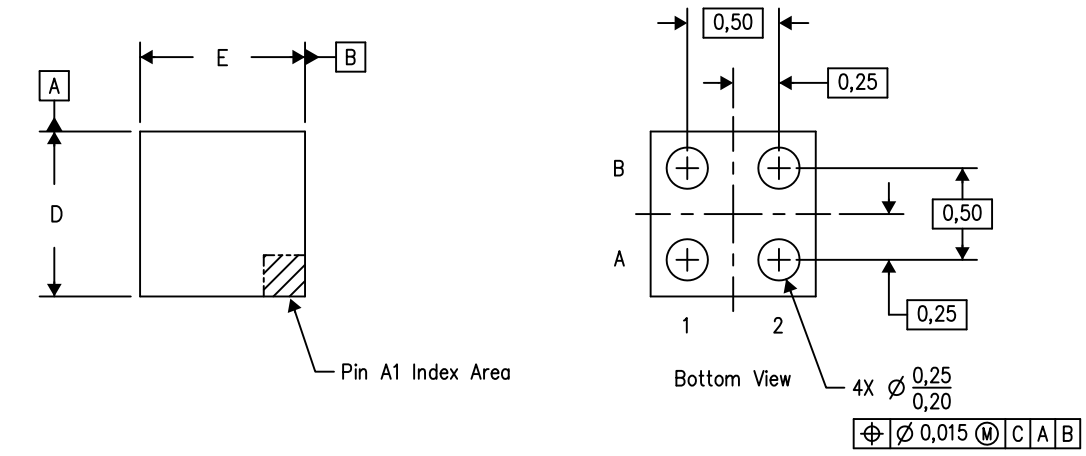
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

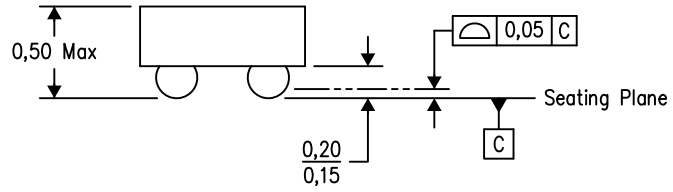
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY





D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

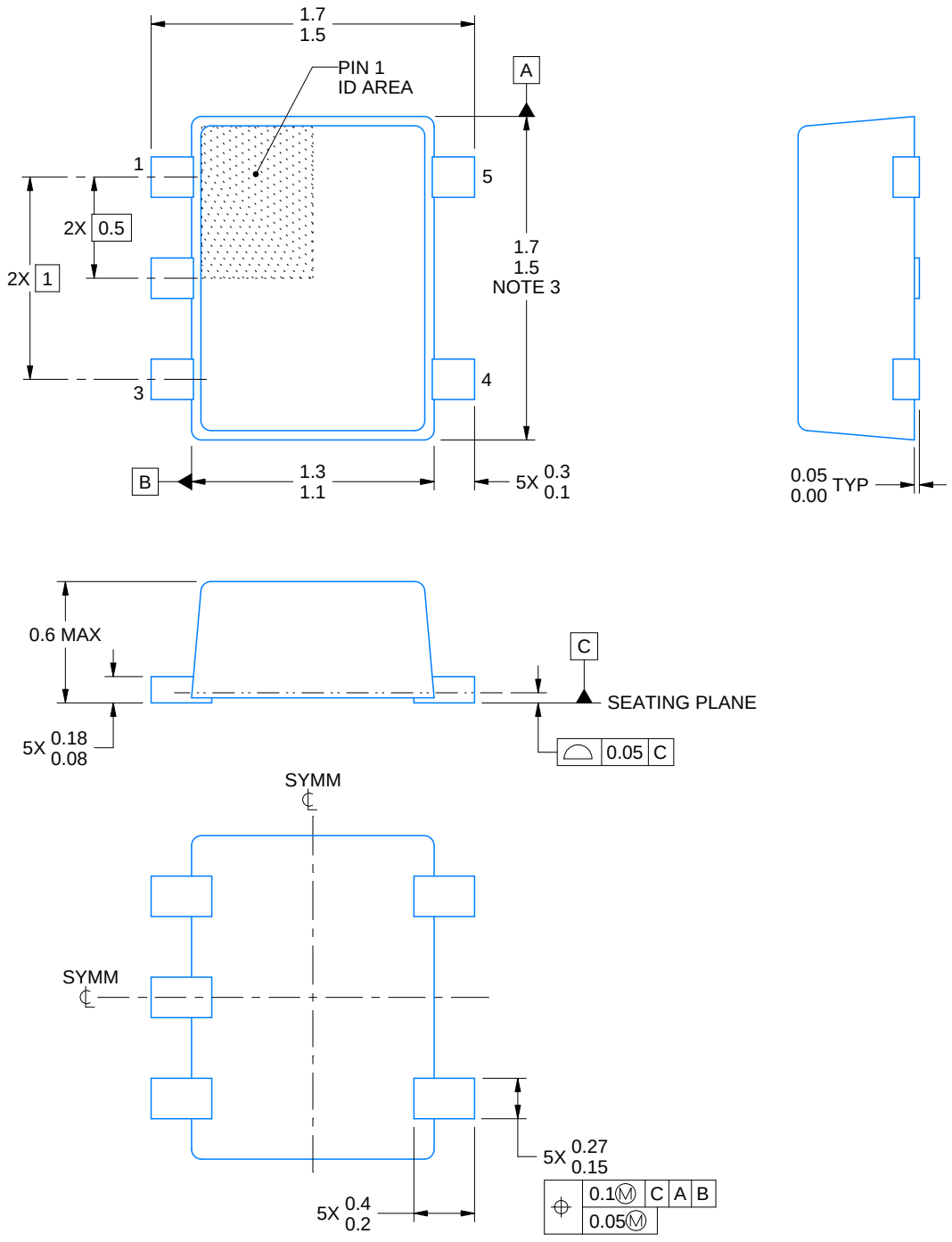
NanoFree is a trademark of Texas Instruments.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

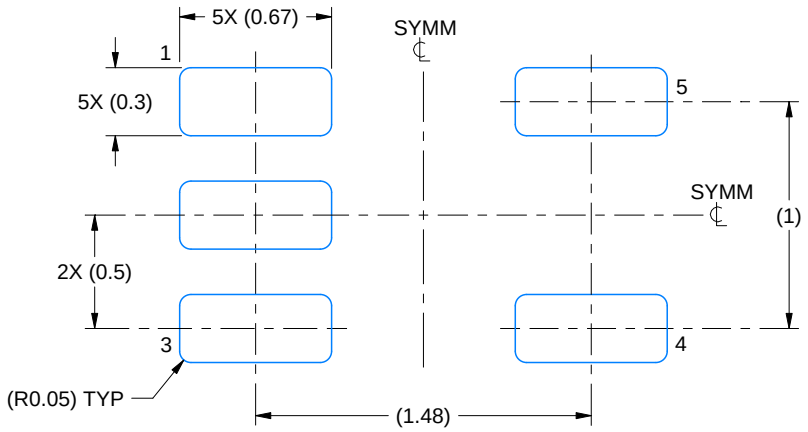
PLASTIC SMALL OUTLINE



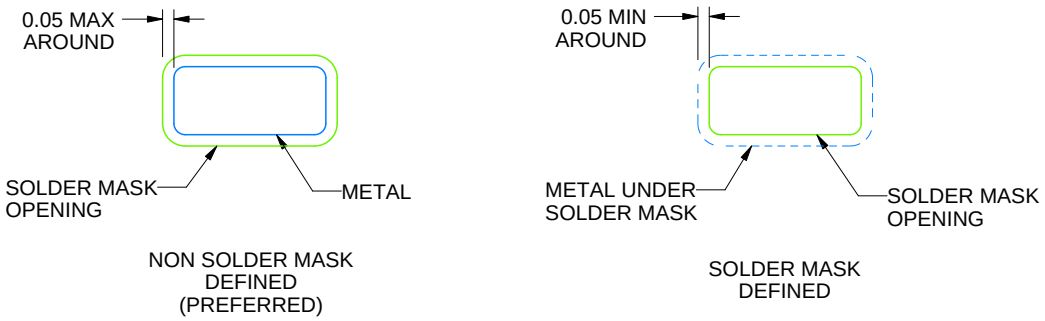
4220753/B 12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

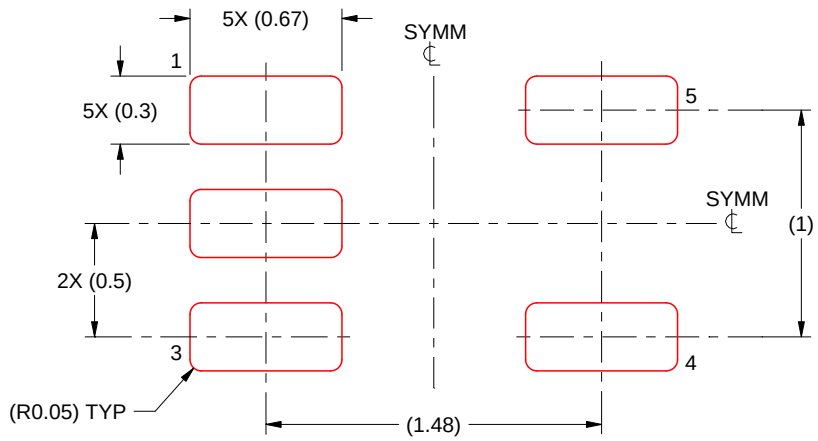


SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

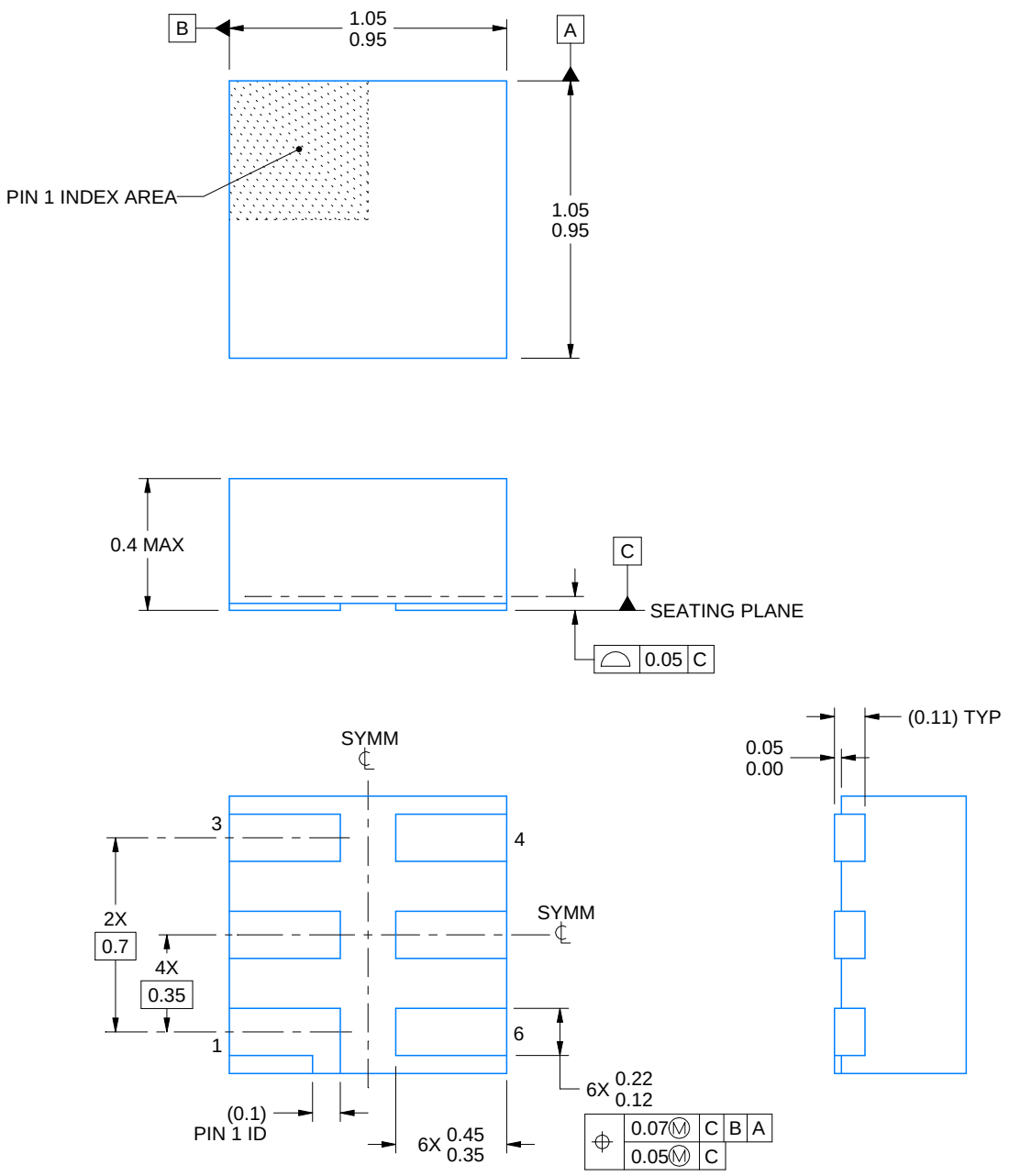
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

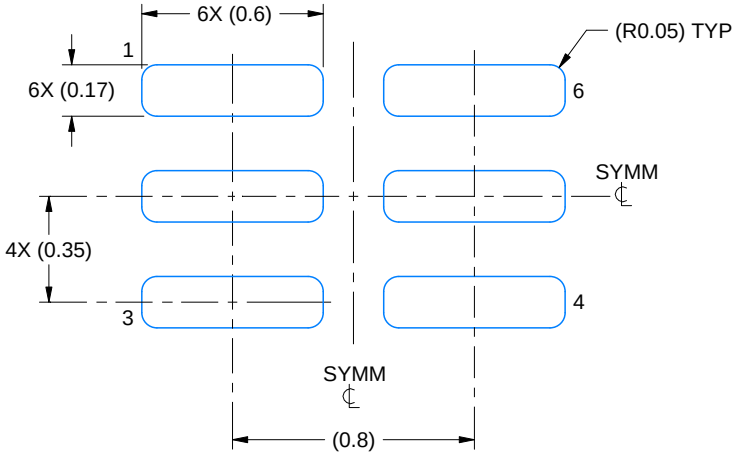
PLASTIC SMALL OUTLINE - NO LEAD



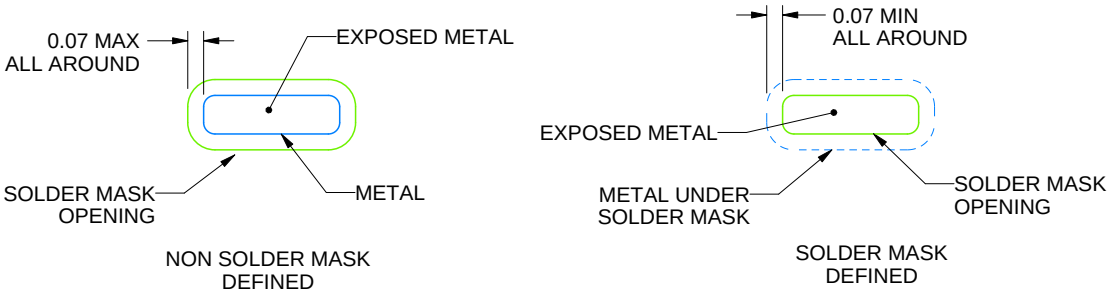
4220597/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

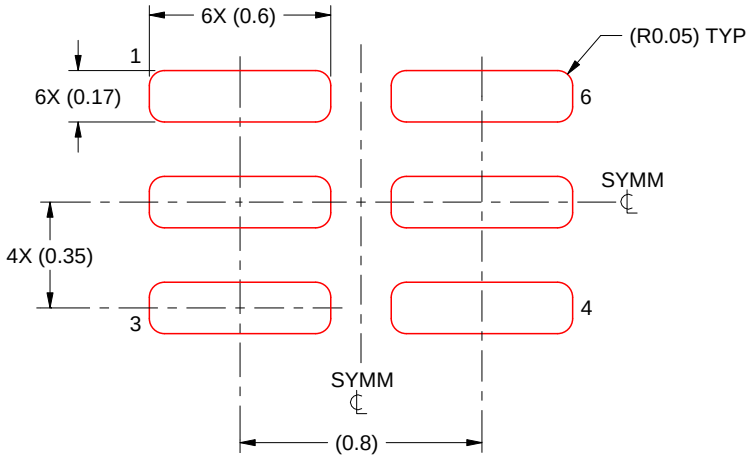
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



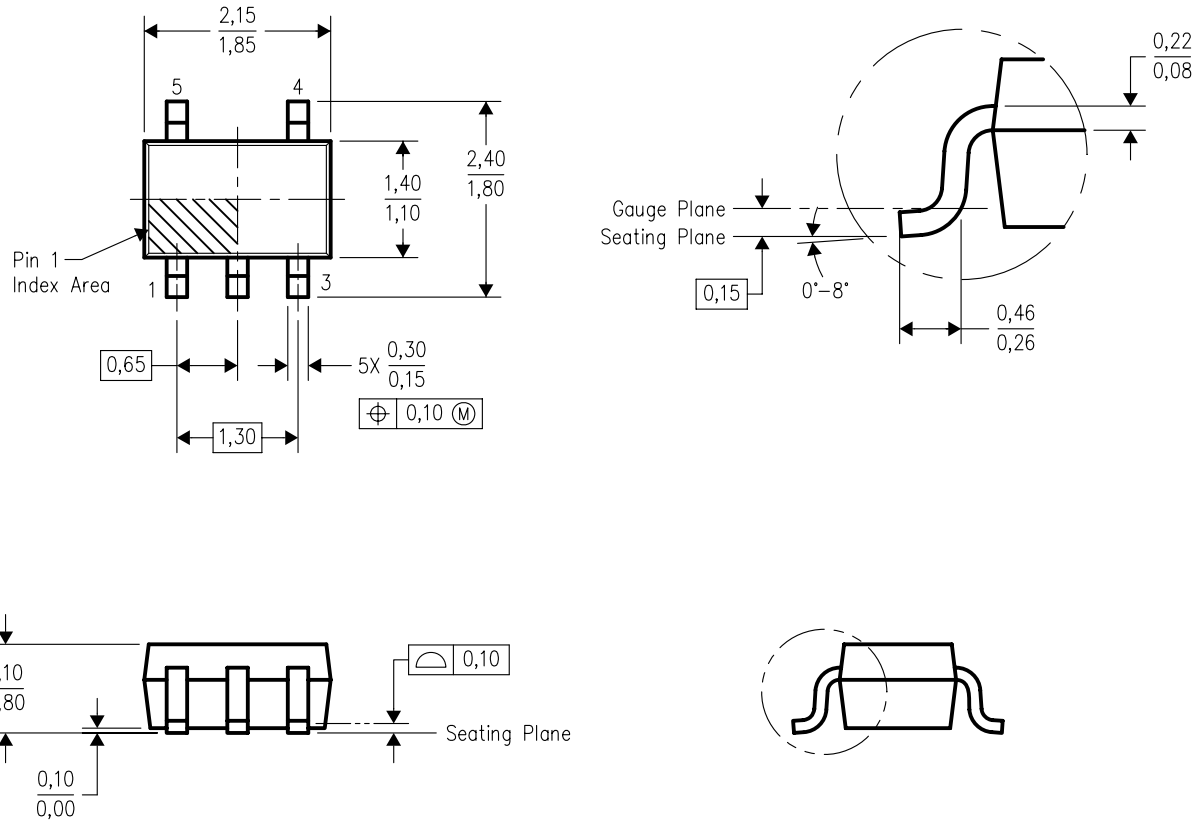
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

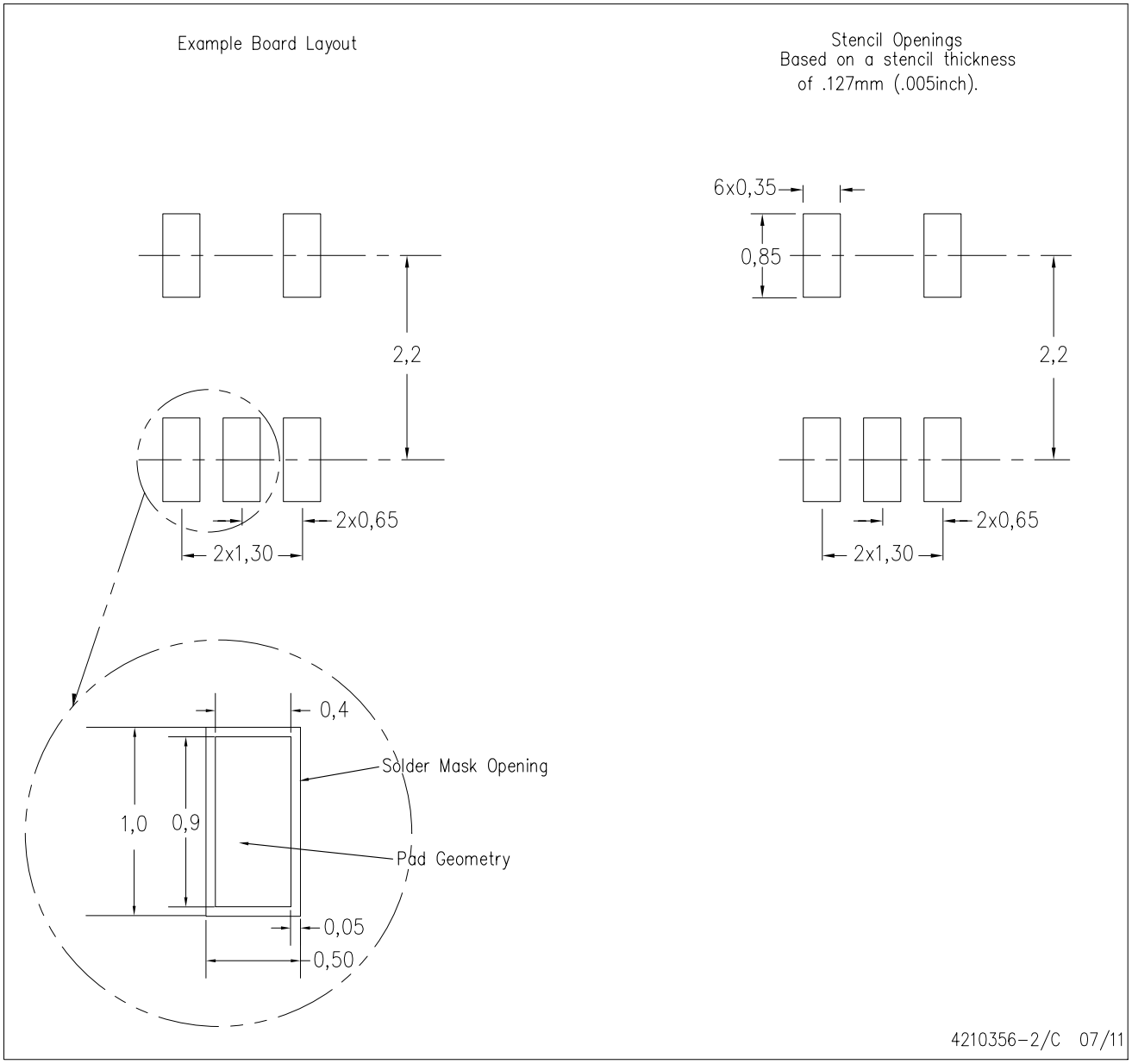
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

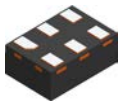
DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

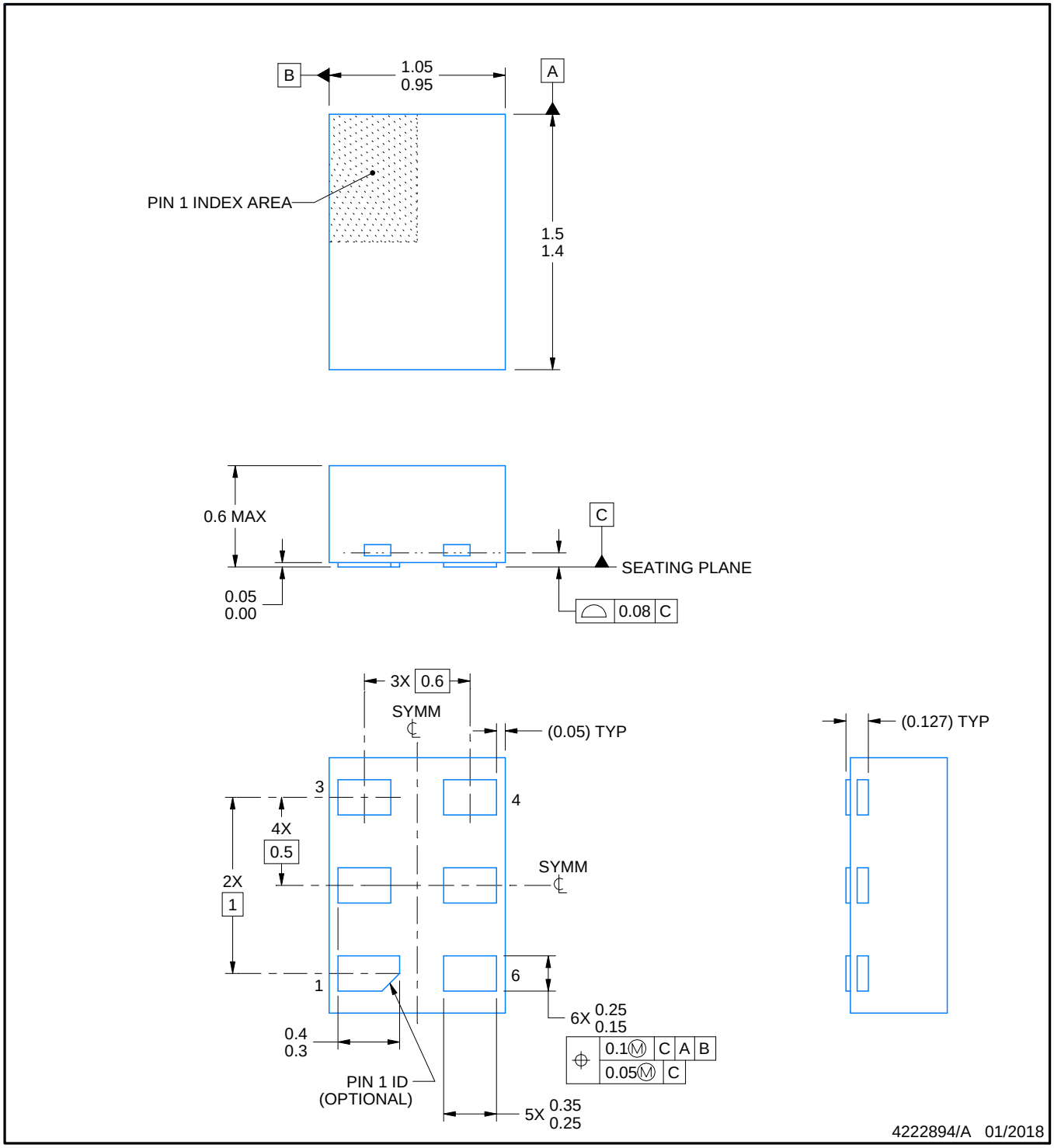
DRY0006A



PACKAGE OUTLINE

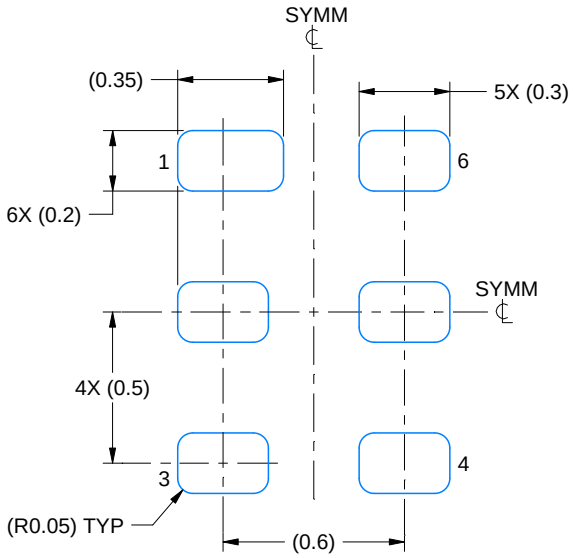
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

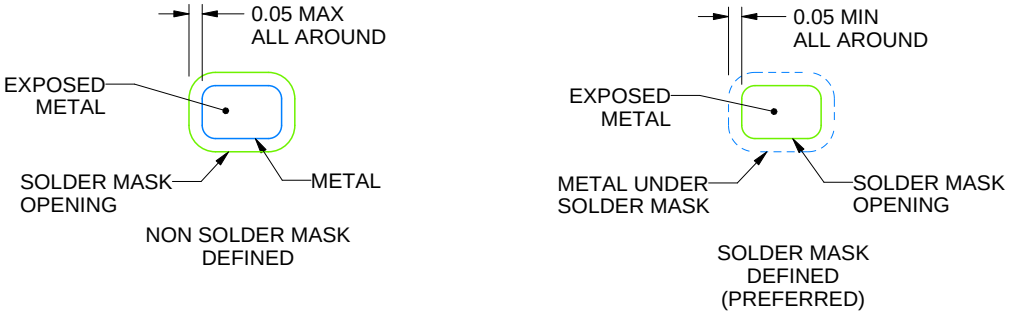


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

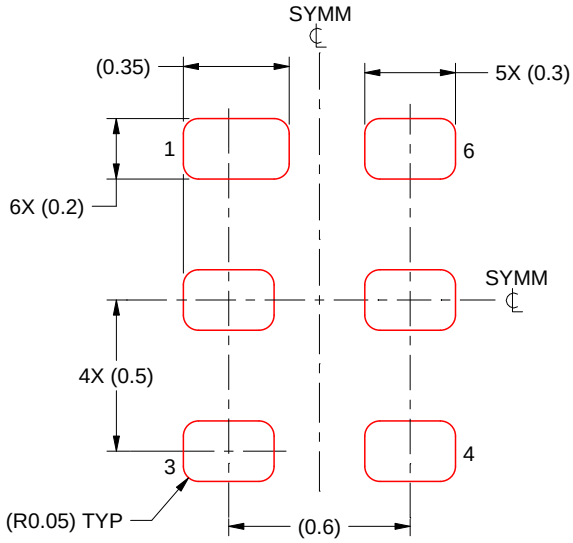
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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