OPA164x-Q1 SoundPlus™ JFET 输入汽车级音频运算放大器

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度等级 1：环境工作温度范围为 –40°C 至 +125°C
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 低噪声：1kHz 时为 5.1 nV/√Hz
- 超低失真：1kHz 时为 0.00005%
- 高转换率：20V/μs
- 单位增益稳定
- 无相位反转
- 低静态电流：每通道 1.8mA
- 轨到轨输出
- 宽电源电压范围：±2.25V 至 ±18V
- 单路、双路、四路版本可用

2 应用

- 汽车
- HEV 和 EV 动力传动
- 高级驾驶员辅助系统 (ADAS)
- 信息娱乐系统
- 车内麦克风

3 说明

OPA1641-Q1（单路）和 OPA1642-Q1（双路）系列均属于 JFET 输入、超低失真、低噪声运算放大器，可完全适用于音频 设计。

轨至轨输出摆幅可增加余量，使这些器件非常适合用于任何音频电路中。特性 包括：5.1nV/√Hz 噪声，低总谐波失真 + 噪声 (THD+N) (0.00005%)，2 pA 低输入偏置电流，以及每通道 1.8mA 的低静态电流。

这些器件可在 ±2.25V 至 ±18V 的极宽电源电压范围内工作。OPA164x-Q1 系列运算放大器具有稳定的单位增益，在各种负载条件下可提供出色的动态行为。

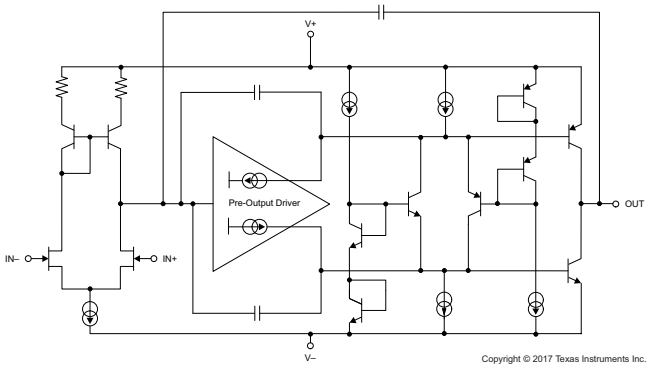
双路版本 具有 完全独立的电路，可将串扰降到最低，即使在过驱动或过载时也不受通道间相互作用的影响。

器件信息(1)

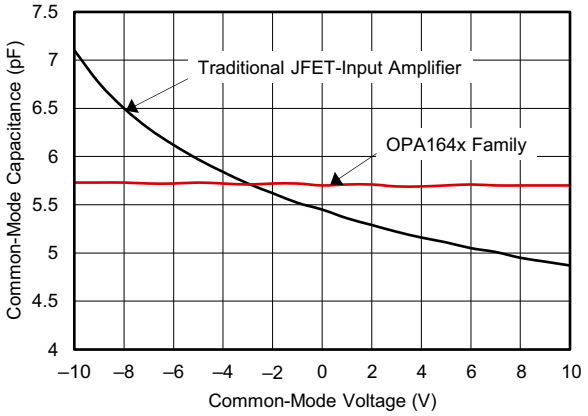
器件型号	封装	封装尺寸（标称值）
OPA1641-Q1	SOIC (8)	4.90mm × 3.90mm
	VSSOP (8)	3.00mm × 3.00mm
OPA1642-Q1	SOIC (8)	4.90mm × 3.90mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化内部原理图



极为稳定的输入电容



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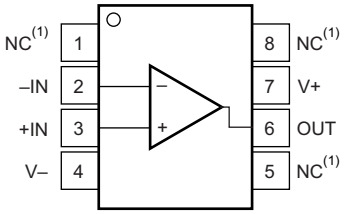
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (June 2017) to Revision A	Page
• Added separate A_{OL} values for OPA1642-Q1	6

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5 Pin Configuration and Functions

OPA1641-Q1: D and DGK Packages
8-Pin SOIC and VSSOP
Top View

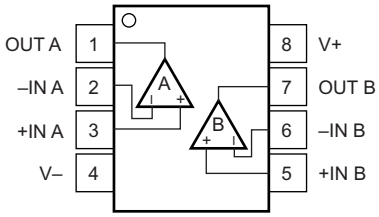


(1) NC - no internal connection

Pin Functions: OPA1641-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	2	I	Inverting input
+IN	3	I	Noninverting input
NC	1, 5, 8	—	No connection
OUT	6	O	Output
V–	4	—	Negative (lowest) power supply
V+	7	—	Positive (highest) power supply

OPA1642-Q1: D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Pin Functions: OPA1642-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		40	V
V_{IN}	Input voltage(2)	(V–) – 0.5	(V+) + 0.5	V
I_{IN}	Input current(2)		±10	mA
$V_{IN(DIFF)}$	Differential input voltage		±VS	V
I_O	Output short-circuit(3)	Continuous		
T_A	Operating temperature	–55	125	°C
T_J	Junction temperature	–65	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less. The input voltage and output negative-voltage ratings can be exceeded if the input and output current ratings are followed.
(3) Short-circuit to V_S / 2 (ground in symmetrical dual-supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±3000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage (V+, V–)	Single supply	4.5		36	V
	Dual supply	±2.25		±18	
Specified temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA1641-Q1, OPA1642-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9	n/a	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at T_A = 25°C, V_S = 4.5 V to 36 (±2.25 V to ±18 V), R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}		0.00005%		
				–126		dB
IMD	Intermodulation distortion	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz), G = 1, V_O = 3 V_{RMS}		0.00004%		
				–128		dB
		DIM 30 (3-kHz square wave and 15-kHz sine wave), G = 1, V_O = 3 V_{RMS}		0.00008%		
				–122		dB
		CCIF twin-tone (19 kHz and 20 kHz), G = 1, V_O = 3 V_{RMS}		0.00007%		
				–123		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 1		11		MHz
SR	Slew rate	G = 1		20		V/µs
	Full-power bandwidth(1)	V_O = 1 V_P		3.2		MHz
	Overload recovery time(2)	G = –10		600		ns
	Channel separation (dual and quad)	f = 1 kHz		–126		dB
NOISE						
	Input voltage noise	f = 20 Hz to 20 kHz		4.3		μV_{PP}
e_n	Input voltage noise density	f = 10 Hz		8		nV/√Hz
		f = 100 Hz		5.8		
		f = 1 kHz		5.1		
I_n	Input current noise density	f = 1 kHz		0.8		fA/√Hz
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±18 V		1	3.5	mV
PSRR	V_{OS} vs power supply	V_S = ±2.25 V to ±18 V		0.14	2	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		±2	±20	pA
I_{OS}	Input offset current	V_{CM} = 0 V		±2	±20	pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	V_{CM} = (V–) – 0.1 V to (V+) – 3.5 V, V_S = ±18 V	120	126		dB
INPUT IMPEDANCE						
	Differential			10^{13} || 8		Ω || pF
	Common-mode	V_{CM} = (V–) – 0.1 V to (V+) – 3.5 V		10^{13} || 6		Ω || pF

(1) Full power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) See Figure 19 and Figure 20.

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Electrical Characteristics (continued)

at T_A = 25°C, V_S = 4.5 V to 36 (±2.25 V to ±18 V), R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	OPA1641-Q1: (V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ	120	134		dB
		OPA1641-Q1: (V–) + 0.35 V ≤ V_O ≤ (V+) – 0.35 V, R_L = 2 kΩ	114	126		
		OPA1642-Q1: (V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ	114	134		
		OPA1642-Q1: (V–) + 0.35 V ≤ V_O ≤ (V+) – 0.35 V, R_L = 2 kΩ	111	126		
OUTPUT						
V_O	Voltage output swing from rail	R_L = 10 kΩ, A_{OL} ≥ 120 dB (OPA1641-Q1) A_{OL} ≥ 114 dB (OPA1642-Q1)	(V–) + 0.2		(V+) – 0.2	V
		R_L = 2 kΩ, A_{OL} ≥ 114 dB (OPA1641-Q1) A_{OL} ≥ 111 dB (OPA1642-Q1)	(V–) + 0.35		(V+) – 0.35	
I_{OUT}	Output current		See *Typical Characteristics*			
Z_O	Open-loop output impedance		See *Typical Characteristics*			
I_{SC}	Short-circuit current	Source		36		mA
		Sink		–30		
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			
POWER SUPPLY						
V_S	Specified voltage		±2.25		±18	V
I_Q	Quiescent current (per amplifier)	I_{OUT} = 0 A		1.8	2.3	mA
TEMPERATURE RANGE						
	Specified range		–40		125	°C
	Operating range		–55		125	°C

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6.6 Typical Characteristics

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

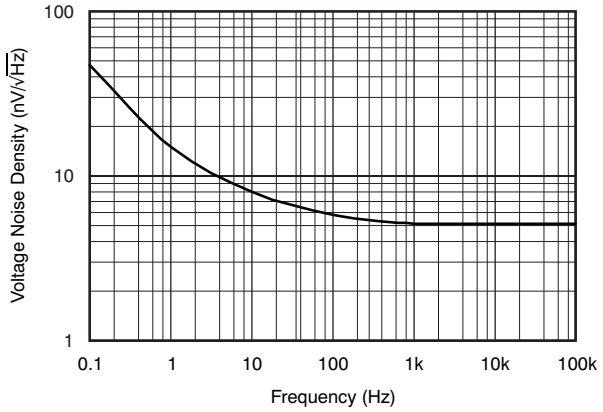


图 1. Input Voltage Noise Density vs Frequency

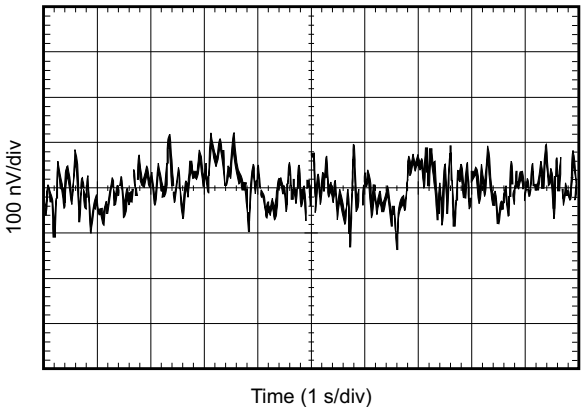


图 2. 0.1-Hz to 10-Hz Noise

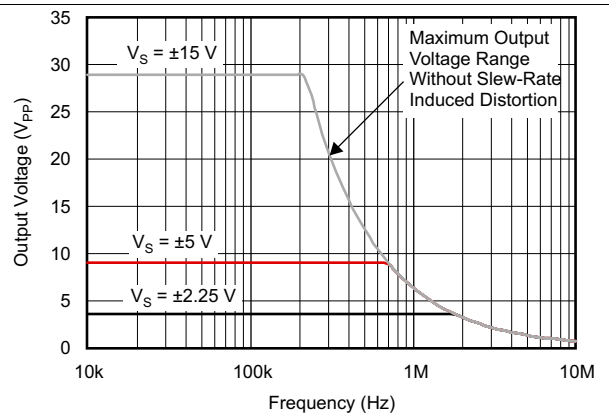


图 3. Maximum Output Voltage vs Frequency

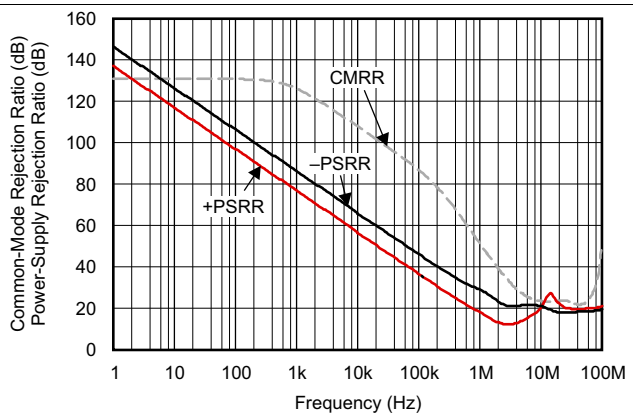


图 4. CMRR and PSRR vs Frequency (Referred to Input)

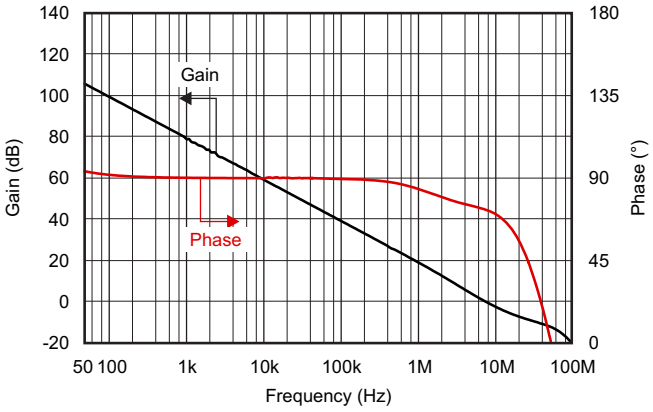


图 5. Gain and Phase vs Frequency

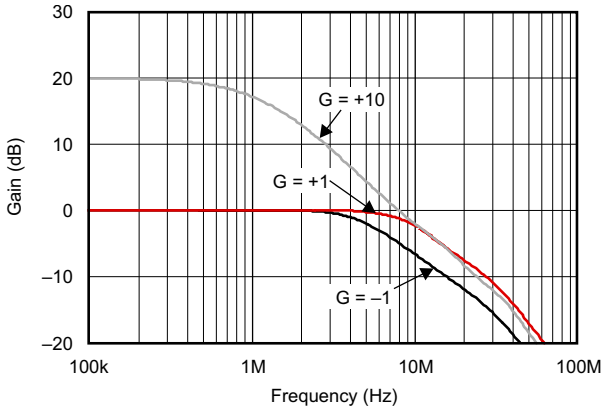
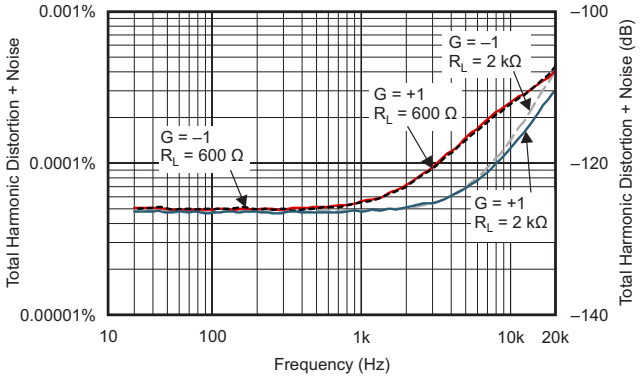


图 6. Closed-Loop Gain vs Frequency

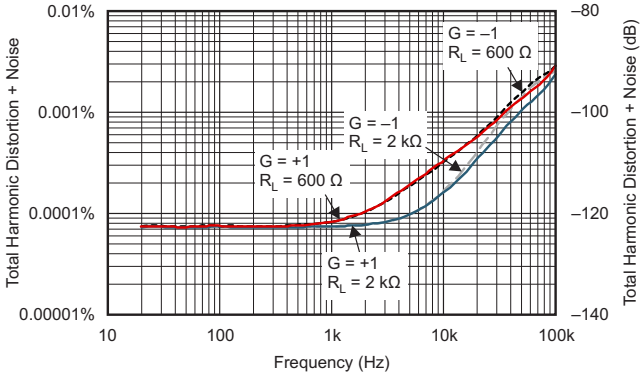
Typical Characteristics (接下页)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)



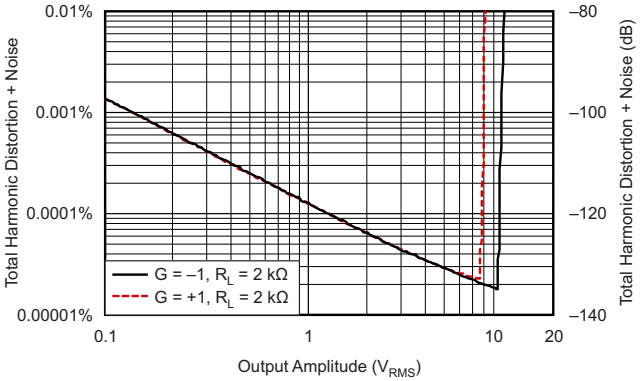
VOUT = 3 V_{RMS} BW = 80 kHz

图 7. THD+N Ratio vs Frequency



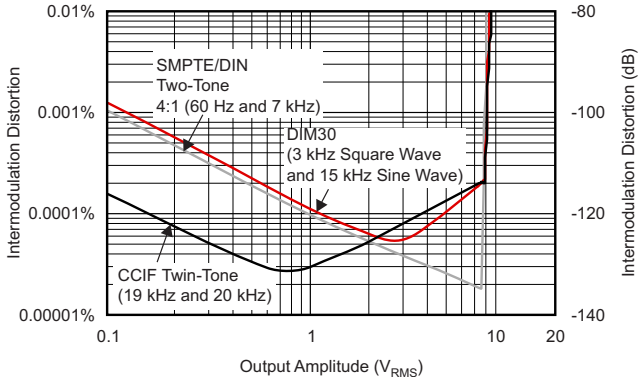
VOUT = 3 V_{RMS} BW > 500 kHz

图 8. THD+N Ratio vs Frequency



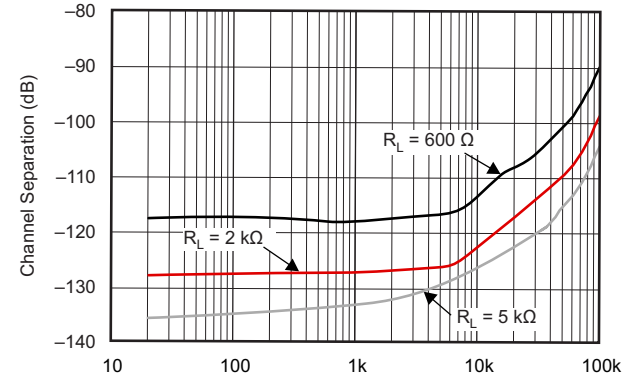
BW = 80 kHz 1 kHz Signal R_{SOURCE} = 0 Ω

图 9. THD+N Ratio vs Output Amplitude



G = 1

图 10. Intermodulation Distortion vs Output Amplitude



V_S = ±15 V V_{OUT} = 3 V_{RMS} G = 1

图 11. Channel Separation vs Frequency

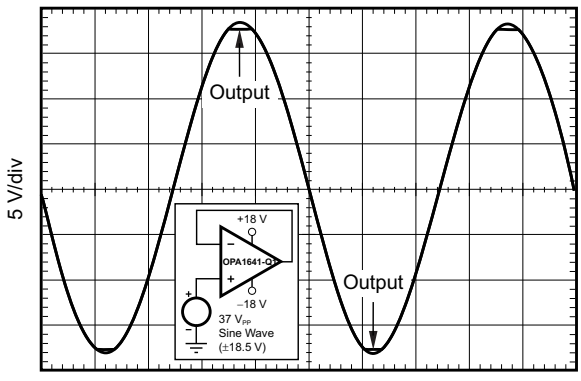
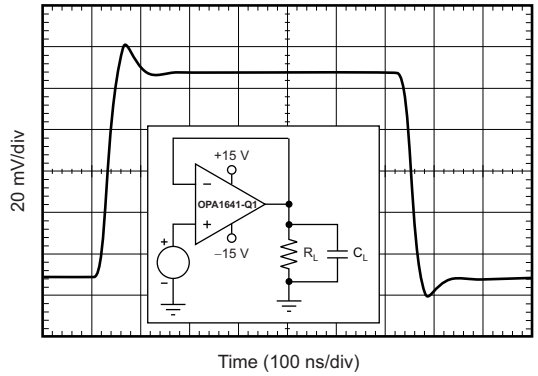


图 12. No Phase Reversal

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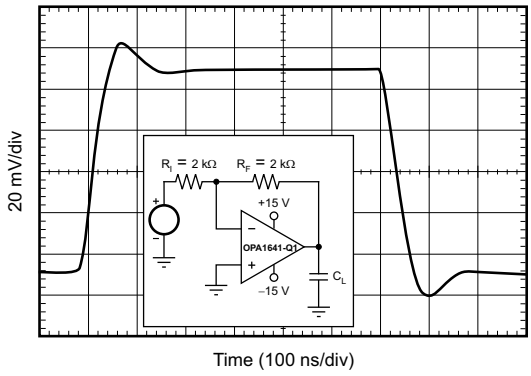
Typical Characteristics (接下页)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)



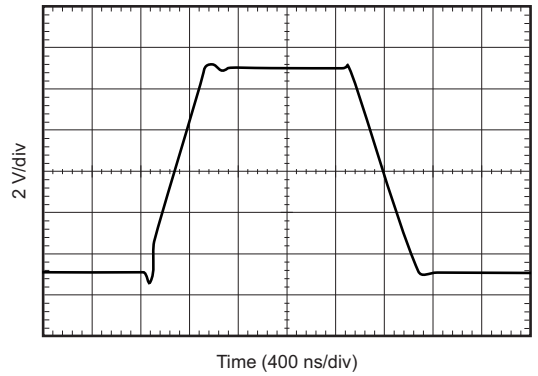
G = 1 C_L = 100 pF

图 13. Small-Signal Step Response (100 mV)



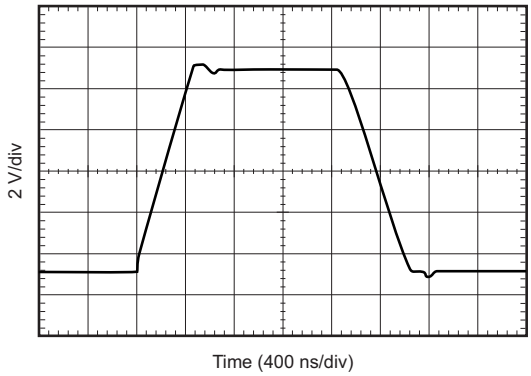
G = –1 C_L = 100 pF

图 14. Small-Signal Step Response (100 mV)



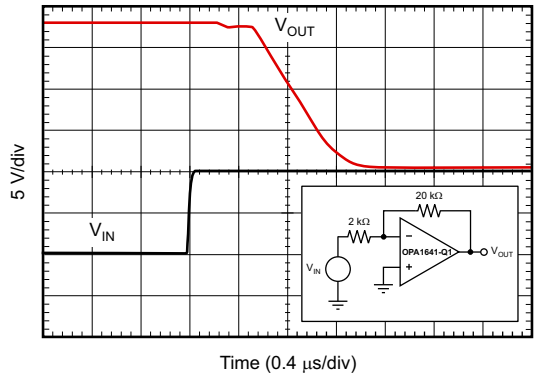
G = 1 C_L = 100 pF

图 15. Large-Signal Step Response



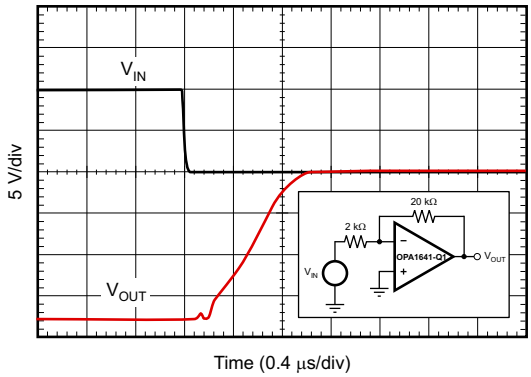
G = –1 C_L = 100 pF

图 16. Large-Signal Step Response



G = –10

图 17. Positive Overload Recovery



G = –10

图 18. Negative Overload Recovery

Typical Characteristics (接下页)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

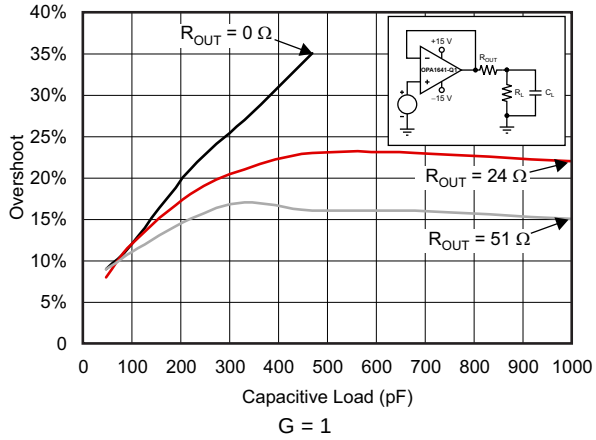


图 19. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

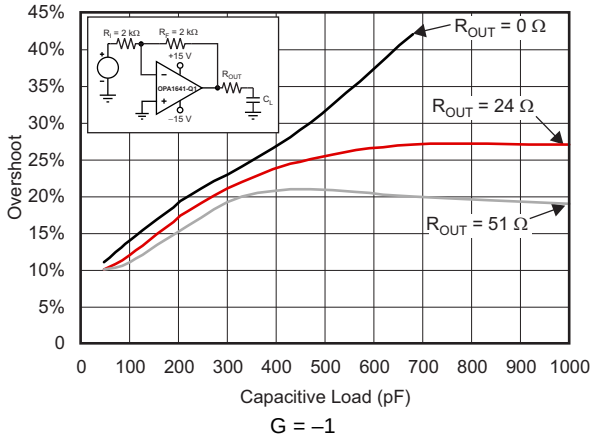


图 20. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

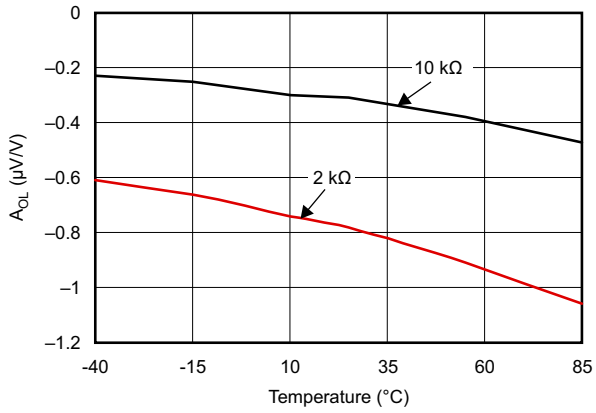


图 21. Open-Loop Gain vs Temperature

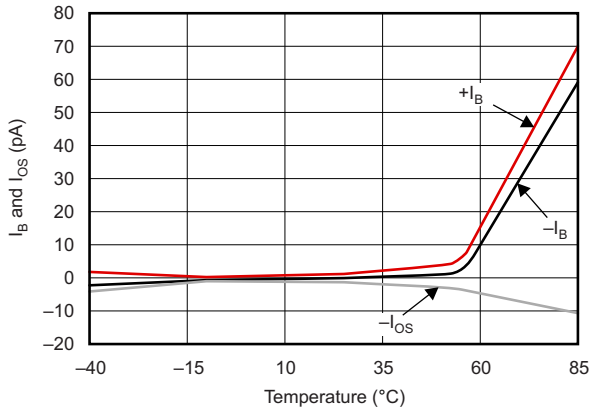


图 22. I_B and I_{OS} vs Temperature

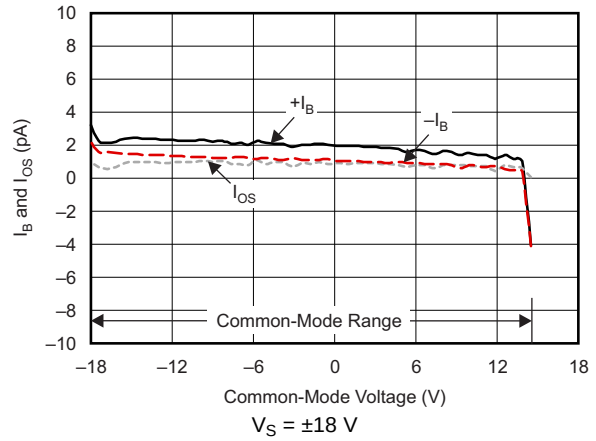


图 23. I_B and I_{OS} vs Common-Mode Voltage

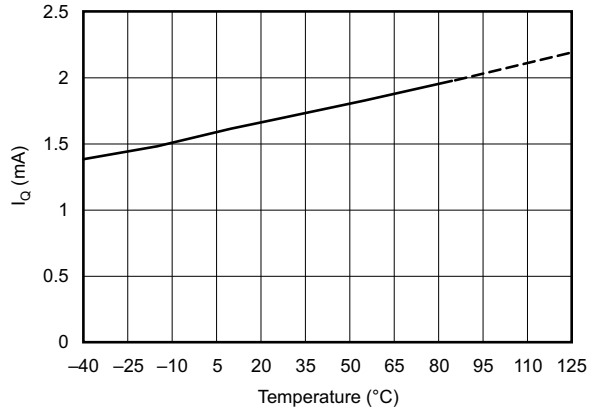


图 24. Quiescent Current vs Temperature

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Typical Characteristics (接下页)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

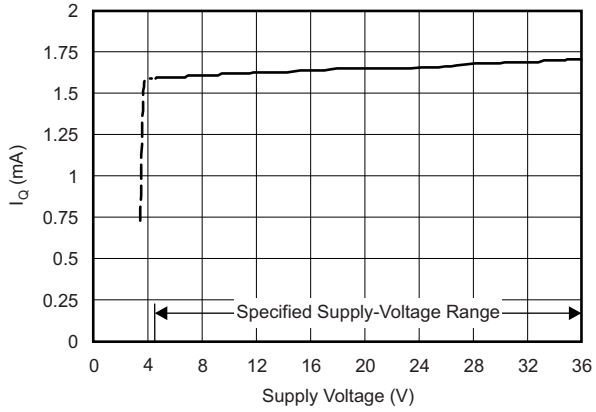
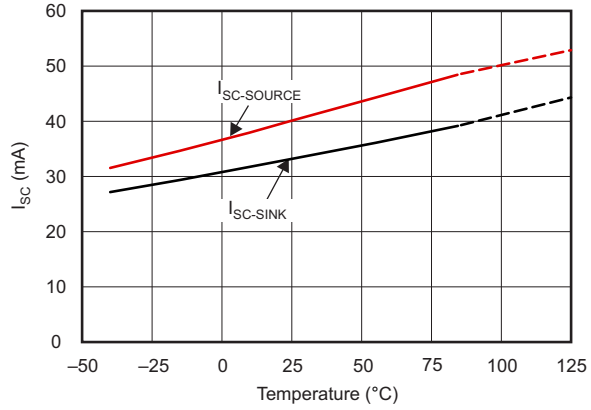


图 25. Quiescent Current vs Supply Voltage



V_{OUT} = Midsupply (includes self-heating)

图 26. Short-Circuit Current vs Temperature

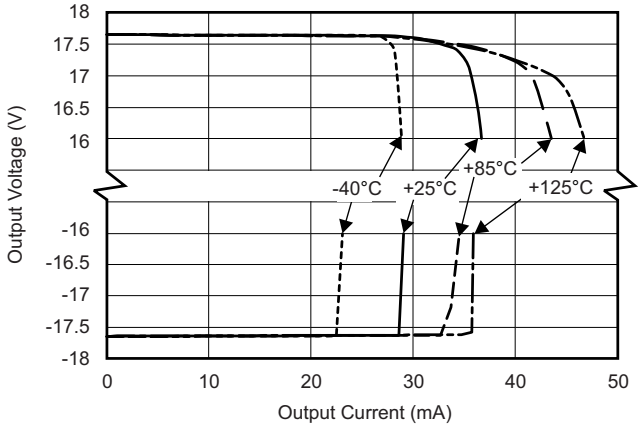


图 27. Output Voltage vs Output Current

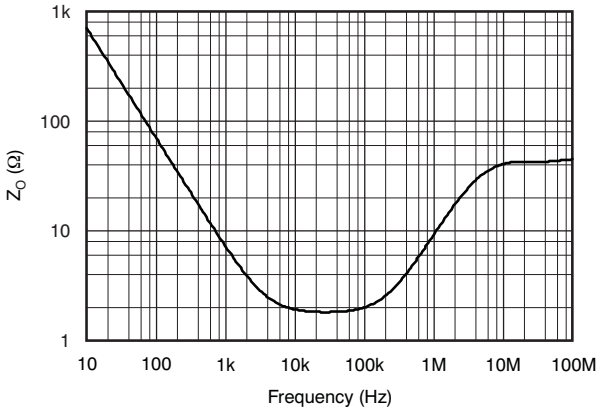


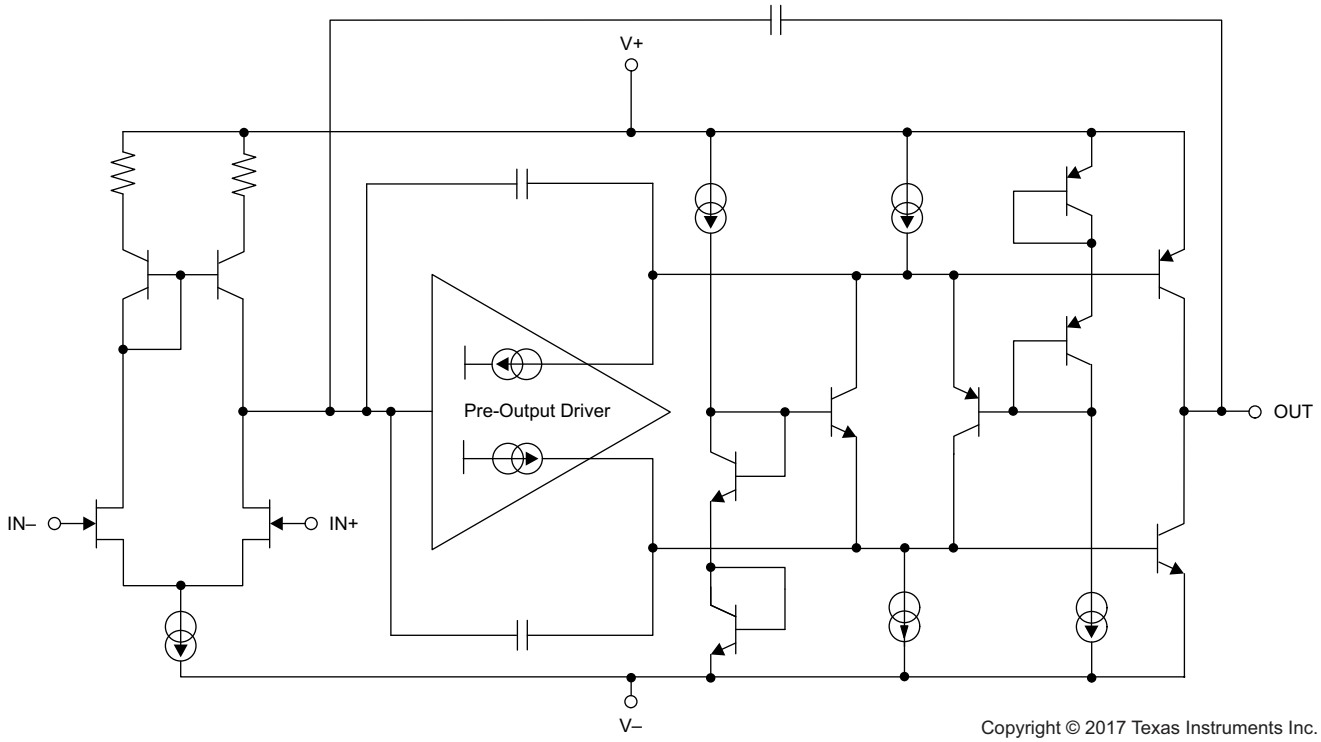
图 28. Open-Loop Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The OPA164x-Q1 family of operational amplifiers combine an ultra-low noise JFET input stage with a rail-to-rail output stage to provide high overall performance in audio applications. The internal topology is selected specifically to deliver extremely low distortion, consume limited power, and accommodate small packages. These amplifiers are well-suited for analog signal processing applications such as active filter circuits, pre-amplifiers, and tone controls. The unique input stage design and semiconductor processes used in this device deliver extremely high performance even in applications with high source impedance and wide common-mode voltage swings.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Phase Reversal Protection

The OPA164x-Q1 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA164x-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in 图 29.

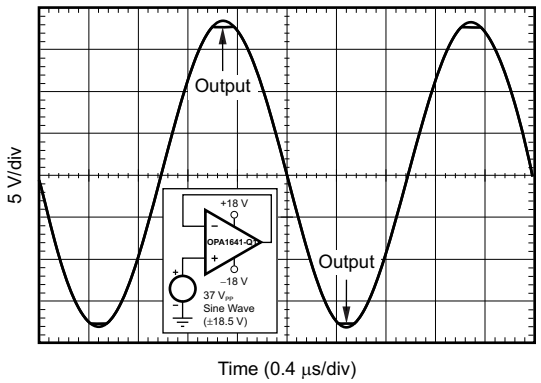


图 29. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

7.3.2 Output Current Limit

The output current of the OPA164x-Q1 series is limited by internal circuitry to 36 mA and –30 mA (sourcing and sinking), to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature; see 图 26.

Although uncommon for most modern audio applications to require 600-Ω load drive capability, many audio operational amplifier applications continue to specify the total harmonic distortion (THD+N) at 600-Ω load for comparative purposes. 图 7 and 图 8 provide typical THD+N measurement curves for the OPA164x-Q1 series, where the output drives a 3-V_{RMS} signal into a 600-Ω load. However, correct device operation cannot be ensured when driving 600-Ω loads at full supply. Depending on supply voltage and temperature, this operating condition can possibly trigger the output current limit circuitry of the device.

7.3.3 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this document provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report *EMI Rejection Ratio of Operational Amplifiers*, available for download at www.ti.com.

Feature Description (接下页)

The EMIRR IN+ of the OPA164x-Q1 is plotted versus frequency in 图 30. If available, any dual and quad operational amplifier device versions have nearly identical EMIRR IN+ performance. The OPA164x-Q1 unity-gain bandwidth is 11 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

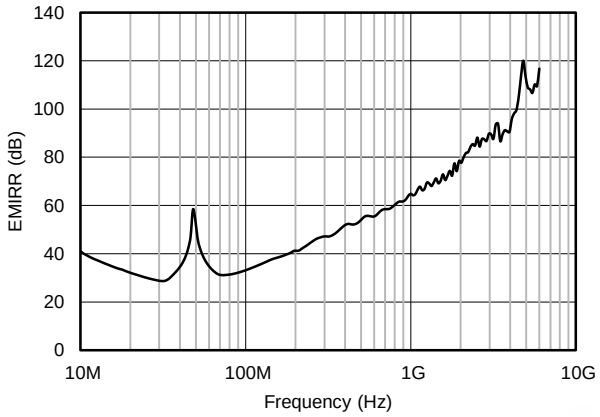


图 30. OPA164x-Q1 EMIRR vs Frequency

表 1 lists the EMIRR IN+ values for the OPA164x-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 1 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

表 1. OPA164x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, UHF	53.1 dB
900 MHz	GSM, radio communication and navigation, GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	72.2 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	80.7 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio and satellite, S-band	86.8 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	91.7 dB
5 GHz	802.11a/n, aero communication and navigation, mobile communication, space and satellite operation, C-band	96.6 dB

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7.3.3.1 EMIRR IN+ Test Configuration

图 31 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. See *EMI Rejection Ratio of Operational Amplifiers* for more details.

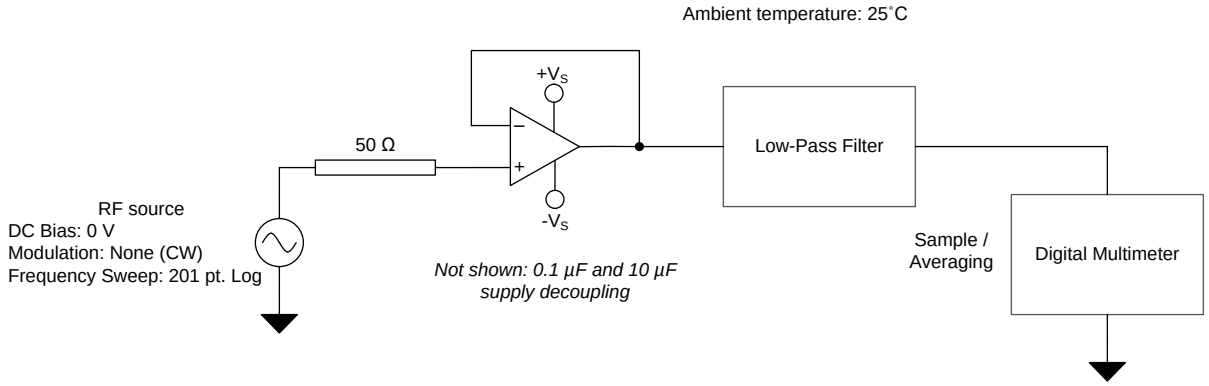


图 31. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

7.4.1 Operating Voltage

The OPA164x-Q1 series of operational amplifiers can be used with single or dual supplies from an operating range of V_S = 4.5 V (±2.25 V) and up to V_S = 36 V (±18 V). These devices do not require symmetrical supplies; only a minimum supply voltage of 4.5 V (±2.25 V) is required. For V_S less than ±3.5 V, the common-mode input range does not include midsupply. Supply voltages higher than 40 V can permanently damage the device; see *Absolute Maximum Ratings* for more information. Key parameters are specified over the operating temperature range, T_A = –40°C to +85°C. Key parameters that vary over the supply voltage or temperature range are shown in *Typical Characteristics*.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA164x-Q1 amplifiers are unity-gain stable, audio operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-μF capacitors are adequate. 图 32 shows a simplified schematic of the OPA1641-Q1.

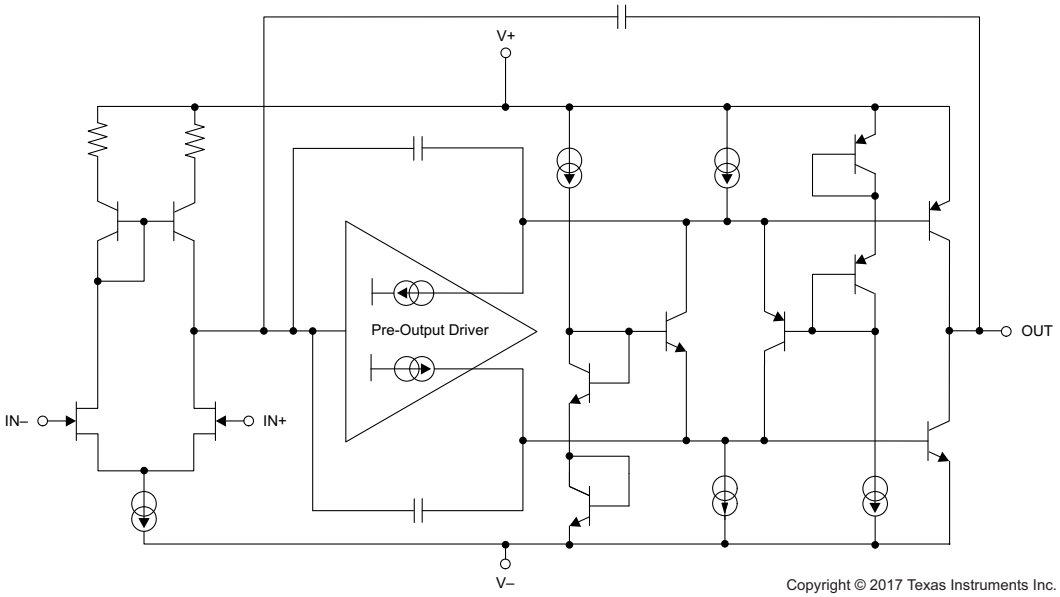


图 32. Simplified Internal Schematic

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Application Information (接下页)

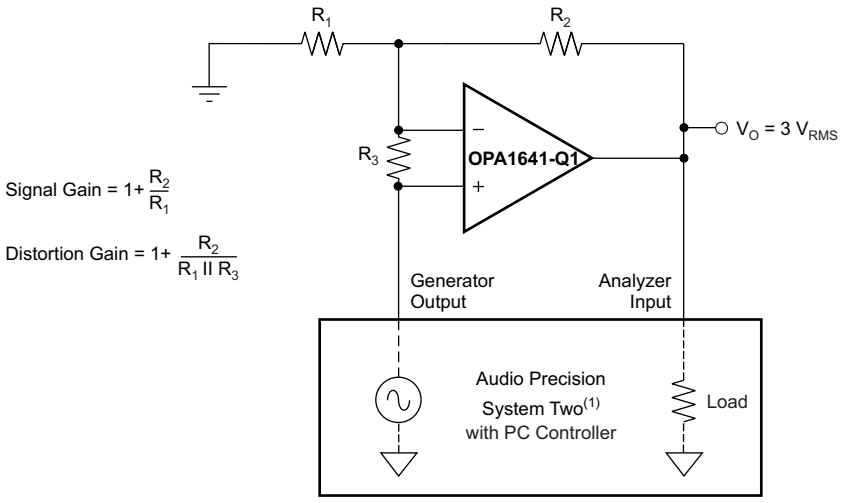
8.1.1 Total Harmonic Distortion Measurements

The OPA164x-Q1 series operational amplifiers have excellent distortion characteristics. THD + noise is below 0.00005% (G = 1, V_O = 3 V_{RMS}, BW = 80 kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see 图 7).

The distortion produced by the OPA164x-Q1 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as shown in 图 33) can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. 图 33 shows a circuit that causes the operational amplifier distortion to be 101 times (or approximately 40 dB) greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, extending the resolution by 101. The input signal and load applied to the op amp are the same as with conventional feedback without R_3. Keep the value of R_3 small to minimize any effect on distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this document were made with an audio precision system two distortion and noise analyzer that greatly simplifies repetitive measurements. However, the measurement technique can be performed with manual distortion measurement instruments.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
1	101	∞	1 kΩ	10 Ω
11	101	100 Ω	1 kΩ	11 Ω

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(1) For measurement bandwidth, see 图 7 through 图 10.

图 33. Distortion Test Circuit

8.1.2 Source Impedance and Distortion

In traditional JFET-input op amps, the impedance applied to the positive and negative inputs in noninverting applications must be matched for lowest distortion. Legacy methods for fabricating the JFETs in the FET input stage exhibit a varying input capacitance with applied common-mode input voltage. In inverting configurations, the input does not vary with input voltage because the inverting input is held at virtual ground. However, in noninverting applications, the inputs do vary, and the gate-to-source voltage is not constant. This effect produces increased distortion resulting from the varying capacitance for unmatched source impedances. However, the OPA164x-Q1 family of amplifiers is designed to maintain a constant input capacitance with varying common-mode voltage to prevent this mechanism of distortion. The variation of input capacitance with common-mode voltage for a traditional amplifier is compared to the OPA164x-Q1 family in 图 34.

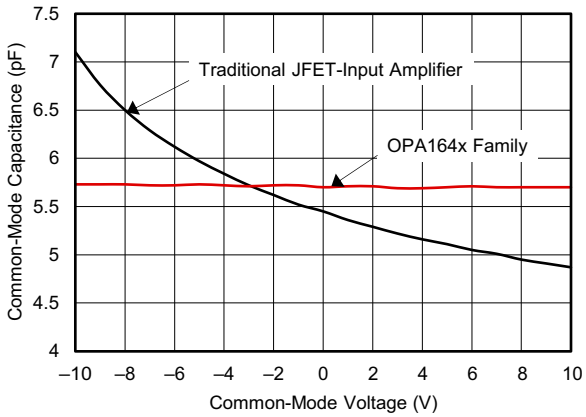


图 34. Input Capacitance of the OPA164x-Q1 Family of Amplifiers Compared to Traditional JFET-input Amplifiers

By stabilizing the input capacitance, the distortion performance of the amplifier is greatly improved for noninverting configurations with high source impedances. The measured performance of an OPA164x-Q1 amplifier is compared to a traditional JFET-input amplifier in 图 35. The unity-gain configuration, high source impedance, and large-signal amplitude produce additional distortion in the traditional amplifier.

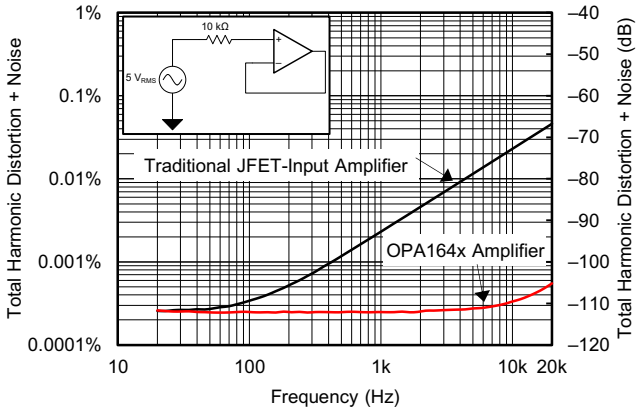


图 35. Measured THD+N of the OPA164x-Q1 Family of Amplifiers Compared to Traditional JFET-input Amplifiers

8.1.3 Capacitive Load and Stability

The dynamic characteristics of the OPA164x-Q1 are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω, for example) in series with the output.

图 19 and 图 20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT}. For details of analysis techniques and application circuits, see see *Feedback Plots Define Op Amp AC Performance* available for download at www.ti.com

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8.1.4 Power Dissipation and Thermal Protection

The OPA164x-Q1 op amps are capable of driving 2-kΩ loads with power-supply voltages of up to ±18 V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8 kΩ at a supply voltage of 36 V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance can be used, as long as the output current does not exceed 13 mA; otherwise, the device short-circuit current-protection circuit can activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA164x-Q1 series of devices improves heat dissipation compared to conventional materials. PCB layout can help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by functioning as an additional heat sink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to midsupply, the typical short-circuit current of 36 mA leads to an internal power dissipation of over 600 mW at a supply of ±18 V. In case of a dual OPA1642-Q1 in an VSSOP-8 package (thermal resistance $R_{\theta JA}$ = 180°C/W), such a power dissipation results in the die temperature to be 220°C above ambient temperature, when both channels are shorted. This temperature increase destroys the device.

To prevent such excessive heating that can destroy the device, the OPA164x-Q1 series has an internal thermal shutdown circuit that shuts down the device if the die temperature exceeds approximately 180°C. When this thermal shutdown circuit activates, a built-in hysteresis of 15°C ensures that the die temperature must drop to approximately 165°C before the device switches on again.

8.1.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 图 36 illustrates the ESD circuits contained in the OPA164x-Q1 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines where an internal absorption device is connected. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger (or threshold voltage) that is above the normal operating voltage of the OPA164x-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

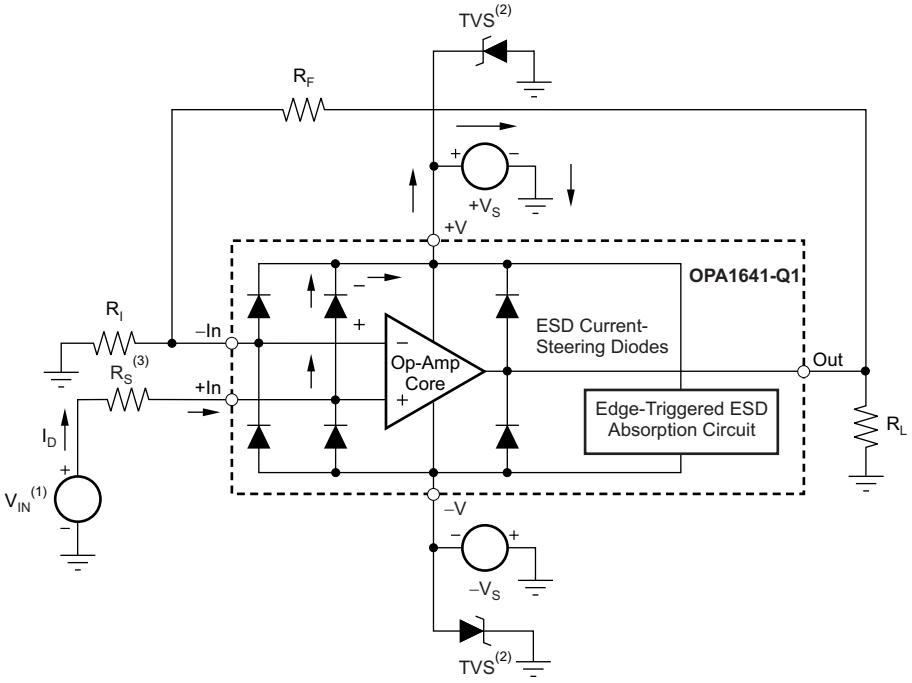
When the operational amplifier connects into a circuit as shown in 图 36, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, some of the internal ESD protection circuits can be biased on and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

图 36 depicts a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies $+V_S$ and $–V_S$ are at 0 V. The amplifier behavior depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes can be added to the supply pins, as shown in 图 36. The Zener voltage must be selected so the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



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(1) $V_{IN} = +V_S + 500$ mV.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value is approximately 1 kΩ.

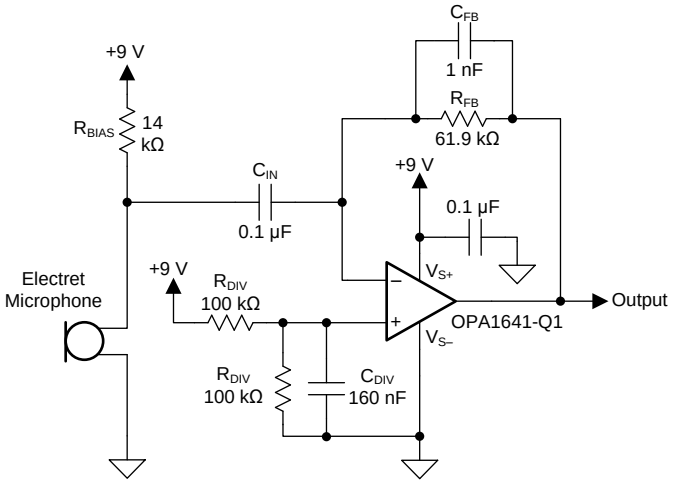
图 36. Equivalent Internal ESD Circuitry and the Relation to a Typical Circuit Application

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8.2 Typical Application

8.2.1 Single-Supply Electret Microphone Preamplifier for Speech

Electret microphones are commonly used in automotive hands-free phone systems because of their small size, low cost, and relatively good signal-to-noise ratio (SNR). The low noise and distortion of the OPA1641-Q1 makes the device a good choice for preamplifier circuits for electret microphones. The circuit shown in 图 37 is a single-supply preamplifier circuit for electret microphones with a bandwidth from 100 Hz to 3 kHz for capturing speech.



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图 37. Preamplifier Circuit for Electret Microphones Using a Single Power Supply Voltage

8.2.1.1 Design Requirements

- 9-V single supply
- 1-V_{RMS} output for 100-dB_{SPL} input
- Approximately 100-Hz to 3-kHz, –3-dB Bandwidth
- Microphone sensitivity: 8 µA / Pa
- Microphone operating voltage: 2 V to 10 V
- Microphone bias current: 500 µA

8.2.1.2 Detailed Design Procedure

In this circuit, the op amp is configured as a transimpedance amplifier which converts the signal current of the microphone into an output voltage. The bandwidth of this circuit is limited to the vocal range as is common in telephony systems. The gain of the circuit is determined by the feedback resistor (R_{FB}), which must be calculated according to the microphone sensitivity. For this design, a microphone output current of 8 µA per Pascal (Pa) of air pressure was selected. Using this value, the output current for a sound pressure level of 100 dB_{SPL}, or 2 Pa air pressure, is calculated in 公式 1.

$$i_{mic} = \frac{8\ \mu A}{1\ Pa} \times 2\ Pa = 16\ \mu A \tag{1}$$

R_{FB} is then calculated from this current to produce 1-V_{RMS} output for a 100-dB_{SPL} input signal in 公式 2.

$$R_{FB} = \frac{V_O}{i_{mic}} = \frac{1\ V_{RMS}}{16\ \mu A} = 62500 \rightarrow 61.9\ k\Omega \tag{2}$$

The feedback capacitor (C_{FB}) is calculated to limit the bandwidth of the amplifier to 3 kHz in 公式 3.

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot R_{FB} \cdot f_H} = \frac{1}{2 \cdot \pi \cdot (61.9\ k\Omega) \cdot (3\ kHz)} = 857 \times 10^{-12} \rightarrow 1\ nF \tag{3}$$

Typical Application (接下页)

R_{BIAS} is necessary to divert the microphone signal current through capacitor C_{IN} rather than flowing from the power supply (V_{CC}). Larger values of R_{BIAS} allow for a smaller capacitor to be used for C_{IN} and reduces the overall noise of the circuit. However, the maximum value for R_{BIAS} is limited by the microphone bias current and minimum operating voltage.

The value of R_{BIAS} is calculated in 公式 4.

$$R_{BIAS} = \frac{V_{CC} - V_{MIC}}{I_{BIAS}} = \frac{9\ V - 2\ V}{500\ \mu A} = 14\ k\Omega \tag{4}$$

Input capacitor C_{IN} forms a high-pass filter in combination with resistor R_{BIAS}. The filter corner frequency calculation is shown in 公式 5 to place the high-pass corner frequency at 100 Hz.

$$C_{IN} = \frac{1}{2 \cdot \pi \cdot R_{BIAS} \cdot f_L} = \frac{1}{2 \cdot \pi \cdot (14\ k\Omega) \cdot (100\ Hz)} = 113.7 \times 10^{-9} \rightarrow 100\ nF \tag{5}$$

The voltage divider network at the op amp noninverting input is used to bias the op amp output to the midsupply point (V_{CC} / 2) to maximize the output voltage range of the circuit. This result is easily achieved by selecting the same value for both resistors in the divider. The absolute value of those resistors is limited by the acceptable power-supply current drawn by the voltage divider. Choosing 50 µA as an acceptable limit of supply current gives a value of 100 kΩ for the resistors in the divider, as 公式 6 shows.

$$R_{DIV} \geq \frac{V_{CC}}{2 \cdot I_{DIV}} \geq \frac{9\ V}{2 \cdot 50\ \mu A} \geq 90\ k\Omega \rightarrow 100\ k\Omega \tag{6}$$

Finally, to minimize the additional noise contribution from the voltage divider, a capacitor is placed at the op amp noninverting input. This capacitor forms a low-pass filter with the parallel combination of the voltage divider resistors. Selecting a filter corner frequency of 20 Hz minimizes the noise contribution of the voltage divider inside the amplifier passband; see 公式 7.

$$C_{DIV} = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{DIV}}{2}\right) \cdot f_L} = \frac{1}{2 \cdot \pi \cdot \left(\frac{100\ k\Omega}{2}\right) \cdot (20\ Hz)} = 1.592 \times 10^{-7} \rightarrow 160\ nF \tag{7}$$

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Typical Application (接下页)

8.2.1.3 Application Curve

The transfer function of the microphone preamplifier circuit is shown in 图 38. The nominal gain of the circuit is 95.46 dB, or 59,292.5 V per amp of input current. The –3-dB bandwidth limits of the circuit are 105.7 Hz and 2.77 kHz.

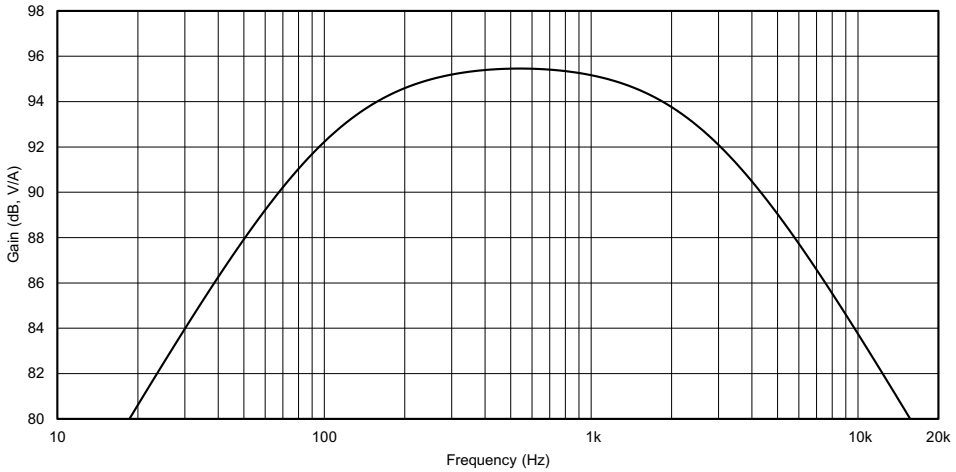


图 38. Microphone Preamplifier Transfer Function

9 Power Supply Recommendations

The OPA164x-Q1 devices are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

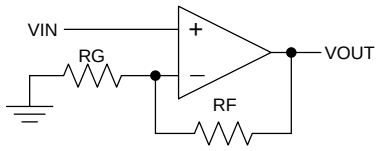
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in 图 39, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example



(Schematic Representation)

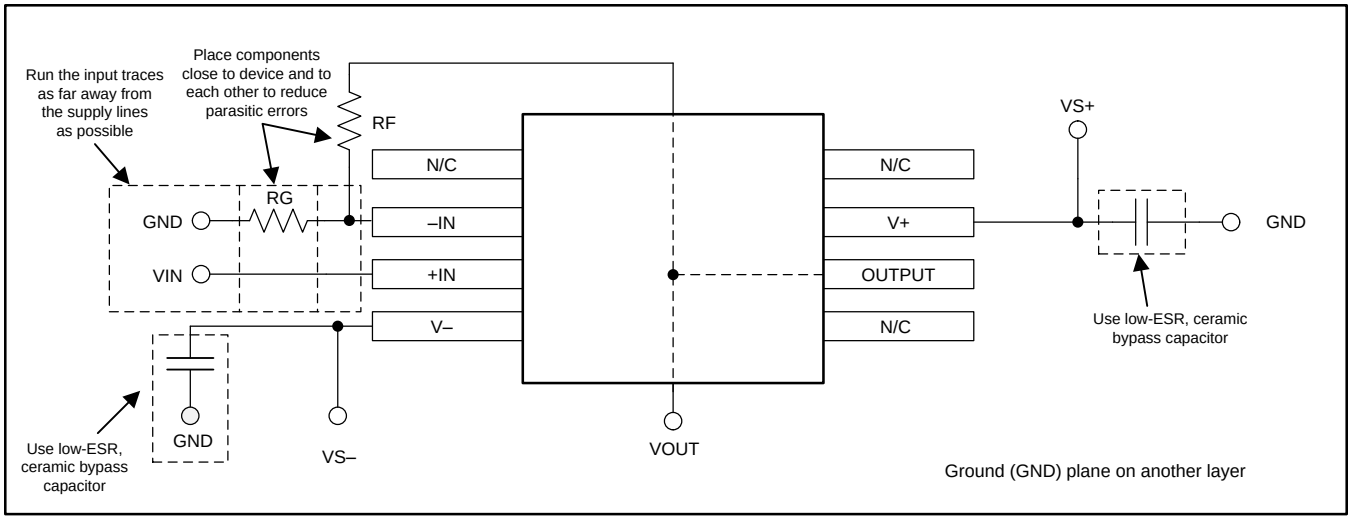


图 39. OPA1641-Q1 Layout Example

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11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 TI 高精度设计

TI 高精度设计（请访问 http://www.ti.com.cn/ww/analog/precision-designs/ 获取）是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

11.1.1.3 WEBENCH® 滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。借助 WEBENCH 滤波器设计器并选择使用 TI 运算放大器以及 TI 供应商合作伙伴提供的无源组件来构建优化滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在数分钟内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- *《运算放大器增益稳定性》，第 3 部分：交流增益误差分析*
- *《运算放大器增益稳定性》，第 2 部分：直流增益误差分析*
- *《在全差分有源滤波器中使用无限增益、MFB 滤波器拓扑》*
- *运算放大器性能分析*
- *运算放大器的单电源操作*
- *调优放大器*
- *无铅成品组件的储存寿命评估*

11.3 相关链接

表 2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
OPA1641-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA1642-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.6 商标

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1641AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1641	Samples
OPA1642AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1642	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

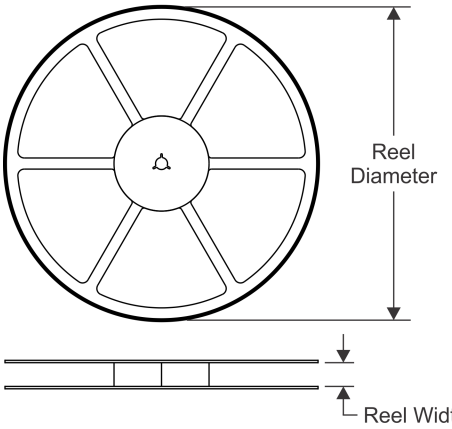
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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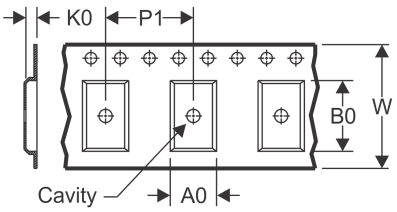
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

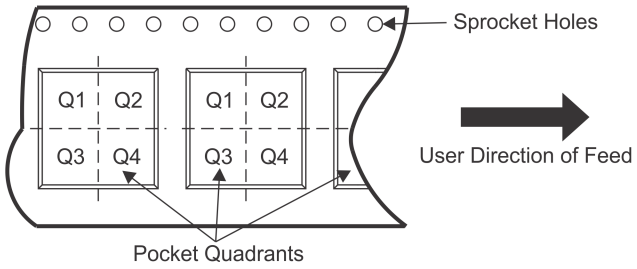


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

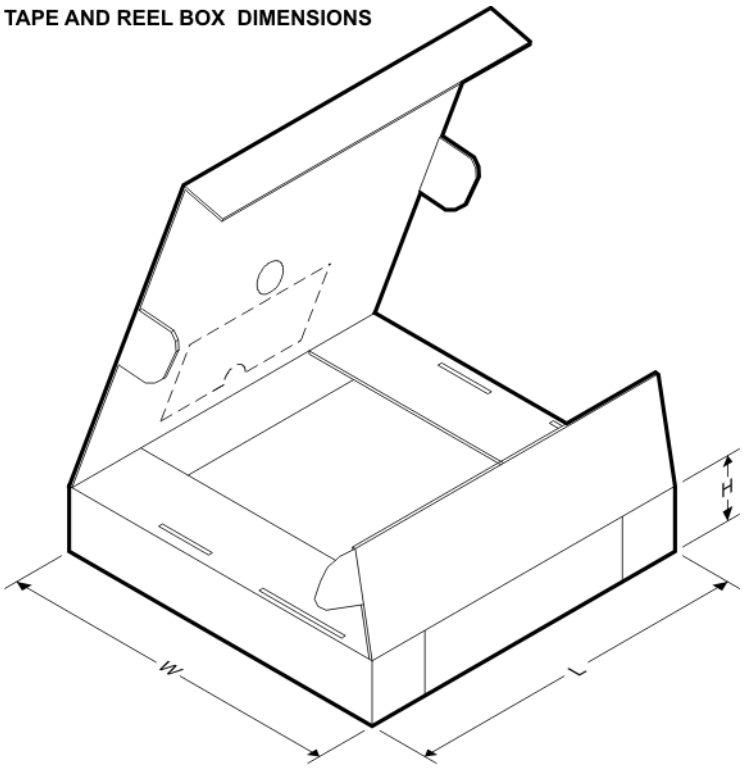
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1641AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

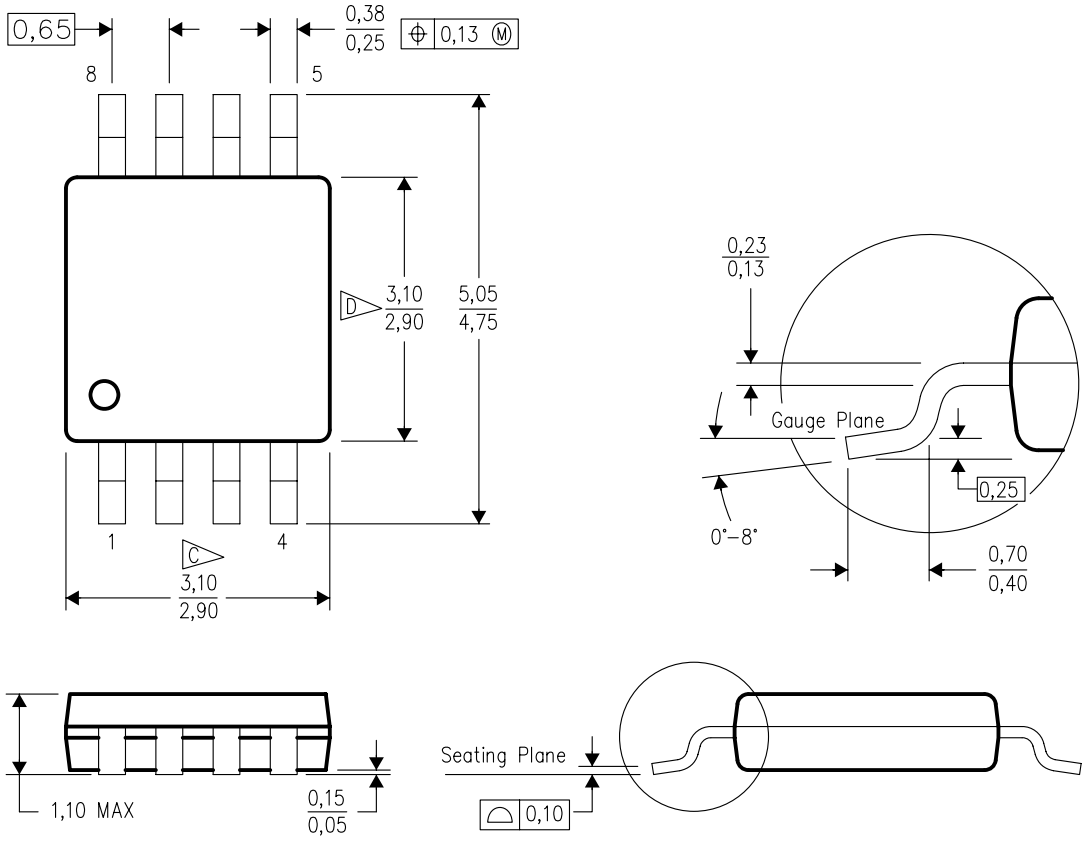
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1641AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

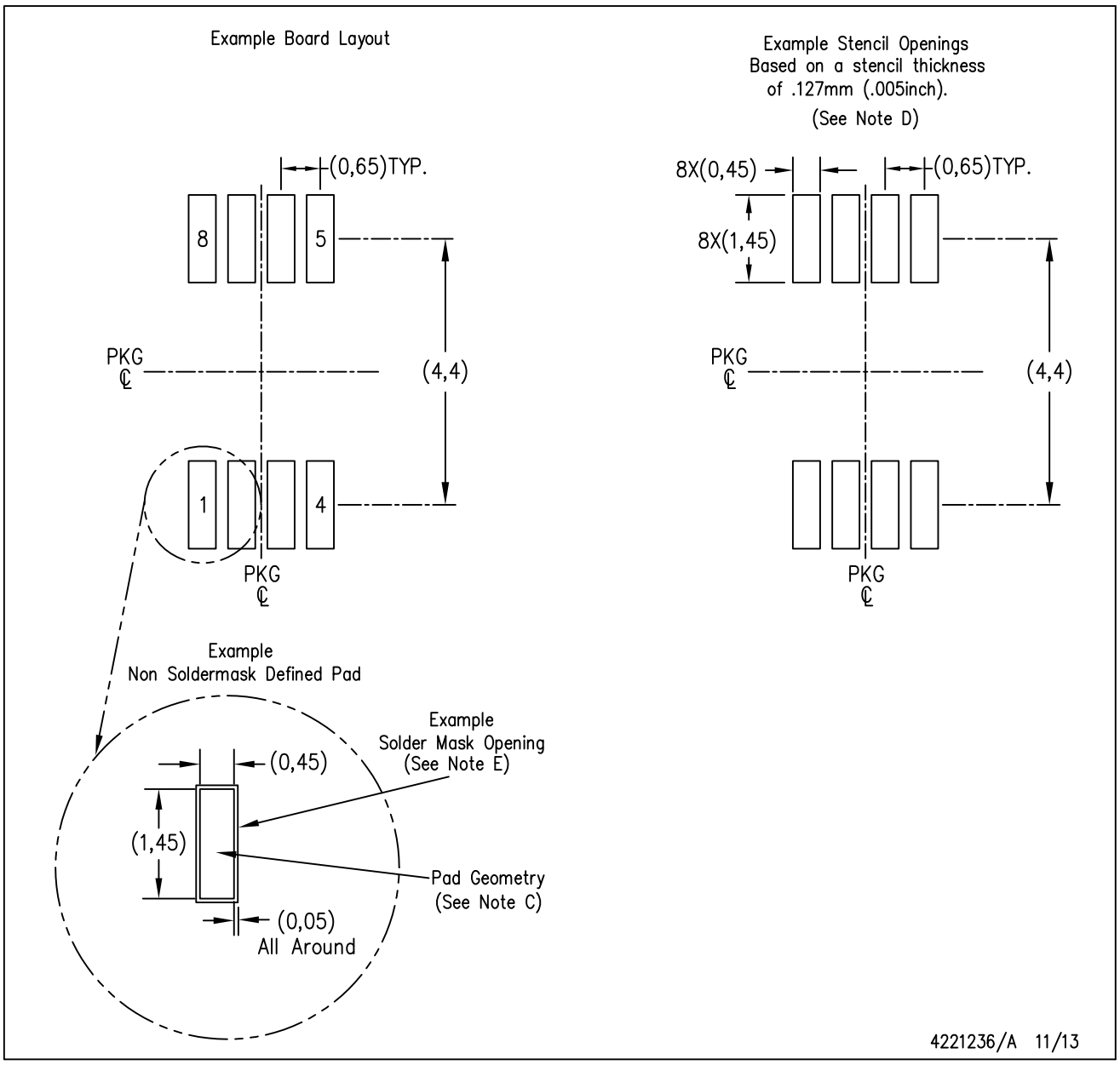
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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