AMC7834 具有温度、电流和电压监控功能的 12 位集成功率放大器监视和控制系统

1 特性

- 8 个具有可编程范围的单调性 12 位数模转换器 (DAC)
  - 4 个双极 DAC：–4V 至 1V，–5V 至 0V 以及 0V 至 5V
  - 4 个单极 DAC：0V 至 5V 以及 2.5V 至 7.5V
  - 高电流驱动能力：高达 ±10mA
  - 可选钳位电压
- 多通道 12 位逐次逼近寄存器 (SAR) 模数转换器 (ADC)
  - 4 个外部模拟输入：0V 至 2.5V 范围
  - 4 个用于双极 DAC 监视的内部输入
  - 可编程超范围警报
- 4 个高侧电流感测放大器
  - 共模电压：4V 至 60V
  - 可选闭环漏极电流控制器操作
- 温度感测功能
  - 内部温度传感器
  - 2 个远程温度二极管驱动器
- 2.5V 内部基准电压
- 4 个通用 I/O 端口 (GPIO)
- 低功耗 SPI 兼容串行接口
  - 4 线模式，1.7V 至 3.6V 工作电压
- 工作温度范围：-40°C 至 +125°C
- 采用 56 引脚超薄型四方扁平无引线 (VQFN) 封装

2 应用范围

- 通信基础设施：
  - 蜂窝基站
  - 微波回程
  - 光纤网络
- 通用监视器和控制
- 数据采集系统

3 说明

AMC7834 器件是一款针对功率放大器 (PA) 偏置的高度集成、低功耗、模拟监视和控制解决方案，能够对温度、电流和电压进行监控。

该器件集成了一个多通道 12 位模数转换器 (ADC)；八个 12 位数模转换器 (DAC)；四个高侧电流感测放大器，可以选择设置它们作为四个独立闭环漏极电流控制器的一部分；一个精确的片上温度传感器和两个远程温度二极管驱动器；四个可配置的通用 I/O 端口 (GPIO)；以及一个精确的内部基准。其高集成度极大地减少了组件数量，并且简化了 PA 偏置系统设计。

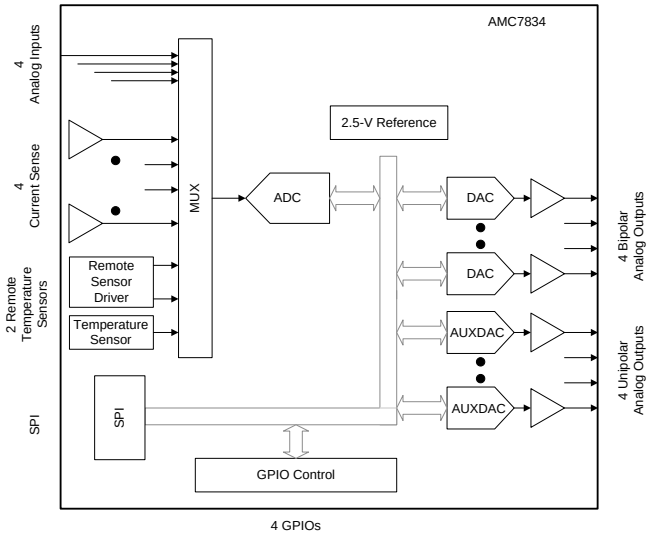
该器件具有功能集成和宽工作温度范围等诸多优势，因此适合用作多通道射频 (RF) 通信系统中 PA 的一体化、低成本偏置控制电路。凭借灵活的 DAC 输出范围和宽共模电压电流传感器，此器件可用作针对多种晶体管技术（例如 LDMOS、GaA 和 GaN）的偏置解决方案。AMC7834 功能集对通用监视器和控制系统而言同样有益。

德州仪器 (TI) 提供 了一个完备的模拟监视和控制 (AMC) 产品系列， 以满足各类应用不同的通道数、附加特性或者转换器解决方案需求。更多信息，敬请访问 www.ti.com.cn/amc。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC7834	VQFN (56)	8.00mm x 8.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。



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4 修订历史记录

Changes from Revision A (April 2015) to Revision B **Page**

- deleted text from the Description of pin 1 in the *Pin Functions* table " If unused the pin requires a 10 kΩ pullup resistor to the IOV_{DD} pin." ... 5
- Added: Bipolar DACs in AVSS clamp mode To the Clamp Output Mode section of *Electrical Characteristics—DAC Specifications* ... 10
- Deleted text from the Accuracy Test Conditions: "32 Samples Average" in *Electrical Characteristics—ADC, Current and Temperature Sensor Specifications* ... 11
- Added: AV_{DD} alarm threshold to *Electrical Characteristics—General Specifications* ... 12
- Changed the I_{IOVDD} (Power-Mode 10) TYP value From: 1 µA To 1.75 µA in *Electrical Characteristics—General Specifications* ... 13
- Changed the I_{IOVDD} (Power-Mode 00) TYP value From: 0.2 µA To 1.75 µA in *Electrical Characteristics—General Specifications* ... 13
- Added Figure 29 ... 19
- Changed Figure 45 ... 27
- Added text to the itemized list in *DAC Clamp Operation*: "If the output buffer is inactive the clamp voltage is fixed to AV_{SS}." ... 29
- Added text to the end of *DAC Clamp Operation*: "Additionally, in the unique case..." ... 29
- Changed text in paragraph 1 of *ADC Sequencing* From: "The AMC7834 supports autonomous ADC conversion" To: The AMC7834 supports autonomous and direct-mode conversions..." ... 31
- Change the paragraph: "Once the conversion cycle starts..." in *ADC Sequencing* ... 31
- Deleted text from paragraph 3 of *ADC Sequencing*: "The first conversion sequence is reserved for calibration and the corresponding ADC results should be ignored." ... 31
- Added text to the last paragraph of *ADC Sequencing*: "In direct-mode conversion the DAV/ADC_RDY pin ... for each channel group. " ... 33
- Added text to paragraph 3 of *Drain Switch Control*: The PA_ON signal state is also triggered by the AVDD monitoring circuit ... 39

修订历史记录 **(**接下页**)**

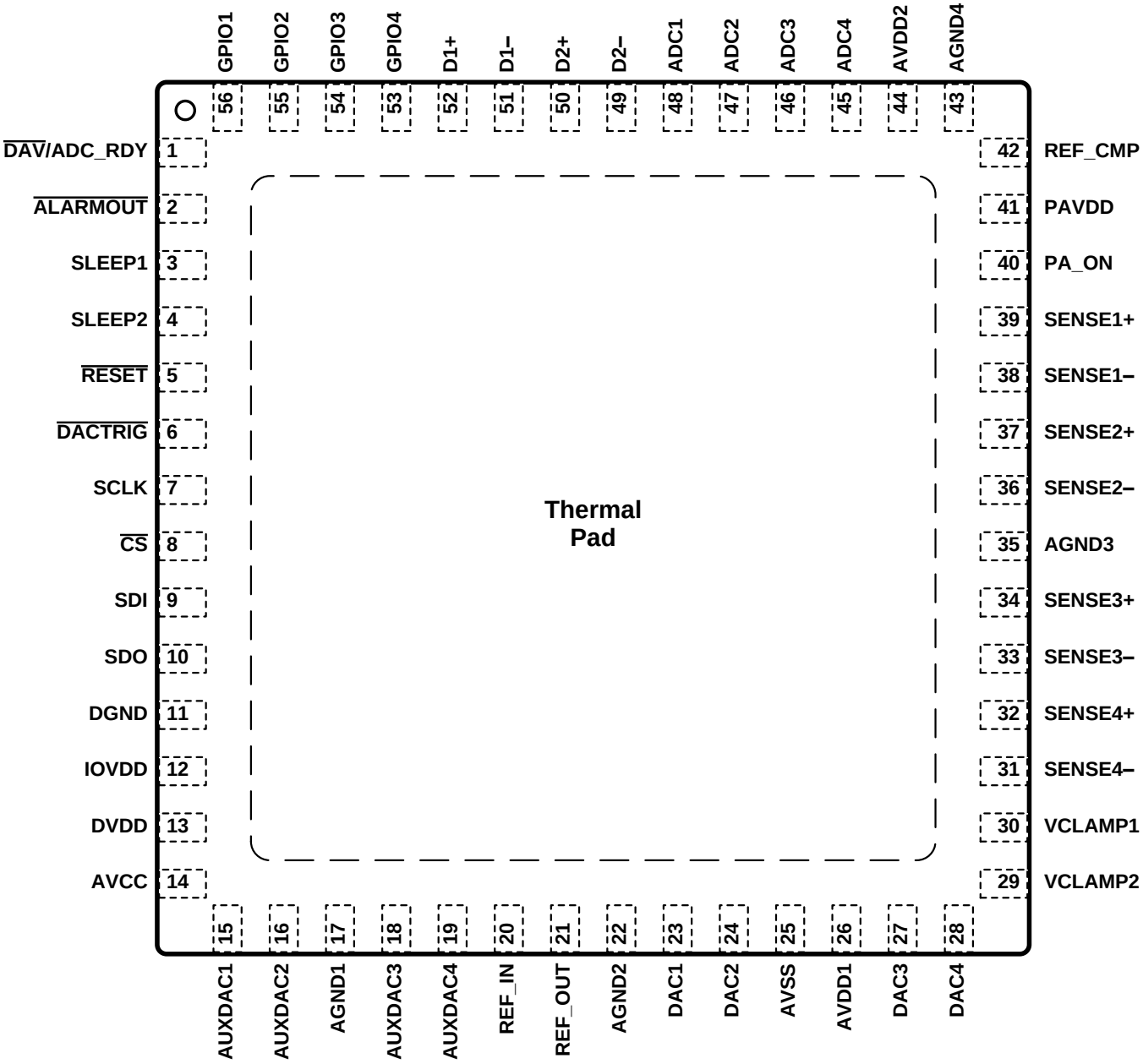
- Changed text in two locations of paragraph 4 in *Drain Switch Control*: From: "AV_{SS}" To: "AV_{DD} and AV_{SS}" 39
- Added text to the last paragraph of *Drain Switch Control*: "The AV_{DD} detection circuit is set to trigger the PA_ON signal to the OFF state in response to an out of range event." 39
- Added section: *AV_{DD} Detection Alarm* 42
- Changed text in the second paragraph of *Open-Loop Mode* From: "The current-sense amplifier outputs are converted continuously by the device ADC.." To: "The current-sense amplifier outputs are converted by the device ADC.." 47
- Changed 0x06 Default value From: 0000 To: 0001 in Table 9 52
- Changed R-00h To: R-01h in Bits 7:0 of Figure 69 54
- Changed the Reset value From: 0000h To: 0001h in Table 13 54
- Changed Bit 12 of Table 15 From: Reserved To: CMODE 55
- Changed Bit 10 of Table 18 From: 000: Invalid To: 000: 1 56
- Changed Bit 5-4 of Table 18 From: 00: Invalid To: 00: 1 56
- Changed Bit 3-2 of Table 18 From: 00: Invalid To: 00: 1 57
- Changed Bit 1-0 of Table 18 From: 00: Invalid To: 00: 1 57
- Changed *General Status Register (address = 0x1F) [reset = 0x0000]* 67
- Added text to item 2 of *Initialization Procedure*: A 250 µs POR delay occurs..." 82

Changes from Original (November 2014) to Revision A **Page**

- 发布完整版量产数据数据表 1

5 Pin Configuration and Functions

RTQ Package
56-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADC1	48	I	Analog inputs channels. These channels are used for general monitoring. The input range of these pins is 0 to V_{ref}.
ADC2	47	I	
ADC3	46	I	
ADC4	45	I	
AGND1	17	—	Analog ground. These pins are the ground reference point for all analog circuitry on the device. Connect the AGND1, AGND2, AGND3, and AGND4 pins to the same potential (AGND). Ideally, the analog and digital grounds should be at the same potential (GND) and must not differ by more than ±0.3 V.
AGND2	22	—	
AGND3	35	—	
AGND4	43	—	
$\overline{\text{ALARMOUT}}$	2	O	$\overline{\text{ALARMOUT}}$ is an open drain global alarm output. An external 10 kΩ pullup resistor to a voltage no higher than AV_{DD} is required. The $\overline{\text{ALARMOUT}}$ output polarity is defined through the ALARMOUT-POLARITY bit in register 0x1B. The default polarity is active low.
AUXDAC1	15	O	Auxiliary DAC Outputs. The power-on-reset and clamp voltage for these DACs is always AGND.
AUXDAC2	16	O	
AUXDAC3	18	O	
AUXDAC4	19	O	
AV_{CC}	14	—	Positive analog power supply for the auxiliary DACs.
AV_{DD1}	26	—	Analog supply voltage (4.5 V to 5.5 V). Connect the AV_{DD1} and AV_{DD2} pins to the same potential (AV_{DD}). These pins must have the same value as the DV_{DD} pin.
AV_{DD2}	44	—	
AV_{SS}	25	—	Lowest potential in the system. This pin is typically tied to a negative supply voltage. If all the bipolar DACs are set to operate in positive output ranges can be connected to the analog ground.
$\overline{\text{CS}}$	8	I	Active low serial data enable. This input is the frame synchronization signal for the serial data. When this signal goes low, it enables the serial interface input shift register.
D1+	52	I	Remote temperature sensor D1. This pin is a positive input when D1 is enabled. This pin can be left unconnected if unused.
D1–	51	I	Remote temperature sensor D1. This pin is a negative input when D1 is enabled. This pin can be left unconnected if unused. Pins D1– and D2– are internally shorted.
D2+	50	I	Remote temperature sensor D2. This pin is a positive input when D2 is enabled. This pin can be left unconnected if unused.
D2–	49	I	Remote temperature sensor D2. This pin is a negative input when D2 is enabled. This pin can be left unconnected if unused. Pins D1– and D2– are internally shorted.
DAC1	23	O	Bipolar DAC outputs 1 and 2. These DACs share the same range and clamp voltage.
DAC2	24	O	
DAC3	27	O	Bipolar DAC outputs 3 and 4. These DACs share the same range and clamp voltage.
DAC4	28	O	
$\overline{\text{DACTRIG}}$	6	I	DAC trigger active low control input. When the DACTRIG pin is low, the contents of the DAC data registers are transferred to the DAC active registers. The DAC outputs update only after the DAC active registers have been loaded. This pin is only operational in open loop current sensing mode.
$\overline{\text{DAV}}$/ADC_RDY	1	O	The $\overline{\text{DAV}}$/ADC_RDY pin is in high-impedance mode by default and must be enabled through the DAVPIN-EN bit in register 0x11 to access the $\overline{\text{DAV}}$ or ADC_RDY functionality. $\overline{\text{DAV}}$ is an active low ADC synchronization signal. A 20 µs pulse (active low) on this pin is used to indicate the end of a conversion sequence. Alternatively the pin can be set to operate as ADC_RDY through the DAVPIN-SEL bit in register 0x11. ADC_RDY is an active high synchronization signal used to indicate when the ADC is in the READY state.
DGND	11	—	Digital ground. This pin is the ground reference point for all digital circuitry on the device. Ideally, the analog and digital grounds should be at the same potential (GND) and must not differ by more than ±0.3 V.
DV_{DD}	13	—	Digital supply voltage (4.5 V to 5.5 V). This pin must be the same value as the AV_{DD} pins.
GPIO1	56	I/O	General-purpose digital I/Os. These pins are bidirectional open-drain, digital I/Os and requires an external 10 kΩ pullup resistor to a voltage no higher than AV_{DD}. If unused, the GPIO pins should be connected to ground.
GPIO2	55	I/O	
GPIO3	54	I/O	
GPIO4	53	I/O	

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
IOV_{DD}	12	—	IO supply voltage (1.7 V to 3.6 V). This pin sets the I/O operating voltage and threshold levels.
PAV_{DD}	41	—	Power supply for the PA_ON control signal (4 V to 20 V).
PA_ON	40	O	PA_ON is a synchronization signal capable of driving an external PMOS switch and controlling the flow of drain current to a power amplifier (PA) transistor. The PA_ON pin has an internal 120 kΩ pull-up resistor to the PAV_{DD} pin. The maximum output voltage is set by the PAV_{DD} pin and limited to 20 V. For drain voltages higher than 20 V, tying the PAV_{DD} pin to the AV_{DD} pins and scaling the control signal externally is recommended. The PA_ON signal state can be set through a register write but it can also be configured to trigger automatically in the case of an ALARM event or when any of the SLEEP signals is activated.
REF_CMP	42	I/O	Reference compensation capacitor connection. Connect a 4.7 µF capacitor between this pin and the AGND4 pin for ADC reference compensation.
REF_IN	20	I	Reference input to the device. This pin can be connected to the REF_OUT pin to use the device internal reference or alternatively to an external voltage reference source.
REF_OUT	21	O	Internal voltage reference output. Connect this pin directly to the REF_IN pin to operate the device in internal reference mode. An external buffer amplifier with a high impedance input is required to drive an external load. This pin can be left unconnected.
$\overline{\text{RESET}}$	5	I	Active low reset input. Logic low on this pin causes the device to perform a hardware reset.
SCLK	7	I	Serial interface clock.
SDI	9	I	Serial interface data input. Data is clocked into the input shift register on each rising edge of the SCLK pin.
SDO	10	O	Serial interface data output. The SDO pin is in high impedance when the $\overline{\text{CS}}$ pin is high. Data is clocked out of the input shift register on each falling edge of the SCLK pin.
SENSE1+	39	I	Current sense 1 external sense resistor power connection
SENSE1–	38	I	Current sense 1 external sense resistor load connection
SENSE2+	37	I	Current sense 2 external sense resistor power connection
SENSE2–	36	I	Current sense 2 external sense resistor load connection
SENSE3+	34	I	Current sense 3 external sense resistor power connection
SENSE3–	33	I	Current sense 3 external sense resistor load connection
SENSE4+	32	I	Current sense 4 external sense resistor power connection
SENSE4–	31	I	Current sense 4 external sense resistor load connection
SLEEP1	3	I	Active high asynchronous power down digital input 1. The power down functions of this pin are register configurable.
SLEEP2	4	I	Active high asynchronous power down digital input 2. The power down functions of this pin are register configurable.
VCLAMP1	30	I	Power-on reset and clamp voltage control input for bipolar DACs 1 and 2. The resulting power-on reset (POR) and clamp voltage value is given by Equation 1. $CLAMP = -3 \times VCLAMP[1:2]$ (1)
VCLAMP2	29	I	Power-on reset and clamp voltage control input for bipolar DACs 3 and 4. The resulting POR and clamp voltage value is given by Equation 1.
Thermal Pad		—	The thermal pad is located on the bottom-side of the device package. The thermal pad should be tied to the same potential as the AV_{SS} pin for optimal thermal dissipation. Alternatively, the thermal pad can be left unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AV_{DD} to GND	–0.3	6	V
	DV_{DD} to GND	–0.3	6	
	IOV_{DD} to GND	–0.3	6	
	AV_{CC} to GND	–0.3	13	
	AV_{SS} to GND	–6	0.3	
	PAV_{DD} to AV_{SS}	–0.3	26	
	DGND to AGND	–0.3	0.3	
Pin voltage	ADC analog input voltage to GND	–0.3	AV_{DD} + 0.3	V
	Current sense input voltage to GND	–0.3	65	
	Bipolar DAC outputs to GND	AV_{SS} – 0.3	AV_{DD} + 0.3	
	Auxiliary DAC outputs to GND	–0.3	AV_{CC} + 0.3	
	VCLAMP1, VCLAMP2 inputs to GND	–0.3	AV_{DD} + 0.3	
	D1+, D1–, D2+ and D2– to GND	–0.3	AV_{DD} + 0.3	
	REF_CMP, REF_IN to GND	–0.3	AV_{DD} + 0.3	
	REF_OUT to GND	–0.3	AV_{DD} + 0.3	
	PA_ON to GND	–0.3	PAV_{DD} + 0.3	
	$\overline{CS}$, SCLK, SDI, DACTRIG, $\overline{RESET}$, SLEEP1, SLEEP2 and $\overline{DAV}$/ADC_RDY to GND	–0.3	IOV_{DD} + 0.3	
	SDO to GND	–0.3	IOV_{DD} + 0.3	
	GPIOs, $\overline{ALARMOUT}$ to GND	–0.3	6	
Pin current	ADC analog input current	–10	10	mA
	REF_OUT output current	–0.3	0.3	
	GPIOs, $\overline{ALARMOUT}$ sinking current		5	
Operating temperature range		–40	125	°C
Junction temperature range, T_J max		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±750	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	AV_{DD} (1)	4.5	5	5.5	V
	DV_{DD} (1)	4.5	5	5.5	
	IOV_{DD}	1.7	3.3	3.6	
	AV_{CC}	4.5	5	12.5	
	AV_{SS} (2)	–5.5	–5	0	
	PAV_{DD}	4	5	20	
Specified performance temperature		–40	25	105	°C
Operating temperature		–40	25	125	°C

(1) The value of the DV_{DD} pin must be equal to that of the AV_{DD} pins.
(2) The value of the AV_{SS} pin is only equal to AGND when all bipolar DACs are set to operate in positive voltage ranges.

6.4 Thermal Information

THERMAL METRIC (1) (2)		RTQ (VQFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	2.7	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	2.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) TI strongly recommends to solder the device thermal pad to a board plane connected to the AV_{SS} pin.

6.5 Electrical Characteristics—DAC Specifications

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, IOV_{DD} = 3.3 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to +105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIPOLAR DAC DC ACCURACY						
	Resolution		12			Bits
INL	Relative accuracy	Measured by line passing through codes 040h and FC0h. 0 to 5 V range		±0.3	±1	LSB
		Measured by line passing through codes 040h and FC0h. –4 to 1 V and –5 to 0 V ranges		±0.3	±1	
DNL	Differential nonlinearity	Specified monotonic. Measured by line passing through codes 040h and FC0h. 0 to 5 V range		±0.05	±1	LSB
		Specified monotonic. Measured by line passing through codes 040h and FC0h. –4 to 1 V and –5 to 0 V ranges		±0.05	±1	
TUE	Total unadjusted error	T_A = 25°C, 0 to 5 V range		±1	±15	mV
		T_A = 25°C, –4 to 1 V and –5 to 0 V ranges		±2	±15	
	Offset error	T_A = 25°C. Measured by line passing through codes 040h and FC0h. 0 to 5 V range		±0.2	±10	mV
	Zero-code error	T_A = 25°C. Code 000h. –4 to 1 V and –5 to 0 V ranges. AV_{SS} = –5.5 V		±2	±10	mV
	Gain error	T_A = 25°C. Measured by line passing through codes 040h and FC0h. 0 to 5 V range		±0.02	±0.2	%FSR
		T_A = 25°C. Measured by line passing through codes 040h and FC0h. –4 to 1 V and –5 to 0 V ranges		±0.02	±0.2	
	Offset temperature drift	0 to 5 V range		±1		ppm/°C
	Zero-code temperature drift	–4 to 1 V and –5 to 0 V ranges. AV_{SS} = –5.5 V		±1.5		ppm/°C
	Gain temperature drift	All output ranges		±1		ppm/°C
AUXILIARY DAC DC ACCURACY						
	Resolution		12			Bits
INL	Integral nonlinearity	Measured by line passing through codes 040h and FC0h. 0 to 5 V range		±0.5	±1.25	LSB
		Measured by line passing through codes 040h and FC0h. 2.5 to 7.5 V range. AV_{CC} = 12 V		±0.5	±1.25	
DNL	Differential nonlinearity	Specified monotonic. Measured by line passing through codes 040h and FC0h. 0 to 5 V range		±0.05	±1	LSB
		Specified monotonic. Measured by line passing through codes 040h and FC0h. 2.5 to 7.5 V range. AV_{CC} = 12 V		±0.05	±1	
TUE	Total unadjusted error	T_A = 25°C. 0 to 5 V range		±2	±15	mV
		T_A = 25°C. 2.5 to 7.5 V range. AV_{CC} = 12 V		±2	±15	
	Offset error	T_A = 25°C. Measured by line passing through codes 040h and FC0h. 0 to 5 V range		±0.3	±10	mV
		T_A = 25°C. Measured by line passing through codes 040h and FC0h. 2.5 to 7.5 V range. AV_{CC} = 12 V		±1	±10	
	Gain error	T_A = 25°C. Measured by line passing through codes 040h and FC0h. 0 to 5 V range		±0.03	±0.2	%FSR
		T_A = 25°C. Measured by line passing through codes 040h and FC0h. 2.5 to 7.5 V range. AV_{CC} = 12 V		±0.03	±0.2	
	Offset temperature drift	All output ranges		±1		ppm/°C
	Gain temperature drift	All output ranges		±1		ppm/°C

Electrical Characteristics—DAC Specifications (continued)

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, IOV_{DD} = 3.3 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to +105°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC OUTPUT CHARACTERISTICS					
Bipolar DAC range(1)	DAC*n*_range set to 00	–4		1	V
	DAC*n*_range set to 01	–5		0	
	DAC*n*_range set to 10	–5		0	
	DAC*n*_range set to 11	0		5	
Auxiliary DAC range(2)	AUXDAC*n*_range set to 0	0		5	V
	AUXDAC*n*_range set to 1	2.5		7.5	
Short-circuit current	Bipolar DACs: Full-scale current shorted to AV_{SS} or AV_{DD} Auxiliary DACs: Full-scale current shorted to AGND or AV_{CC}		45		mA
Load current(3)	Bipolar DACs: Source or sink with 300 mV headroom from AV_{DD} or AV_{SS}, voltage drop < 25 mV Auxiliary DACs: Source or sink with 300 mV headroom from AV_{CC} or AGND, voltage drop < 25 mV	±10			mA
Maximum capacitive load(4)	All DAC outputs. R_L = ∞	0		10	nF
DC output impedance	All DAC outputs. Code set to 800h, ±10 mA		1		Ω
Glitch energy	All DAC outputs. Transition: Code 7FFh to 800h; 800h to 7FFh		1		nV-s
Output noise	Auxiliary DACs. 1 kHz, code 800h		200		$nV/\sqrt{Hz}$
	Bipolar DACs. 1 kHz, code 800h		100		
	Auxiliary DACs. Integrated noise from 0.1 Hz to 10 Hz, code 800h		20		μV_{PP}
	Bipolar DACs. Integrated noise from 0.1 Hz to 10 Hz, code 800h		10		
CLAMP OUTPUT MODE					
VCLAMP [1:2] voltage range		0		$–AV_{SS}$ / 3	V
VCLAMP [1:2] input current				±0.5	µA
Clamp output voltage	Bipolar DACs. Clamp voltage = –3 × VCLAMP[1:2]	AV_{SS}		0	V
	Auxiliary DACs		AGND		
Clamp output current	Bipolar DACs. Source, sink, or both with 300-mV headroom from AV_{SS}, voltage drop < 25 mV	±10			mA
Clamp pull-down resistance	Auxiliary DACs. Measured to AGND		9		kΩ
	Bipolar DACs. VCLAMP buffers inactive (AV_{SS} clamp mode). Measured to AV_{SS}		550		Ω

(1) The output voltage must not be greater than AV_{DD} or lower than AV_{SS}. A minimum of 100 mV headroom from AV_{DD} is required.
(2) The output voltage must not be greater than AV_{CC} or lower than AGND. A minimum of 100 mV headroom from AV_{CC} is required.
(3) If all channels are simultaneously loaded, care must be taken to ensure the thermal conditions for the device are not exceeded.
(4) To be sampled during initial release to ensure compliance; not subject to production testing.

6.6 Electrical Characteristics—ADC, Current and Temperature Sensor Specifications

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, IOV_{DD} = 1.8 to 3.3 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to +105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL ANALOG INPUTS (ADC1, ADC2, ADC3 and ADC4)						
	Resolution		12			Bits
INL	Integral nonlinearity			±0.5	±1	LSB
DNL	Differential nonlinearity	Specified monotonic		±0.5	±1	LSB
	Offset error			±0.3	±4.5	LSB
	Offset error match			±1		LSB
	Gain error			±0.3	±4	LSB
	Gain error match			±1		LSB
	Full-scale input range(1)		0		V_{ref}	V
	Input capacitance			48		pF
	DC-input leakage current	Unselected ADC input			±2	µA
INTERNAL MONITORING INPUTS (BIPOLAR DAC-OUTPUT MONITORING)						
	Full scale input range(1)		–5		2.5	V
	Resolution	LSB size		1.83		mV
CURRENT-SENSE INPUTS						
	Common mode voltage		4		60	V
	Full scale sense voltage(1)	SENSE*n*+ – SENSE*n*-	0		200	mV
	Input resistance	Per current sense input terminal		192		kΩ
	Gain accuracy			±0.1%	±1%	
	Input offset error	CS-FILTER[2:0] = 100 Common mode voltage = 4 V		±50	±500	µV
	CMRR	CS-FILTER[2:0] = 100		80		dB
	Resolution	LSB size		48.83		µV
TEMPERATURE SENSOR: INTERNAL						
	Operating range(1)(2)	Specified monotonic over entire range.	–55		125	°C
	Accuracy(2)	T_J = –40°C to 125°C			±3	°C
	Resolution	LSB size T_J = –40°C to 125°C		0.25		°C
TEMPERATURE SENSOR: EXTERNAL (USING 2N3906 EXTERNAL TRANSISTOR)						
	Operating range(1)(2)		–55		150	°C
	Accuracy(2)	RT-SET[2:0] = 011, CS-FILTER[2:0] = 100 T_A = –40°C to 125°C, $T_{(DIODE)}$ = –40°C to 150°C			±3	°C
	Resolution	LSB size T_A = –40°C to 125°C, $T_{(DIODE)}$ = –40°C to 150°C		0.25		°C

(1) Input range for all monitoring inputs must be met for accuracy specifications to apply.
(2) Not tested during production. Specified by design and characterization.

6.7 Electrical Characteristics—General Specifications

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, IOV_{DD} = 1.8 to 3.3 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL REFERENCE INPUT						
V_{REF_IN}	Input voltage range	REF_IN pin		2.5		V
	Input current	V_{REF_IN} = 2.5 V		1	100	µA
	DAC reference buffer offset	T_A = 25°C			±5	mV
	ADC reference buffer offset	T_A = 25°C			±5	mV
INTERNAL REFERENCE						
	Output voltage	T_A = 25°C, REF_OUT pin	2.4925	2.5	2.5075	V
	Reference temperature coefficient			10	35	ppm/°C
	Output voltage noise	1 kHz		260		nV/√Hz
		Integrated noise from 0.1 Hz to 10 Hz		13		$µV_{PP}$
PA_ON OUTPUT						
	PA_ON output voltage	PAV_{DD} ≤ 20 V	AGND		PAV_{DD}	V
SUPPLY ALARMS(1)						
	AV_{SS} alarm threshold		–4.4	–4.1	–3.8	V
	AV_{DD} alarm threshold		3.4	3.9	4.4	V
DIGITAL LOGIC(1)						
V_{IH}	High-level input voltage	IOV_{DD} = 1.7 V to 3.6 V	0.7 × IOV_{DD}			V
V_{IL}	Low-level input voltage	IOV_{DD} = 1.7 V to 3.6 V			0.3 × IOV_{DD}	V
V_{hys}	Hysteresis voltage	IOV_{DD} = 1.7 V to 3.6 V	0.1 × IOV_{DD}			V
V_{OH}	High-level output voltage	SDO and $\overline{DAV}$/ADC_RDY. IOV_{DD} = 1.7 V, $I_{(LOAD)}$ = 1 mA	IOV_{DD} – 0.4			V
V_{OL}	Low-level output voltage	IOV_{DD} = 1.7 V to 3.6 V, $I_{(LOAD)}$ = –1 mA			0.4	V
	High impedance leakage				±0.5	µA
	High impedance output capacitance			10		pF

(1) Not tested during production. Specified by design and characterization.

Electrical Characteristics—General Specifications (continued)

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, IOV_{DD} = 1.8 to 3.3 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS						
I_{AVDD}	AV_{DD} supply current	POWER-MODE = 10. AV_{DD} = DV_{DD} = 5.5 V, AV_{CC} = 5.5 V PAV_{DD} = 20 V, AV_{SS} = –5.5 V, IOV_{DD} = 3.6 V All monitoring channels enabled Bipolar DACs in –5 to 0 V range Auxiliary DACs in 0 to 5 V range All DACs at 800h code. PA_ON in "ON" state		10	12.5	mA
I_{AVCC}	AV_{CC} supply current			1.5	2	mA
I_{AVSS}	AV_{SS} supply current		–3.5	–2.5		mA
I_{DVDD}	DV_{DD} supply current			2.5	3	mA
I_{IOVDD}	IOV_{DD} supply current			1.75	2.5	µA
I_{PAVDD}	PAV_{DD} supply current			170	250	µA
	Power consumption			95	120.5	mW
I_{AVDD}	AV_{DD} supply current	POWER-MODE = 00. AV_{DD} = DV_{DD} = 5.5 V, AV_{CC} = 5.5 V PAV_{DD} = 20 V, AV_{SS} = –5.5 V, IOV_{DD} = 3.6 V All DACs in clamp mode at 0 V PA_ON in "OFF" state		3.5		mA
I_{AVCC}	AV_{CC} supply current			0.2		mA
I_{AVSS}	AV_{SS} supply current			–2		mA
I_{DVDD}	DV_{DD} supply current			2.5		mA
I_{IOVDD}	IOV_{DD} supply current			1.75		µA
I_{PAVDD}	PAV_{DD} supply current			12		µA
	Power consumption			45		mW

6.8 Serial Interface Timing Requirements(1)(2)

AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to +105°C (unless otherwise noted)

			IOV_{DD} = 1.7 TO 2.7 V		IOV_{DD} = 2.7 TO 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
f_{SCLK}	SCLK frequency		0.2	10	0.2	15	MHz
t_p	SCLK period	See Figure 1 and Figure 2.	100		66.67		ns
t_{PH}	SCLK pulse width high		40		26		ns
t_{PL}	SCLK pulse width low		40		26		ns
t_{su}	SDI setup		10		10		ns
t_h	SDI hold		10		10		ns
$t_{(ODZ)}$	SDO driven to tri-state	See Figure 2.	0	15	0	10	ns
$t_{(OZD)}$	SDO tri-state to driven		0	20	0	15	ns
$t_{(OD)}$	SDO output delay		0	20	0	15	ns
$t_{su(\overline{CS})}$	$\overline{CS}$ setup	See Figure 1 and Figure 2	5		5		ns
$t_{h(\overline{CS})}$	$\overline{CS}$ hold		20		20		ns
$t_{(IAG)}$	Inter-access gap		15		15		ns

(1) Specified by design and characterization. Not tested during production.
(2) SDO loaded with 10 pF load capacitance for SDO timing specifications.

6.9 Switching Characteristics—DAC Specifications

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, IOV_{DD} = 3.3 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to +105°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC OUTPUT CHARACTERISTICS					
Output voltage settling time	Transition: Code 400h to C00h to within ½ LSB. R_L= 2 kΩ, C_L = 200 pF. All DAC outputs. All output ranges		10		µs
Slew rate	Transition: Code 400h to C00h, 10% to 90%. R_L= 2 kΩ, C_L = 200 pF. All DAC outputs. All output ranges		1.25		V/µs
CLAMP OUTPUT MODE					
Clamp shutdown delay(1)	All DAC outputs. R_L = ∞, C_L = 200 pF, clamp from 3.5 V output, within 10% accuracy of active DAC output, measured from SLEEP 0 to 1 transition			5	µs
Wake-up from clamp delay(1)	All DAC outputs. R_L = ∞, C_L = 200 pF, wake-up to 3.5 V output, within 10% accuracy of active DAC output, measured from SLEEP 1 to 0 transition			5	µs

(1) Not tested during production. Specified by design and characterization.

6.10 Switching Characteristics—ADC, Current and Temperature Sensor Specifications

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, IOV_{DD} = 1.8 to 3.3 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to +105°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC INTERNAL OSCILLATOR					
Internal oscillator frequency		3.7	4	4.3	MHz
EXTERNAL ANALOG INPUTS (ADC1, ADC2, ADC3 and ADC4)					
Update time	All four external inputs enabled Internal monitoring inputs disabled		1		ms
INTERNAL MONITORING INPUTS (BIPOLAR DAC-OUTPUT MONITORING)					
Update time	All four internal monitoring inputs enabled External analog inputs disabled		1		ms
CURRENT-SENSE INPUTS					
Update time	All four current sense inputs enabled CS-FILTER[2:0] = 000		200		µs
TEMPERATURE SENSOR: INTERNAL					
Update time	Remote temperature sensors disabled		2		ms
TEMPERATURE SENSOR: EXTERNAL (USING 2N3906 EXTERNAL TRANSISTOR)					
Update time	Single external temperature sensor Internal temperature sensor disabled RT-SET[2:0] = 000		8		ms

6.11 Switching Characteristics—General Specifications

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V, AV_{SS} = –5 V, IOV_{DD} = 1.8 to 3.3 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, external 2.5 V reference, DAC output range = 0 to 5 V for all DACs, no load on the DACs, current sense inputs common mode at 48 V, T_A = –40°C to 105°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PA_ON OUTPUT(1)					
PA_ON OFF state enable	Measured from AV_{SS} alarm event, C_L = 1 nF			1	ms
	Measured from SLEEP 0 to 1 transition, C_L = 1 nF			1	ms
PA_ON ON state enable	Measured from SLEEP 1 to 0 transition, C_L = 1 nF			0.5	ms
RESET REQUIREMENTS(1)					
Reset delay	Delay to normal operation from hardware reset		100	250	µs
	Delay to normal operation from software reset			10	µs
Reset pulse width		20			ns

(1) Not tested during production. Specified by design and characterization.

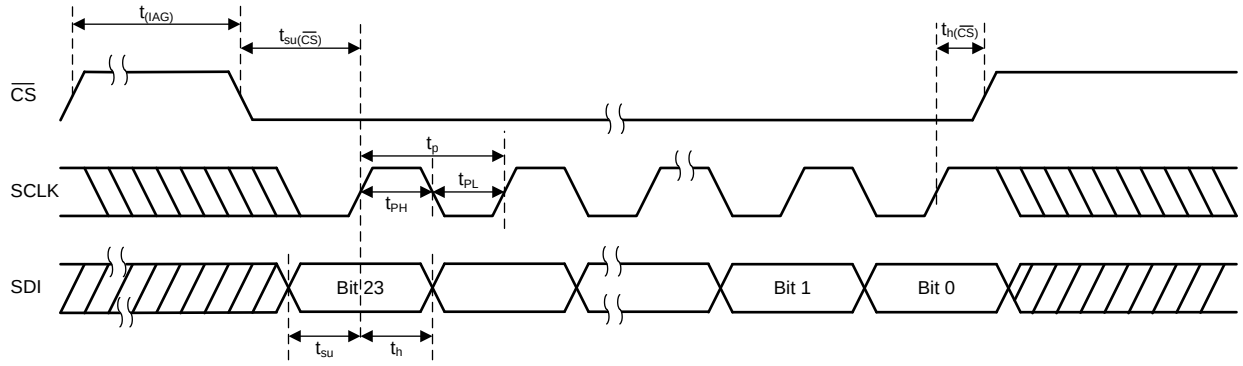


Figure 1. Serial Interface Write Timing Diagram

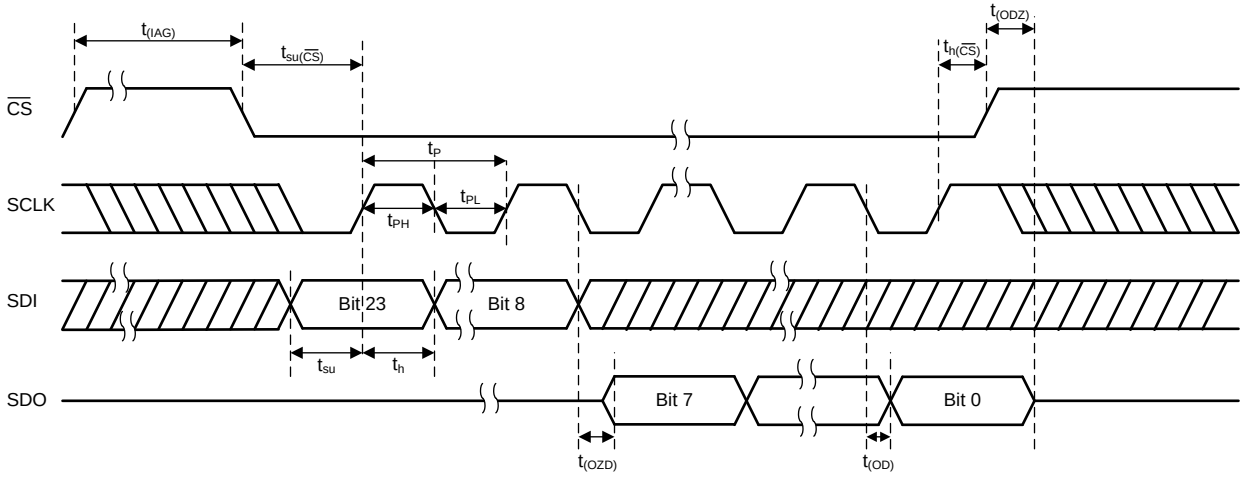
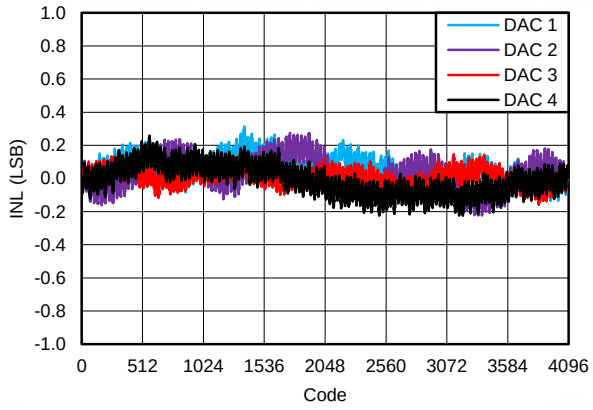


Figure 2. Serial Interface Read Timing Diagram

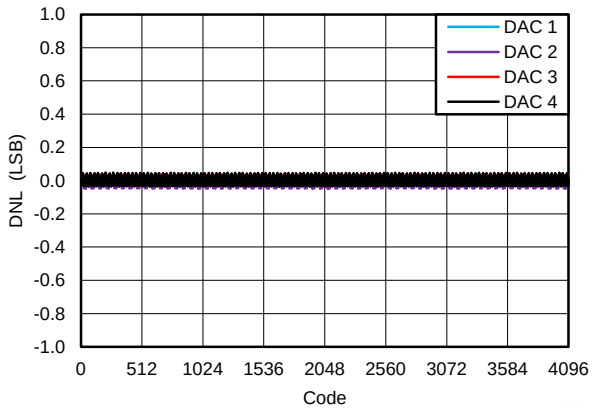
6.12 Typical Characteristics

6.12.1 Typical Characteristics: DAC



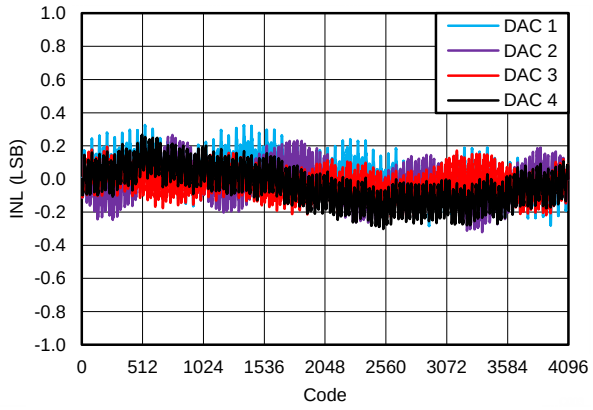
DAC range = 0 to 5 V, AV_{DD} = 5.5 V

Figure 3. Bipolar DAC Integral Non-Linearity



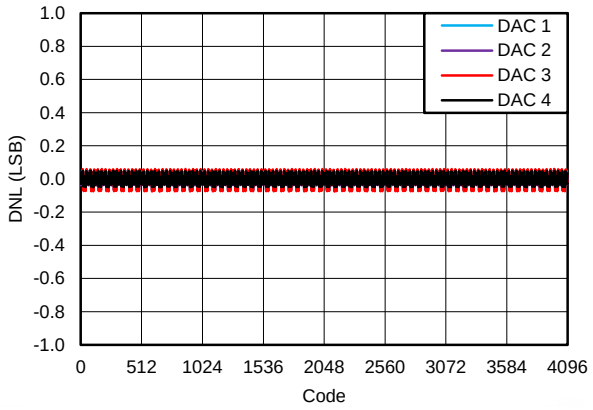
DAC range = 0 to 5 V, AV_{DD} = 5.5 V

Figure 4. Bipolar DAC Differential Non-Linearity



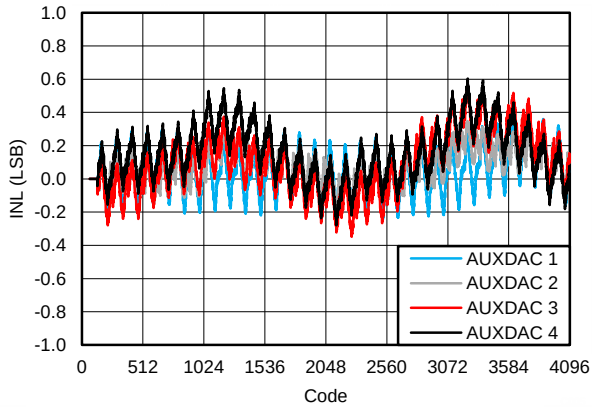
DAC range = –5 to 0 V, AV_{SS} = –5.5 V

Figure 5. Bipolar DAC Integral Non-Linearity



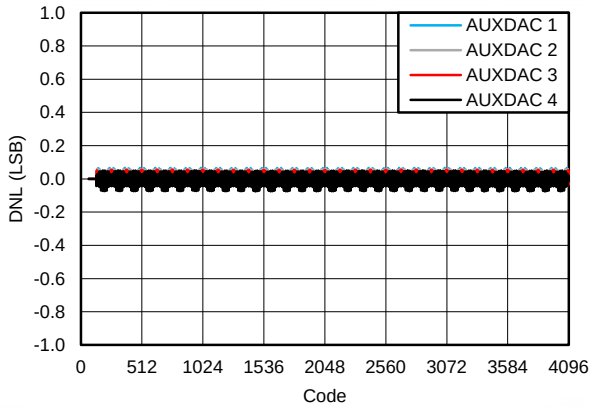
DAC range = –5 to 0 V, AV_{SS} = –5.5 V

Figure 6. Bipolar DAC Differential Non-Linearity



DAC range = 0 to 5 V, AV_{CC} = 5.5 V

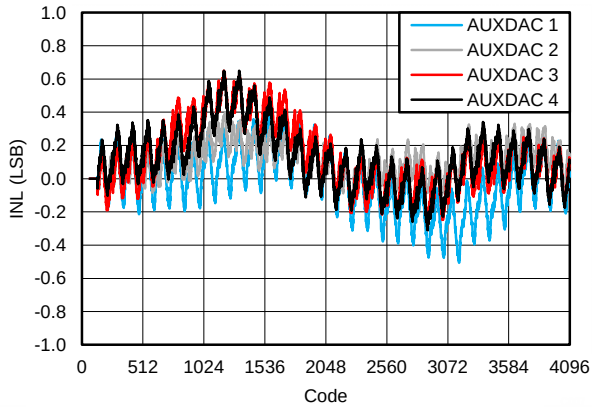
Figure 7. Auxiliary DAC Integral Non-Linearity



DAC range = 0 to 5 V, AV_{CC} = 5.5 V

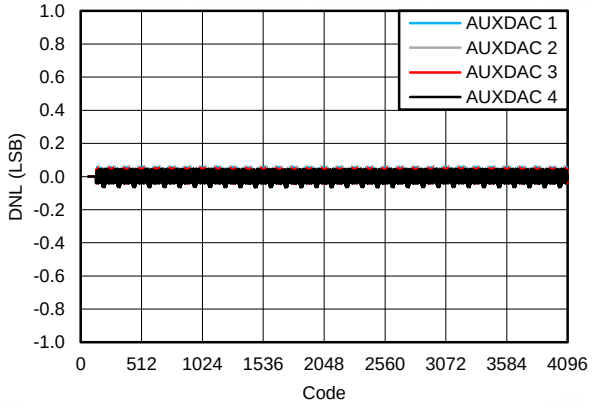
Figure 8. Auxiliary DAC Differential Non-Linearity

Typical Characteristics: DAC (continued)



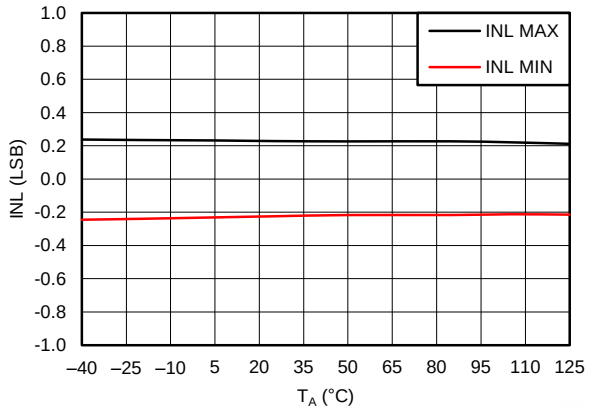
DAC range = 2.5 to 7.5 V, AV_{CC} = 12 V

Figure 9. Auxiliary DAC Integral Non-Linearity



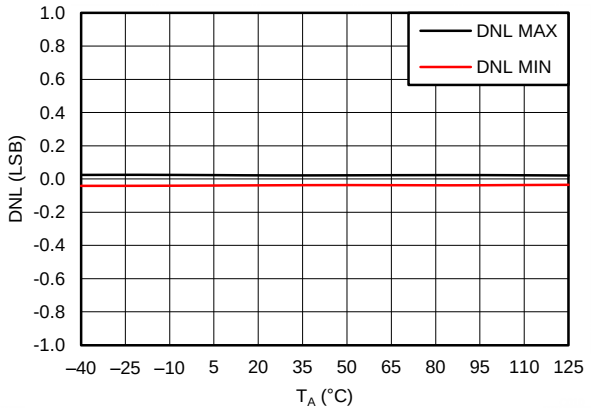
DAC range = 2.5 to 7.5 V, AV_{CC} = 12 V

Figure 10. Auxiliary DAC Differential Non-Linearity



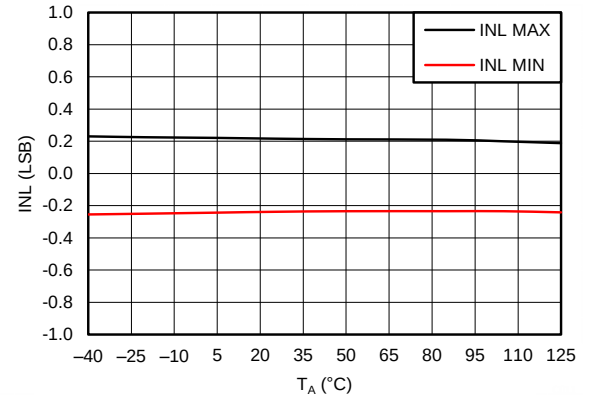
DAC range = 0 to 5 V, AV_{DD} = 5.5 V

Figure 11. Bipolar DAC INL vs Temperature



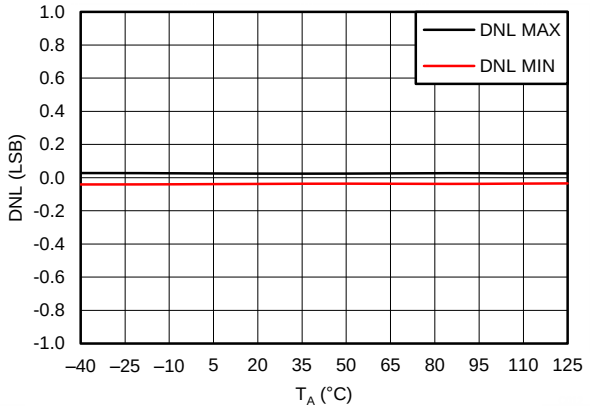
DAC range = 0 to 5 V, AV_{DD} = 5.5 V

Figure 12. Bipolar DAC DNL vs Temperature



DAC range = –5 to 0 V, AV_{SS} = –5.5 V

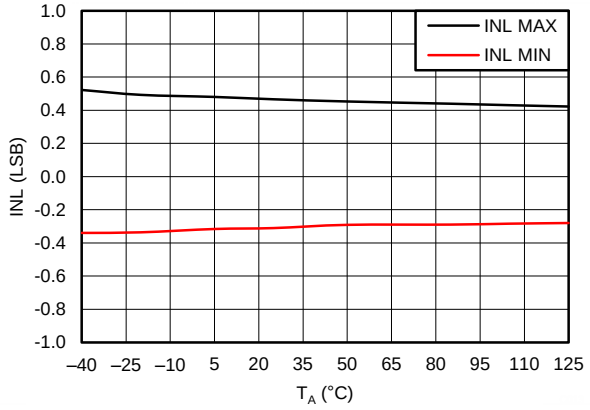
Figure 13. Bipolar DAC INL vs Temperature



DAC range = –5 to 0 V, AV_{SS} = –5.5 V

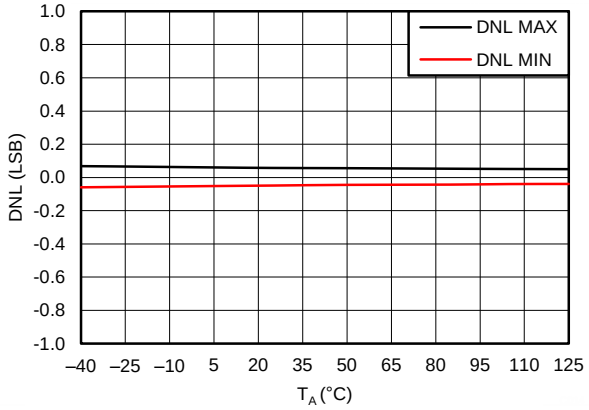
Figure 14. Bipolar DAC DNL vs Temperature

Typical Characteristics: DAC (continued)



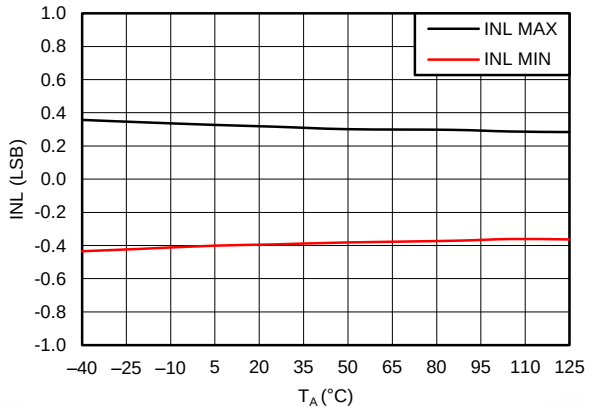
DAC range = 0 to 5 V, AV_{CC} = 5.5 V

Figure 15. Auxiliary DAC INL vs Temperature



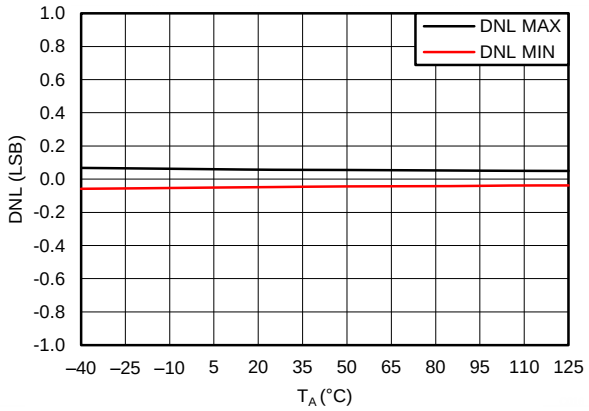
DAC range = 0 to 5 V, AV_{CC} = 5.5 V

Figure 16. Auxiliary DAC DNL vs Temperature



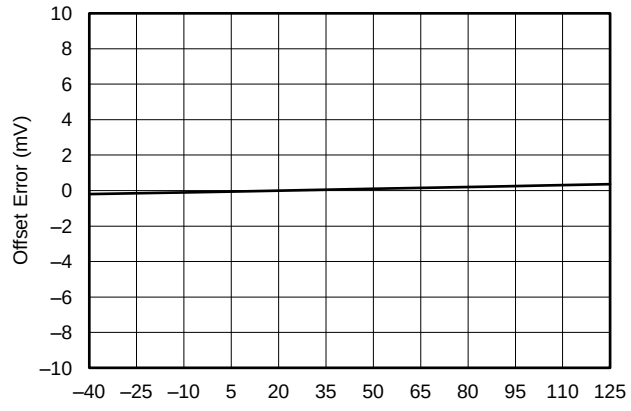
DAC range = 2.5 to 7.5 V, AV_{CC} = 12 V

Figure 17. Auxiliary DAC INL vs Temperature



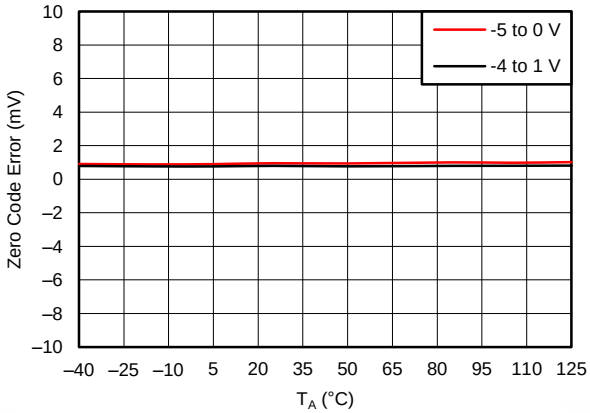
DAC range = 2.5 to 7.5 V, AV_{CC} = 12 V

Figure 18. Auxiliary DAC DNL vs Temperature



DAC range = 0 to 5 V

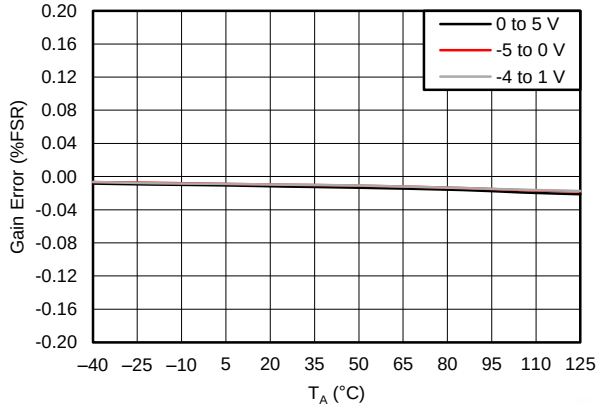
Figure 19. Bipolar DAC Offset Error vs Temperature



AV_{SS} = –5.5 V

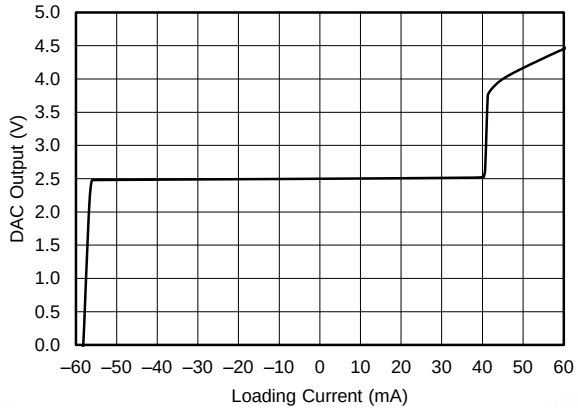
Figure 20. Bipolar DAC Zero Code Error vs Temperature

Typical Characteristics: DAC (continued)



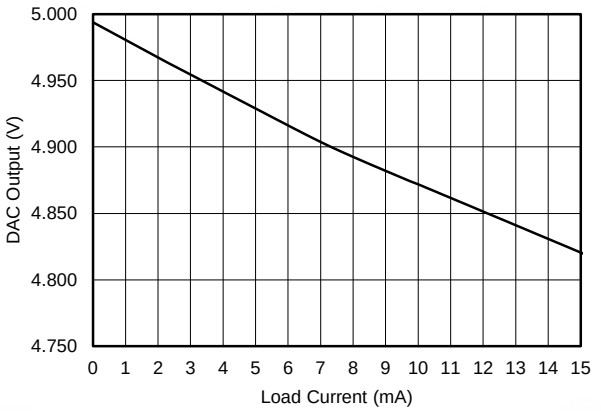
AV_{DD} = 5.5 V, AV_{SS} = –5.5 V

Figure 21. Bipolar DAC Gain Error vs Temperature



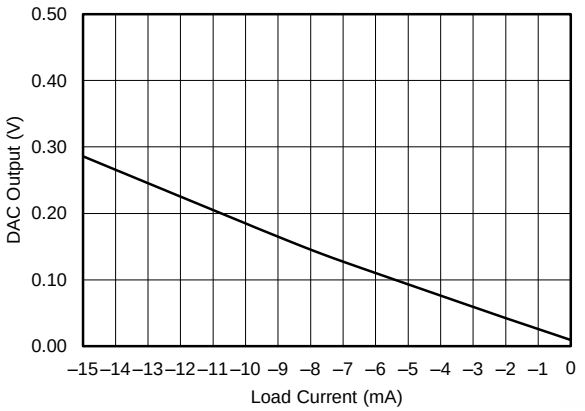
DAC range = 0 to 5 V, Code 0x800

Figure 22. DAC Output Voltage vs Load Current



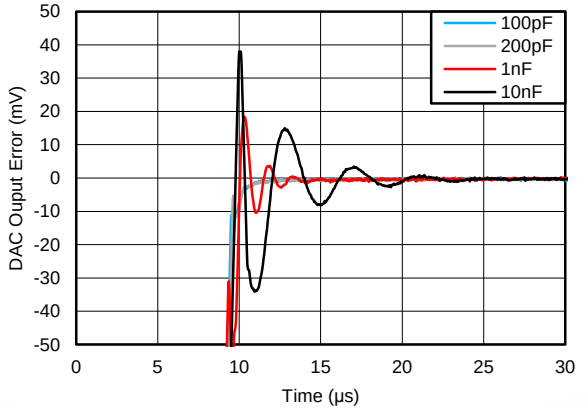
DAC range = 0 to 5 V, Code 0xFFF

Figure 23. DAC Source Current



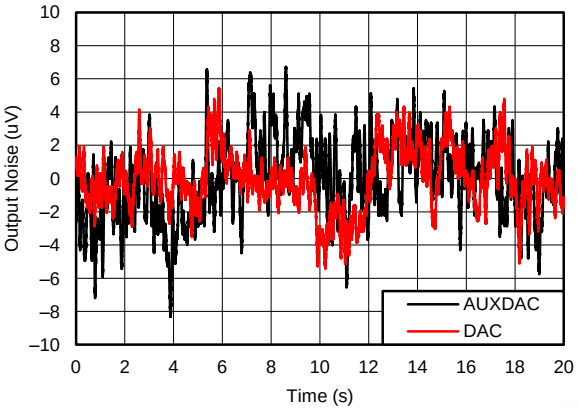
DAC range = 0 to 5 V, Code 0x000, AV_{SS} = 0 V

Figure 24. DAC Sink Current



Code 0x000 to 0xFFF to within 0.5% of final value

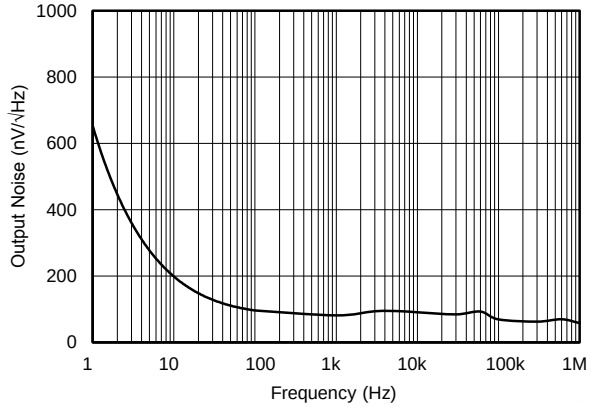
Figure 25. DAC Settling Time



Code 0x800

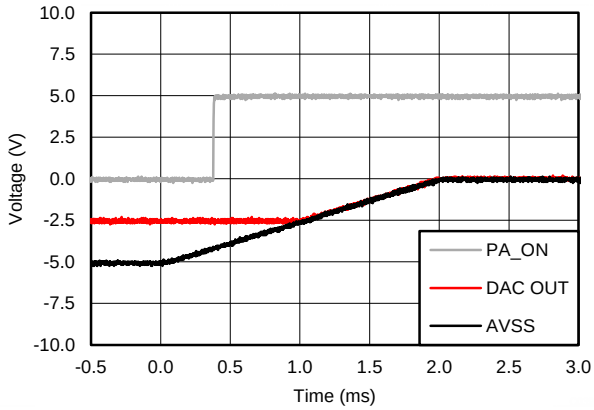
Figure 26. DAC Output Noise, 0.1 Hz to 10 Hz

Typical Characteristics: DAC (continued)



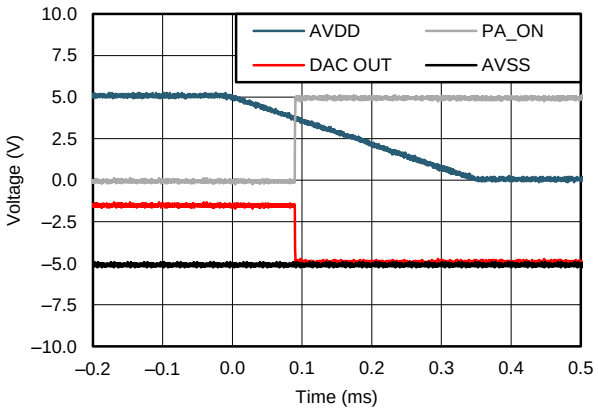
Bipolar DAC, Code 0x800

Figure 27. DAC Noise Voltage vs Frequency



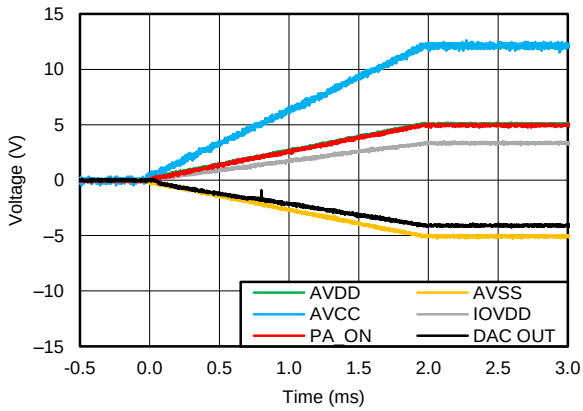
DAC range: –5 to 0 V, Code 0x800

Figure 28. PA_ON Response to AV_{SS} Supply Collapse



DAC range: –4 to 1 V, Code 0x800

Figure 29. Response to AV_{DD} Supply Collapse



DAC range: –4 to 1 V, VCLAMP[1:2] = 4/3 V

Figure 30. DAC Power On

6.12.2 Typical Characteristics: ADC

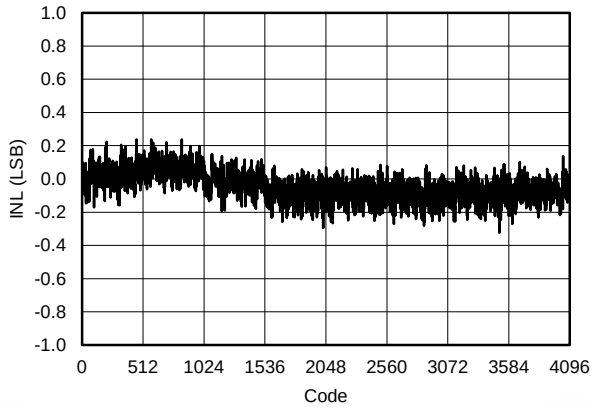


Figure 31. ADC INL

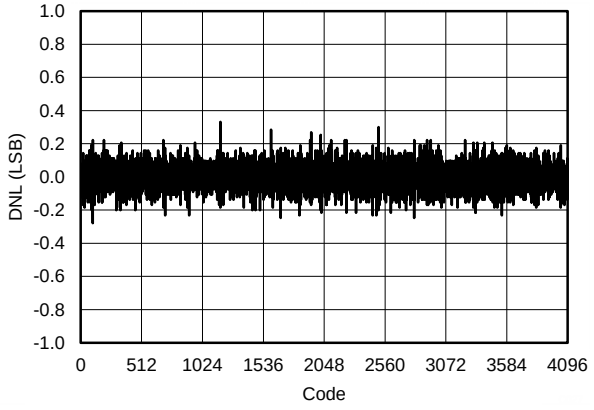


Figure 32. ADC DNL

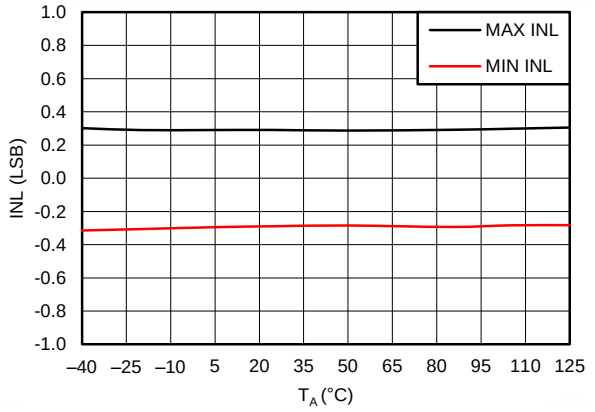


Figure 33. ADC INL vs Temperature

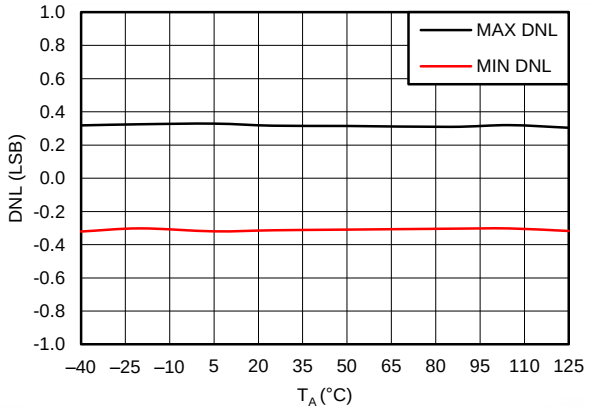


Figure 34. ADC DNL vs Temperature

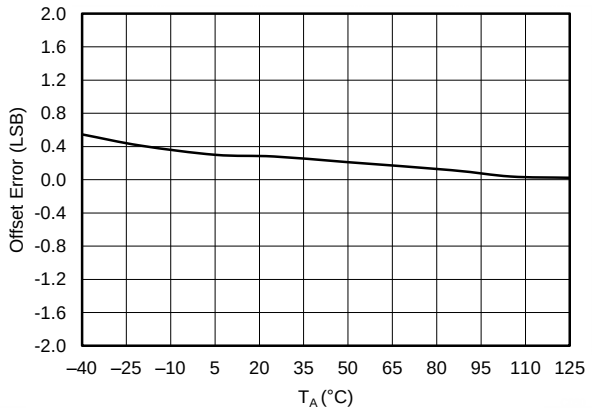


Figure 35. ADC Offset Error vs Temperature

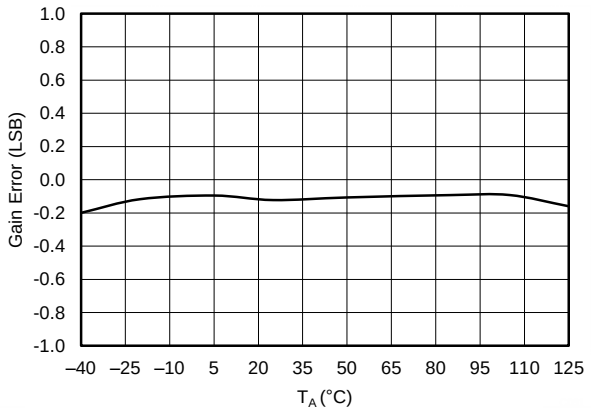
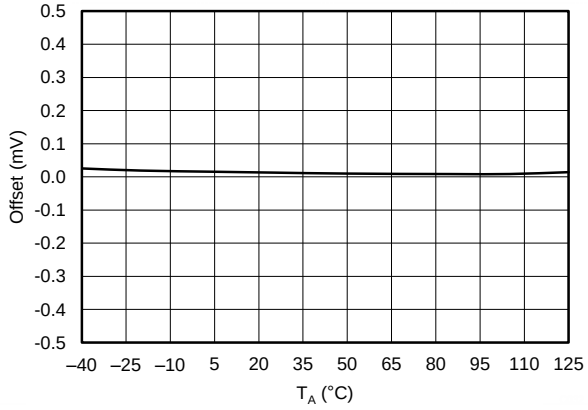


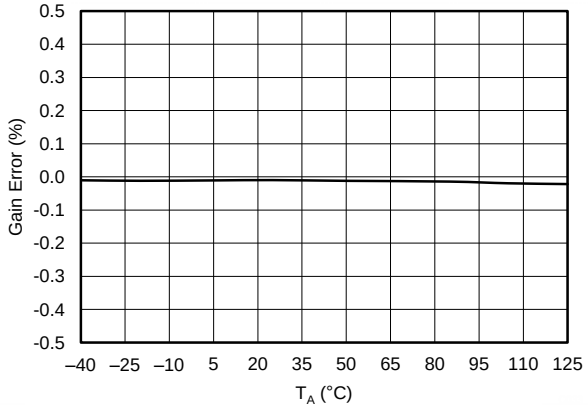
Figure 36. ADC Gain Error vs Temperature

6.12.3 Typical Characteristics: Current Sense



V_{CM} = 28 V, V_{SENSE} = 0 V, CS-FILTER[2:0] = 100

Figure 37. Current Sense Offset Voltage vs Temperature



V_{CM} = 28 V

Figure 38. Current Sense Gain Error vs Temperature

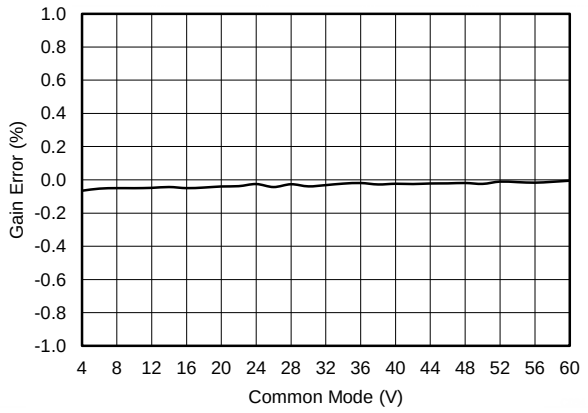
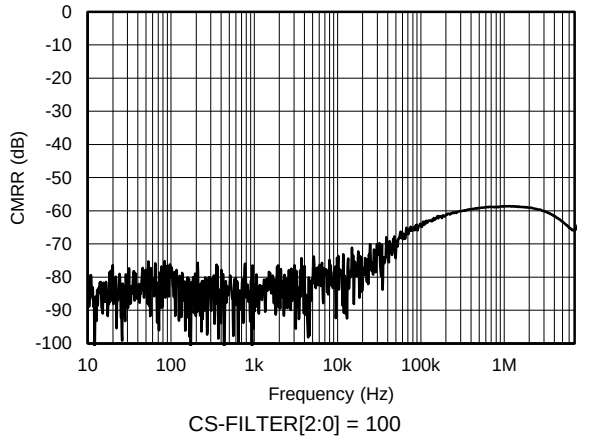


Figure 39. Current Sense Gain Error vs Common-Mode Voltage



CS-FILTER[2:0] = 100

Figure 40. Current Sense CMRR vs Frequency

6.12.4 Typical Characteristics: Temperature Sensor

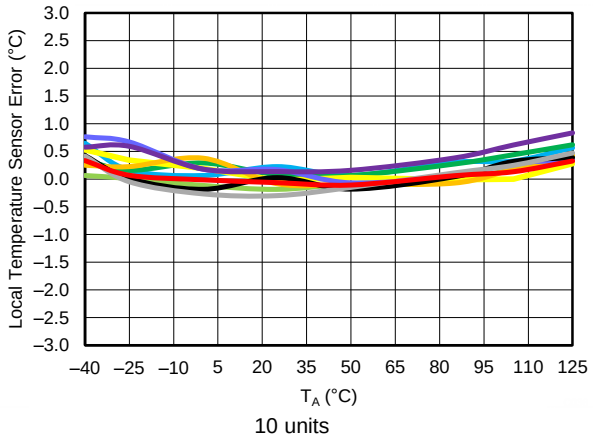


Figure 41. Local Temperature Sensor Error vs Temperature

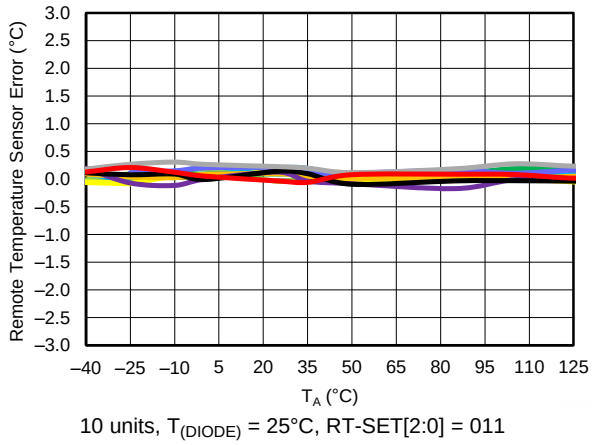


Figure 42. Remote Temperature Sensor Error vs Temperature

6.12.5 Typical Characteristics: Reference

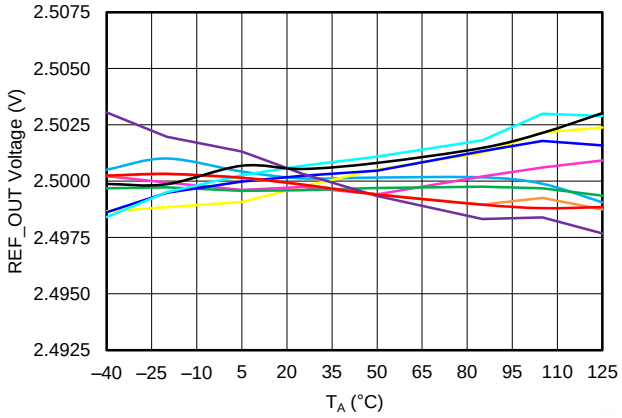


Figure 43. Reference Output Voltage vs Temperature

7 Detailed Description

7.1 Overview

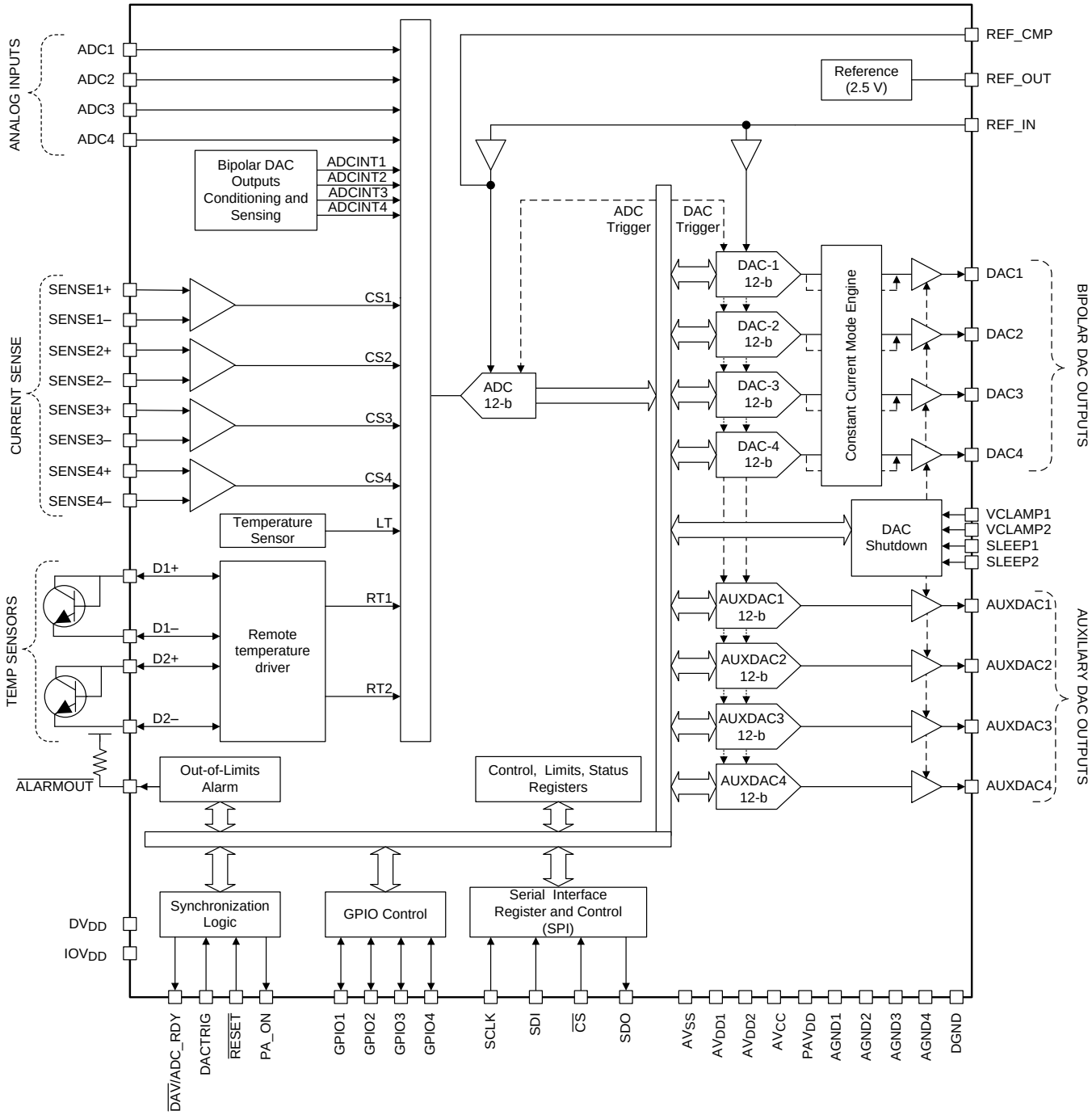
The AMC7834 is a highly-integrated analog-monitoring and control solution for power-amplifier (PA) biasing capable of current, temperature, and voltage supervision. The AMC7834 integrates the following features:

- Eight, 12-bit digital-to-analog converters (DACs) with programmable output ranges
  - Four bipolar DACs with selectable output ranges: –4 to 1 V, –5 to 0 V, and 0 to 5 V
    - The clamp and power-on-reset (POR) voltage for these DACs is pin-configurable.
  - Four auxiliary DACs with selectable output ranges: 0 to 5 V and 2.5 to 7.5 V
    - The clamp and POR voltage for these DACs is fixed to AGND.
  - The DACs can be configured to clamp automatically upon detection of an alarm event.
- A multi-channel, 12-bit analog-to-digital converter (ADC) for voltage, temperature, and current sensing
  - Four external analog inputs: 0 to 2.5 V
  - Four internal inputs for monitoring the bipolar DAC outputs
  - Programmable threshold detectors
- Four high-side current-sense amplifiers
  - Common mode voltages from 4 V up to 60 V
  - The current sensors can optionally be set to operate as part of four independent closed-loop drain-current controllers
- Temperature sensing capabilities
  - On-chip temperature sensor
  - Two remote temperature sensor diode drivers
- Four general-purpose I/O (GPIO) ports
- Internal 2.5 V precision reference
  - The device can operate from an internal reference. Alternatively an external reference can be used.
- Four-wire SPI-compatible interface supporting 1.7 to 3.6 V operation

The AMC7834 device is characterized for operation over the temperature range of –40ºC to 125ºC which makes the device suitable for harsh-condition applications. The device is available in an 8-mm × 8-mm 56-pin VQFN PowerPAD package.

The AMC7834 high-integration makes it an ideal all-in-one, low-cost, bias-control circuit for the PAs found in multi-channel RF communication systems. The flexible DAC output ranges allow the device to be used as a biasing solution for a large variety of transistor technologies such as LDMOS, GaAs, and GaN. The AMC7834 feature set is similarly beneficial in general-purpose monitor and control systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital-to-Analog Converters (DACs)

The AMC7834 device features an analog-control system centered on eight, 12-bit DACs that can operate from an external reference or the device internal reference. Each DAC core consists of a string DAC and an output-voltage buffer.

The resistor-string structure consists of a series of resistors, each with a value of R. The code loaded to the DAC determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier (see Figure 44). The resistor string architecture has inherent monotonicity, voltage output, and low glitch. The resistor string architecture is also linear because all the resistors are of equal value.

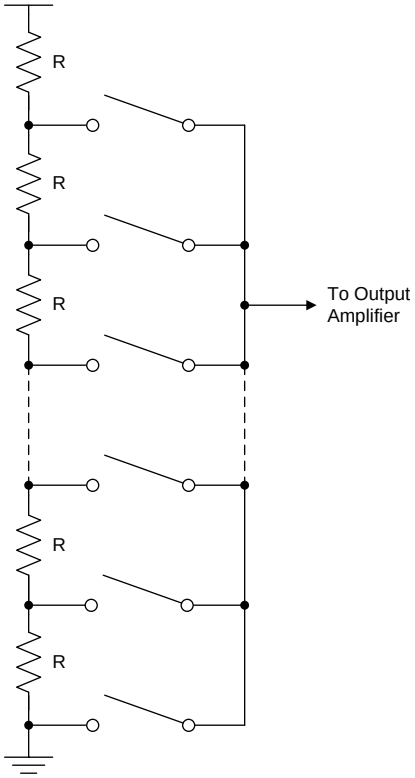


Figure 44. DAC Resistor String

Feature Description (continued)

7.3.1.1 DAC Configuration

The eight DACs are split into bipolar and auxiliary outputs based on their output range and clamping capabilities as listed in Table 1. After power-on or a reset event the DAC outputs are directed automatically to the corresponding clamp value and all DAC buffer and active registers are set to the default values.

Table 1. DAC Group Configuration

DAC	TYPE	OUTPUT RANGES	CLAMP VOLTAGE	POWER SUPPLY RANGE	CLOSED LOOP OPERATION CAPABLE?
DAC1 and DAC2	Bipolar	0 to 5 V –4 to 1 V –5 to 0 V	–3 × VCLAMP1 or AV_{SS}	AV_{SS} to AV_{DD}	Yes
DAC3 and DAC4			–3 × VCLAMP2 or AV_{SS}		
AUXDAC1	Auxiliary	0 to 5 V 2.5 to 7.5 V	AGND	AGND to AV_{CC}	No
AUXDAC2					
AUXDAC3					
AUXDAC4					

7.3.1.1.1 Bipolar DACs (DAC1, DAC2, DAC3, and DAC4)

The bipolar DACs are configured as DAC pairs (DAC1-DAC2 and DAC3-DAC4). The output range for each bipolar DAC pair can be configured through the DAC Range register (address 0x16) to one of the following: 0 to 5 V, –5 to 0 V, or –4 to 1 V. The POR and clamp value of each DAC pair is set by the pins VCLAMP1 (for the DAC1-DAC2 pair) and VCLAMP2 (for the DAC3-DAC4 pair) to any voltage between AV_{SS} and 0 V during normal operation. If AV_{DD} falls outside the device specified operating range the bipolar DACs enter the special AV_{SS} clamp mode and their outputs are set to AV_{SS}. The full-scale output range of the bipolar DACs is limited by the power supplies, AV_{DD} and AV_{SS}.

The bipolar DACs operate as standalone DACs when the AMC7834 is set in open-loop mode (LOOP-EN bit set to 0 in register 0x10). Figure 45 shows a high level block diagram of each bipolar DAC when operating in open-loop mode.

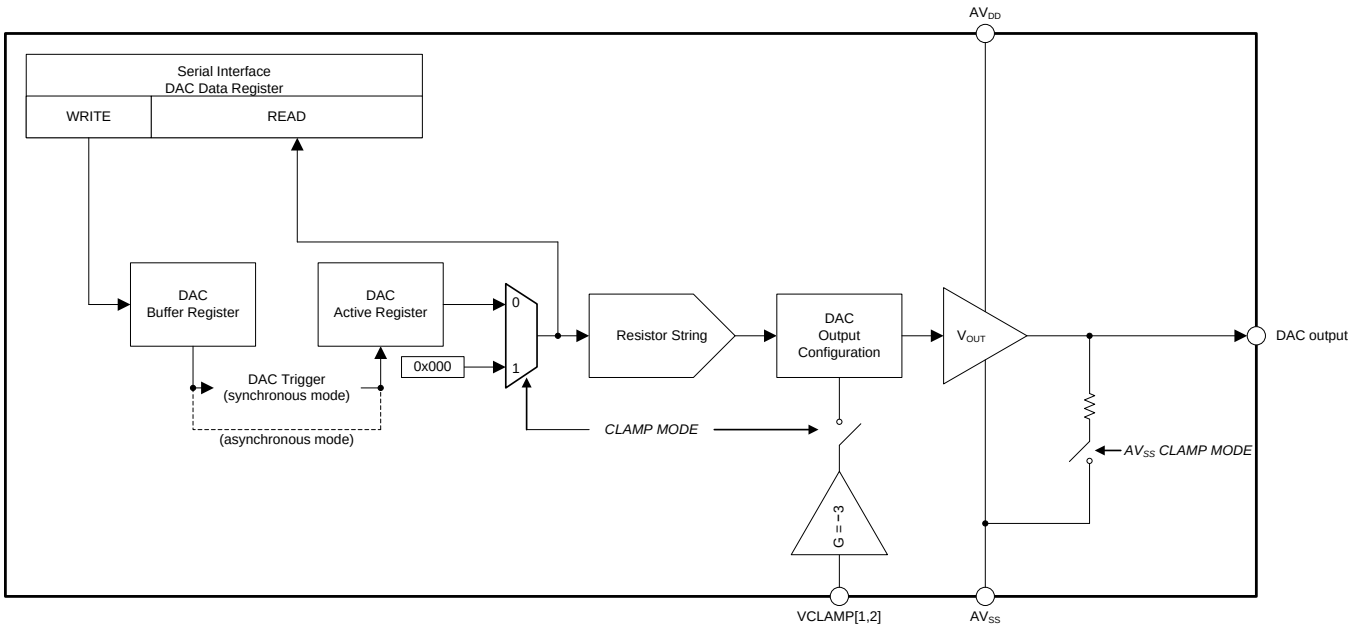


Figure 45. Bipolar DAC Block Diagram — Open Loop Operation

Alternatively, with the AMC7834 set in closed-loop mode (LOOP-EN bit set to 1 in register 0x10) each bipolar DAC output updates automatically in response to one of the four current sensors in the device (see the *Closed-Loop Mode* section). In closed-loop mode the AMC7834 bipolar DACs operate as four autonomous closed-loop current controllers.

The DAC upper threshold registers (address 0x4E through 0x4F) sets an upper output limit other than full-scale for the bipolar DACs when operating in closed-loop mode. The upper threshold feature can be used to limit the maximum output voltage for each bipolar DAC. When a closed-loop controller attempts to set its bipolar DAC to a value exceeding the corresponding DAC upper threshold register, the DAC is updated with the threshold code instead.

7.3.1.1.2 Auxiliary DACs (AUXDAC1, AUXDAC2, AUXDAC3, and AUXDAC4)

The output range for each auxiliary DAC can be independently set through the DAC Range register (address 0x16) to either 0 to 5 V or 2.5 to 7.5 V. The POR and clamp value of each of the auxiliary DACs is fixed to AGND. The maximum and minimum outputs from these DACs cannot exceed AV_{CC} or be lower than AGND, respectively. Figure 46 shows a high level block diagram of each auxiliary DAC.

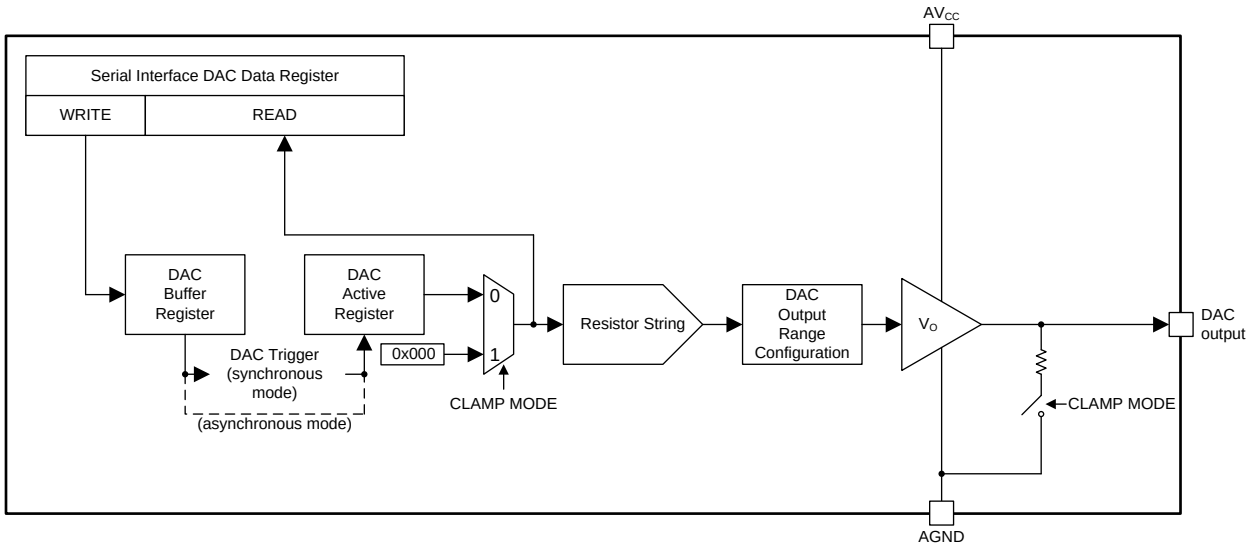


Figure 46. Auxiliary DAC Block Diagram

7.3.1.2 DAC Register Structure

The input data of the DACs is written to the individual DAC data registers (address 0x30 through 0x37) in straight binary format for all output ranges (see Table 2).

Table 2. DAC Data Format

DIGITAL CODE	DAC OUTPUT VOLTAGE (V)			
	0 TO 5 V RANGE	2.5 TO 7.5 V RANGE	–4 TO 1 V RANGE	–5 TO 0 V RANGE
0000 0000 0000	0	2.5	–4	–5
0000 0000 0001	0.00122	2.50122	–3.99878	–4.99878
1000 0000 0000	2.5	5	–1.5	–2.5
1111 1111 1110	4.99756	7.49756	0.99756	–0.00244
1111 1111 1111	4.99878	7.49878	0.99878	–0.00122

Data written to the DAC data registers is initially stored in the DAC buffer registers. The transfer of data from the DAC buffer registers to the active registers can be set to occur immediately (asynchronous mode) or initiated by a DAC trigger signal (synchronous mode). When the active registers are updated, the DAC outputs change to the new values. When the host reads from a DAC data register, the value held in the DAC active register is returned (not the value held in the buffer register).

The update mode of the DACs is determined by the DAC sync register (address 0x15). In asynchronous mode, a write to a DAC data register results in an immediate update of the DAC active register and the corresponding output. In synchronous mode, writing to a DAC data register does not automatically update the DAC output. Instead, the update occurs only after a DAC trigger event. A DAC trigger is generated either through the DACTRIG bit in the DAC and ADC trigger register (address 0x1C) or by the $\overline{\text{DACTRIG}}$ pin. By setting the synchronization properly, several DACs can be updated simultaneously.

7.3.1.3 DAC Clamp Operation

Each DAC can be set to a clamp mode using either hardware or software. When a DAC goes to clamp mode, the DAC output is immediately set to the corresponding clamp voltage. However, clamping does not clear the DAC buffer or active registers making it possible to return to the same voltage being output before the clamp event was issued. The DAC data registers can be updated while the DACs are in clamp mode allowing the DACs to output new values upon return to normal operation. When the DACs exit clamp mode, the DACs are immediately loaded with the data in the DAC active registers and the output is set back to the corresponding level to restore operation regardless of the DAC synchronization setting.

The clamp voltage is dependent on the DAC output:

- DAC1 and DAC2: Clamp voltage is set by the voltage at pin VCLAMP1 and is equal to –3 × VCLAMP1 during normal operation. In the special AV_{SS} clamp mode the clamp voltage for DAC1 and DAC2 is fixed to AV_{SS}.
- DAC3 and DAC4: Clamp voltage is set by the voltage at pin VCLAMP2 and is equal to –3 × VCLAMP2 during normal operation. In the special AV_{SS} clamp mode the clamp voltage for DAC3 and DAC4 is fixed to AV_{SS}.
- AUXDAC1 through AUXDAC4: The clamp voltage for each of the auxiliary DACs is fixed to AGND.

The clamp register (address 0x17) allows clamping of the DACs through software. The DAC1-DAC2 pair, DAC3-DAC4 pair, and each auxiliary DAC has a corresponding DAC clamp bit. Setting this bit to 1 forces the corresponding DAC pair or individual auxiliary DAC to enter clamp mode. Clearing the bit to 0 restores normal operation.

Additionally, in the unique case of the AV_{DD} supply falling outside its specified operating range the bipolar DACs enter the alternative AV_{SS} clamp mode. With the AV_{DD} supply outside of the valid operating range the bipolar DAC output buffers become inactive thus creating the potential for unexpected output voltages. The AV_{SS} clamp mode prevents this condition by setting all bipolar DAC outputs to AV_{SS} through a resistive path.

NOTE

If the DAC or DAC pair is forced to clamp by one of the SLEEP pins, write commands to the corresponding DAC clamp bit are ignored.

The DACs can also be forced to clamp through the SLEEP1 and SLEEP2 pins. When either pin goes high, the corresponding DAC pair and auxiliary DAC associated with each pin are forced into clamp mode. The SLEEP1 register (address 0x18) determines which DACs are forced to clamp when the SLEEP1 pin goes high. The register contains one bit for each DAC pair (DAC1-DAC2 and DAC3-DAC4) and each auxiliary DAC. Likewise, the SLEEP2 register (address 0x19) determines which DACs go into clamp when the SLEEP2 pin goes high. In addition to forcing the DACs into clamp mode, the SLEEP1 and SLEEP2 pin and registers allow control of the PA_ON pin.

Although a high state on the SLEEP pins force the associated DACs to clamp immediately, returning to a low state does not necessarily force the DAC to return to normal operation. If the end application requires the DACs to exit clamp mode in a particular sequence, this sequence can be controlled by the SNOOZE bits in the SLEEP1 and SLEEP2 registers. When a SNOOZE bit is set to 1, bringing a DAC back to normal operation requires the SLEEP pin to return to a low state first, followed by a write to the DAC clamp register (address 0x17) to clear the clamp condition. If the SNOOZE bit is cleared to 0, setting the SLEEP pin to a low state immediately clears the clamp condition and returns the DAC to normal operation without the need for any register writes.

The DACs can be forced to enter clamp mode by the alarm events controlling the $\overline{\text{ALARMOUT}}$ pin. The $\overline{\text{ALARMOUT}}$ clamp register (address 0x1A) selects the DAC or DAC pairs that enter clamp mode when the $\overline{\text{ALARMOUT}}$ pin goes active. Restoring the $\overline{\text{ALARMOUT}}$ pin does not automatically return the DAC or DAC pairs back to normal operation.

7.3.2 Analog-to-Digital Converter (ADC)

The AMC7834 device features a monitoring system centered on a 12-bit successive approximation register (SAR) ADC fronted by a 15-channel multiplexer and an on-chip track-and-hold circuit. The monitoring system is capable of sensing up to 4 external inputs (0 to 2.5 V range), 4 internal inputs (bipolar DAC monitoring), 4 current-sense amplifier inputs, 2 remote temperature sensors, and an internal analog-temperature sensor.

The ADC can operate from either an external 2.5 V reference or the device internal reference (V_{ref}). The ADC input range is 0 V to V_{ref}. All ADC inputs are internally mapped to this range. The ADC timing signals are derived from an on-chip temperature-compensated oscillator. The conversion results can be accessed through the device serial interface.

7.3.2.1 External Analog Inputs

The AMC7834 has 4 analog inputs for external voltage sensing (ADC1 through ADC4). Figure 47 shows the equivalent circuit for each external analog input pin. The two diodes, D1 and D2, provide electrostatic discharge (ESD) protection for the individual analog pins. Diode D1 turns on when any of the inputs is greater than AV_{DD} + 0.3 V. Similarly diode D2 turns on when any of the inputs is less than AGND – 0.3 V. The switch is open while the ADC is in the READY state.

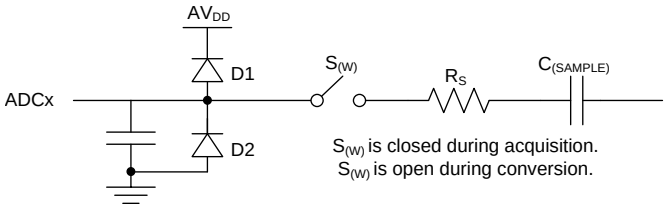


Figure 47. ADC External Inputs Equivalent Circuit

The analog input range for inputs ADC1 through ADC4 is 0 V to V_{ref} and the LSB (least-significant bit) size is given by V_{ref} / 4096. The analog input conversion values are stored in straight binary format in the ADC-External Data registers (address 0x24 through 0x27). The input voltage is calculated using Equation 2.

$$V_{IN} = \frac{CODE \times V_{ref}}{4096} \tag{2}$$

To achieve specified performance it is recommended to drive each analog input pin with a low impedance source. In applications where the signal source has high impedance, analog input must be buffered.

7.3.2.2 Internal Bipolar DAC Monitoring Inputs

The AMC7834 has 4 internal inputs used for monitoring the bipolar DAC outputs (ADCINT1 through ADCINT4). The internal monitoring inputs are particularly useful when the AMC7834 operates in closed-loop mode as the bipolar DAC outputs are autonomously updated by the closed-loop controllers. Continuous monitoring of the bipolar DAC outputs helps in detecting closed-loop controller issues.

The input range for the internal monitoring channels is -2 × V_{ref} to V_{ref} and the LSB size is given by 3 × V_{ref}/4096. The monitored signals are scaled through a resistor divider so that they map to the native input range of the ADC (0 to 2 × V_{ref}).

The internal monitoring inputs conversion values are stored in straight binary format in the ADC-Internal Data registers (address 0x20 through 0x23). The monitored bipolar DAC output voltage is calcualted by Equation 3.

$$V_{ADCINT} = V_{ref} + 3\left(\frac{V_{ref} \times CODE}{4096} - V_{ref}\right) \tag{3}$$

7.3.2.3 ADC Sequencing

The AMC7834 supports autonomous and direct-mode ADC conversions. The conversion method is selected in the AMC configuration 0 register (address 0x10). The default conversion method is autonomous conversion. In both conversion methods, the channel or group of channels to be converted by the ADC must be first configured in the ADC MUX register (address 0x12). The input channels to the ADC include 4 external inputs, 4 DAC monitoring internal inputs, 4 current-sense inputs, 2 remote temperature sensor inputs, and the internal temperature sensor.

The ADC must be in the READY state before a conversion cycle is started. The ADC enters the READY state once powered-up and at least one input channel is enabled in the ADC MUX register. The ADC READY status can be determined either through software (ADC-READY bit in the General Status register, 0x1F) or hardware ($\overline{\text{DAV}}$/ADC_RDY pin). To use the $\overline{\text{DAV}}$/ADC_RDY pin as a READY status indicator, the pin must first be enabled through the DAVPIN-EN bit in register 0x11. Furthermore the ADC_RDY functionality must be selected by setting the DAVPIN-SEL bit in register 0x11 to '1'.

The conversion cycle is initiated by setting the ADC-TRIG bit to 1 in the DAC and ADC Trigger register (address 0x1C) which issues an ADC trigger signal. If the trigger signal is issued while the ADC is not in the READY state it is ignored.

Once the conversion cycle starts the ADC leaves the READY state. In direct-mode conversion upon completion of the first conversion sequence the ADC returns to the READY state and waits for a new trigger signal. Alternatively, in autonomous conversion upon completion of the first conversion another sequence is automatically started. Conversion of the selected channels occurs repeatedly until the conversion is stopped by issuing another trigger signal, at which point the ADC returns to the READY state.

The following ADC registers should only be updated while the ADC is not in a conversion cycle:

- Device configuration register (address 0x02)
- AMC configuration 0 register (address 0x10)
- AMC configuration 1 register (address 0x11)
- ADC MUX register (address 0x12)
- ALARMOUT configuration register (0x1B)
- Threshold registers (0x40 – 0x4D)
- Hysteresis registers (0x50 – 0x56)

After updating any of the configuration registers listed above, either a minimum 2 µs wait time or READY state must be ensured before issuing an ADC trigger signal.

Since the ADC is used for voltage, current, and temperature sensor conversions, all of which have significantly different update times, an interleaved conversion sequence is followed. The interleaved sequence ensures the wait time between measurement updates is minimized. Figure 48 illustrates the ADC conversion sequence with all input channels enabled and set to their fastest update time (CS-FILTER[2:0] = 000 and RT-SET[2:0] = 000 in the AMC Configuration register - 0x10).

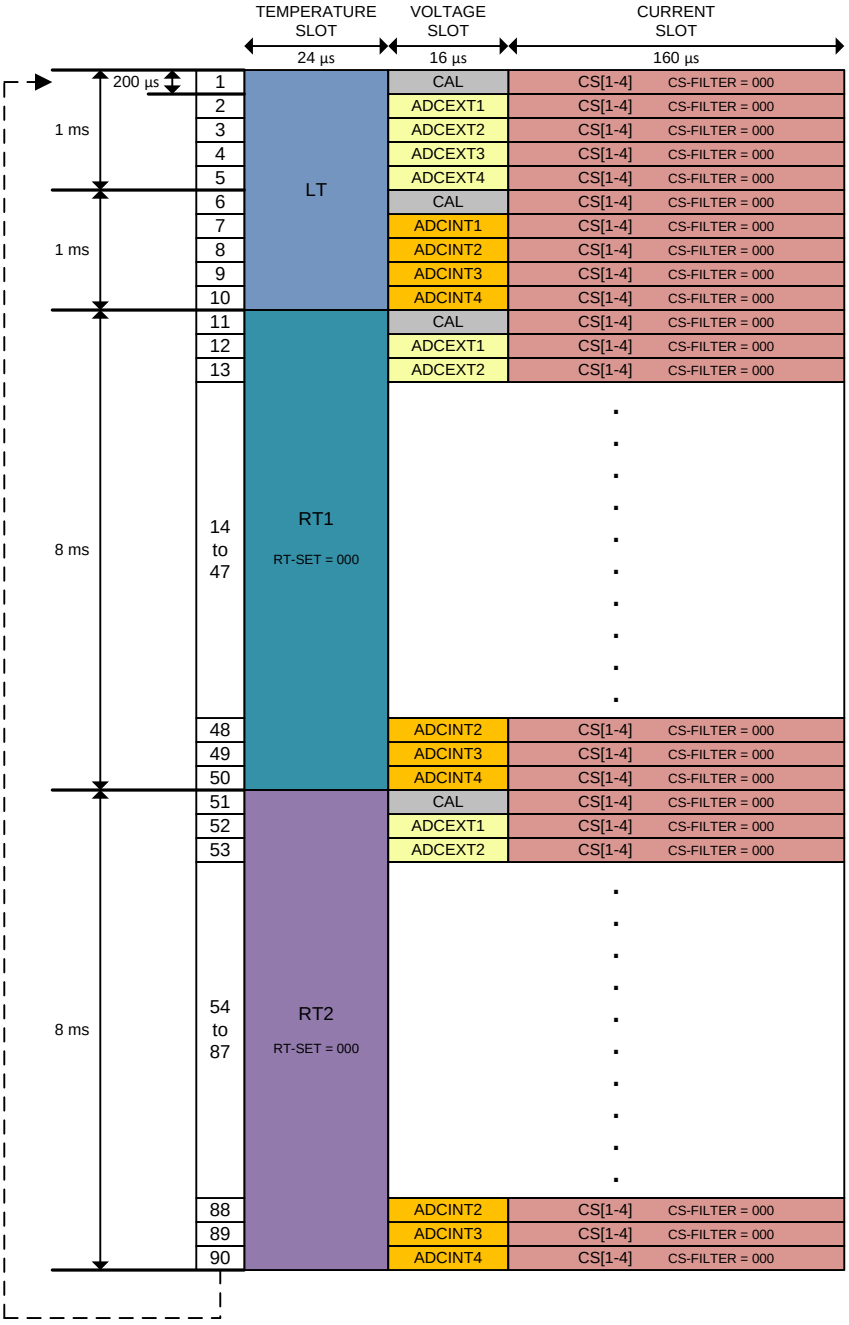


Figure 48. ADC General Interleaved Sequence

Each ADC interleave step takes 200 µs and is segmented intro three sensing slots: temperature, voltage and current. The temperature slot is 24 µs long and allocates the temperature sensing channel conversions (internal temperature sensor and two remote temperature sensors) following the order LT → RT1 → RT2 → LT → ... If one of the temperature channels is not selected for conversion it is skipped. For example, if RT1 is not selected for conversion, the temperature slot conversion sequence is LT → RT2 → LT → ... Figure 48 illustrates the conversion sequence for the lowest remote temperature sensor update time, which is configured by setting RT-SET[2:0] = 000 in register 0x10. If a longer temperature sensor is selected to improve measurement accuracy a higher number of interleave steps is allocated for the remote temperature sensors.

The voltage slot takes 16 µs and allocates the four external inputs and four DAC monitoring internal inputs conversions. The external inputs, if enabled, are converted first. If none of the channels in a group (external or internal) are selected, no time is allocated for conversion of that group. However if at least one of the input channels in a group is enabled, five interleave steps (1 ms) are allocated regardless of the total number of input channels.

The current slot allocates the four current sensing channel conversions. The current slot is 160 µs long independent of how many current sense channels are enabled. The current sensors are updated on each interleave step (200 µs) when the CS-FILTER[2:0] set to 000 in register 0x10. If a longer current sense update time is selected to improve measurement accuracy a higher number of interleave steps is allocated for the current sense conversions.

The update time for all monitoring inputs is determined by the interleave sequence followed. Direct-mode conversions require an additional 40 µs of update time. In order to simplify synchronization, the AMC7834 provides a data-available signal through the DAV/ADC_RDY pin. The DAV/ADC_RDY pin must first be enabled through the DAVPIN-EN bit in register 0x11. Furthermore the DAV functionality must be selected by clearing the DAVPIN-SEL bit in register 0x11 to '0'.

In direct-mode conversion the DAV/ADC_RDY pin goes low after the conversion sequence has been completed. Additionally, in direct-mode conversion the data available flags in the General status register (address 0x1F) can be used to determine when new data is available for each data-available channel group. In autonomous conversion the DAV/ADC_RDY pin indicates when new data is available for each data-available channel group by issuing a 20 µs pulse (active low).

In both conversion methods the data-available function identifies six channel groups:

1. Current sense inputs: CS1 through CS4
2. External analog inputs: ADC1 through ADC4
3. Internal monitoring inputs: ADCINT1 through ADCINT4
4. Internal temperature sensor: LT
5. Remote temperature sensor 1: RT1
6. Remote temperature sensor 2: RT2

7.3.3 Temperature Sensors

The AMC7834 device includes one on-chip and two remote temperature sensors. The temperature sensors monitor the three temperature inputs. The on-chip integrated temperature sensor measures the device temperature and two remote diode-sensor inputs measure two external temperature points. All three temperature-sensor results are converted by the device ADC and stored in two's complement format. If any sensor is not used, it can be disabled in the register configuration. When any of the temperature sensors is disabled it is not converted by the ADC.

7.3.3.1 Internal Temperature Sensor

The AMC7834 device has an on-chip temperature sensor that measures the device die temperature. The temperature-sensor results are converted by the device ADC (see the *Analog-to-Digital Converter (ADC)* section for more information). If internal temperature sensor conversion is not needed, it can be disabled in the ADC MUX register (address 0x12). When disabled the temperature sensor output is not converted by the ADC.

The temperature sensor provides 0.25°C resolution over the device operating temperature range. Additionally, the AMC7834 internal temperature sensor is specified monotonic down to –55°C. The temperature value is stored in 12-bit two's complement format in the LT-data register (address 0x2D).

Table 3. Temperature Sensor Data Format

TEMPERATURE (°C)	DIGITAL CODE
–55	1111 0010 0100
–40	1111 0110 0000
–25	1111 1001 1100
–10	1111 1101 1000
–0.25	1111 1111 1111
0	0000 0000 0000
0.25	0000 0000 0001
10	0000 0010 1000
25	0000 0110 0100
50	0000 1100 1000
75	0001 0010 1100
100	0001 1001 0000
105	0001 1010 0100
125	0001 1111 0100

Use Equation 4 and Equation 5 to calculate the positive or negative temperature according to the polarity of the temperature data MSB (0 = positive, 1 = negative).

$$\text{Positive Temperature (°C)} = \frac{\text{Code}}{4} \quad (4)$$

$$\text{Negative Temperature (°C)} = \frac{4096 - \text{Code}}{4} \quad (5)$$

7.3.3.2 Remote Temperature Sensors

The AMC7834 device includes two remote junction-temperature sensors. The remote sensing transistors can be a discrete, small-signal type transistor or a substrate transistor built within the power amplifier. These transistors are typically low-cost NPN- or PNP-type transistors such as the 2N3904 and 2N3906. Figure 49 shows the recommended connection for NPN and PNP transistors in diode configuration.

The AMC7834 device also allows PNP transistor configuration as shown in Figure 50. PNP transistor configuration for both remote temperature sensors is enabled by setting the RMT-GND-COLL bit to 1 in register 0x11.

NOTE

Pins D1– and D2– are internally shorted. Total parasitic capacitance to AGND on these pins must be less than 800 pF.

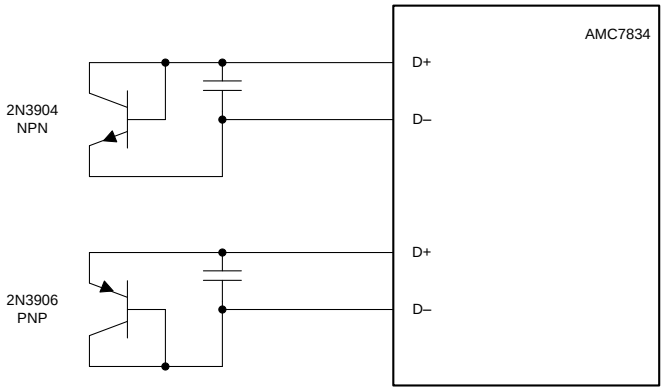


Figure 49. NPN and PNP Diode Configuration

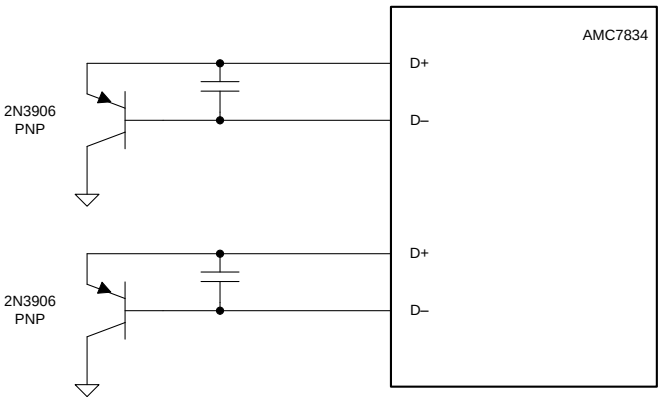


Figure 50. PNP Transistor Configuration

Errors in remote temperature sensor readings are typically the consequence of misalignment in the ideality factor and current excitation used by the AMC7834 versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a low-level (I_{LOW}) and high-level (I_{HIGH}) current for the temperature-sensing substrate transistors. The AMC7834 uses an I_{LOW} of 7 µA and I_{HIGH} of 112 µA and is designed to work with discrete transistors, such as the 2N3904 and SN3906. If an alternative transistor is used, the following conditions should be met:

1. Base-emitter voltage (V_{BE}) > 0.25 V at 7 µA for the highest sensed temperature
2. Base-emitter voltage (V_{BE}) < 1.20 V at 112 µA for the lowest sensed temperature
3. Base resistance < 100 Ω
4. Tight control of V_{BE} characteristics indicated by small variations in h_{FE} (50 to 150)

The ideality factor (η) is a measured characteristic of a remote temperature sensor diode as compared to an ideal one. The AMC7834 is trimmed for η = 1.008. If the selected remote sensing transistor's ideality factor is different, the effective η-factor should be adjusted at the system level.

Remote junction-temperature sensors are usually implemented in a noisy environment. Noise is most often created by fast digital signals and can corrupt measurements. A bypass capacitor placed differentially across the inputs of the remote temperature sensors can make the application more robust against unwanted coupled signals. If filtering is required, its time constant, including any routing resistance, should be limited to 5 µs or less. The combined series resistance on the remote temperature sensor pins must be less than 1 kΩ.

The two remote temperature sensor results are converted by the device ADC (see the *Analog-to-Digital Converter (ADC)* section for more information). The two remote temperature sensors can be disabled in the ADC MUX register (address 0x12). When disabled, the remote temperature sensor outputs are not converted by the ADC. The remote temperature values are stored in 12-bit two's complement format in the RT-data registers (address 0x2E and 0x2F) using the same data format as the internal temperature sensor (see Table 3).

The AMC7834 device enables optimization of the remote temperature measurements by increasing the update time. The remote temperature-sensor update time is selected by the RT-SET[2:0] setting in register 0x10. Table 4 lists the total update time for the two remote temperature sensors with respect to the RT-SET[2:0] setting.

Table 4. Two Remote Temperature Sensors Update Time

RT-SET[2:0]	TOTAL UPDATE TIME (ms)
000	16
001	16
010	18
011	26
100	50
101	98
All others	Not valid

Optimal remote temperature sensor accuracy is achieved with the current-sense inputs disabled. In applications requiring simultaneous current-sensor and remote temperature sensor conversions it is recommended to implement external remote temperature conversion averaging to attain best accuracy results.

7.3.4 Current Sensors

The AMC7834 device integrates four unidirectional high-side current-sense amplifiers that amplify a small differential voltage developed across a current-sense resistor in the presence of high-input common-mode voltages. The AMC7834 current-sense amplifiers accept input signals with a common-mode voltage range from 4 V to 60 V. Each amplifier can operate with differential voltages up to 200 mV.

As shown in Figure 51, current flowing through R_{SENSE} develops a voltage drop, V_{SENSE}. The voltage across the sense resistor, V_{SENSE}, is applied to one of the AMC7834 current-sense amplifier inputs. The current sense inputs should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

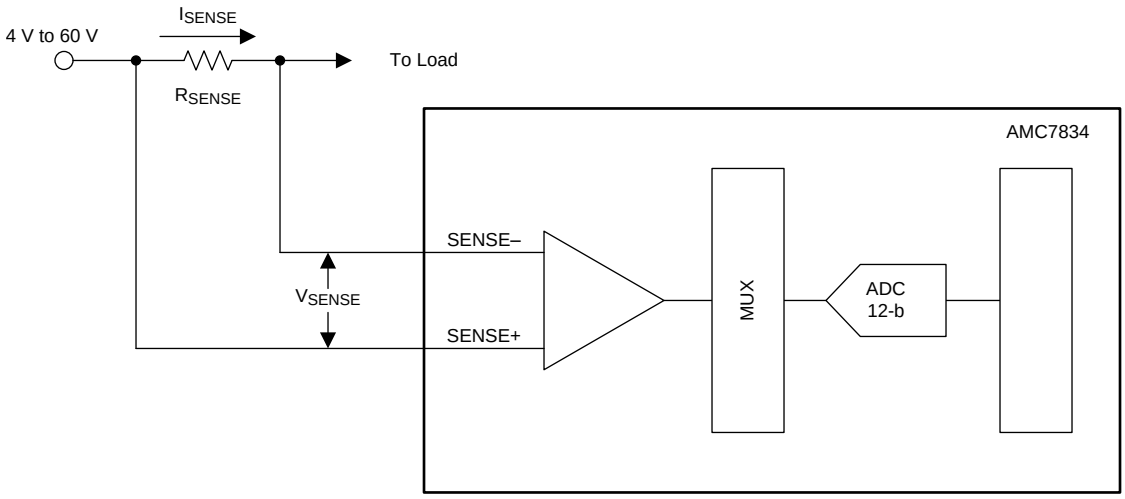


Figure 51. AMC7834 Current-Sense Amplifier

The accuracy of the current measurement depends heavily on the accuracy of the shunt resistor, $R_{(SENSE)}$. The use of a *Kelvin* sense resistor is highly recommended (see Figure 52).

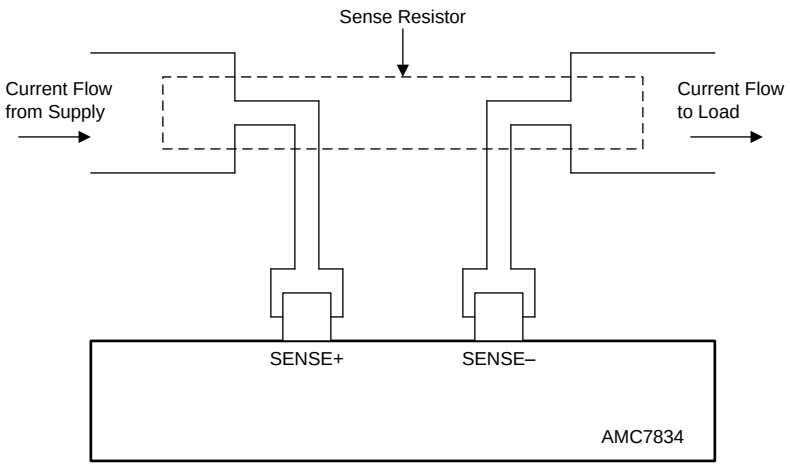


Figure 52. Kelvin Connection to the Sense Resistor

The sense-resistor value is application dependent and is typically a compromise between small-signal accuracy, maximum permissible voltage drop, and allowable power dissipation in the current measurement circuit. For best results, the value of the resistor is calculated from the maximum-expected load current, I_{Lmax}, and the maximum differential voltage supported by the current-sense amplifier (200 mV). High values of $R_{(SENSE)}$ provide better accuracy at lower currents by minimizing the effects of the current-sense amplifier offset. Low values of $R_{(SENSE)}$ minimize load voltage loss, but at the expense of low current accuracy. In general, a compromise between low current accuracy and load circuit losses must be made.

The maximum differential voltage, V_{SENSE}, supported by the AMC7834 current-sense amplifiers is 200 mV. Use Equation 6 to calculate the $R_{(SENSE)}$ value.

$$R_{(SENSE)} = V_{SENSE} / I_{Lmax} \quad (6)$$

The maximum power dissipation of the sense resistor should not be exceeded. Use Equation 7 to calculate the maximum sense resistor power dissipation.

$$P_{R(SENSE)} = V_{SENSE} \times I_{Lmax} \quad (7)$$

The current sensors operate as four standalone current-sense amplifiers when the AMC7834 is set in open-loop mode (LOOP-EN bit set to 0 in register 0x10). In open-loop mode the current-sense amplifier outputs are converted by the device ADC and the results are stored in straight binary format in the CS-Data registers (address 0x29 through 0x2B). Use Equation 8 to calculate the differential voltage, V_{SENSE}.

$$V_{SENSE} = \frac{CODE \times 0.2}{4096} \quad (8)$$

Alternatively, with the AMC7834 set in closed-loop mode (LOOP-EN bit set to 1 in register 0x10) the current sensors operate as part of four independent closed-loop current controllers. In closed-loop operation, four autonomous closed-loop current controllers are implemented by continuously adjusting the bipolar DAC outputs in response to the current-sense amplifier outputs (see the *Closed-Loop Mode* section).

The AMC7834 device enables digital filtering of the current sense measurements to improve their accuracy at the cost of a longer update time. The current sense digital filter is enabled by the CS-FILTER[2:0] setting in register 0x10 and its corresponding transfer function is given by Equation 9.

$$H(z) = \frac{1}{1-(K-1)z^{-1}} \quad (9)$$

Table 5 lists the K value associated with each of the allowable CS-FILTER[2:0] settings as well as the corresponding update time.

Table 5. Current Sense Digital Filter Configuration

CS-FILTER[2:0]	K	UPDATE TIME (ms)
000	1	0.2
001	2	3.4
010	4	6.6
011	8	13
100	16	25.6
All others	Not valid	

7.3.5 Drain Switch Control

The AMC7834 device includes an output-control voltage (PA_ON pin) capable of driving an external PMOS switch that turns on and off the drain current to a PA FET. The use of this control signal in conjunction with the DAC clamp option allows control of the sequence in which the PA FET is powered up and powered down.

The OFF and ON states of the PA_ON signal are equal to the PAV_{DD} and AGND pins, respectively. The default state of the PA_ON signal is off (PMOS switch off).

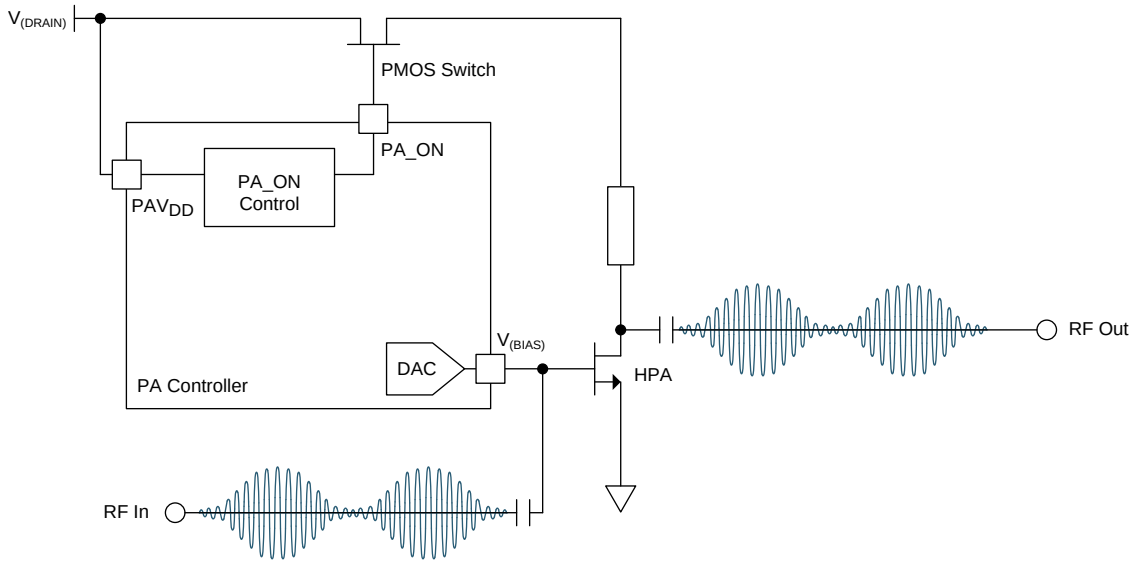


Figure 53. PA_ON Operation

The maximum output voltage is determined by the PAV_{DD} pin and limited to a maximum of 20 V. For PA FETs with drain voltages higher than 20 V, tying the PAV_{DD} pin to one of the other supply devices (preferably AV_{DD}) and scaling the control signal externally is recommended.

The PA_ON signal state can be set through a register write, but it can also be configured to be triggered automatically by the $\overline{\text{ALARMOUT}}$ pin, any of the SLEEP signals or by the special AV_{SS} and AV_{DD} monitoring circuits.

For FETs requiring a negative bias voltage, such as GaN, ensuring that the bias voltage remains within an acceptable range is crucial otherwise significant and irreversible damage to the FET can occur. The AMC7834 bipolar DAC operation and clamping mechanism rely on the AV_{DD} and AV_{SS} voltages for proper operation. For this reason, when either the AV_{DD} or AV_{SS} voltage falls outside its acceptable range, turning off the drain current to the FET is desirable.

The AV_{DD} detection circuit is set to trigger the PA_ON signal to the OFF state in response to an out of range event. Additionally, the AV_{SS} detection alarm can be set to trigger the PA_ON signal to the OFF state by setting the PAON_AVSS bit to 1 in the AMC configuration 1 register (address 0x11). The AV_{SS} alarm is set by default to prevent the PA_ON output from entering the ON state (PMOS switch on). In this case writing to the PA_ON register bit to enable the ON state is ignored. If this additional protection is not needed it can be disabled by clearing the PAON_AVSS bit.

7.3.6 Programmable Out-of-Range Alarms

The AMC7834 device is capable of continuously analyzing the four internal ADC monitoring inputs (bipolar DAC-output monitoring), current sensors, temperature sensors, and negative supply for normal operation.

Normal operation is established through the lower and upper threshold registers (address 0x40 through 0x4D). When any of the monitored inputs is out of the specified range, an alarm event is issued and the global alarm bit, GALARM in the General Status register (address 0x1F), is set (see Figure 54). The alarm status register (address 0x1E) indicates the source of the alarm event.

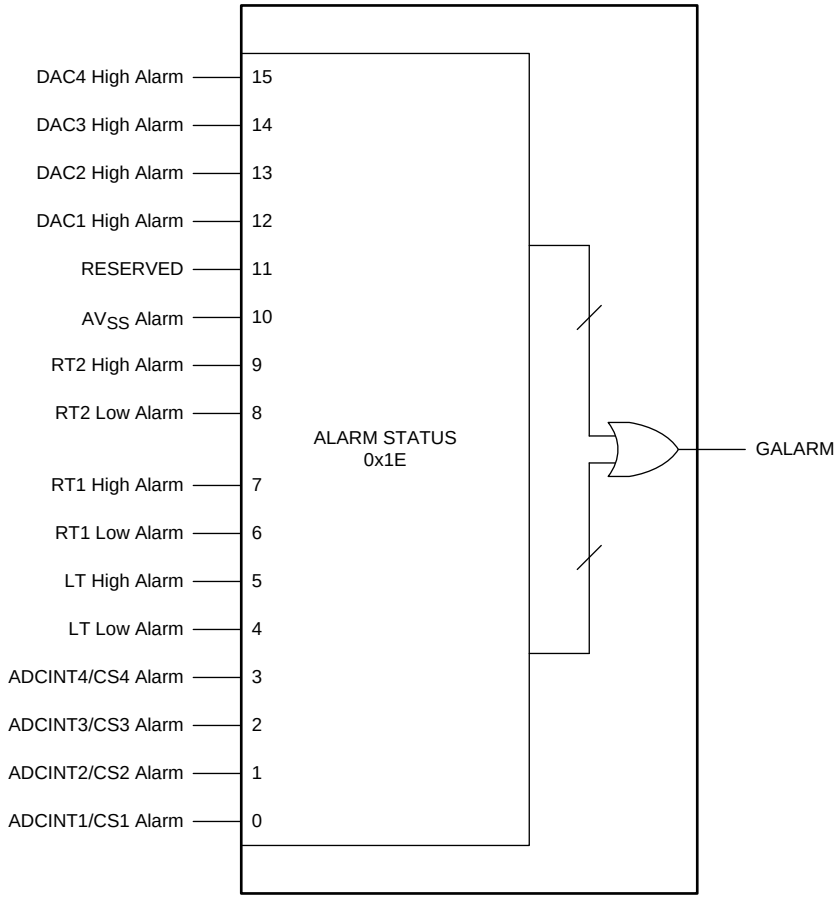


Figure 54. AMC7834 Alarm Status Register

The ALARM-LATCH-DIS bit in the ALARMOUT configuration register (address 0x1B) sets the latching behavior for all alarms. When the ALARM-LATCH-DIS bit is cleared to 0 the alarm bits in the alarm status register are latched. The alarm bits are referred to as being latched because the bits remain set until read by software. This design ensures that out-of-limit events cannot be missed if the software is periodically polling the device. All bits are cleared when reading the alarm status register, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle, unless otherwise noted. When the ALARM-LATCH-DIS bit is set to 1, the alarm bits are not latched. The alarm bits in the alarm status register are set to 0 when the error condition subsides, regardless of whether the bit is read or not.

All of the alarms can be set to activate the $\overline{\text{ALARMOUT}}$ pin. The $\overline{\text{ALARMOUT}}$ pin is an open-drain pin and therefore an external pullup resistor to a voltage no higher than that of the AV_{DD} pin is required. The $\overline{\text{ALARMOUT}}$ output polarity is defined through the ALARMOUT-POLARITY bit in the ALARMOUT configuration register (address 0x1B). The default polarity is active low (ALARMOUT-POLARITY = 0). The polarity can be changed to active high by setting the ALARMOUT-POLARITY bit to 1. The $\overline{\text{ALARMOUT}}$ pin works as an interrupt to the host so that it can query the alarm status register to determine the alarm source. Any alarm event can activate the pin as long as the alarm is not masked in the ALARMOUT configuration register. When an alarm event is masked, the occurrence of the event sets the corresponding status bit in the alarm status register, but does not activate the $\overline{\text{ALARMOUT}}$ pin.

The $\overline{\text{ALARMOUT}}$ status can be configured to automatically clamp specific DACs or set the PA_ON signal to the OFF state. The ALARMOUT clamp register selects the DAC or DAC pairs that enter the clamp mode as well as the PA_ON behavior when the $\overline{\text{ALARMOUT}}$ pin is active. Clearing the alarm events does not automatically bring the DAC or DAC pairs back to normal operation or return the PA_ON to the ON state.

7.3.6.1 ADC Internal Monitoring Input Out-of-Range Alarm

The AMC7834 device can provide out-of-range detection for the four internal ADC inputs monitoring the bipolar DAC outputs when operating in closed-loop mode. The ADCINT/CS-SELECT bit in register 0x1B must be cleared to 0 to enable out-of-range detection on the internal ADC inputs.

Figure 55 shows the out-of-range detection block. When the measurement is out-of-range, the corresponding alarm bit in the alarm status register is set to 1 to flag the out-of-range condition. The values in the ADCINTn/CSn upper and lower threshold registers (address 0x40 through 0x47) define the upper- and lower-bound thresholds for these inputs when the ADCINT/CS-SELECT bit in the ALARMOUT configuration register (address 0x1B) is cleared to 0.

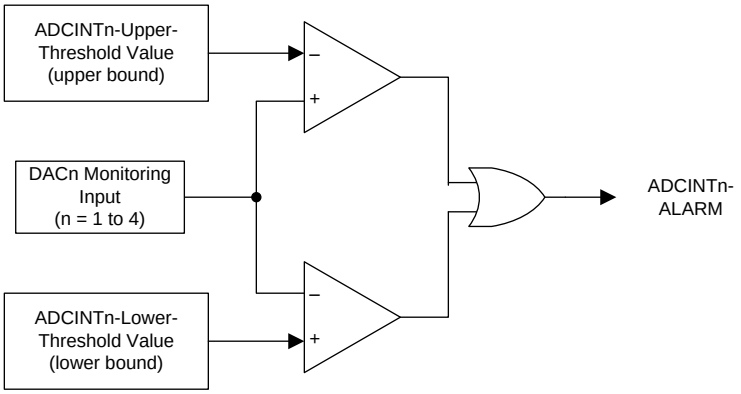


Figure 55. ADC Monitoring Out-of-Range Alarm

7.3.6.2 Current-Sense Out-of-Range Alarm

The AMC7834 device is capable of providing out-of-range detection for the four current-sense inputs when operating in open-loop mode. The current-sense out-of-range detection is only active if the ADCINT/CS-SELECT bit in register 0x1B is set to 1.

Figure 56 shows the current sense detection block. When the measurement is out-of-range, the corresponding alarm bit in the alarm status register is set to 1 to flag the out-of-range condition. The values in the ADCINTx/CSx upper and lower threshold registers (address 0x40 through 0x47) define the upper- and lower-bound thresholds for these inputs when the ADCINT/CS-SELECT bit in the ALARMOUT configuration register (address 0x1B) is set to 1.

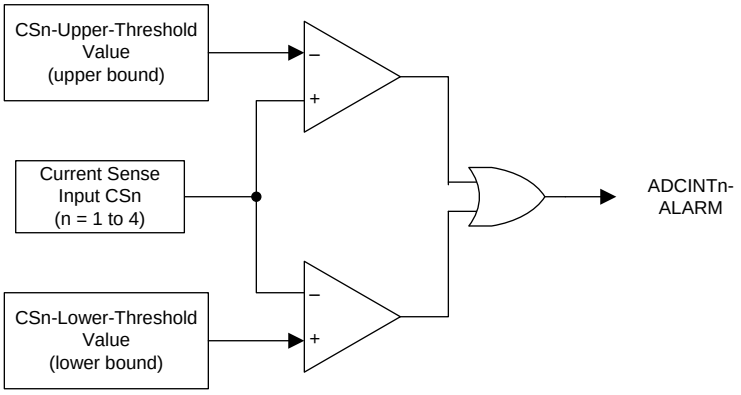


Figure 56. Current-Sense Out-of-Range Alarm

7.3.6.3 Temperature Sensors Out-of-Range Alarm

The AMC7834 device also includes high-limit or low-limit detection for the temperature sensors. Figure 57 shows the temperature detection block. The values in the temperature sensors upper and lower threshold registers (address 0x48 through 0x4D) set the limits for the temperature sensors. The temperature sensors can issue either a high alarm (HIGH-ALARM bit) or a low alarm (LOW-ALARM bit) in the alarm status register (address 0x1E) depending on whether the high or low thresholds were exceeded. To implement single, upper-bound threshold detection for the temperature sensors, the host processor can set the upper-bound threshold to the desired value and the lower-bound threshold to the default value. For lower-bound threshold detection, the host processor can set the lower-bound threshold to the desired value and the upper-bound threshold to the default value.

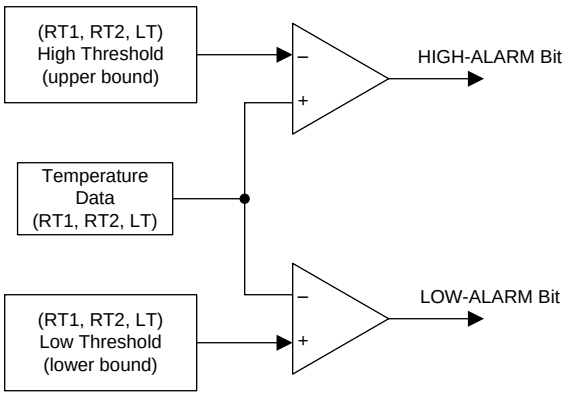


Figure 57. Temperature Out-of-Range Alarm

7.3.6.4 Bipolar DACs High Alarm

The AMC7834 device includes configurable upper-limit detection for the bipolar DACs in closed-loop mode. Figure 58 shows the alarm detection block. The values in the bipolar DAC upper threshold registers (address 0x4E through 0x4F) set a limit other than full-scale limit for the bipolar DACs. When a closed-loop controller attempts to set its bipolar DAC to a value exceeding the corresponding upper-threshold register, the DAC is instead updated with the threshold value and a DAC high-alarm is issued in the alarm status register.

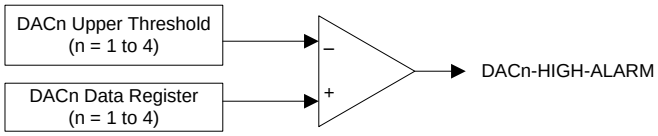


Figure 58. Bipolar DAC High Alarm

7.3.6.5 AV_{SS} Detection Alarm

The device continuously monitors the AV_{SS} supply to ensure it is within the required operating threshold. By setting the PAON_AVSS bit to 1 in the AMC configuration 1 register (address 0x11) the AV_{SS} alarm can be set to automatically set the PA_ON pin to the OFF state and prevent it from getting configured back to the ON state unless the AV_{SS} alarm has been cleared.

7.3.6.6 AV_{DD} Detection Alarm

The device continuously monitors the AV_{DD} supply to ensure it is within the required operating threshold. An AV_{DD} alarm initiates a POR event which sets the PA_ON pin to the OFF state, bipolar DACs to the AV_{SS} clamp mode and auxiliary DACs to clamp mode.

7.3.6.7 Hysteresis

If a monitored signal is out of range and the alarm is enabled, the corresponding alarm bit is set to 1. However, the alarm condition is cleared only when the conversion result returns either a value lower than the high threshold register setting or higher than the low threshold register setting by the number of codes specified in the hysteresis setting (Figure 59). The hysteresis registers (address 0x50 through 0x56) store the hysteresis value for the programmable alarms. The hysteresis is a programmable value between 0 LSB to 127 LSB for the internal ADC monitoring and current-sense alarms and 0°C to 31°C for the temperature-sensor alarms.

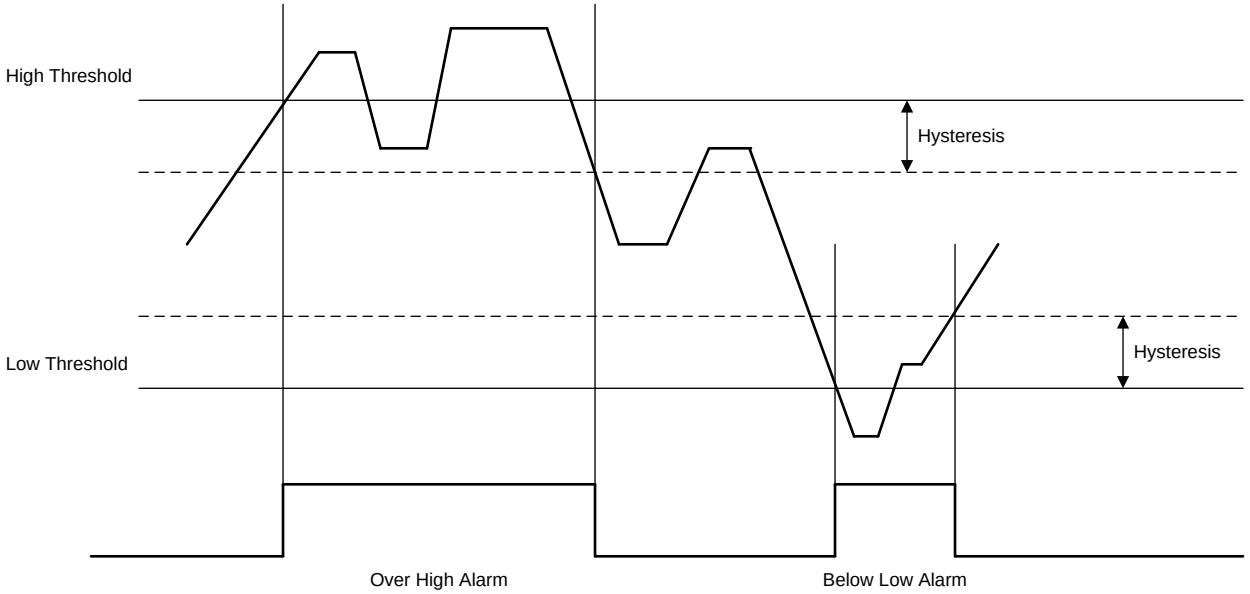


Figure 59. Device Hysteresis

7.3.6.8 False-Alarm Protection

To prevent false alarms, an alarm event is only registered when the monitored signal is out of range for an *N* number of consecutive conversions. If the monitored signal returns to the normal range before N consecutive conversions, an alarm event is not issued. The false alarm factor, N, can be configured in the AMC configuration 1 register (address 0x11).

7.3.7 Reference Specifications

The AMC7834 device includes a high-performance 2.5 V reference. Operation from an external reference is also supported.

7.3.7.1 Internal Reference Operation

The AMC7834 device includes a 2.5 V bipolar transistor-based, precision bandgap reference. The internal reference is externally available at the REF_OUT pin and can be used to drive the ADC and eight DACs by connecting the REF_OUT pin to the REF_IN pin (see Figure 60). A 10-nF capacitor is recommended between REF_OUT and AGND for noise filtering. An external buffer amplifier with a high-impedance input must be used to drive any external load. A compensation capacitor (4.7 µF, typical) should be connected between the REF_CMP pin and the AGND4 pin.

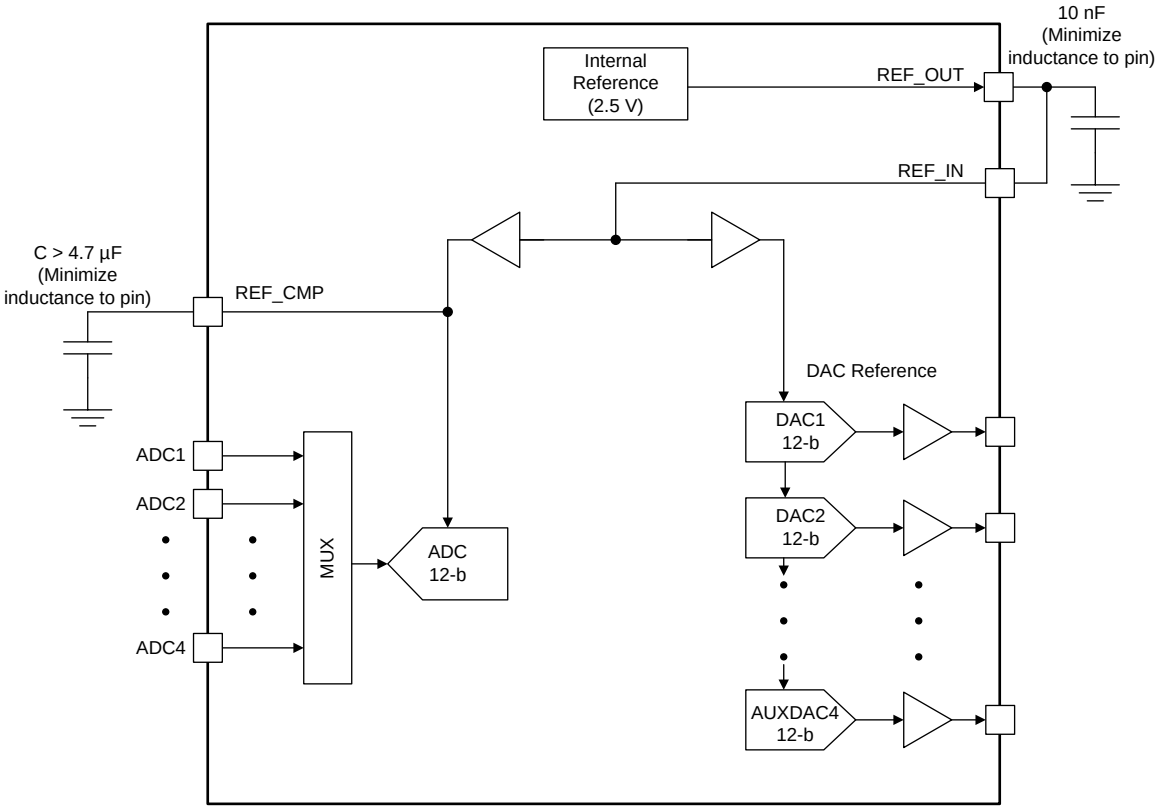


Figure 60. Internal Reference Operation

7.3.7.2 External Reference Operation

The AMC7834 device can also operate from an external reference. The external reference can be applied to the REF_IN pin and is used to drive both the ADC and the eight DACs through separate buffers (see Figure 61). As with the internal-reference case a compensation capacitor (4.7 µF, typical) should be connected between the REF_CMP pin and the AGND4 pin. The REF_OUT pin can be left floating if unused.

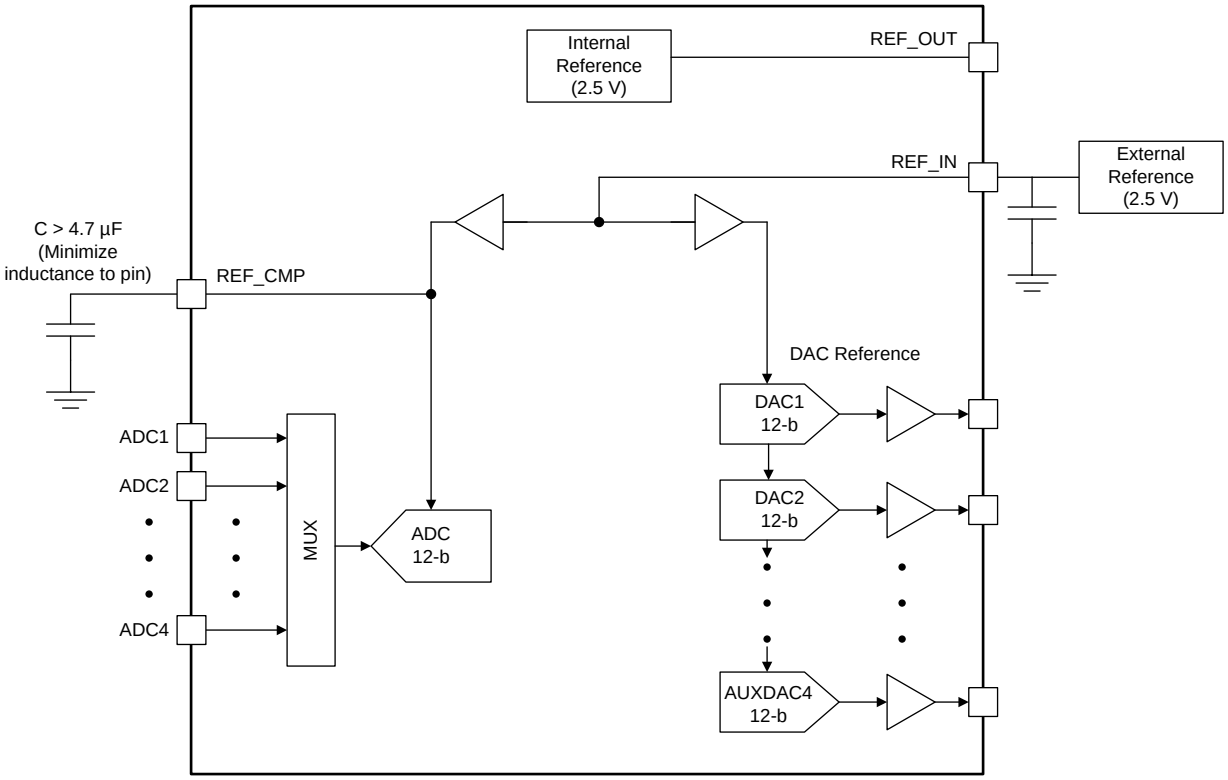


Figure 61. External Reference Operation

7.3.8 General Purpose I/Os

The AMC7834 device includes four GPIO pins. The GPIO pins can receive an input or produce an output (see Figure Figure 62). When the GPIOn pin acts as an output, it has an open-drain, and the status of this pin is determined by the corresponding GPIO bit in the GPIO register (address 0x58). The output state is high impedance when the GPIOn bit is set to 1, and is logic low when the GPIOn bit is cleared to 0.

NOTE

A 10-kΩ pullup resistor is required when using a GPIO pin as an output. The pullup voltage must not exceed the AV_{DD} supply.

To use a GPIO pin as an input, the corresponding GPIO bit in the GPIO register must be set to 1. When a GPIO pin acts as input, the digital value on the pin is acquired by reading the corresponding GPIO bit. After a power-on reset or any forced reset, all GPIO bits are set to 1, and the GPIO pins enter a high impedance state.

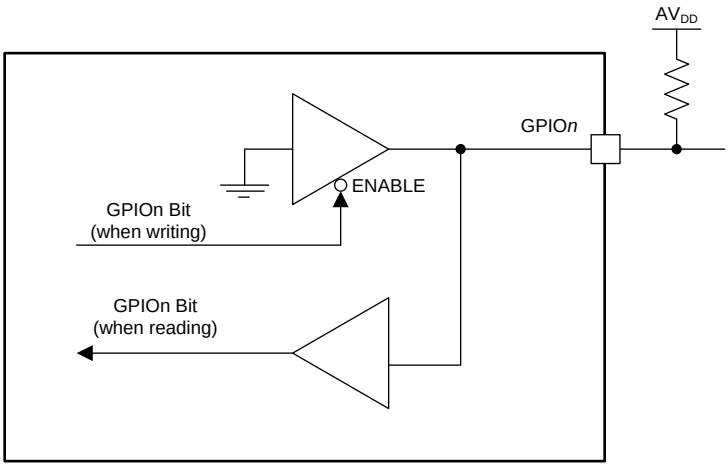


Figure 62. AMC7834 GPIO Pin

7.4 Device Functional Modes

The AMC7834 four high-side current-sense amplifiers and bipolar DACs operate in one of the following modes as selected by the LOOP-EN bit in register 0x10:

- Open-Loop Mode
- Closed-Loop Mode

7.4.1 Open-Loop Mode

The AMC7834 is set by default in open-loop mode. In open-loop mode, the current-sense amplifiers and bipolar DACs operate independently.

The AMC7834 four current sensors can operate with differential voltages up to 200 mV and accept common-mode voltages from 4 V to 60 V. The current-sense amplifier outputs are converted by the device ADC and the results are stored in straight binary format in the CS-Data registers (address 0x29 through 0x2B) to be accessed by a digital control device for further processing.

The AMC7834 four bipolar DACs are configured as DAC pairs (DAC1-DAC2 and DAC3-DAC4). The output range for each bipolar DAC pair can be configured through the DAC Range register to one of the following: 0 to 5 V, -5 to 0V, or -4 to 1 V. The POR and clamp value for each DAC pair is set by the pins VCLAMP1 (for the DAC1-DAC2 pair) and VCLAMP2 (for the DAC3-DAC4 pair) to any voltage between AV_{SS} and 0 V. The full-scale output range of the bipolar DACs is limited by the power supplies, AV_{DD} and AV_{SS}. In open-loop mode the DAC output voltage is set by by a digital controller by writing the corresponding code in straight binary format to the DAC data registers (address 0x30 through 0x33).

Table 6 lists the typical register configurations for open-loop mode.

Table 6. Open-Loop Mode Register Configuration

REGISTER SETTING	REGISTER ADDRESS	COMMENT
LOOP-EN	0x10	Set to 0
CS-FILTER[2:0]	0x10	Configurable
ADCINT*n*	0x12	Set to 0
LOOP*n*-SET[3:0]	0x14	Unused
DAC*n*-SYNC	0x15	Configurable
ADCINT/CS-SELECT	0x1B	Set to 1
DAC*nn*LOOP-ALARMEN	0x1B	Set to 0
DAC*n*-HIGH-ALARM	0x1E	Unused
ADCINT*n*-DATA[11:0]	0x20 to 0x23	Unused
CS*n*-DATA[11:0]	0x28 to 0x2B	Readable
DAC*n*-DATA[11:0]	0x30 to 0x33	Configurable
CLOSEDLOOP*n*[11:0]	0x38 to 0x3B	Unused
DAC*nn*-UP-THRES[11:0]	0x4E to 0x4F	Unused

7.4.2 Closed-Loop Mode

In closed-loop mode the current sensors and bipolar DACs operate as four independent closed-loop current controllers. In closed-loop operation, four autonomous closed-loop current controllers are implemented by continuously adjusting the bipolar DAC outputs in response to the current-sense amplifier outputs.

Table 7 lists the typical register configurations for closed-loop mode.

Table 7. Closed-Loop Mode Register Configuration

REGISTER SETTING	REGISTER ADDRESS	COMMENT
LOOP-EN	0x10	Set to 1
CS-FILTER[2:0]	0x10	Configurable
ADCINT*n*	0x12	Set to 1
LOOP*n*-SET[3:0]	0x14	Configurable
DAC*n*-SYNC	0x15	Unused
ADCINT/CS-SELECT	0x1B	Set to 0
DAC*nn*LOOP-ALARMEN	0x1B	Configurable
DAC*n*-HIGH-ALARM	0x1E	Used
ADCINT*n*-DATA[11:0]	0x20 to 0x23	Readable
CS*n*-DATA[11:0]	0x28 to 0x2B	Unused
DAC*n*-DATA[11:0]	0x30 to 0x33	Unused
CLOSEDLOOP*n*[11:0]	0x38 to 0x3B	Configurable
DAC*nn*-UP-THRES[11:0]	0x4E to 0x4F	Configurable

Figure 63 shows a typical analog implementation of a closed-loop current controller.

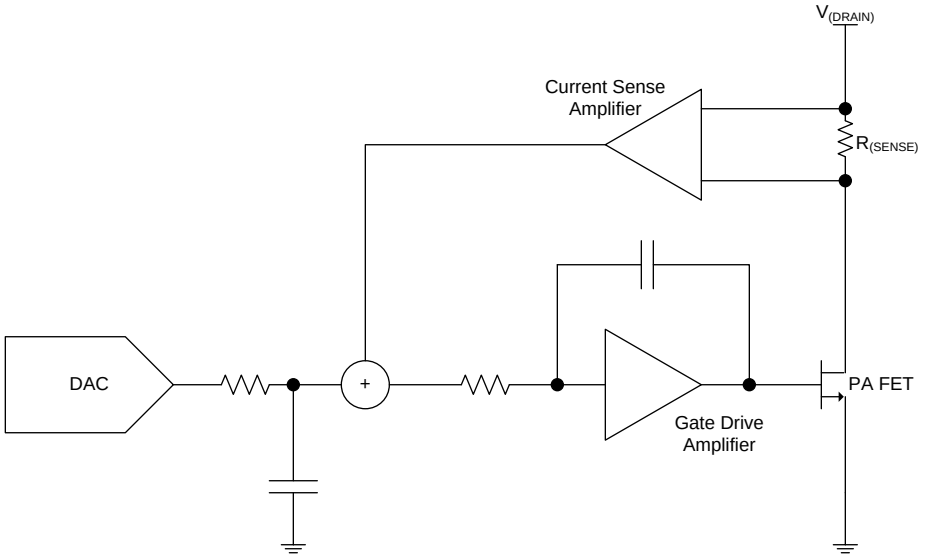


Figure 63. Analog Closed-Loop Current Controller

Although the analog current controller is capable of setting and maintaining a given drain current (and therefore, gain) through a PA FET it lacks the flexibility to scale easily to a large variety of FETs. The AMC7834 implements four closed-loop current controllers as a digital system thus giving it higher flexibility while satisfying or improving on the specifications given by a typical analog closed-loop current controller.

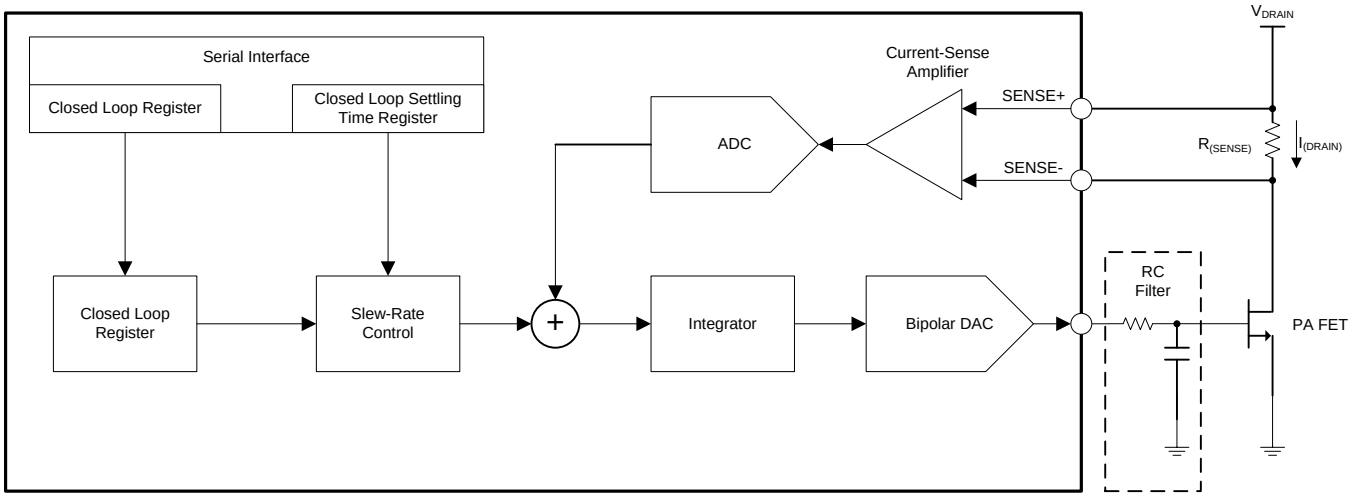


Figure 64. AMC7834 Closed-Loop Current Controller

Each of the four digital control loops consists of a digital integrator and a bipolar DAC in the forward path to drive the gate of a PA FET. A high-side current-sense amplifier in the feedback path senses the drain bias current and its output is converted by the device ADC.

As with the DACs in open-loop operation, the closed-loop current controllers can be set to clamp mode. When a current-controller goes into clamp mode the bipolar DAC output is immediately set to its corresponding clamp voltage and current-sense conversions are stopped. Note that with the exception of the current-sense inputs all other monitoring inputs continue to be converted by the device ADC while in clamp mode. Clamping does not clear the closed-loop state making it possible to return to the same voltage being output before the clamp event was issued.

Since the drain current does not immediately update in response to the out-of-clamp gate voltage, it is recommended to stop the ADC conversion prior to leaving the clamp state and re-starting conversion only after the drain current has stabilized. The stabilization time is dependent on the filtering at the bipolar DAC output and the PA FET characteristics.

The target drain current is set by the Closed Loop registers (address 0x38 to 0x3B) and is given by Equation 10.

$$I_{(DRAIN)} = \frac{CLOSEDLOOPn[11:0] \times V_{ref}}{R_{(SENSE)} \times 51200} \quad (10)$$

where

- $I_{(DRAIN)}$ is the PA drain current (in Amperes)
- CLOSEDLOOP*n*[11:0] is the 12-bit digital code that is input to the control loop to set $I_{(DRAIN)}$
- V_{ref} is the device reference voltage
- $R_{(SENSE)}$ is the sense resistor resistance (in Ohms)

The control loop sets the target drain current by continuously maintaining a constant voltage across the shunt resistor ($V_{(SENSE)} = I_{(DRAIN)} \times R_{(SENSE)}$). The control loop continuously attempts to zero-out the error at the input of the integrator by adjusting the DAC output voltage and consequently keeping the drain current constant. Assuming negligible drift in the sense resistor, any variation in the drain current due to changes in the PA FET characteristics over time and temperature are automatically tracked and corrected.

Based on the target drain current and required PA gain ramp rate, the Closed Loop input code step can be divided by the slew-rate control block into smaller steps that are applied to the control loop every 200 µs. The slew-rate for each control loop is set by the Closed Loop Settling Time register (address 0x14). Issuing multiple, smaller code steps over time instead of one large code step helps achieve a more linear PA-gain ramp rate. Table 8 shows the control-loop settling time as a function of the slew-rate control setting.

Table 8. Closed-Loop Settling Time

LOOP*n*-SET[3:0]	SETTLING TIME (ms)
0000	0.8
0001	1.6
0010	2.4
0011	3.2
0100	4.8
0101	6.4
0110	9.6
0111	12.8
1000	19.2
1001	25.6
1010	28.8
All others	Not valid

Under normal conditions the code output by the slew-rate control block equals the ADC output in steady state. When the loop is disturbed as a result of a change on the target drain current or PA characteristics, the error between the slew-rate controller and ADC outputs is accumulated every 200 µs by the digital integrator. An optional external RC filter at the DAC output helps to smooth out the DAC steps at the input of the PA FET gate. The external filter time constant must be less than 50 µs.

The gain from the DAC output to the ADC input is given by Equation 11.

$$gm_{(PA\_FET)} \times R_{(SENSE)} \quad (11)$$

where

- $gm_{(PA\_FET)}$ is the transconductance for the PA FET

This value should be less than 0.8 to ensure stability of the control loop.

7.5 Programming

The AMC7834 device is controlled through a flexible four-wire serial interface that is compatible with SPI-type interfaces used on many microcontrollers and DSP controllers. The interface provides read and write (R/W) access to all registers of the AMC7834 device.

Each serial-interface access cycle is exactly 24 bits long. A frame is initiated by asserting the $\overline{CS}$ pin low. The frame ends when the $\overline{CS}$ pin is deasserted high. The first bit transferred is the R/W bit. The next 7 bits are the register address (128 addressable registers), and the remaining 16 bits are data. For all writes, data is clocked in on the rising edge of SCLK. If the write access is not equal to 24 clocks, the data bits are not committed. On a read access, data is clocked out on the falling edge of the serial interface clock, SCLK, on the SDO pin.

Figure 65 and Figure 66 show the access protocol used by the interface. Data is accepted as MSB first.

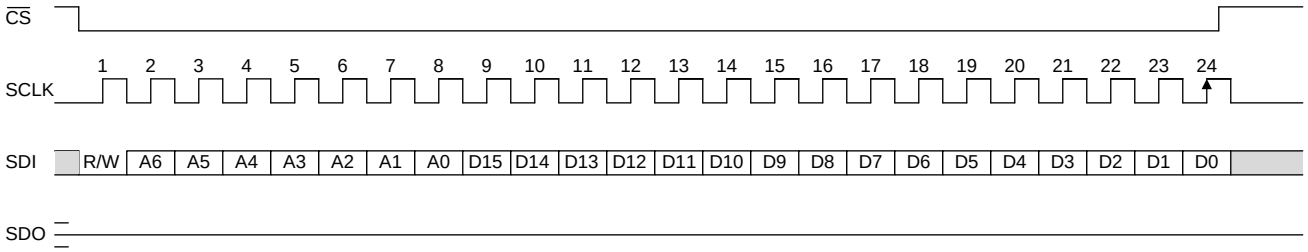


Figure 65. Serial Interface Write Bus Cycle

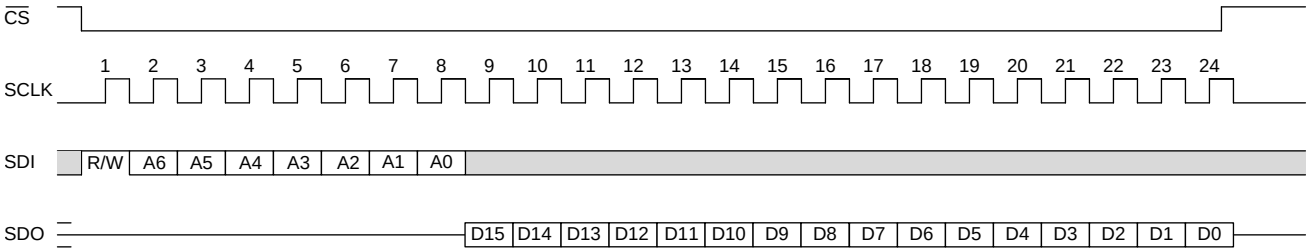


Figure 66. Serial Interface Read Bus Cycle

7.6 Register Maps

Table 9. Memory Map

ADDRESS	TYPE	DEFAULT	REGISTER NAME		ADDRESS	TYPE	DEFAULT	REGISTER NAME
0x00 to 0x01	—	—	Reserved		0x30	R/W	0000	DAC1-Data
0x02	R/W	0000	Power Mode		0x31	R/W	0000	DAC2-Data
0x03	—	—	Reserved		0x32	R/W	0000	DAC3-Data
0x04	R	0C34	Device ID		0x33	R/W	0000	DAC4-Data
0x05	—	—	Reserved		0x34	R/W	0000	AUXDAC1-Data
0x06	R	0001	Version ID		0x35	R/W	0000	AUXDAC2-Data
0x07 to 0x0B	—	—	Reserved		0x36	R/W	0000	AUXDAC3-Data
0x0C	R	0451	Vendor ID		0x37	R/W	0000	AUXDAC4-Data
0x0D – 0x0F	—	—	Reserved		0x38	R/W	0000	ClosedLoop1
0x10	R/W	0300	AMC Configuration 0		0x39	R/W	0000	ClosedLoop2
0x11	R/W	036A	AMC Configuration 1		0x3A	R/W	0000	ClosedLoop3
0x12	R/W	0000	ADC MUX		0x3B	R/W	0000	ClosedLoop4
0x13	—	—	Reserved		0x3C to 0x3F	—	—	Reserved
0x14	R/W	2222	Closed Loop Settling Time		0x40	R/W	0FFF	ADCINT1/CS1-Upper-Thresh
0x15	R/W	0000	DAC Sync		0x41	R/W	0000	ADCINT1/CS1-Lower-Thresh
0x16	R/W	0000	DAC Range		0x42	R/W	0FFF	ADCINT2/CS2-Upper-Thresh
0x17	R/W	003F	CLAMP Configuration		0x43	R/W	0000	ADCINT2/CS2-Lower-Thresh
0x18	R/W	FF00	SLEEP1 Configuration		0x44	R/W	0FFF	ADCINT3/CS3-Upper-Thresh
0x19	R/W	FF00	SLEEP2 Configuration		0x45	R/W	0000	ADCINT3/CS3-Lower-Thresh
0x1A	R/W	0000	ALARMOUT Clamp		0x46	R/W	0FFF	ADCINT4/CS4-Upper-Thresh
0x1B	R/W	0000	ALARMOUT Configuration		0x47	R/W	0000	ADCINT4/CS4-Lower-Thresh
0x1C	W	0000	DAC/ADC Trigger		0x48	R/W	07FF	LT-Upper-Thresh
0x1D	W	0000	Software Reset		0x49	R/W	0800	LT-Lower-Thresh
0x1E	R	0000	Alarm Status		0x4A	R/W	07FF	RT1-Upper-Thresh
0x1F	R	0000	AMC Status		0x4B	R/W	0800	RT1-Lower-Thresh
0x20	R	0000	ADC1-Internal-Data		0x4C	R/W	07FF	RT2-Upper-Thresh
0x21	R	0000	ADC2-Internal-Data		0x4D	R/W	0800	RT2-Lower-Thresh
0x22	R	0000	ADC3-Internal-Data		0x4E	R/W	0FFF	DAC12-Upper-Thresh
0x23	R	0000	ADC4-Internal-Data		0x4F	R/W	0FFF	DAC34-Upper-Thresh
0x24	R	0000	ADC1-External-Data		0x50	R/W	0008	ADCINT1/CS1-Hysteresis
0x25	R	0000	ADC2-External-Data		0x51	R/W	0008	ADCINT2/CS2-Hysteresis
0x26	R	0000	ADC3-External-Data		0x52	R/W	0008	ADCINT3/CS3-Hysteresis
0x27	R	0000	ADC4-External-Data		0x53	R/W	0008	ADCINT4/CS4-Hysteresis
0x28	R	0000	CS1-Data		0x54	R/W	0008	LT-Hysteresis
0x29	R	0000	CS2-Data		0x55	R/W	0008	RT1-Hysteresis
0x2A	R	0000	CS3-Data		0x56	R/W	0008	RT2-Hysteresis
0x2B	R	0000	CS4-Data		0x57	—	—	Reserved
0x2C	—	—	Reserved		0x58	R/W	000F	GPIO
0x2D	R	0000	LT-Data		0x59 to 0x5F	—	—	Reserved
0x2E	R	0000	RT1-Data		0x60 to 0x6F	—	—	Reserved
0x2F	R	0000	RT2-Data		0x70 to 0x7F	—	—	Reserved

Register Maps (continued)

7.6.1 Power Mode: Address 0x02

7.6.1.1 Power Mode Register (address = 0x02) [reset = 0x000]

Figure 67. Power Mode Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
Reserved						POWER-MODE	
R/W-00h						R/W-00	

Table 10. Power Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	Reserved	R/W	All zeros	Reserved for factory use.
1–0	POWER-MODE	R/W	00	Power down mode for the AMC7834 device. See Table 11.

Table 11. POWER-MODE Configuration

POWER MODE	Value	Reference	Current Sensors	ADC	ADC Reference Buffer	DAC Reference Buffer	Auxiliary DACs	Bipolar DACs
Power-Down Mode	0x	ON	OFF	OFF	OFF	OFF	OFF	ON
Active Mode	10	ON	ON	ON	ON	ON	ON	ON
Reserved Mode	11	Not valid. Reserved for factory use.						

7.6.2 Device Identification: Address 0x04 through 0x0C

7.6.2.1 Device ID Register (address = 0x04) [reset = 0x0C34]

Figure 68. Device ID Register (R)

15	14	13	12	11	10	9	8
DEVICEID							
R-0Ch							
7	6	5	4	3	2	1	0
DEVICEID							
R-34h							

Table 12. Device ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEVICEID	R	0C34h	Device ID.

7.6.2.2 Version ID Register (address = 0x06) [reset = 0x0001]

Figure 69. Version ID Register (R)

15	14	13	12	11	10	9	8
VERSIONID							
R-00h							
7	6	5	4	3	2	1	0
VERSIONID							
R-01h							

Table 13. Version ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VERSIONID	R	0001h	AMC7834 version ID. Subject to change.

7.6.2.3 Vendor ID Register (address = 0x0C) [reset = 0x0451]

Figure 70. Vendor ID Register (R)

15	14	13	12	11	10	9	8
VENDORID							
R-04h							
7	6	5	4	3	2	1	0
VENDORID							
R-51h							

Table 14. Vendor ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDORID	R	0451h	Vendor ID.

7.6.3 General Device Configuration: Address 0x10 through 0x16

7.6.3.1 AMC Configuration 0 Register (address = 0x10) [reset = 0x0300]

Figure 71. AMC Configuration 0 Register (R/W)

15	14	13	12	11	10	9	8
Reserved			CMODE	Reserved	CS-FILTER[2:0]		
R/W-000			R/W-0	R/W-0	R/W-011		
7	6	5	4	3	2	1	0
Reserved	RT-SET[2:0]			Reserved			LOOP-EN
R/W-0	R/W-000			R/W-000			R/W-0

Table 15. AMC Configuration 0 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	Reserved	R/W	000	Reserved for factory use.
12	CMODE	R/W	0	0: Autonomous ADC conversion 1: Direct-mode ADC conversion
11	Reserved	R/W	0	Reserved for factory use.
10-8	CS-FILTER[2:0]	R/W	011	Current sense filter setting. Improves noise of current sensors measurements by trading off the update time. The digital filter has the transfer function: $H(z) = \frac{1}{1-(K-1)z^{-1}}$ (12) See Table 16 for its configuration.
7	Reserved	R/W	0	Reserved for factory use.
6-4	RT-SET[2:0]	R/W	000	Improves noise of the remote temperature sensors measurements by trading off the update time. See Table 17 for its configuration.
3-1	Reserved	R/W	000	Reserved for factory use.
0	LOOP-EN	R/W	0	When set to 1 enables closed-loop mode operation.

Table 16. CS-FILTER Configuration

CS-FILTER[2:0]	K	Approximate Update Time (ms)
000	1	0.2
001	2	3.4
010	4	6.6
011	8 (default)	13
100	16	25.6
All others	Not valid	

Table 17. RT-SET Configuration

RT-SET[2:0]	Two Remote Sensors Update Time (ms)
000	16
001	16
010	18
011	26
100	50
101	98
All others	Not valid

7.6.3.2 AMC Configuration 1 Register (address = 0x11) [reset = 0x036A]

Figure 72. AMC Configuration 1 Register (R/W)

15	14	13	12	11	10	9	8
DAVPIN-EN	DAVPIN-SEL	Reserved			CH-FALR[2:0]		
R/W-0	R/W-0	R/W-000			R/W-011		
7	6	5	4	3	2	1	0
RMT-GND-COLL	PAON_AVSS	LT-FALR[1:0]		RT2-FALR[1:0]		RT1-FALR[1:0]	
R/W-0	R/W-1	R/W-10		R/W-10		R/W-10	

Table 18. AMC Config1 Field Descriptions

Bit	Field	Type	Reset	Description
15	DAVPIN-EN	R/W	0	When set to 1 it enables the $\overline{\text{DAV}}$/ADC_RDY pin output function. When cleared to 0 the $\overline{\text{DAV}}$/ADC_RDY pin is in high impedance mode.
14	DAVPIN-SEL	R/W	0	When cleared to 0 and if DAVPIN-EN is equal to 1 the $\overline{\text{DAV}}$/ADC_RDY pin operates as a $\overline{\text{DAV}}$ pin. When set to 1 and if DAVPIN-EN is equal to 1 the $\overline{\text{DAV}}$/ADC_RDY pin operates as an ADC_RDY pin.
13-11	Reserved	R/W	000	Reserved for factory use.
10	CH-FALR[2:0]	R/W	011	False alarm protection for ADC channels. Use the following configurations for the consecutive samples before the alarm is set: 000: 1 001: 4 010: 8 011: 16 (default) 100: 32 101: 64 110: 128 111: 256
7	RMT-GND-COLL	R/W	0	When set to 1 enables PNP transistor configuration on both remote temperature sensors.
6	PAON_AVSS	R/W	1	When PAON_AVSS = 1 an AVSS alarm event automatically switches the PA_ON pin to the OFF state. The AVSS alarm must be cleared before the PA_ON pin can be switch back to the ON state. When PAON_AVSS = 0 the PA_ON pin is unaffected by an AVSS alarm event.
5-4	LT-FALR[1:0]	R/W	10	False alarm protection for local temperature sensor. Use the following configurations for the consecutive samples before the alarm is set: 00: 1 01: 2 10: 4 (default) 11: 8

Table 18. AMC Config1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	RT2-FALR[1:0]	R/W	10	False alarm protection for remote temperature sensor 2 (D2+, D2–). Use the following configurations for the consecutive samples before the alarm is set: 00: 1 01: 2 10: 4 (default) 11: 8
1–0	RT1-FALR[1:0]	R/W	10	False alarm protection for remote temperature sensor 1 (D1+, D1–). Use the following configurations for the consecutive samples before the alarm is set: 00: 1 01: 2 10: 4 (default) 11: 8

7.6.3.3 ADC MUX Register (address = 0x12) [reset = 0x0000]

Figure 73. ADC MUX Register (R/W)

15	14	13	12	11	10	9	8
Reserved	LT	RT2	RT1	CS4	CS3	CS2	CS1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
ADCEXT4	ADCEXT3	ADCEXT2	ADCEXT1	ADCINT4	ADCINT3	ADCINT2	ADCINT1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 19. ADC MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	When set to 1 the corresponding analog input channel to the ADC mux is accessed during an ADC conversion cycle. When cleared to 0 the corresponding input channel to the ADC mux is ignored during an ADC conversion cycle.
14	LT	R/W	0	
13	RT2	R/W	0	
12	RT1	R/W	0	
11	CS4	R/W	0	
10	CS3	R/W	0	
9	CS2	R/W	0	
8	CS1	R/W	0	
7	ADCEXT4	R/W	0	
6	ADCEXT3	R/W	0	
5	ADCEXT2	R/W	0	
4	ADCEXT1	R/W	0	
3	ADCINT4	R/W	0	
2	ADCINT3	R/W	0	
1	ADCINT2	R/W	0	
0	ADCINT1	R/W	0	

7.6.3.4 Closed Loop Settling Time Register (address = 0x14) [reset = 0x2222]

Figure 74. Closed Loop Settling Time Register (R/W)

15	14	13	12	11	10	9	8
LOOP4-SET[3:0]				LOOP3-SET[3:0]			
R/W-0010				R/W-0010			
7	6	5	4	3	2	1	0
LOOP2-SET[3:0]				LOOP1-SET[3:0]			
R/W-0010				R/W-0010			

Table 20. Closed Loop Settling Time Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	LOOP4-SET[3:0]	R/W	0010	Slew rate controller. Sets the maximum voltage transition rate of each closed-loop current controller. See Table 21 for its configuration.
11–8	LOOP3-SET[3:0]	R/W	0010	
7-4	LOOP2-SET[3:0]	R/W	0010	
3-0	LOOP1-SET[3:0]	R/W	0010	

Table 21. Closed-Loop Settling Time Configuration

LOOP*n*-SET[3:0]	Settling Time (ms)
0000	0.8
0001	1.6
0010	2.4
0011	3.2
0100	4.8
0101	6.4
0110	9.6
0111	12.8
1000	19.2
1001	25.6
1010	28.8
All others	Not valid

7.6.3.5 DAC Sync Register (address = 0x15) [reset = 0x0000]

Figure 75. DAC Sync Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
AUXDAC4-SYNC	AUXDAC3-SYNC	AUXDAC2-SYNC	AUXDAC1-SYNC	DAC4-SYNC	DAC3-SYNC	DAC2-SYNC	DAC1-SYNC
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 22. DAC Sync Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Reserved	R/W	0x00	Reserved for factory use.
7	AUXDAC4-SYNC	R/W	0	When set to 1 the corresponding DAC output is set to synchronous-mode. When cleared to 0 the corresponding DAC output is set to asynchronous-mode. In closed-loop mode DAC1, DAC2, DAC3 and DAC4 are always in asynchronous-mode.
6	AUXDAC3-SYNC	R/W	0	
5	AUXDAC2-SYNC	R/W	0	
4	AUXDAC1-SYNC	R/W	0	
3	DAC4-SYNC	R/W	0	
2	DAC3-SYNC	R/W	0	
1	DAC2-SYNC	R/W	0	
0	DAC1-SYNC	R/W	0	

7.6.3.6 DAC Range Register (address = 0x16) [reset = 0x0000]

Figure 76. DAC Range Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
AUXDAC4-RANGE	AUXDAC3-RANGE	AUXDAC2-RANGE	AUXDAC1-RANGE	DAC34-RANGE[1:0]		DAC12-RANGE[1:0]	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-00		R/W-00	

Table 23. DAC Range Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Reserved	R/W	0x00	Reserved for factory use.
7	AUXDAC4-RANGE	R/W	0	When cleared to 0 the corresponding AUXDAC output range is 0 to 5 V. When set to 1 the corresponding AUXDAC output range is 2.5 to 7.5 V.
6	AUXDAC3-RANGE	R/W	0	
5	AUXDAC2-RANGE	R/W	0	
4	AUXDAC1-RANGE	R/W	0	
3-2	DAC34-RANGE[1:0]	R/W	00	Sets the bipolar DAC output range. Use the following configurations for the DAC output range: 00: –4 to 1 V 01: –5 to 0 V 10: –5 to 0 V 11: 0 to 5 V
1–0	DAC12-RANGE[1:0]	R/W	00	

7.6.4 Clamp and Alarm Configuration: Address 0x17 through 0x1B

7.6.4.1 CLAMP Configuration Register (address = 0x17) [reset = 0x003F]

Figure 77. CLAMP Configuration Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
Reserved	PAON	AUXDAC4-CLAMP	AUXDAC3-CLAMP	AUXDAC2-CLAMP	AUXDAC1-CLAMP	DAC34-CLAMP	DAC12-CLAMP
R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Table 24. CLAMP Configuration Field Descriptions

Bit	Field	Type	Reset	Description
15-7	Reserved	R/W	All zeros	Reserved for factory use.
6	PAON	R/W	0	Direct control of the PA_ON pin. When cleared to 0 the PA_ON pin is in the OFF state (PAVDD). When set to 1 the PA_ON pin is in the ON state (AGND). When read, the value of this bit reflects the state of the PA_ON pin.
5	AUXDAC4-CLAMP	R/W	1	This register uses software to force the corresponding DAC into clamp. If 1, the corresponding DAC or DAC pair is forced into clamp. If 0, the corresponding DAC or DAC pair is restored to normal operation. If a DAC or DAC pair is in clamp mode through a SLEEP pin the corresponding clamp bit is automatically set to 1.
4	AUXDAC3-CLAMP	R/W	1	
3	AUXDAC2-CLAMP	R/W	1	
2	AUXDAC1-CLAMP	R/W	1	
1	DAC34-CLAMP	R/W	1	
0	DAC12-CLAMP	R/W	1	

7.6.4.2 SLEEP1 Configuration Register (address = 0x18) [reset = 0xFF00]

Figure 78. SLEEP1 Configuration Register (R/W)

15	14	13	12	11	10	9	8
Reserved	PAON-SNOOZE1	AUXDAC4-SNOOZE1	AUXDAC3-SNOOZE1	AUXDAC2-SNOOZE1	AUXDAC1-SNOOZE1	DAC34-SNOOZE1	DAC12-SNOOZE1
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
7	6	5	4	3	2	1	0
Reserved	PAON-SLEEP1	AUXDAC4-SLEEP1	AUXDAC3-SLEEP1	AUXDAC2-SLEEP1	AUXDAC1-SLEEP1	DAC34-SLEEP1	DAC12-SLEEP1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 25. SLEEP1 Configuration Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	1	Reserved for factory use.
14	PAON-SNOOZE1	R/W	1	Setting this bit to 1 imposes an additional write to the PA_ON register to set the PA_ON pin to the ON state after clearing the SLEEP1 pin. Setting this bit to 0 enables the SLEEP1 pin to set the PA_ON pin to the ON state directly.
13	AUXDAC4-SNOOZE1	R/W	1	Setting any of these bits to 1 imposes an additional write to the CLAMP Configuration register to wake-up the corresponding DAC or DAC pair from clamp after clearing the SLEEP1 pin. Clearing any of these bits to 0 enables the SLEEP1 pin to wake-up the DAC or DAC pairs directly.
12	AUXDAC3-SNOOZE1	R/W	1	
11	AUXDAC2-SNOOZE1	R/W	1	
10	AUXDAC1-SNOOZE1	R/W	1	
9	DAC34-SNOOZE1	R/W	1	
8	DAC12-SNOOZE1	R/W	1	
7	Reserved	R/W	0	Reserved for factory use
6	PAON-SLEEP1	R/W	0	Setting this bit to 1 allows control of the PA_ON pin through the SLEEP1 pin. When SLEEP1 pin goes high the PA_ON pin enters the OFF state. Bringing the SLEEP1 pin low is required but not necessarily sufficient to return the PA_ON pin to the ON state as determined by the SNOOZE bits. Setting this bit to 0 causes the PA_ON pin to be unaffected by the SLEEP1 pin.
5	AUXDAC4-SLEEP1	R/W	0	Setting any of these bits to 1 allows control of the corresponding DAC or DAC pair through the SLEEP1 pin. When SLEEP1 pin goes high the DAC or DAC pair goes into clamp mode. Bringing the SLEEP1 pin low is required but not necessarily sufficient to return the DAC or DAC pairs to normal operation as determined by the SNOOZE bits. Clearing any of these bits to 0 causes the corresponding DAC or DAC pair to be unaffected by the SLEEP1 pin.
4	AUXDAC3-SLEEP1	R/W	0	
3	AUXDAC2-SLEEP1	R/W	0	
2	AUXDAC1-SLEEP1	R/W	0	
1	DAC34-SLEEP1	R/W	0	
0	DAC12-SLEEP1	R/W	0	

7.6.4.3 SLEEP2 Configuration Register (address = 0x19) [reset = 0xFF00]

Figure 79. SLEEP2 Configuration Register (R/W)

15	14	13	12	11	10	9	8
Reserved	PAON-SNOOZE2	AUXDAC4-SNOOZE2	AUXDAC3-SNOOZE2	AUXDAC2-SNOOZE2	AUXDAC1-SNOOZE2	DAC34-SNOOZE2	DAC12-SNOOZE2
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
7	6	5	4	3	2	1	0
Reserved	PAON-SLEEP2	AUXDAC4-SLEEP2	AUXDAC3-SLEEP2	AUXDAC2-SLEEP2	AUXDAC1-SLEEP2	DAC34-SLEEP2	DAC12-SLEEP2
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 26. SLEEP2 Configuration Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	1	Reserved for factory use
14	PAON-SNOOZE2	R/W	1	Setting this bit to 1 imposes an additional write to the PA_ON register to set the PA_ON pin to the ON state after clearing the SLEEP2 pin. Setting this bit to 0 enables the SLEEP2 pin to set the PA_ON pin to the ON state directly.
13	AUXDAC4-SNOOZE2	R/W	1	Setting any of these bits to 1 imposes an additional write to the CLAMP Configuration register to wake-up the corresponding DAC or DAC pair from clamp after clearing the SLEEP2 pin. Clearing any of these bits to 0 enables the SLEEP2 pin to wake-up the DAC or DAC pairs directly.
12	AUXDAC3-SNOOZE2	R/W	1	
11	AUXDAC2-SNOOZE2	R/W	1	
10	AUXDAC1-SNOOZE2	R/W	1	
9	DAC34-SNOOZE2	R/W	1	
8	DAC12-SNOOZE2	R/W	1	
7	Reserved	R/W	0	Reserved for factory use
6	PAON-SLEEP2	R/W	0	Setting this bit to 1 allows control of the PA_ON pin through the SLEEP2 pin. When SLEEP2 pin goes high the PA_ON pin enters the OFF state. Bringing the SLEEP2 pin low is required but not necessarily sufficient to return the PA_ON pin to the ON state as determined by the SNOOZE bits. Setting this bit to 0 causes the PA_ON pin to be unaffected by the SLEEP2 pin.
5	AUXDAC4-SLEEP2	R/W	0	Setting any of these bits to 1 allows control of the corresponding DAC or DAC pair through the SLEEP2 pin. When SLEEP2 pin goes high the DAC or DAC pair goes into clamp mode. Bringing the SLEEP2 pin low is required but not necessarily sufficient to return the DAC or DAC pairs to normal operation as determined by the SNOOZE bits. Clearing any of these bits to 0 causes the corresponding DAC or DAC pair to be unaffected by the SLEEP2 pin.
4	AUXDAC3-SLEEP2	R/W	0	
3	AUXDAC2-SLEEP2	R/W	0	
2	AUXDAC1-SLEEP2	R/W	0	
1	DAC34-SLEEP2	R/W	0	
0	DAC12-SLEEP2	R/W	0	

7.6.4.4 ALARMOUT Clamp Register (address = 0x1A) [reset = 0x0000]

Figure 80. ALARMOUT Clamp Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
Reserved	PAON-ALARMOUT	AUXDAC4-ALARMOUT	AUXDAC3-ALARMOUT	AUXDAC2-ALARMOUT	AUXDAC1-ALARMOUT	DAC34-ALARMOUT	DAC12-ALARMOUT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 27. ALARMOUT Clamp Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	Reserved	R/W	All zeros	Reserved for factory use.
6	PAON-ALARMOUT	R/W	0	PAON-ALARMOUT = 1 allows control of the PA_ON pin through ALARMOUT. When ALARMOUT is active the PA_ON pin goes into the OFF state. Clearing the alarms does not return PA_ON to the ON state. PAON-ALARMOUT = 0 causes the PA_ON pin to be unaffected by ALARMOUT.
5	AUXDAC4-ALARMOUT	R/W	0	Setting any of these bits to 1 allows control of the corresponding DAC or DAC pair clamp through ALARMOUT. When ALARMOUT is active the DAC or DAC pair goes into clamp mode. Clearing the alarms does not return the DAC or DAC pairs to normal operation. Clearing any of these bits to 0 causes the corresponding DAC or DAC pair to be unaffected by ALARMOUT.
4	AUXDAC3-ALARMOUT	R/W	0	
3	AUXDAC2-ALARMOUT	R/W	0	
2	AUXDAC1-ALARMOUT	R/W	0	
1	DAC34-ALARMOUT	R/W	0	
0	DAC12-ALARMOUT	R/W	0	

7.6.4.5 ALARMOUT Configuration Register (address = 0x1B) [reset = 0x0000]

Figure 81. ALARMOUT Configuration Register (R/W)

15	14	13	12	11	10	9	8
ALARM-LATCH-DIS	ALARMOUT-POLARITY	ADCINT/CS-SELECT	DAC34LOOP-ALARMEN	DAC12LOOP-ALARMEN	AVSS-ALARMEN	RT2-HIGH-ALARMEN	RT2-LOW-ALARMEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
RT1-HIGH-ALARMEN	RT1-LOW-ALARMEN	LT-HIGH-ALARMEN	LT-LOW-ALARMEN	ADCINT4/CS4-ALARMEN	ADCINT3/CS3-ALARMEN	ADCINT2/CS2-ALARMEN	ADCINT1/CS1-ALARMEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 28. ALARMOUT Configuration Field Descriptions

Bit	Field	Type	Reset	Description
15	ALARM-LATCH-DIS	R/W	0	Alarm latch disable bit. When cleared to 0 the alarm bits are latched. When an alarm occurs, the corresponding alarm bit is set to 1. The alarm bit remains until the error condition subsides and the alarm register is read. Before reading, the alarm bit is not cleared even if the alarm condition disappears. When set to 1 the alarm bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the alarm bits have been read or not.
14	ALARMOUT-POLARITY	R/W	0	ALARMOUT polarity bit. When cleared to 0 the ALARMOUT pin is active low. When set to 1 the ALARMOUT pin is active high.
13	ADCINT/CS-SELECT	R/W	0	When cleared to 0 the threshold values in registers 0x40 to 0x47 apply to ADC inputs ADCINT[1–4]. This setting should be used for closed-loop mode operation. When set to 1 the threshold values in registers 0x40 to 0x47 apply to current sense measurements CS[1–4]. This setting should be used for open-loop mode operation.
12	DAC34LOOP-ALARMEN	R/W	0	These bits select the alarm events that trigger the ALARMOUT pin. When set to 1 an alarm event associated with the corresponding bit will trigger the ALARMOUT pin. When cleared to 0 an alarm event associated with the corresponding bit does not affect the ALARMOUT pin.
11	DAC12LOOP-ALARMEN	R/W	0	
10	AVSS-ALARMEN	R/W	0	
9	RT2-HIGH-ALARMEN	R/W	0	
8	RT2-LOW-ALARMEN	R/W	0	
7	RT1-HIGH-ALARMEN	R/W	0	
6	RT1-LOW-ALARMEN	R/W	0	
5	LT-HIGH-ALARMEN	R/W	0	
4	LT-LOW-ALARMEN	R/W	0	
3	ADCINT4/CS4-ALARMEN	R/W	0	
2	ADCINT3/CS3-ALARMEN	R/W	0	
1	ADCINT2/CS2-ALARMEN	R/W	0	
0	ADCINT1/CS1-ALARMEN	R/W	0	

7.6.5 Conversion Trigger: Address 0x1C

7.6.5.1 DAC and ADC Trigger Register (address = 0x1C) [reset = 0x0000]

Figure 82. DAC and ADC Trigger Register (W)

15	14	13	12	11	10	9	8
Reserved							
W-00h							
7	6	5	4	3	2	1	0
Reserved						DAC-TRIG	ADC-TRIG
W-00h						W-0	W-0

Table 29. DAC/ADC Trigger Field Descriptions

Bit	Field	Type	Reset	Description
15-2	Reserved	W	All zeros	Reserved for factory use.
1	DAC-TRIG	W	0	Internal DAC conversion trigger. Set this bit to 1 to synchronously load those DACs who have been set in synchronous mode in the DAC Sync register. This bit is automatically cleared to 0 after the DAC Data registers are updated.
0	ADC-TRIG	W	0	Internal ADC conversion bit. Set this bit to 1 to start the ADC conversion. The bit is automatically cleared to 0 after the ADC conversion starts. If the bit is set to 1 while the ADC is not in READY mode the conversion command is ignored.

7.6.6 Reset: Address 0x1D

7.6.6.1 Software Reset Register (address = 0x1D) [reset = 0x0000]

Figure 83. Software Reset Register (W)

15	14	13	12	11	10	9	8
Reserved							
W-00h							
7	6	5	4	3	2	1	0
Reserved				SOFT-RESET[3:0]			
W-0000				W-0000			

Table 30. Software Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	Reserved	W	All zeros	Reserved for factory use.
3-0	SOFT-RESET[3:0]	W	0000	When set to reserved code 1100 resets the device to its default state. Auto clears with execution.

7.6.7 Device Status: Address 0x1E and 0x1F

7.6.7.1 Alarm Status Register (address = 0x1E) [reset = 0x0000]

Figure 84. Alarm Status Register (R)

15	14	13	12	11	10	9	8
DAC4-HIGH-ALARM	DAC3-HIGH-ALARM	DAC2-HIGH-ALARM	DAC1-HIGH-ALARM	Reserved	AVSS-ALARM	RT2-HIGH-ALARM	RT2-LOW-ALARM
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
RT1-HIGH-ALARM	RT1-LOW-ALARM	LT-HIGH-ALARM	LT-LOW-ALARM	ADCINT4/CS4-ALARM	ADCINT3/CS3-ALARM	ADCINT2/CS2-ALARM	ADCINT1/CS1-ALARM
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Table 31. Alarm Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DAC4-HIGH-ALARM	R	0	DAC4-HIGH-ALARM = 1 when DAC4 has exceeded the upper output limit set by DAC34-UP-THRESH[11:0].
14	DAC3-HIGH-ALARM	R	0	DAC3-HIGH-ALARM = 1 when DAC3 has exceeded the upper output limit set by DAC34-UP-THRESH[11:0].
13	DAC2-HIGH-ALARM	R	0	DAC2-HIGH-ALARM = 1 when DAC2 has exceeded the upper output limit set by DAC12–UP-THRESH[11:0].
12	DAC1-HIGH-ALARM	R	0	DAC1-HIGH-ALARM = 1 when DAC1 has exceeded the upper output limit set by DAC12–UP-THRESH[11:0].
11	Reserved	R	0	Reserved for factory use.
10	AVSS-ALARM	R	0	AVSS_ALARM = 1 when AV_{SS} is out of range.
9	RT2-HIGH-ALARM	R	0	RT2-HIGH-ALARM = 1 when remote temperature sensor 2 is out of the range defined by the upper threshold. Always zero when the remote sensor is disabled.
8	RT2-LOW-ALARM	R	0	RT2-LOW-ALARM = 1 when remote temperature sensor 2 is out of the range defined by the lower threshold. Always zero when the remote sensor is disabled.
7	RT1-HIGH-ALARM	R	0	RT1-HIGH-ALARM = 1 when remote temperature sensor 1 is out of the range defined by the upper threshold. Always zero when the remote sensor is disabled.
6	RT1-LOW-ALARM	R	0	RT1-LOW-ALARM = 1 when remote temperature sensor 1 is out of the range defined by the lower threshold. Always zero when the remote sensor is disabled.
5	LT-HIGH-ALARM	R	0	LT-HIGH-ALARM = 1 when the local temperature sensor is out of the range defined by the upper threshold. Always zero when the on-chip sensor is disabled.
4	LT-LOW-ALARM	R	0	LT-LOW-ALARM = 1 when the local temperature sensor is out of the range defined by the lower threshold. Always zero when the on-chip sensor is disabled.
3	ADCINT4/CS4-ALARM	R	0	ADCINT4/CS4-ALARM = 1 when the ADC reading of internal channel 4 (closed-loop) or the measurement of current sense 4 (open-loop) is out of range defined by the alarm threshold registers.
2	ADCINT3/CS3-ALARM	R	0	ADCINT3/CS3-ALARM = 1 when the ADC reading of internal channel 3 (closed-loop) or the measurement of current sense 3 (open-loop) is out of range defined by the alarm threshold registers.

Table 31. Alarm Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ADCINT2/CS2-ALARM	R	0	ADCINT2/CS2-ALARM = 1 when the ADC reading of internal channel 2 (closed-loop) or the measurement of current sense 2 (open-loop) is out of range defined by the alarm threshold registers.
0	ADCINT1/CS1-ALARM	R	0	ADCINT1/CS1-ALARM = 1 when the ADC reading of internal channel 1 (closed-loop) or the measurement of current sense 1 (open-loop) is out of range defined by the alarm threshold registers.

7.6.7.2 General Status Register (address = 0x1F) [reset = 0x0000]

Figure 85. General Status Register (R)

15	14	13	12	11	10	9	8
GDAV	ADC-READY	LT-DAV	RT2-DAV	RT1-DAV	ADCINT-DAV	ADCEXT-DAV	CS-DAV
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
Reserved				SLEEP2-STATUS	SLEEP1-STATUS	PAON-STATUS	GALARM
R-0000				R-0	R-0	R-0	R-0

Table 32. General Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GDAV	R	0	Global data available flag.
14	ADC-READY	R	0	ADC is ready (waiting) to be triggered. At power-up, will remain not ready (0) until the ADC is powered up and at least one channel is selected. If there is any write that would stop the ADC including AMC Configuration 0, ADC MUX, or ADC alarm threshold register writes, this bit also returns to *not ready* until the device completes processing of these changes/updates, after which time the ADC is ready to trigger again. Goes to 0 when the ADC is triggered and is running. This bit returns to 1 once the ADC is stopped.
13	LT-DAV	R	0	Local temperature sensor data available flag for direct-mode conversion.
12	RT2-DAV	R	0	Remote temperature sensor 2 data available flag for direct-mode conversion.
11	RT1-DAV	R	0	Remote temperature sensor 1 data available flag for direct-mode conversion.
10	ADCINT-DAV	R	0	ADCINT data available flag for direct-mode conversion.
9	ADCEXT-DAV	R	0	ADCEXT data available flag for direct-mode conversion.
8	CS-DAV	R	0	Current sense data available flags for direct-mode conversion.
7-4	Reserved	R	0000	Reserved for factory use
3	SLEEP2-STATUS	R	0	Status of SLEEP2 pin.
2	SLEEP1-STATUS	R	0	Status of SLEEP1 pin.
1	PAON-STATUS	R	0	Status of PA_ON pin. If equal to 0 the PA_ON pin is in the OFF state (PAVDD). If equal to 1 the PA_ON pin is in the ON state (AGND).
0	GALARM	R	0	Global alarm bit. This bit is the OR function or all individual alarm bits of the status register. This bit is set to 1 when any alarm condition occurs and remains set until the status register is read. This bit is cleared after reading the Alarm Status register.

7.6.8 ADC Data: Address 0x20 through 0x2F

7.6.8.1 ADCn-Internal-Data Register (address = 0x20 to 0x23) [reset = 0x0000]

This register description applies to the internal monitoring inputs ADCINT1 through ADCINT4.

Figure 86. ADC*n*-Internal-Data Register (R)

15	14	13	12	11	10	9	8
Reserved				ADCINT*n*-DATA[11:8]			
R-0h				R-0h			
7	6	5	4	3	2	1	0
ADCINT*n*-DATA[7:0]							
R-00h							

Table 33. ADC*n*-Internal-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0000	Reserved for factory use.
11–0	ADCINT*n*-DATA[11:0]	R	0x000	Stores the 12–bit ADCINT*n* conversion results in straight binary format. The corresponding voltage is given by: $V_{ref} + 3\left(\frac{V_{ref} \times DATA[11:0]}{4096} - V_{ref}\right)$ (13)

7.6.8.2 ADCn-External-Data Register (address = 0x24 to 0x27) [reset = 0x0000]

This register description applies to the external inputs ADC1 through ADC4.

Figure 87. ADC*n*-External-Data Register (R)

15	14	13	12	11	10	9	8
Reserved				ADCEXT*n*-DATA[11:8]			
R-0h				R-0h			
7	6	5	4	3	2	1	0
ADCEXT*n*-DATA[7:0]							
R-00h							

Table 34. ADC*n*-External-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0000	Reserved for factory use.
11–0	ADCEXT*n*-DATA[11:0]	R	0x000	Stores the 12–bit ADC*n* conversion results in straight binary format.

7.6.8.3 CSn-Data Register (address = 0x28 to 0x2B) [reset = 0x0000]

This register description applies to the current sense inputs CS1 through CS4.

Figure 88. CS*n*-Data Register (R)

15	14	13	12	11	10	9	8
Reserved				CS*n*-DATA[11:8]			
R-0h				R-0h			
7	6	5	4	3	2	1	0
CS*n*-DATA[7:0]							
R-00h							

Table 35. CS*n*-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0000	Reserved for factory use.
11–0	CS*n*-DATA[11:0]	R	0x000	Stores the 12–bit current-sense *n* conversion results in straight binary format (open-loop mode only).

7.6.8.4 LT-Data Register (address = 0x2D) [reset = 0x0000]

Figure 89. LT-Data Register (R)

15	14	13	12	11	10	9	8
Reserved				LT-DATA[11:8]			
R-0h				R-0h			
7	6	5	4	3	2	1	0
LT-DATA[7:0]							
R-00h							

Table 36. LT-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0000	Reserved for factory use.
11–0	LT-DATA[11:0]	R	0x000	Stores the local temperature sensor reading in twos complement format.

7.6.8.5 RTn–Data Register (address = 0x2E to 0x2F) [reset = 0x0000]

This register description applies to the remote temperature sense inputs RT1 and RT2.

Figure 90. RT*n*-Data Register (R)

15	14	13	12	11	10	9	8
Reserved				RT*n*-DATA[11:8]			
R-0h				R-0h			
7	6	5	4	3	2	1	0
RT*n*-DATA[7:0]							
R-00h							

Table 37. RT*n*–Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0000	Reserved for factory use.
11–0	RT*n*-DATA[11:0]	R	0x000	Stores the remote temperature sensor *n* (D*n*+, D*n*–) reading in twos complement format.

7.6.9 DAC Data: Address 0x30 through 0x37

7.6.9.1 DACn-Data Register (address = 0x30 to 0x33) [reset = 0x0000]

This register description applies to the bipolar DAC outputs DAC1 through DAC4.

Figure 91. DAC*n*-Data Register (R/W)

15	14	13	12	11	10	9	8
Reserved				DAC*n*-DATA[11:8]			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
DAC*n*-DATA[7:0]							
R/W-00h							

Table 38. DAC*n*-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0000	Reserved for factory use.
11–0	DAC*n*-DATA[11:0]	R/W	0x000	Stores the 12–bit data to be loaded to DAC*n* in straight binary format. The straight binary format is used for all DAC ranges. Only active in open-loop mode.

7.6.9.2 AUXDACn-Data Register (address = 0x34 to 0x37) [reset = 0x0000]

This register description applies to the auxiliary DAC outputs AUXDAC1 through AUXDAC4.

Figure 92. AUXDAC*n*-Data Register

15	14	13	12	11	10	9	8
Reserved				AUXDAC*n*-DATA[11:8]			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
AUXDAC*n*-DATA[7:0]							
R/W-00h							

Table 39. AUXDAC*n*-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0000	Reserved for factory use.
11–0	AUXDAC*n*-DATA[11:0]	R/W	0x000	Stores the 12–bit data to be loaded to AUXDAC*n* in straight binary format. The straight binary format is used for all DAC ranges.

7.6.10 Closed-Loop Control: Address 0x38 through 0x3B

7.6.10.1 ClosedLoopn Register (address = 0x38 to 0x3B) [reset = 0x0000]

This register description applies to the ClosedLoop1 through ClosedLoop4 registers.

Figure 93. ClosedLoop*n* Register (R/W)

15	14	13	12	11	10	9	8
Reserved				CLOSEDLOOP*n*[11:8]			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
CLOSEDLOOP*n*[7:0]							
R/W-00h							

Table 40. ClosedLoop*n* Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0000	Reserved for factory use.
11–0	CLOSEDLOOP*n*[11:0]	R/W	0x000	Sets the target current for closed loop controller *n* through the following equation: $I_{(DRAIN)} = \frac{CLOSEDLOOPn[11:0] \times V_{ref}}{R_{(SENSE)} \times 51200}$ (14)

7.6.11 Alarm Threshold Configuration: Address 0x40 through 0x4F

7.6.11.1 ADCINTn/CSn-Upper-Threshold Register (address = 0x40, 0x42, 0x44 and 0x46) [reset = 0x0FFF]

This register description applies to the upper threshold alarm registers for ADCINT1/CS1 through ADCINT4/CS4.

Figure 94. ADCINT*n*/CS*n*-Upper-Threshold Register (R/W)

15	14	13	12	11	10	9	8
Reserved				ADCINT-CS*n*-UP-THRESH[11:8]			
R/W-0h				R/W-Fh			
7	6	5	4	3	2	1	0
ADCINT-CS*n*-UP-THRESH[7:0]							
R/W-FFh							

Table 41. ADCINT*n*/CS*n*-Upper-Threshold Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0000	Reserved for factory use.
11–0	ADCINT-CS*n*-UP-THRESH[11:0]	R/W	0xFFF	Sets the 12-bit upper threshold value for the internal ADC *n* (closed-loop mode) or current sense *n* (open-loop mode) alarm in straight binary format as determined by the ADCINT/CS-SELECT bit in register 0x1B.

7.6.11.2 ADCINTn/CSn-Lower-Threshold Register (address = 0x41, 0x43, 0x45 and 0x47) [reset = 0x0000]

This register description applies to the lower threshold alarm registers for ADCINT1/CS1 through ADCINT4/CS4.

Figure 95. ADCINT*n*/CS*n*-Lower-Threshold Register (R/W)

15	14	13	12	11	10	9	8
Reserved				ADCINT-CS*n*-LOW-THRESH[11:8]			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ADCINT-CS*n*-LOW-THRESH[7:0]							
R/W-00h							

Table 42. ADCINT*n*/CS*n*-Lower-Threshold Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0000	Reserved for factory use.
11–0	ADCINT-CS*n*-LOW-THRESH[11:0]	R/W	0x000	Sets the 12-bit lower threshold value for the internal ADC *n* (closed-loop mode) or current sense *n* (open-loop mode) alarm in straight binary format.

7.6.11.3 TS-Upper-Threshold Register (address = 0x48, 0x4A and 0x4C) [reset = 0x07FF]

This register description applies to the upper threshold alarm registers for the device temperature sensors: LT, RT1 and RT2.

Figure 96. *TS*-Upper-Threshold Register (R/W)

15	14	13	12	11	10	9	8
Reserved				*TS*-UP-THRESH[11:8]			
R/W-0h				R/W-7h			
7	6	5	4	3	2	1	0
TS-UP-THRESH[7:0]							
R/W-FFh							

Table 43. *TS*-Upper-Threshold Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0000	Reserved for factory use.
11–0	*TS*-UP-THRESH[11:0]	R/W	0x7FF	Sets the 12-bit upper threshold value for the corresponding temperature sensor (LT, RT1 or RT2) alarm in two's complement format.

7.6.11.4 TS-Lower-Threshold Register (address = 0x49, 0x4B and 0x4D) [reset = 0x0800]

This register description applies to the lower threshold alarm registers for the device temperature sensors: LT, RT1 and RT2.

Figure 97. *TS*-Lower-Threshold Register (R/W)

15	14	13	12	11	10	9	8
Reserved				*TS*-LOW-THRESH[11:8]			
R/W-0h				R/W-8h			
7	6	5	4	3	2	1	0
TS-LOW-THRESH[7:0]							
R/W-00h							

Table 44. *TS*-Lower-Threshold Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0000	Reserved for factory use.
11–0	*TS*-LOW-THRESH[11:0]	R/W	0x800	Sets the 12-bit lower threshold value for the corresponding temperature sensor (LT, RT1 or RT2) alarm in two's complement format.

7.6.11.5 DACnn-Upper-Threshold Register (address = 0x4E and 0x4F) [reset = 0x0FFF]

This register description applies to the upper threshold alarm registers for the bipolar DAC pairs DAC1/DAC2 and DAC3/DAC4.

Figure 98. DAC*nn*-Upper-Threshold Register (R/W)

15	14	13	12	11	10	9	8
Reserved				DAC*nn*-UP-THRESH[11:8]			
R/W-0h				R/W-Fh			
7	6	5	4	3	2	1	0
DAC*nn*-UP-THRESH[7:0]							
R/W-FFh							

Table 45. DAC*nn*-Upper-Threshold Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0000	Reserved for factory use
11–0	DAC*nn*-UP-THRESH[11:0]	R/W	0xFFF	Sets an upper output limit othen than full-scale for the bipolar DAC pairs (DAC1/DAC2 or DAC3/DAC4). When either of the DACs in a given pair is loaded with a value exceeding the limit, its output is updated with the DAC*nn*-UP-THRESH[11:0] value instead.

7.6.12 Alarm Hysteresis Configuration: Address 0x50 and 0x56

7.6.12.1 ADCINTn/CSn-Hysteresis Register (address = 0x50 to 0x53) [reset = 0x0008]

This register description applies to the hysteresis registers for ADCINT1/CS1 through ADCINT4/CS4.

Figure 99. ADCINT*n*/CS*n*-Hysteresis Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
Reserved	ADCINT-CS*n*-HYSTER[6:0]						
R/W-0	R/W-08h						

Table 46. ADCINT*n*/CS*n*-Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
15–7	Reserved	R/W	All zeros	Reserved for factory use.
6–0	ADCINT-CS*n*-HYSTER[6:0]	R/W	0x08	Hysteresis of internal ADC *n* (closed-loop mode) or current sense *n* (open-loop mode), 1 LSB per step.

7.6.12.2 LT-Hysteresis Register (address = 0x54) [reset = 0x0008]

Figure 100. LT-Hysteresis Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
Reserved			LT -HYSTER[4:0]				
R/W-0h			R/W-08h				

Table 47. LT-Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
15–5	Reserved	R/W	All zeros	Reserved for factory use
4–0	LT -HYSTER[4:0]	R/W	0x08	Hysteresis of local temperature sensor, 1°C per step.

7.6.12.3 RTn–Hysteresis Register (address = 0x55 to 0x56) [reset = 0x0008]

This register description applies to the hysteresis registers for RT1 and RT2.

Figure 101. RT*n*–Hysteresis Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
Reserved			RT*n*-HYSTER[4:0]				
R/W-0h			R/W-08h				

Table 48. RT*n*–Hysteresis Field Descriptions

Bit	Field	Type	Reset	Description
15–5	Reserved	R/W	All zeros	Reserved for factory use
4–0	RT*n*-HYSTER[4:0]	R/W	0x08	Hysteresis of remote temperature sensor *n* (D*n*+, D*n*–), 1°C per step.

7.6.13 GPIO: Address 0x58

7.6.13.1 GPIO Register (address = 0x58) [reset = 0x000F]

Figure 102. GPIO Register (R/W)

15	14	13	12	11	10	9	8
Reserved							
R/W-00h							
7	6	5	4	3	2	1	0
Reserved				GPIO4	GPIO3	GPIO2	GPIO1
R/W-0h				R/W-1	R/W-1	R/W-1	R/W-1

Table 49. GPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	Reserved	R/W	All zeros	Reserved for factory use
3	GPIO4	R/W	1	For write operations the GPIO pin operates as an output. Writing a 1 to the GPIO*n* bit sets the GPIO*n* pin to high impedance. Writing a 0 sets the GPIO*n* pin to logic low. An external pullup resistor is required when using the GPIO as an output. For read operations the GPIO pin operates as an input. Read the GPIO*n* bit to receive the status of the GPIO*n* pin. After power-on reset, or any forced hardware or software reset, the GPIO*n* pin is in a high-impedance state.
2	GPIO3	R/W	1	
1	GPIO2	R/W	1	
0	GPIO1	R/W	1	

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The AMC7834 device is a highly integrated, low-power, analog monitoring and control solution that includes one multi-channel 12-bit ADC, eight 12-bit DACs, four high-side current-sense amplifiers and temperature sensing capabilities. The AMC7834 typical application is power amplifier biasing in wireless base stations, however its high level integration make it a good solution for many different systems ranging from industrial control sytems to test-and-measurement units.

The power amplifiers (PAs) used in wireless infrastructure include transistor technologies that are extremely temperature sensitive, and require DC biasing circuits to optimize RF performance, power efficiency, and stability. The AMC7834 device provides eight DAC channels that can be used to bias the inputs of the power amplifiers. The device also includes two remote temperature sensing interfaces, one internal local temperature sensor, four high-side current-sensing channels, and four ADC channels for general-purpose monitoring.

Current sensing and temperature sensing are the two main monitoring schemes for PA bias compensation. The PA drain current is monitored by measuring the differential voltage drop accross a shunt resistor. The AMC7834 internal local-temperature sensor and two remote-sensor driver inputs can be used to detect temperature variations during PA operation. 图 103 shows the circuit diagram of this system.

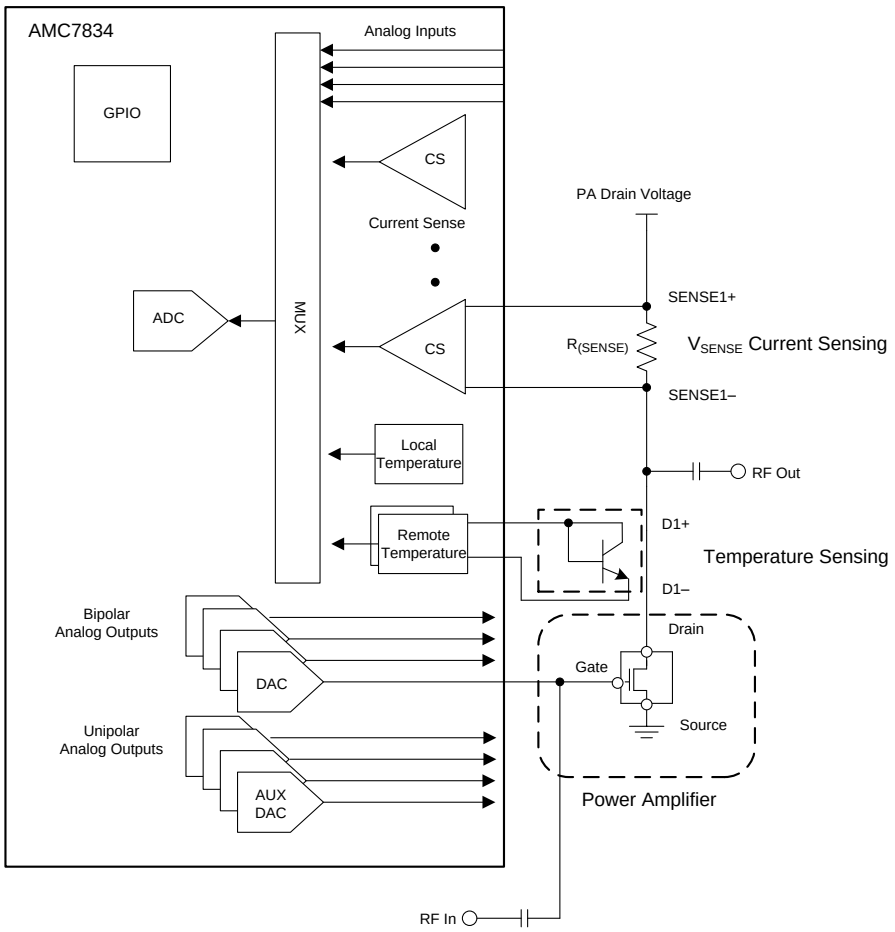


图 103. AMC7834 Example PA Bias System

8.2 Typical Application

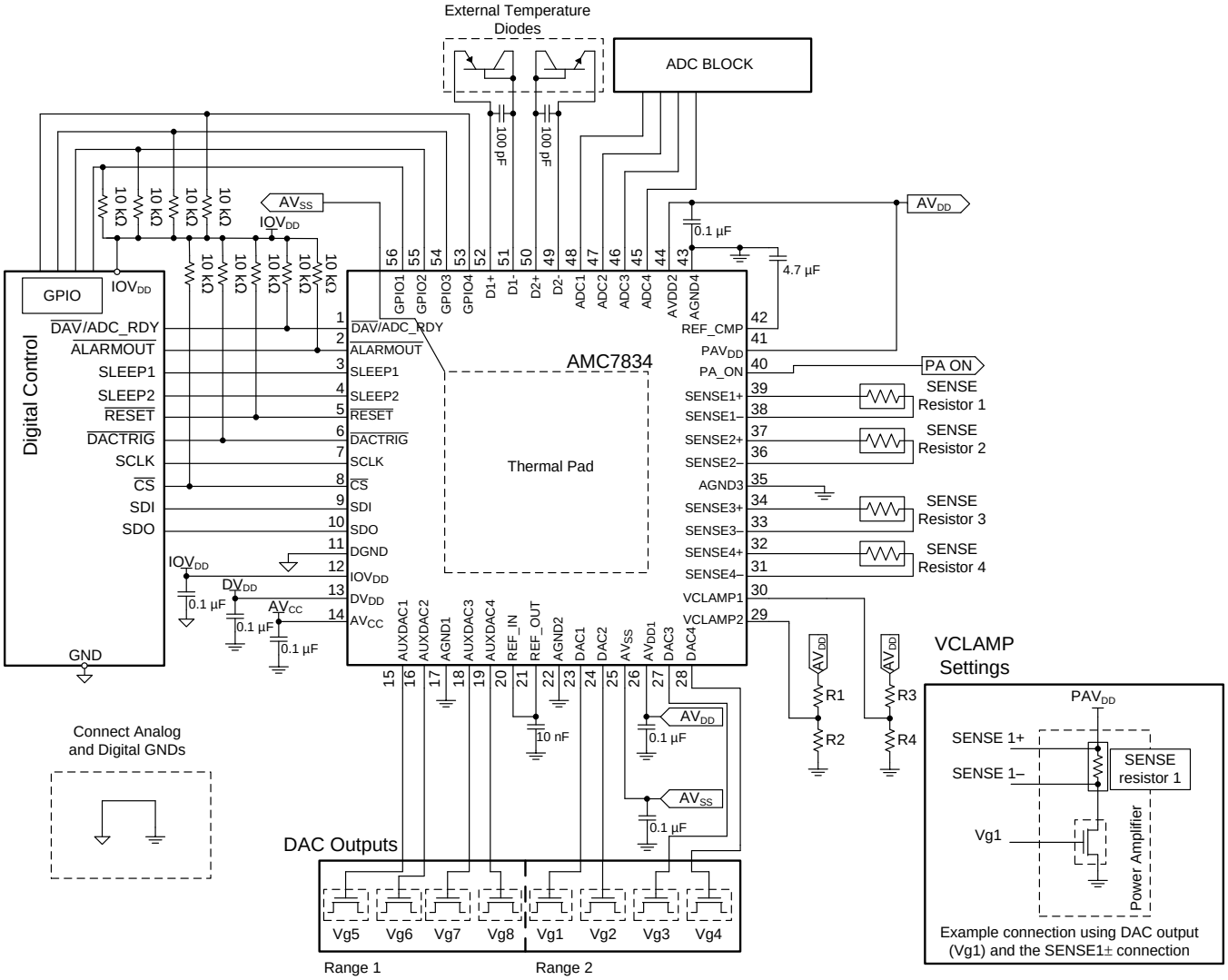


图 104. AMC7834 Example Schematic

8.2.1 Design Requirements

The AMC7834 example schematic uses the majority of the design parameters listed in 表 50.

表 50. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
AV_{CC}	5 V
IOV_{DD}	3.3 V
DV_{DD}	5 V
AV_{DD}	5 V
AV_{SS}	–5 V
4 External unipolar inputs	ADC[1-4]: 0 to 2.5 V range
4 High-Side Current Sense	Differential input of 0 to 200 mV
4 bipolar DAC outputs	–4 to 1 V, –5 to 0 V, and 0 to 5 V
4 unipolar DAC outputs	0 to 5 V, 2.5 to 7.5 V
Remote temperature sensing	Two remote temperature diode drivers

8.2.2 Detailed Design Procedure

Use the following parameters to facilitate the design process:

- AV_{CC} and AV_{SS} voltage values
- ADC and high-side current-sense input voltage range
- DAC output voltage ranges
- Remote temperature applications

8.2.2.1 ADC Input Conditioning

The AMC7834 monitoring system is centered on a single ADC core that features a multichannel input stage to a successive approximation register (SAR) ADC. The analog inputs include four external analog inputs, four internal inputs for bipolar DAC monitoring, four high-side current-sense amplifiers for PA current monitoring, two remote temperature sensors, and an internal analog temperature sensor.

The external analog inputs (ADC1 through ADC4) feature a range of 0 to V_{ref} (V_{ref} corresponds to either an external 2.5 V reference or the device internal reference), while the internal inputs accept a full-scale range of –5 to 2.5 V. The current-sense inputs feature a 4 to 60 V common-mode voltage range, and accept a differential input range of 0 to 200 mV. A 4.7 µF capacitor is recommended between the REF_CMP pin and the AGND4 pin. The value of this capacitor must exceed 470 nF to ensure reference stability. A high-quality ceramic capacitor, type NP0 or X7R, is recommended because of the optimal performance of the capacitor across temperature and very-low dissipation factor.

It is recommended that all external analog inputs are driven with a low impedance source to ensure correct functionality. In applications where the signal-source impedance is high, the analog inputs can be conditioned through a buffer amplifier, such as a voltage follower.

8.2.2.2 DAC Output Range Selection

The AMC7834 device has four bipolar and four unipolar DACs with programmable output ranges. The bipolar DACs feature the ranges –4 to 1 V, –5 to 0 V, and 0 to 5 V. The unipolar DACs feature the ranges 0 to 5 V and 2.5 to 7.5 V. The DAC ranges are configurable by setting the DAC range register (see the *DAC Range Register (address = 0x16) [reset = 0x0000]* section).

The maximum source and sink capability of the DAC internal amplifiers are listed as part of the DAC output characteristics in the *Electrical Characteristics—DAC Specifications* table.

The graph in the *Application Performance Curve* section show the relationship of both stability and settling time with different capacitive and resistive loading structures.

8.2.2.3 Temperature Sensing Applications

The AMC7834 has one local temperature and two temperature diode drivers, as well as four external analog inputs that are easily configurable to remote temperature sensor circuits. The integrated temperature sensor, remote temperature sensor, and analog input registers automatically update with every conversion. 图 105 shows a typical setup for the two temperature diode-driver inputs. Additional noise filtering can be achieved by placing a bypass capacitor across the inputs of the remote temperature sensors. A high-quality ceramic capacitor, type NP0 or X7R, is recommended because of the optimal performance of the capacitor across temperature. See the *Remote Temperature Sensors* section for a details.

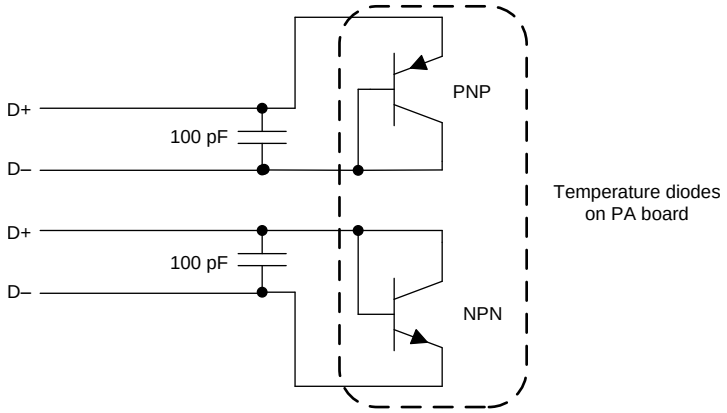


图 105. Remote Temperature Sensors (PNP and NPN)

Additionally, the ADC inputs can be used to accept voltage from other temperature-sensing IC circuits as shown in 图 106. The temperature sensor use for analog input conditioning in this example is the LM50 device which is a high precision integrated-circuit temperature sensor that can sense a –40°C to +125°C temperature range using a single positive supply. The full-scale output of the temperature sensor ranges from 100 mV to 1.75 V for a –40°C to +125°C temperature range. In an extremely noisy environment, adding some filtering to minimize noise pickup may be necessary. A typical recommended value for the bypass capacitor is 0.1 µF from the V+ pin to ground. A high-quality ceramic capacitor, type NP0 or X7R, is recommended because of the optimal performance of the capacitor across temperature and very-low dissipation factor.

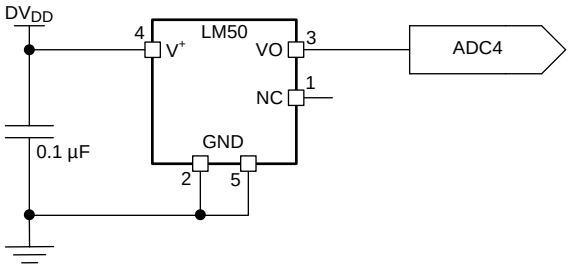


图 106. Temperature Sense Application With LM50

8.2.2.4 Current Sensing Applications

The AMC7834 device also features four high-side current-sense amplifiers that support common-mode voltages from 4 to 60 V and a full-scale sense voltage of 0 to 200 mV. In applications that require current sensing across a power amplifier, the SENSE± differential inputs connect across a resistor to sense small differential voltage that is proportional to current across the PA as shown in 图 107. The current-sense conversion results are stored in the Current sense data registers. The current sensors are also configurable as closed-loop drain current controllers. See the *Current Sensors* section for details.

图 107 shows a method of separating the drain voltage from the power amplifier with a series PMOS transistor. The activation of the PMOS connects the PAV_{DD} voltage supply to the drain pin of the power amplifier. The PMOS is driven with a voltage divider that swings from PAV_{DD} to PAV_{DD}(R2 / [R1 + R2]). The NMOS shown in 图 107 is connected to the PA_ON output which controls the state of the PMOS transistor.

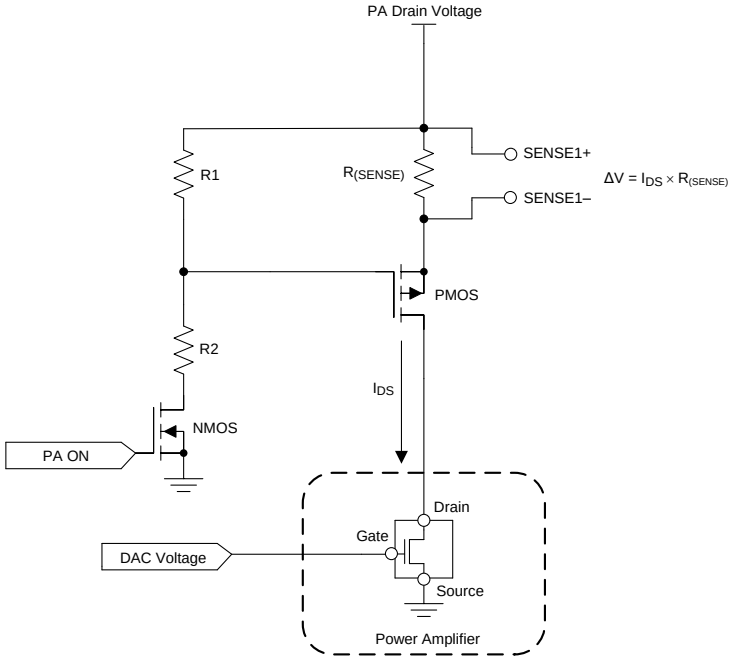
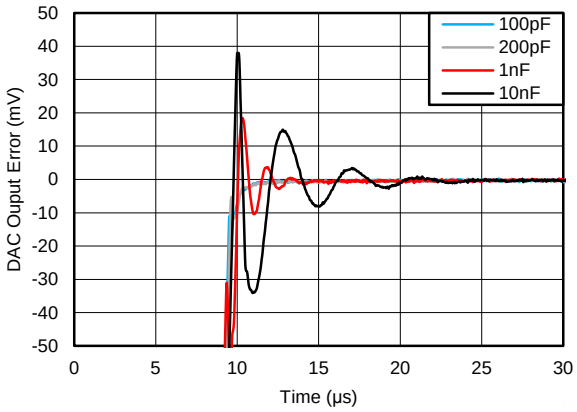


图 107. Current Sense (SENSE) Connections With PMOS ON and OFF

8.2.3 Application Performance Curve



Code 0x000 to 0xFFF to within 0.5% of final value

图 108. DAC Settling Time

8.3 Initialization Set Up

8.3.1 Initialization Procedure

1. Supply all voltages (PAV_{DD}, AV_{DD}, DV_{DD}, IOV_{DD}, AV_{CC}, AV_{SS}) and clamp inputs (VCLAMP1 and VCLAMP2). The AMC7834 does not require a specific supply sequencing.
2. A 250 µs POR delay occurs after a minimum AV_{DD} supply of 4.5 V has been applied. Do not attempt serial communication during this time.
3. It is recommended to issue a hardware or software-reset.
4. Wait for completion of the reset operation (at least 250 µs for a hardware reset or at least 10 µs for a software reset).
5. After reset, the following conditions are met:
   – The device is in open-loop mode and all DAC data registers are set to all zeros.
   – All DAC outputs are set to the clamp value regardless of the SLEEP1 and SLEEP2 pin levels.
   – The PA_ON signal is set to the OFF state.
6. If not already done so, it is recommended to tie the SLEEP1 and SLEEP2 pins low.
7. Configure the AMC7834 without the DACs leaving clamp mode.
8. If the PA_ON control signal is enabled, switch the PA_ON signal to the ON state. By default, the AV_{SS} supply must be present to enable the PA_ON signal to enter the ON state.
9. Release the DACs out of clamp mode.
10. Verify that the ADC has entered the READY state.
11. Issue an ADC trigger signal to initiate conversion of the monitoring inputs.

After initialization the AMC7834 allows switching between open-loop and closed-loop operation. However, before switching between operating modes, it is strongly recommended to clamp the bipolar DAC outputs, stop the ADC conversion cycle, and if applicable, switch the PA_ON signal to the OFF state. To resume operation follow steps 7 through 11 of the Initialization Procedure.

9 Power Supply Recommendations

The AMC7834 supply voltage ranges are specified in the *Recommended Operating Conditions* table.

10 Layout

10.1 Layout Guidelines

- All power supply pins should be bypassed to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance has a value of 0.1 µF and is ceramic with a X7R or NP0 dielectric.
- A 4.7 µF capacitor is recommended between the REF_CMP pin and the AGND4 pin. A minimum capacitor value of 470 nF is required to ensure stability.
- A high-quality ceramic capacitor, type NP0 or X7R, is recommended because of the optimal performance of the capacitor across temperature and very-low dissipation factor.
- The digital and analog sections should have proper placement with respect to the digital pins and analog pins of the AMC7834 device (see 图 110). The separation of analog and digital blocks allows for better design and practice as it ensures less coupling into neighboring blocks and minimizes the interaction between analog and digital return currents.

10.2 Layout Example

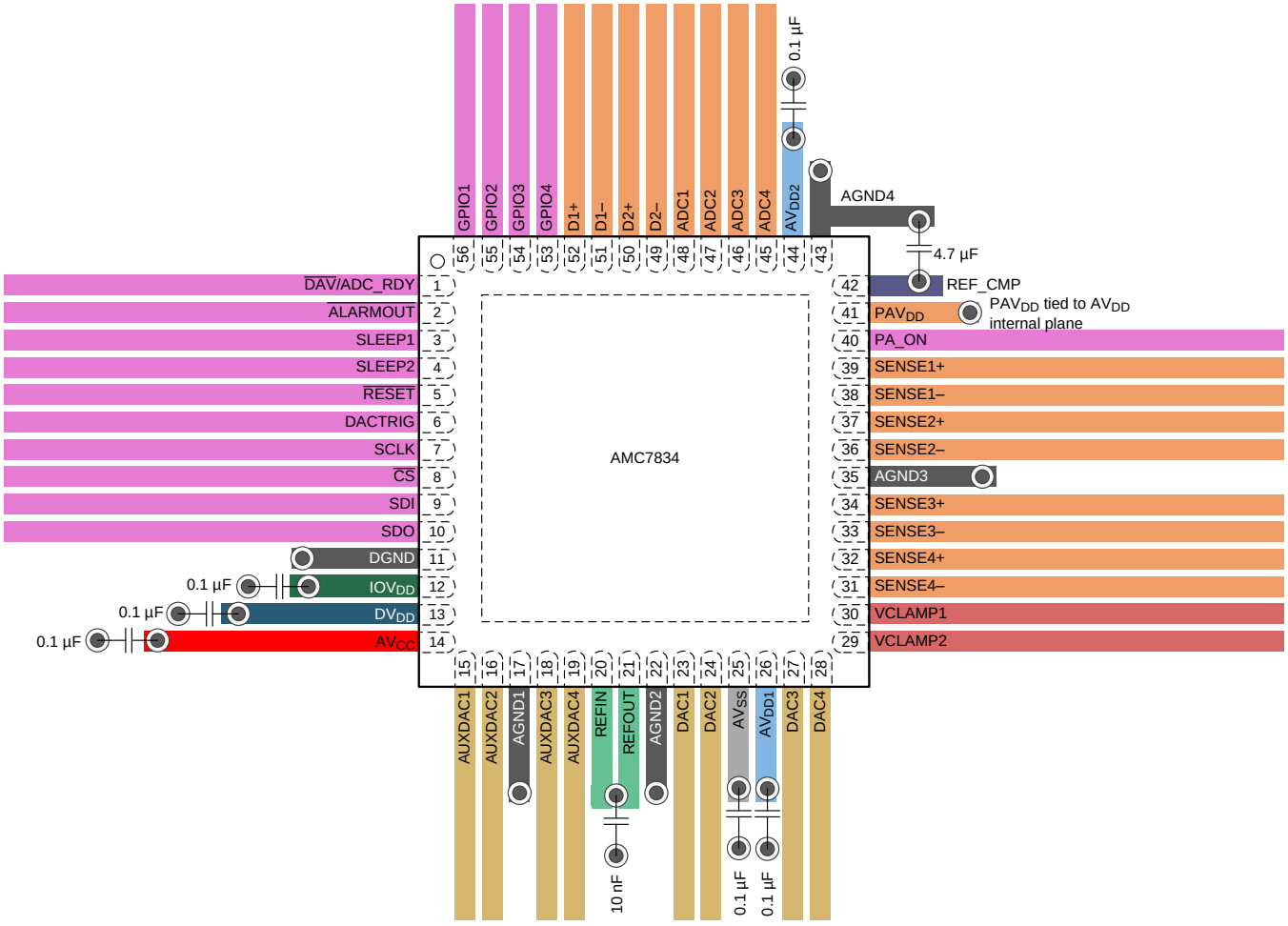


图 109. AMC7834 Layout Example

Layout Example (接下页)

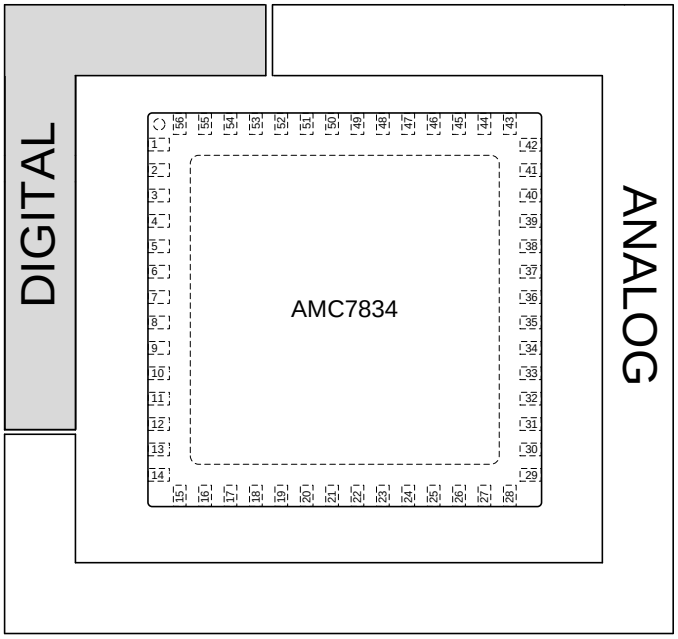


图 110. AMC7834 Example Board Layout — Component Placement

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档请参见以下部分：

- 《*LM50/LM50-Q1 SOT-23 单电源摄氏温度传感器*》，SNIS118
- 《*LMP848x 具有电压输出的高精度 76V 高侧电流感测放大器*》，SNVS829

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC7834IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	AMC7834	Samples
AMC7834IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC7834	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

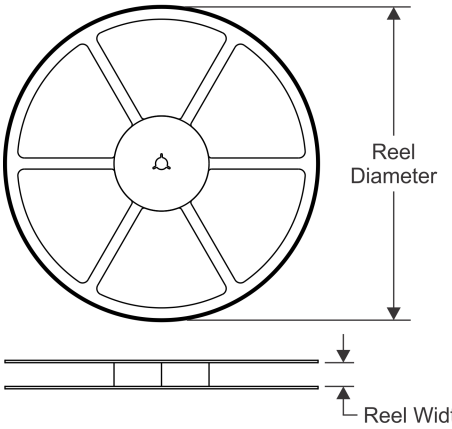
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

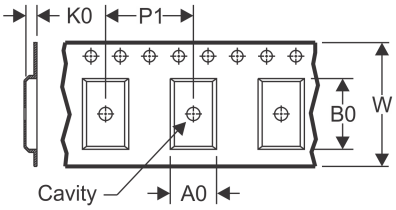
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

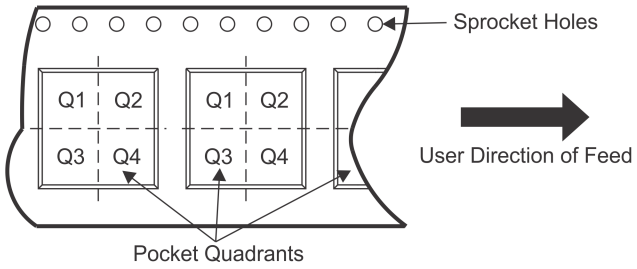


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

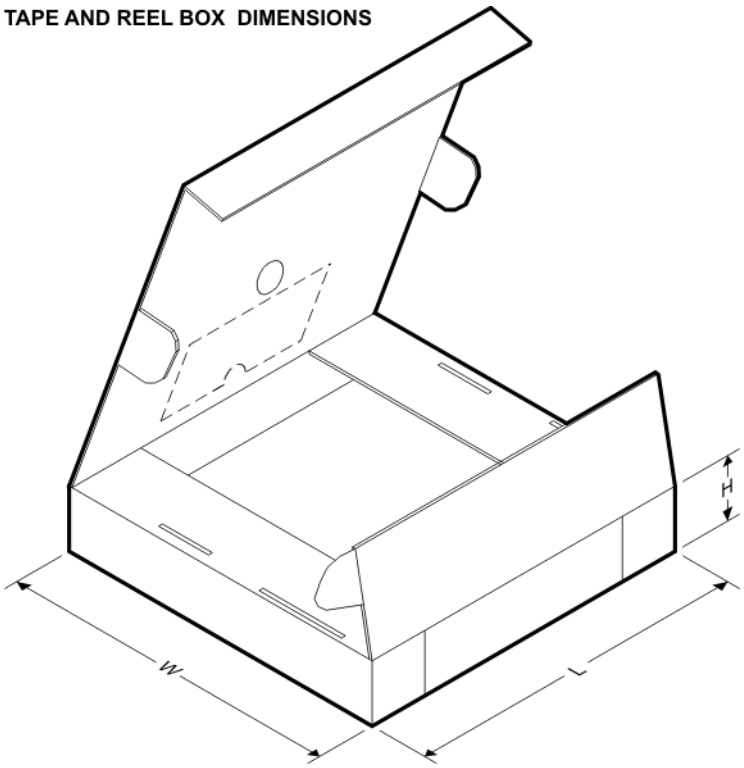
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC7834IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
AMC7834IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
AMC7834IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
AMC7834IRTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC7834IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
AMC7834IRTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
AMC7834IRTQR	QFN	RTQ	56	2000	338.0	355.0	50.0
AMC7834IRTQT	QFN	RTQ	56	250	210.0	185.0	35.0

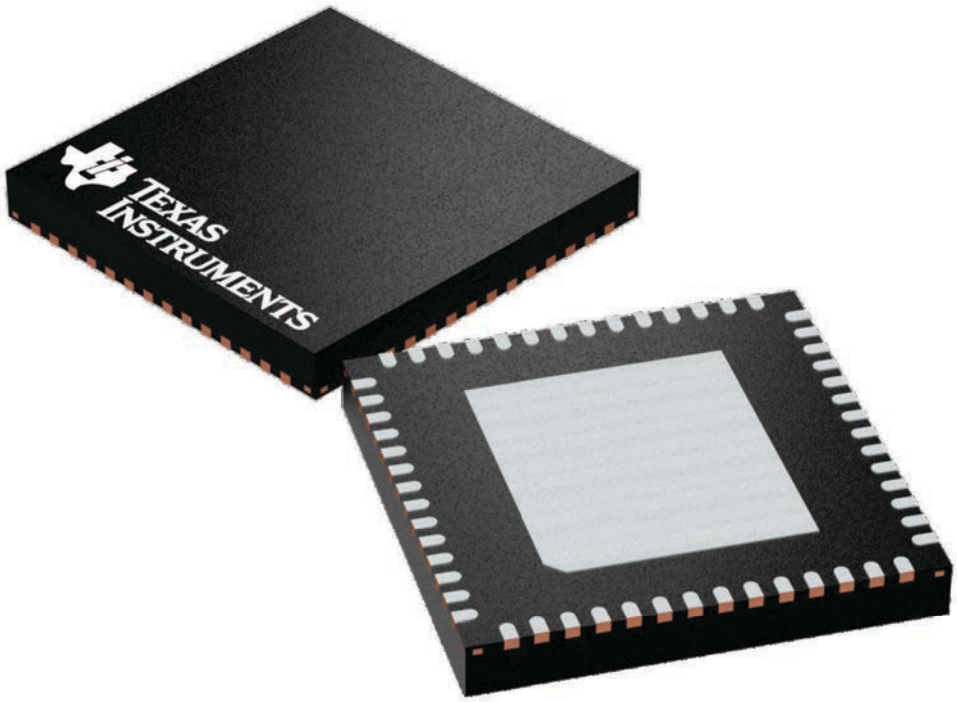
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

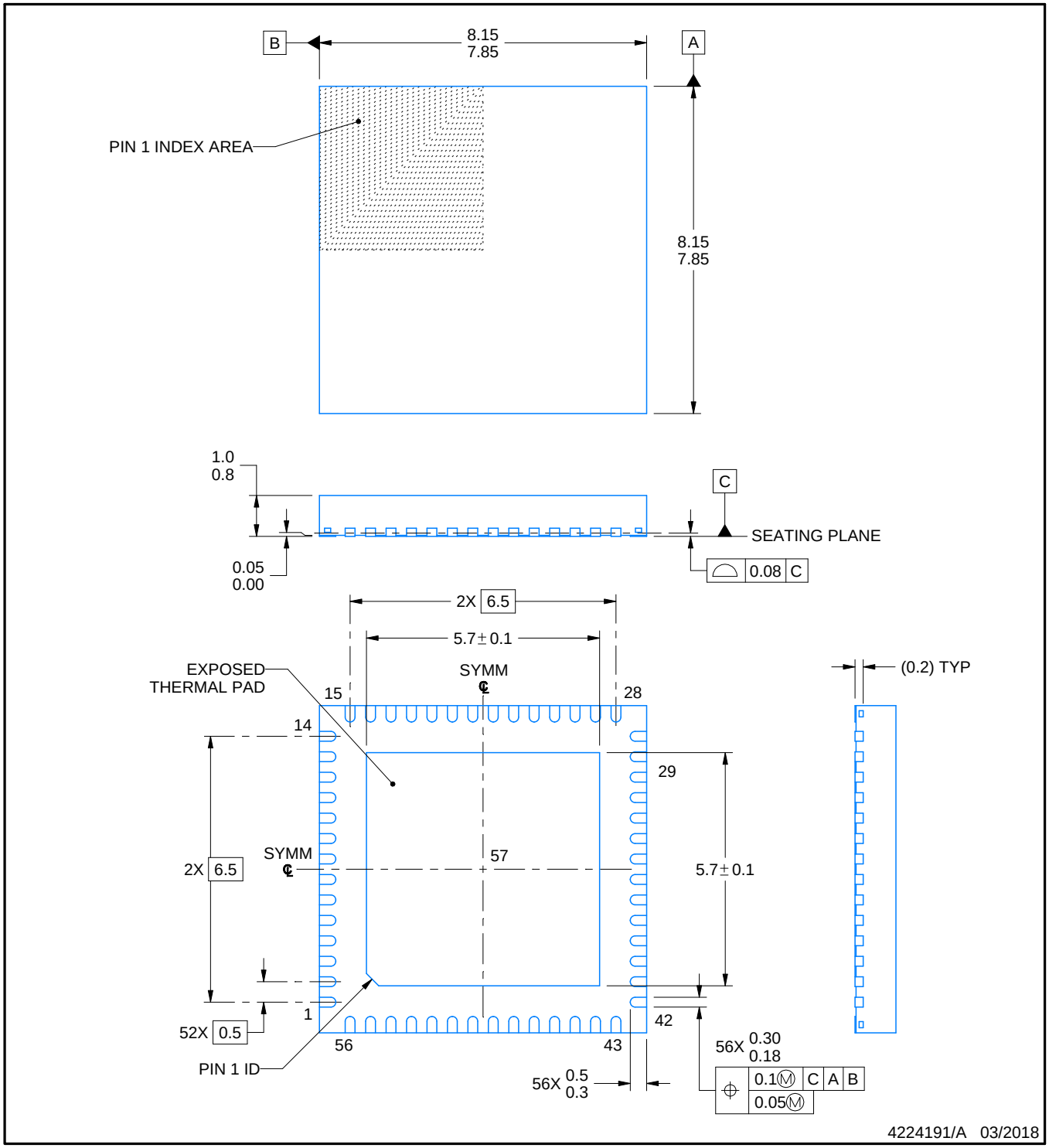
4224653/A

RTQ0056E

PACKAGE OUTLINE

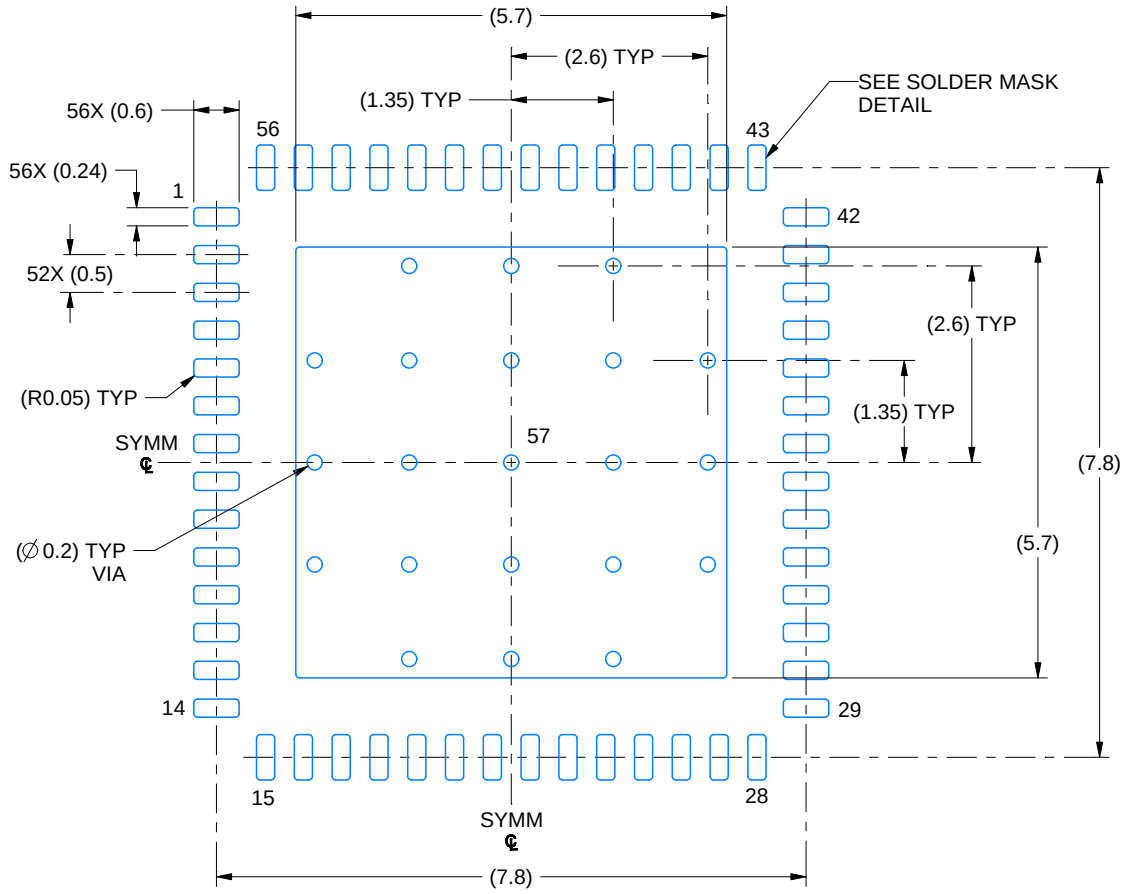
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

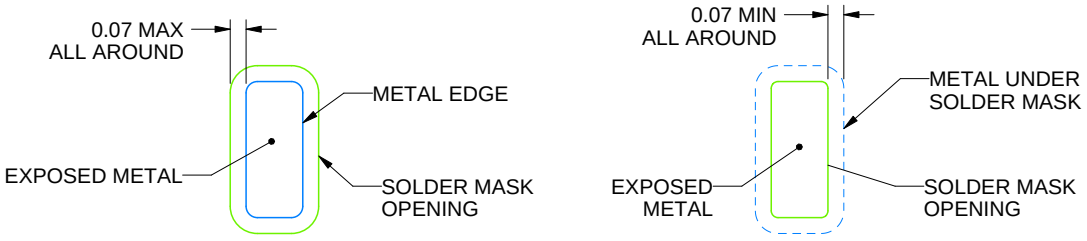


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

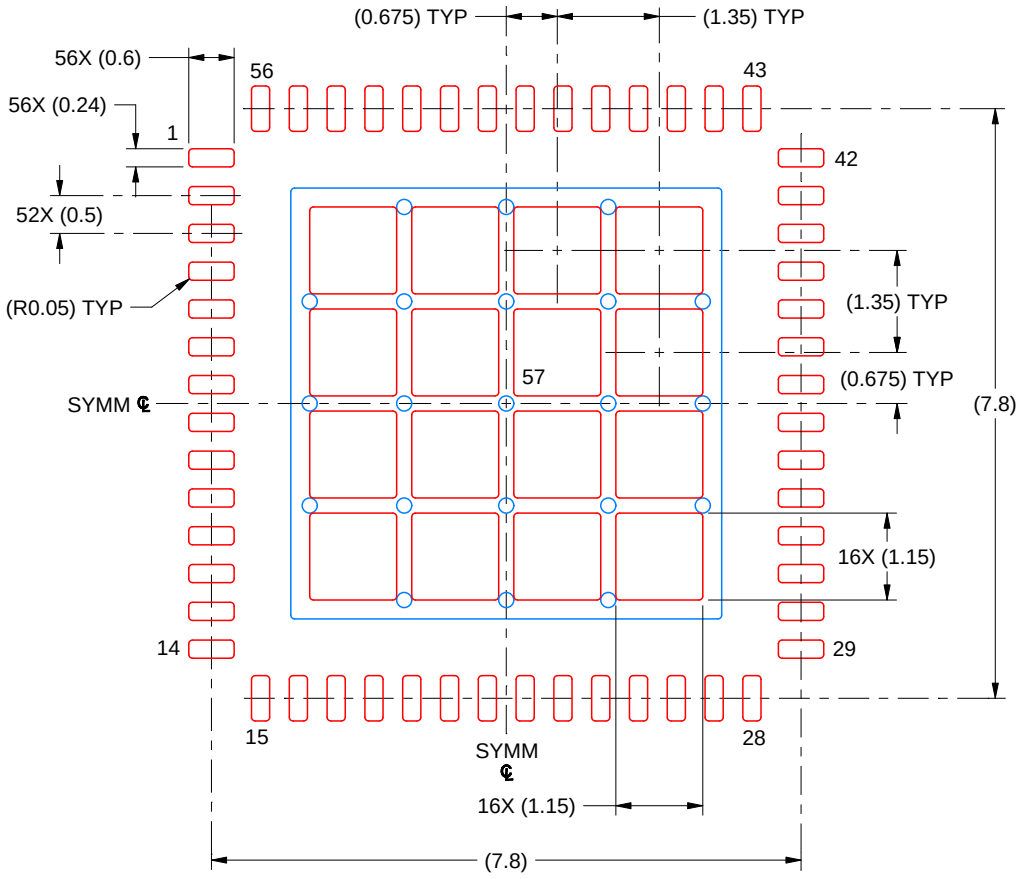


SOLDER MASK DETAILS

4224191/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

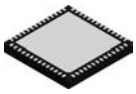
4224191/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

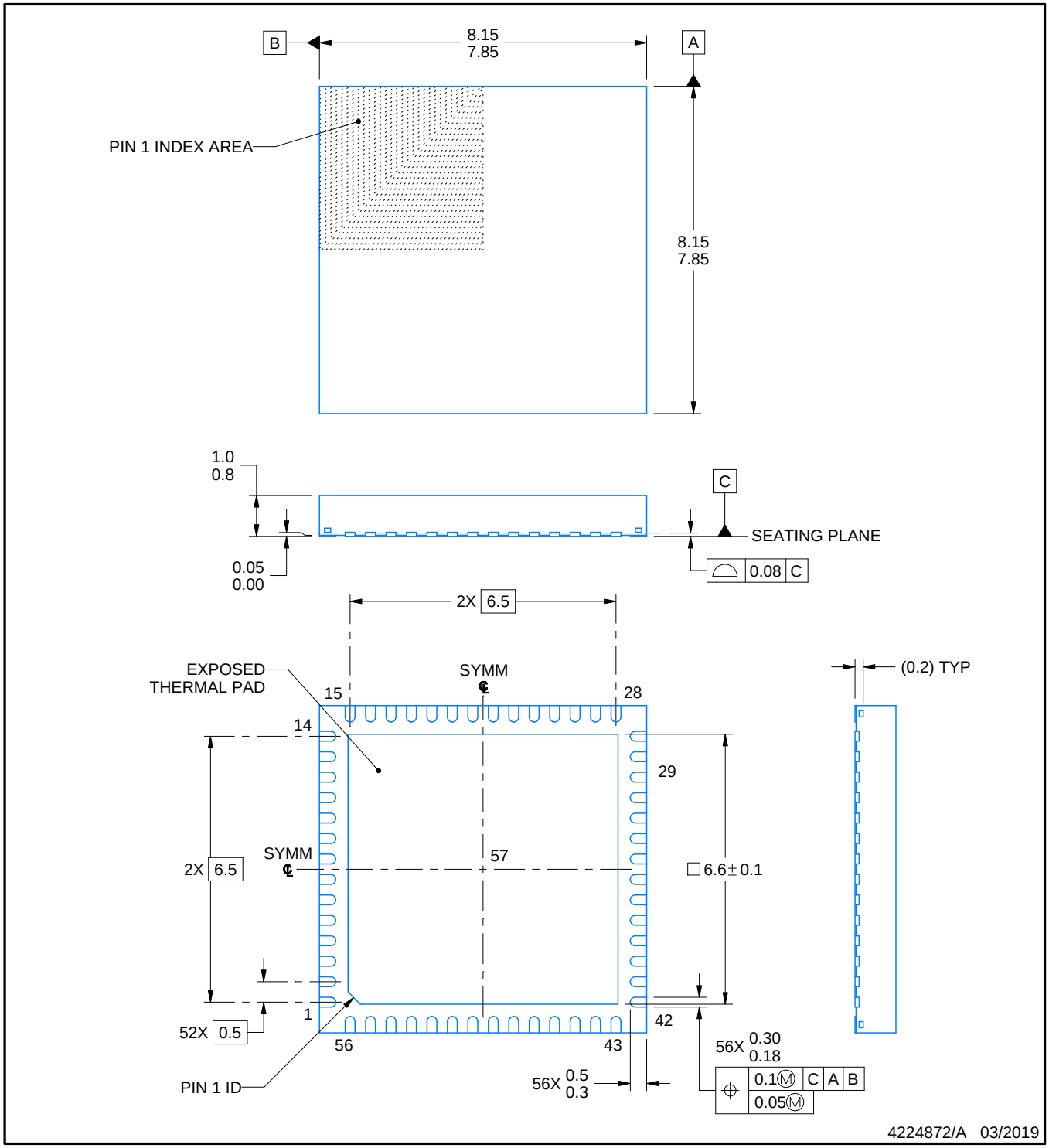
PACKAGE OUTLINE

RTQ0056C



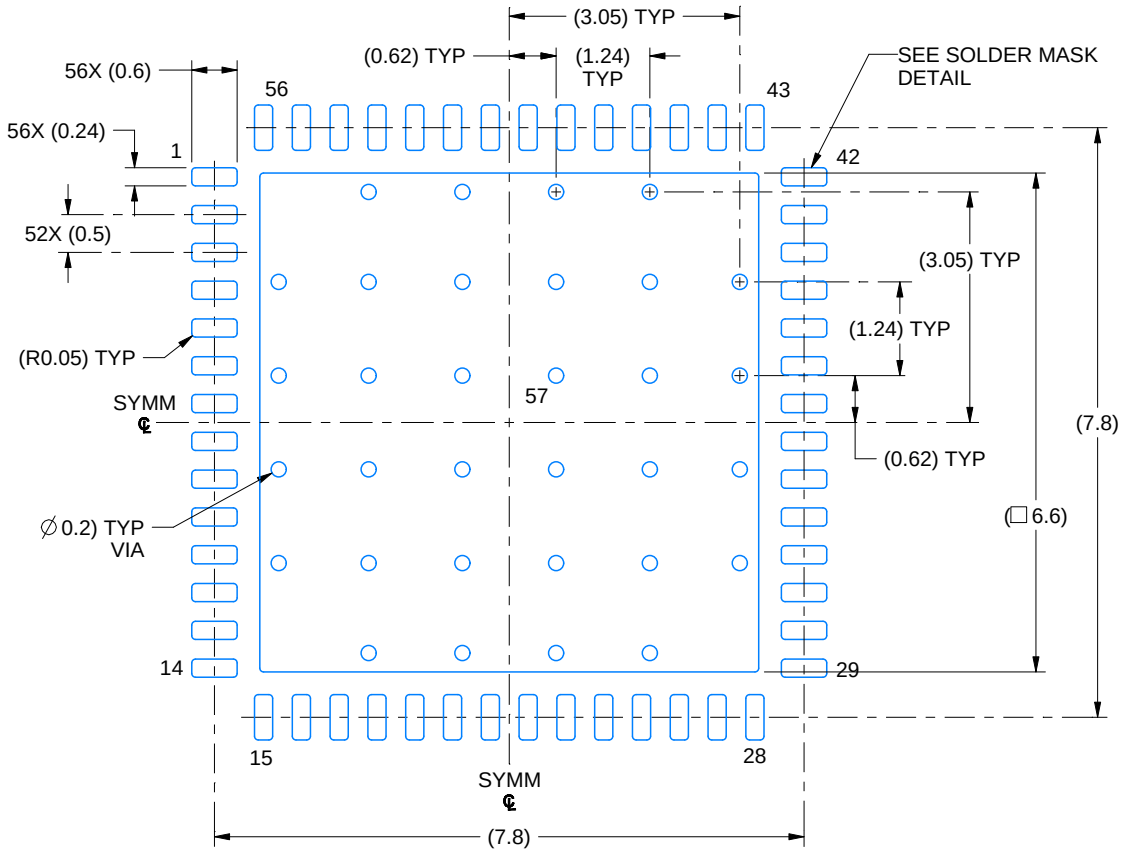
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

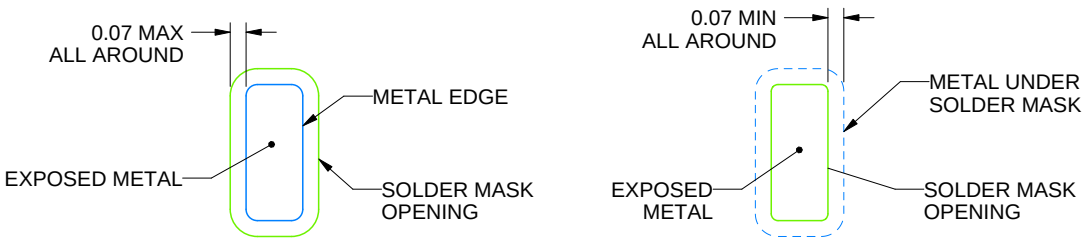


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

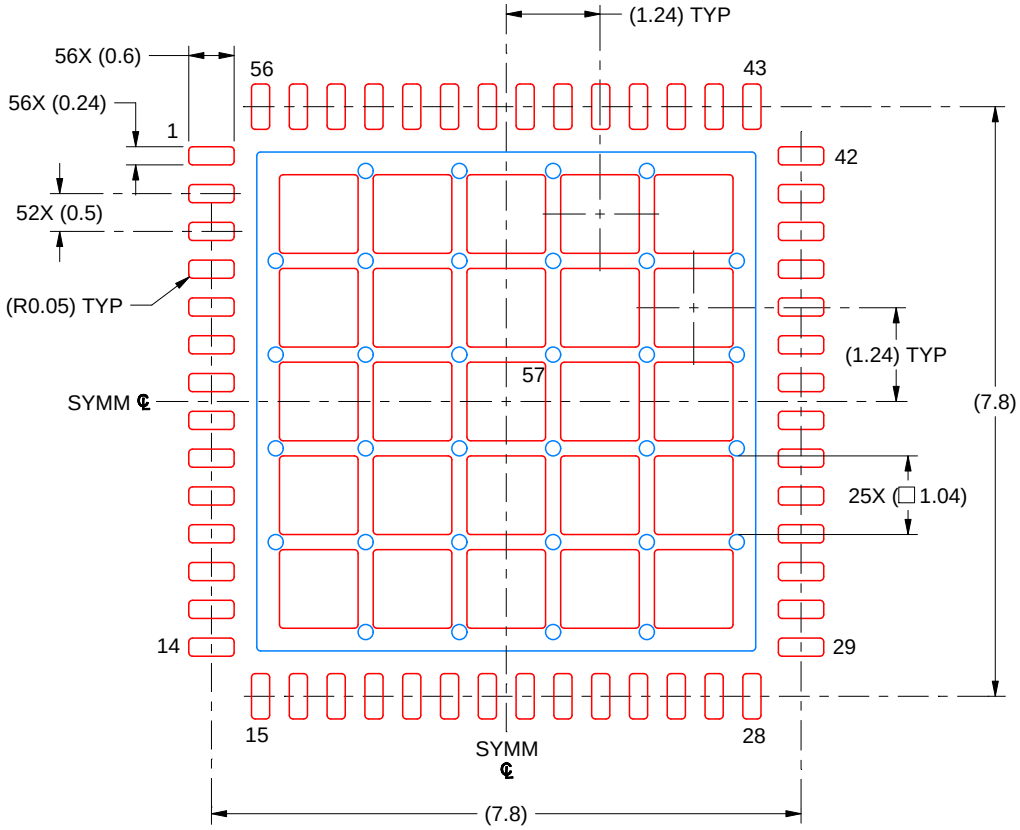


SOLDER MASK DETAILS

4224872/A 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224872/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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