具有双路 LDO 的 TPS65000-Q1 2.25 MHz 降压转换器

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 2 级：
    环境工作温度范围为 –40°C 至 +105°C
  - 器件人体放电模式 (HBM) 静电防护 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 降压转换器：
  - V_{IN} 范围从 2.3V 至 6V
  - 用于降低电磁干扰 (EMI) 的展频时钟 (SSC) 系列产品
  - 2.25MHz 固定频率运行
  - 600mA 输出电流
- LDO：
  - V_{IN} 范围从 1.6V 至 6V
  - 可调输出电压
  - 高达 300mA 输出电流
  - 独立电源输入和使能
- 3 mm × 3 mm 16 引脚 WQFN

2 应用

- 汽车摄像头模块
- 汽车信息娱乐系统
- 汽车仪表盘
- 汽车传感器融合

3 说明

TPS65000-Q1 器件是一款应用于汽车的单片 电源管理集成电路 (IC)。这个器件包含一个带有两个低压降稳压器的单个降压转换器。为了在最大可能的负载电流范围内实现最大效率，这个降压转换器在轻负载时进入低功耗模式。对于低噪声 应用，该器件可通过 MODE 引脚强制进入固定频率 PWM。此降压转换器允许使用小型电感器和电容器，因此可实现较小的解决方案尺寸。电源正常状态输出可用于排序。LDO 可提供 300mA 的电流，且可在 1.6V 到 6V 的输入电压范围内工作，因此可从降压转换器提供。该降压转换器和 LDO 具有单独的电压输入和使能端，从而实现了设计和排序的灵活性。

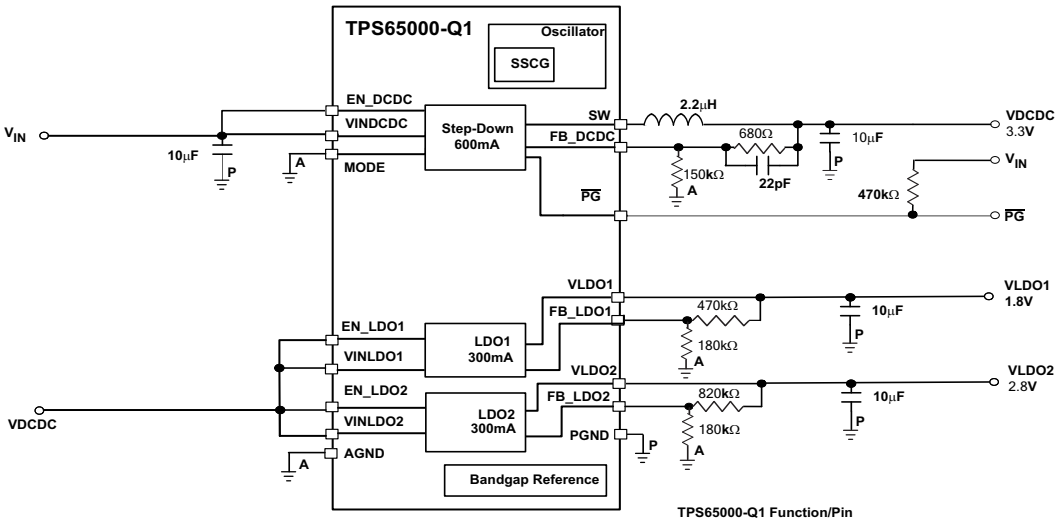
TPS65000-Q1 采用 16 引脚无引线封装 (3mm x 3mm WQFN)。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS65000-Q1	WQFN (16)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (September 2015) to Revision C — **Page**

- 已删除 *文档标题中的* SVS ... 1
- 已更改 *应用列表* ... 1
- Changed the CDM values in the *ESD Ratings* table ... 4
- Changed the temperature range in the *Overview* section from –40°C to +85°C to –40°C to +105°C ... 10
- Changed the PWM description of the MODE pin in the *Device Functional Modes* section ... 15
- Deleted extra devices from the *Design Parameters* table ... 16
- Deleted the tables with recommended inductors and capacitors ... 17
- 已添加 *接收文档更新通知* 部分 ... 21
- 已更改 *静电放电注意事项*声明 ... 21

Changes from Revision A (October 2013) to Revision B — **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值表*，*特性 说明* 部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Original (August 2012) to Revision A — **Page**

- Changed description for MODE pin in Pin Functions table ... 3
- Deleted power dissipationrow of Absolute Maximum Ratings table ... 4
- Changed DCDC to VDCDC in C_O row of Recommended Operating Conditions ... 4
- Changed DCDC to VDCDC in STEP-DOWN CONVERTER OUTPUT VOLTAGE sectiion of Electrical Characteristics ... 6
- Deleted SUPPLY VOLTAGE SUPERVISOR section of Electrical Characteristics table ... 6

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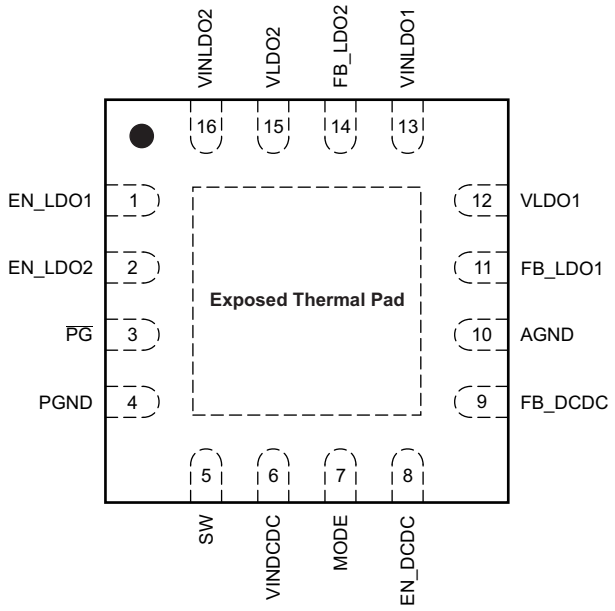
5 Pin Configuration and Functions

RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	10	—	Analog ground – Star back to PGND as close to the IC as possible
EN_DCDC	8	I	Enable DC-DC converter
EN_LDO1	1	I	Enable LDO1
EN_LDO2	2	I	Enable LDO2
FB_DCDC	9	I	Voltage to DC-DC error amplifier
FB_LDO1	11	I	Voltage to LDO1 error amplifier
FB_LDO2	14	I	Voltage to LDO2 error amplifier
MODE	7	I	Selects forced-PWM or PWM-to-PFM automatic-transition mode
$\overline{PG}$	3	O	Open-drain active-low power-good output
PGND	4	—	Power ground – connected to the thermal pad
SW	5	O	Switch pin – connect inductor here
VINDCDC	6	I	Input voltage to DC-DC converter and all other control blocks
VINLDO1	13	I	Input voltage to LDO1
VINLDO2	16	I	Input voltage to LDO2
VLDO1	12	O	LDO1 output voltage
VLDO2	15	O	LDO2 output voltage
EP		—	Exposed thermal pad

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	On all pins except AGND, PGND, EN_DCDC, VLDO1, VLDO2, FB_LDO1, FB_LDO2, FB_DCDC pins with respect to AGND	–0.3	7	V
	On EN_DCDC with respect to AGND	–0.3	V_{IN} + 0.3, ≤ 7	
Output voltage	On VLDO1, VLDO2, FB_LDO1, FB_LDO2, FB_DCDC	–0.3	3.6	V
Current	VINDCDC, SW, PGND,		1800	mA
	VINLDO1, VINLDO2, VLDO1, VLDO1, AGND		800	mA
	At all other pins		1	mA
Operating free-air temperature, T_A		–40	105	°C
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2500	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, 8, 9, 12, 13, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
L1	SW pin inductor	1.5	2.2	3.3	µH
C_I	Input capacitor at VINDCDC	10			µF
	Input capacitor at VINLDO1, VINLDO2	2.2			µF
C_O	Output capacitor for VDCDC	10		22	µF
	Output capacitor for LDO1, LDO2	2.2			µF
I_O	DC-DC converter output current			600	mA
	LDO1 output current			300	mA
	LDO2 output current			300	mA
T_A	Operating ambient temperature	–40		105	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS65000-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25° C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
V_{IN}	Input voltage for VINDCDC of DC-DC converter		2.3		6	V
	Input voltage for LDO1 (VINLDO1)	See [1]	1.6		6	V
	Input voltage for LDO2 (VINLDO2)	See [1]	1.6		6	V
	Internal undervoltage (UVLO) lockout threshold	V_{CC} falling	1.72	1.77	1.82	V
	Internal undervoltage (UVLO) lockout hysteresis			160		mV
SUPPLY CURRENT						
I_Q	Operating quiescent current	MODE low, EN_DCDC high, EN_LDO1, EN_LDO2 low, I_{OUT} = 0 mA and no switching		23	32	µA
		MODE low, EN_DCDC low, EN_LDO1, EN_LDO2 high, I_{OUT} = 0 mA I_{OUT} = 0 mA and no switching		50	57	µA
		EN_DCDC high, MODE high, EN_LDO1, EN_LDO2 low, I_{OUT} = 0 mA		4		mA
I_{SD}	Shutdown Current	EN_DCDC low EN_LDO1 and EN_LDO2 low		0.16	2.2	µA
DIGITAL PINS (EN_DCDC, EN_LDO1, EN_LDO2, MODE, $\overline{PG}$						
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
V_{OL}	Low-level output voltage	$\overline{PG}$ pins only, I_O = –100 µA			0.4	V
I_{lkg}	Input leakage current	MODE, EN_DCDC, EN_LDO1, EN_LDO2 tied to GND or VINDCDC		0.01	0.1	µA
OSCILLATOR						
f_{SW}	Oscillator frequency	SSCG enabled, SSC modulation ratio = 16%	1.722	2.25	2.847	MHz
		SSCG disabled, SSC modulation ratio disabled	2.01	2.25	2.41	MHz
STEP-DOWN CONVERTER POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET ON-resistance	VINDCDC = V_{GS} = 3.6 V		240	480	mΩ
	Low-side MOSFET ON-resistance	VINDCDC = V_{GS} = 3.6 V		185	380	mΩ
I_O	DC output current	2.3 V ≤ VINDCDC ≤ 2.5 V			300	mA
		2.5 V ≤ VINDCDC ≤ 6 V			600	mA

(1) The design principle allows only VINDCDC to be the highest supply in the system. If separate input voltage supplies are used for the DC-DC converter and LDOs, then choose VINDCDC ≥ VINLDO1 and VINDCDC ≥ VINLDO2.

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Electrical Characteristics (continued)

Over full operating ambient temperature range, typical values are at T_A = 25° C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMF}	Forward current limit, PMOS and NMOS	2.3 V ≤ VINDCDC ≤ 6 V	800	1000	1400	mA
STEP-DOWN CONVERTER POWER SWITCH (continued)						
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		30		°C
STEP-DOWN CONVERTER OUTPUT VOLTAGE						
VDCDC	Adjustable output voltage range, VDCDC		0.6		VINDCDC	V
	FB_DCDC pin current				0.1	µA
V_{ref}	Internal reference voltage		0.594	0.6	0.606	V
VDCDC	Output-voltage accuracy (PWM mode)(2)	MODE = high, 2.3 ≤ VINDCDC ≤ 6 V	–1.5%	0%	1.5%	
	Output-voltage accuracy (PFM mode) (3)	MODE low +1% voltage positioning active		1%		
	Load regulation (PWM mode)	MODE high		0.5		%/A
R_{DIS}	Internal discharge resistance at SW	EN_DCDC low		450		Ω
LOW-DROPOUT REGULATORS						
V_I	Input voltage for LDOx (VINLDOx)		1.6		6	V
V_O	Adjustable output voltage, LDOx (VLDOx)(4)		0.73		VINLDOx – V_{DO}	V
I_O	Continuous-pass FET current				300	mA
I_{SC}	Short-circuit current limit	2.3 V ≤ VINLDOx	340		700	mA
		VINLDOx < 2.3 V	210		700	
	FB_LDOx pin current				0.1	µA
	FB_LDOx voltage	Adjustable V_{OUT} mode only		0.5		V
V_{DO}	Dropout voltage (5)	VINLDOx ≥ 2.3 V, I_{OUT} = 250 mA			370	mV
		VINLDOx < 2.3 V, I_{OUT} = 175 mA			370	mV
	Output voltage accuracy (6)	I_O = 1 mA to 300 mA, VINLDOx = 2.3 V–6 V, VLDOx = 1.2 V	–3.5%		3.5%	
		I_O = 1 mA to 175 mA, VINLDOx = 1.6 V–6 V, VLDOx = 1.2 V	–3.5%		3.5%	
	Load regulation	I_O = 1 mA to 300 mA, VINLDOx = 3.6 V VLDOx = 1.2 V	–1.5%		1.5%	
	Line regulation	VINLDOx = 1.6 V–6 V, VLDOx = 1.2 V at I_O = 1 mA	–0.5%		0.5%	
PSRR	Power-supply rejection ratio	f_{NOISE} ≤ 10 kHz, C_{OUT} ≥ 2.2 µF, V_{IN} = 2.3 V, V_{OUT} = 1.3 V, I_{OUT} = 10 mA		40		dB
R_{DIS}	Internal discharge resistance at VLDOx	EN_LDOx low		450		Ω
T_{SD}	Thermal shutdown	Increasing temperature		150		°C
	Thermal shutdown hysteresis	Decreasing temperature		30		°C

(2) For VINDCDC = VDCDC + 1 V
(3) In PFM mode, the internal reference voltage is typically 1.01 × V_{REF}.
(4) Maximum output voltage VLDOx = 3.6 V.
(5) V_{DO} = VINLDOx – VLDOx, where VINLDOx = VLDOx(nom) – 100 mV
(6) Output voltage specification does not include tolerance of external programming resistors.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STEP-DOWN CONVERTER OUTPUT VOLTAGE						
t_{Start}	Start-up time	EN_DCDC to start of switching (10%)		250		µs
t_{Ramp}	VDCDC ramp-up time	VDCDC ramp from 10% to 90%		250		µs
LOW-DROPOUT REGULATORS						
t_{RAMP}	VLDOx ramp time	VLDOx ramp from 10% to 90%		200		µs

6.7 Typical Characteristics

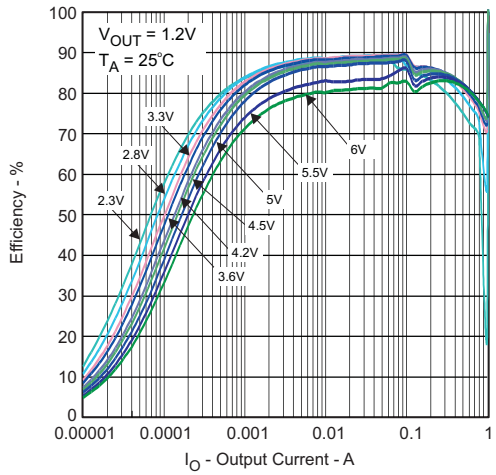

Figure 1. Efficiency (DC-DC 600-mA PFM Mode) vs Output Current

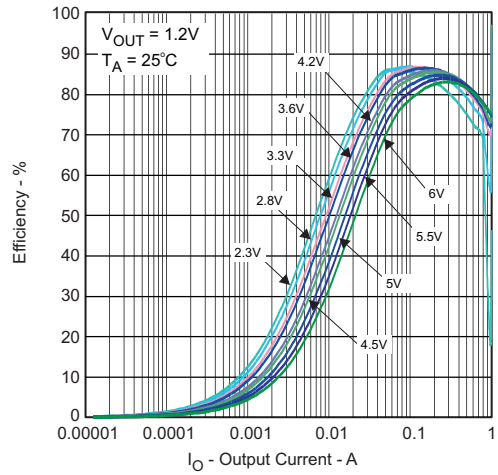

Figure 2. Efficiency (DC-DC 600-mA PWM Mode) vs Output Current

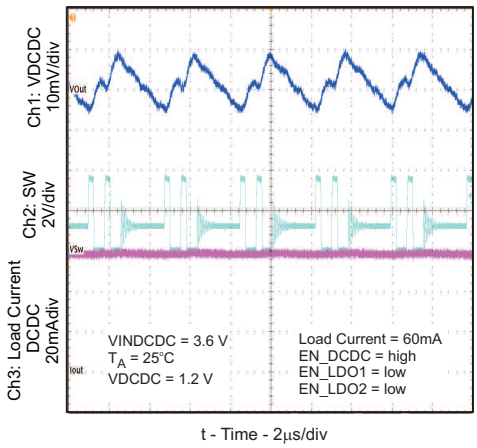

Figure 3. Output Voltage Ripple (DC-DC PFM Mode)

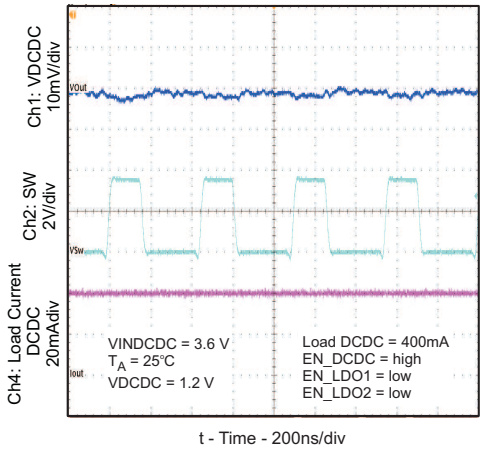

Figure 4. Output Voltage Ripple (DC-DC PWM Mode)

Typical Characteristics (continued)

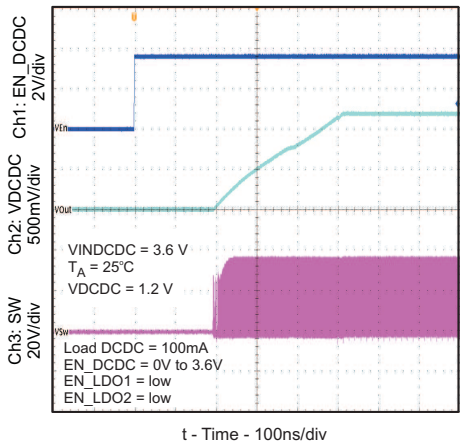

Figure 5. Start-Up Timing (DC-DC)

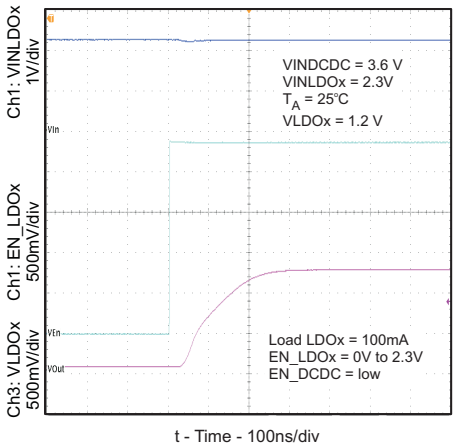

Figure 6. Start-Up Timing (LDOx)

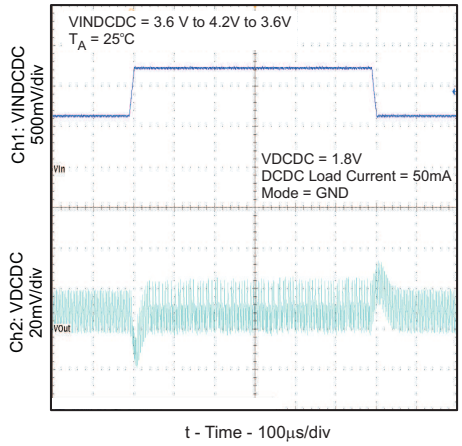

Figure 7. Line Transient Response (DC-DC PFM Mode)

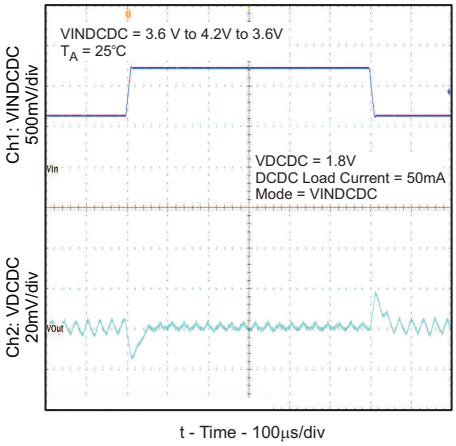

Figure 8. Line Transient Response (DC-DC PWM Mode)

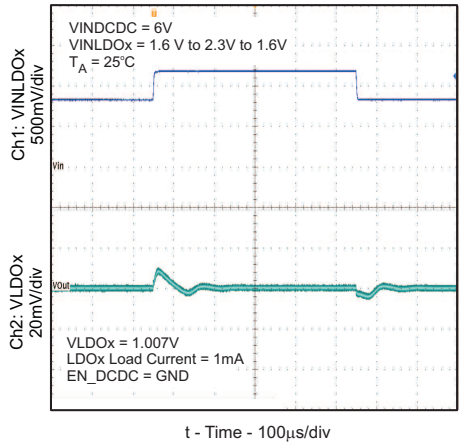

Figure 9. Line Transient Response (LDOx)

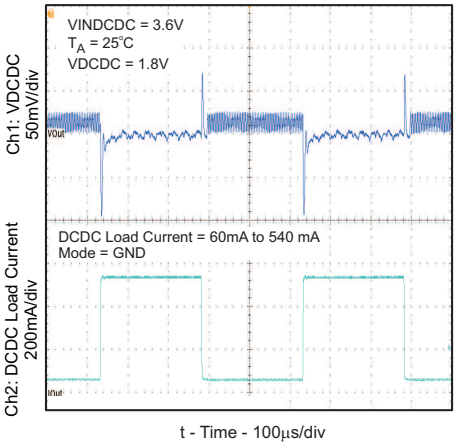

Figure 10. Load Transient Response (DC-DC PFM Mode)

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Typical Characteristics (continued)

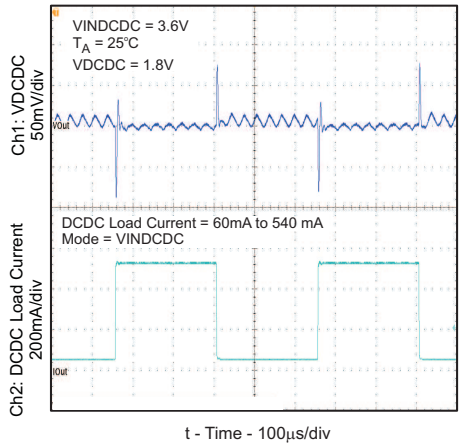


Figure 11. Load Transient Response (DC-DC PWM Mode)

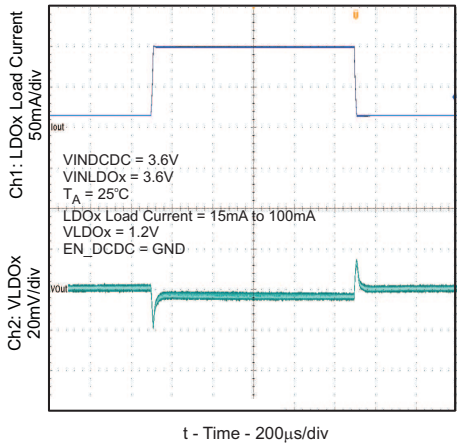


Figure 12. Load Transient Response (LDOx)

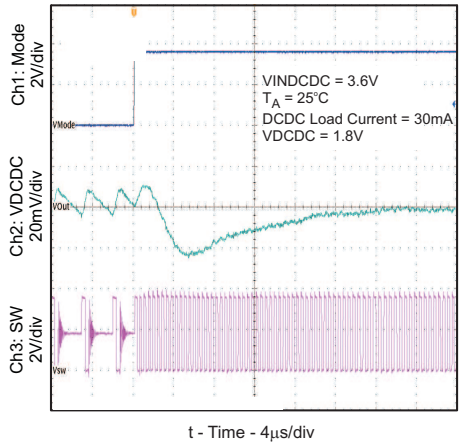


Figure 13. PFM to PWM Transition (DC-DC)

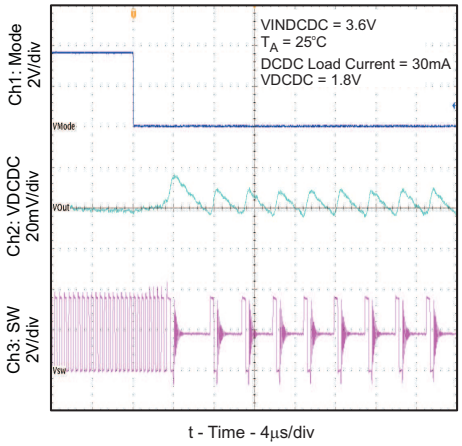


Figure 14. PWM to PFM Transition (DC-DC)

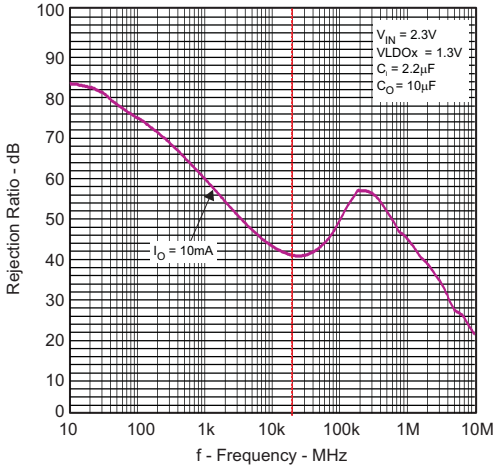


Figure 15. Power-Supply Rejection Ratio (LDOx) vs Frequency

7 Detailed Description

7.1 Overview

The TPS65000-Q1 device provides one step-down converter, two low dropout regulators and spread spectrum clock generation. The device has an input voltage range of
2.3 V to 6 V. This device is intended for (but not limited to) powering automotive camera modules.

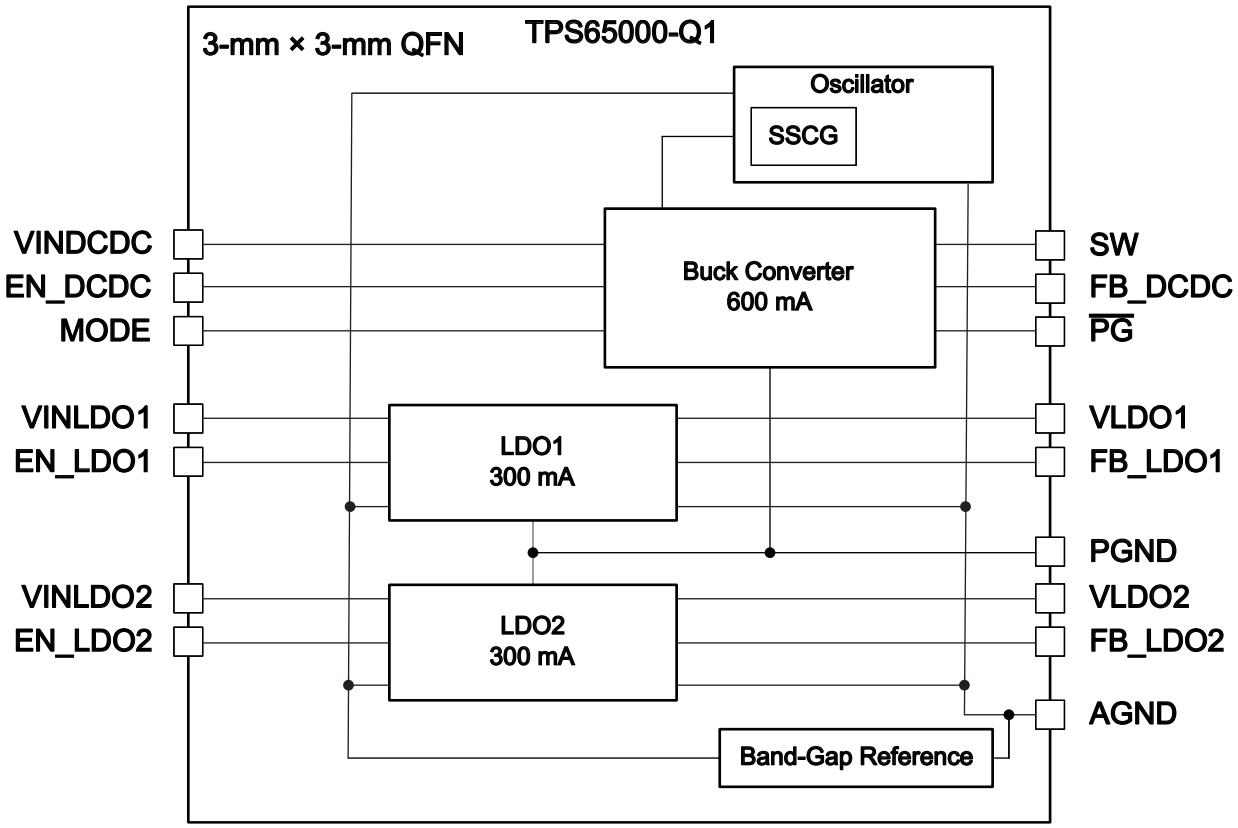
The output voltage of the step-down converter can be selected through resistor networks on the output. To maximize efficiency, there are two modes of operation based on load conditions: PWM or PFM. By pulling the MODE pin high, forced PWM can be achieved. Pulling this pin low results in an automatic adjustment between PFM and PWM modes.

The two general-purpose low-dropout regulators each have their own separate enables and voltage inputs. The inputs can be tied to the output of the step-down converter or to a separate voltage source. Resistor networks are required on the output of the regulator to set the output voltage.

The switching frequency of the step-down converter is handled by the oscillator, with a typical frequency of
2.25 MHz. The spread spectrum clock (SSC) modulates this frequency when the device is in PWM mode. This additional circuit in the oscillator block reduces power that may cause EMI.

The TPS65000-Q1 device also provides a power good signal to monitor the condition of the DC-DC and both LDOs. The DC-DC and LDOs are only monitored if their enable signal is high. If all enabled resources are in regulation, the pin is pulled low. If one or more of the enabled resources are out of regulation, the pin is placed in Hi-Z .

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Step-Down Converter

The step-down converter is intended to allow maximum flexibility in the end equipment. The output voltage is user-selectable with a resistor network on the output. Figure 16 shows the necessary connections.

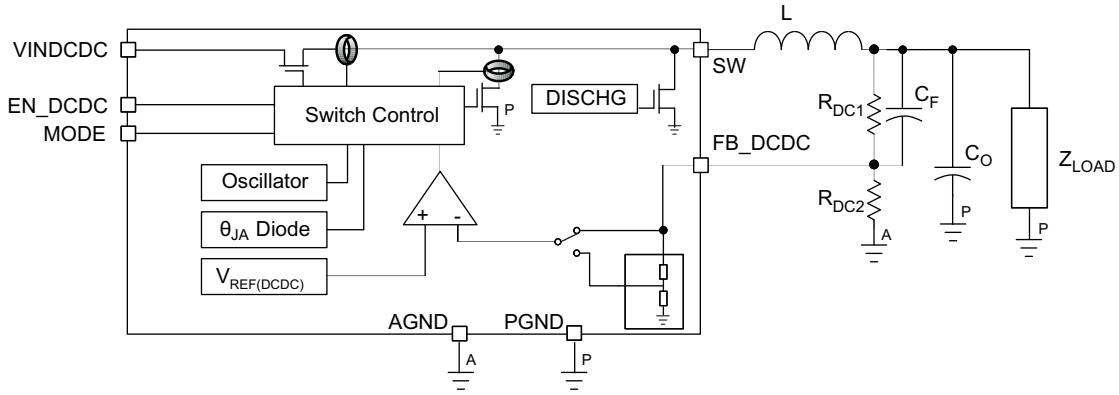

Figure 16. DC-DC Converter Block Diagram and Output Voltage Setting

The output voltage of the DC-DC converter is set by Equation 1:

$$V_{DCDC} = V_{FB_DCDC} \times \frac{(R_{DC1} + R_{DC2})}{R_{DC2}}$$

$$V_{DCDC} = 0.6V \times \frac{(R_{DC1} + R_{DC2})}{R_{DC2}} \quad (1)$$

The combined resistance of R_{DC1} and R_{DC2} should be less than 1 MΩ.

Fixed output voltages and additional current-limit options are also possible. Contact TI for further information.

The step-down converter has two modes of operation to maximize efficiency at different load conditions. At moderate to heavy load currents, the device operates in a fixed-frequency pulse-width modulation (PWM) mode that results in small output ripple and high efficiency. Pulling the MODE pin to a DC-high level results in PWM mode over the entire load range.

At light load currents, the device operates in a pulsed frequency-modulation (PFM) mode to improve efficiency. The transition to this mode occurs when the inductor current through the low-side FET becomes zero, indicating discontinuous conduction. PFM mode also results in the output voltage increasing by 1% from its nominally set value. This voltage positioning is intended to minimize both the voltage undershoot of a load step from light to heavy loads, as when a processor moves from sleep to active modes, and the voltage overshoot at load removal. Figure 17 shows the voltage positioning behavior for a light-to-heavy load step.

Feature Description (continued)

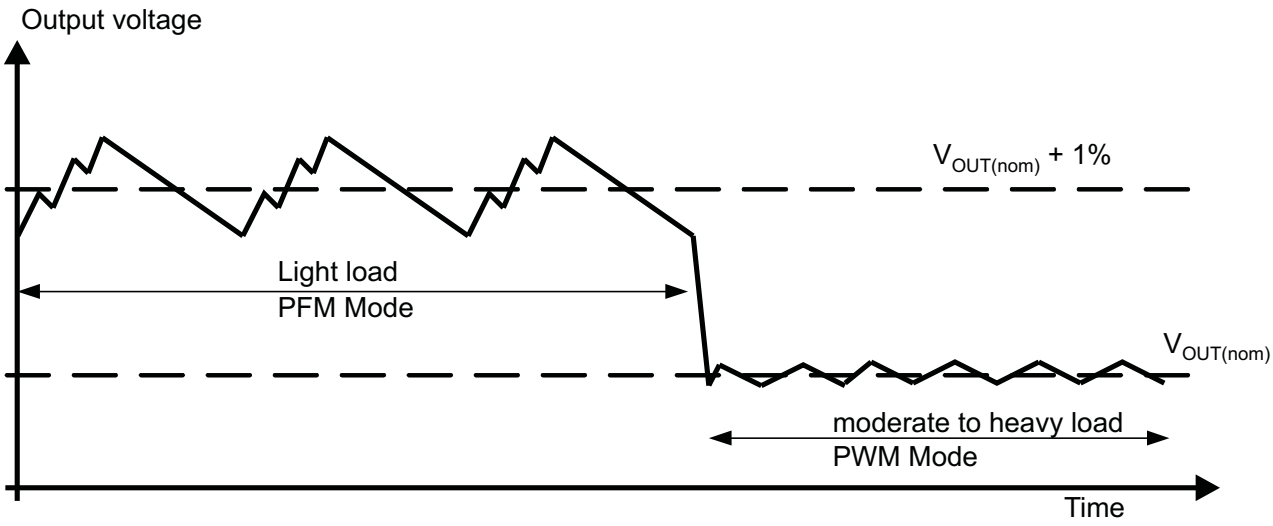

Figure 17. PFM Voltage Positioning

Pulling the MODE pin to DC ground results in an automatic transition between PFM and PWM modes to maximize efficiency.

The DC-DC converter output automatically discharges to ground through an internal 450-Ω load when EN_DCDC goes low or when the UVLO condition is met.

7.3.2 Soft Start

The step-down converter has an internal soft-start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp-up is controlled as shown in Figure 18.

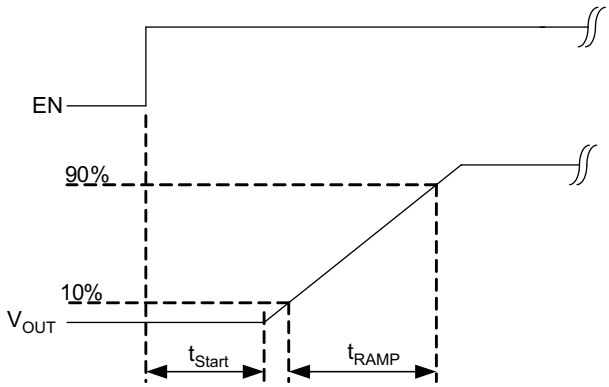

Figure 18. Soft Start

7.3.3 Linear Regulators

The two linear dropout regulators (LDOs) in the TPS65000-Q1 are designed to provide flexibility in system design. Each LDO has a separate voltage input and enable signal. The input can be tied to the output of the step-down converter or the output of another voltage source. Each LDO output discharges to ground automatically when EN_LDOx goes low.

A resistor network is needed to set the output voltage of the LDOs. Fixed-voltage output versions are also available; contact a TI sales representative for more information.

The LDOs are general-purpose devices that can handle inputs from 6 V down to 1.6 V. Figure 19 shows the necessary connections for LDO1. The same architecture applies to LDO2.

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Feature Description (continued)

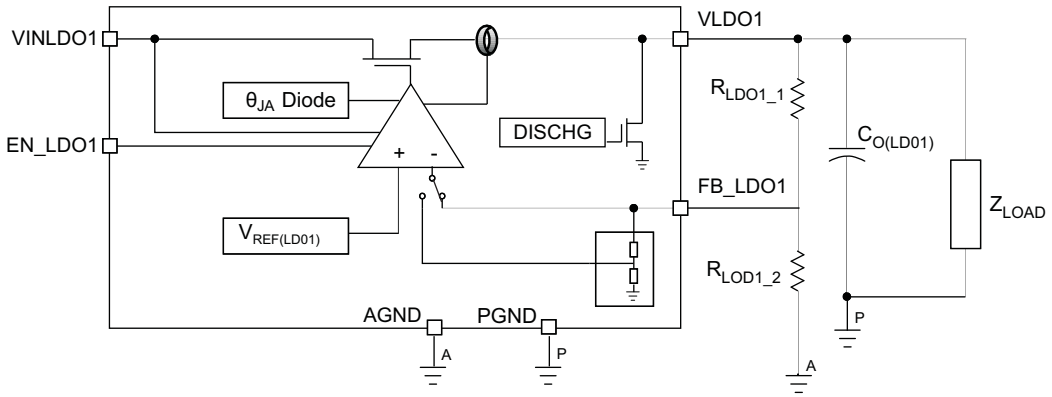

Figure 19. LDO Block Diagram and Output Voltage Setting

The output voltages of the LDOs are set by Equation 2:

$$V_{LDO1} = V_{FB_LDO1} \times \frac{\left(R_{LDO1_1} + R_{LDO1_2}\right)}{R_{LDO1_2}}$$

$$V_{LDO1} = 0.5V \times \frac{\left(R_{LDO1_1} + R_{LDO1_2}\right)}{R_{LDO1_2}} \quad (2)$$

The combined resistance of R_{LDO1_1} and R_{LDO1_2} should be less than 1 MΩ.

7.3.4 Oscillator and Spread-Spectrum Clock Generation

The TPS65000-Q1 contains an internal oscillator running at a typical frequency of 2.25 MHz. This frequency is the fundamental switching frequency of the step-down converter when it is running in PWM mode. An additional circuit in the oscillator block implements spread-spectrum clocking, which modulates the main switching frequency when the device is in PWM mode. This spread-spectrum oscillation reduces the power that may cause EMI. When viewed in the frequency domain, the SSC spreads out the frequency that may introduce interference while simultaneously reducing the power. Because the frequency is continually shifting, the amount of time the switcher spends at any single frequency is reduced. This reduction in time means that the receiver that may see the interference has less time to integrate the interference.

Different spin versions of SSC settings are also possible; contact a TI sales representative for more information.

Figure 20 and Figure 21 show the advantage of SSC with the frequency spectrum centering on the nominal frequency 2.25 MHz. The blue spectrum is the result of the spread change. As shown in the figures, the harmonic spectrum is attenuated to 10 dB, compared to the same device without SSC.

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Feature Description (continued)

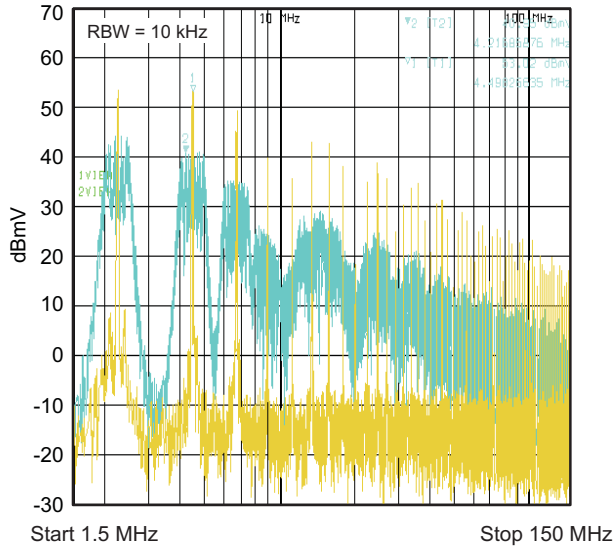

Figure 20. SSC On and Off Comparison from 1.5 MHz to 150 MHz

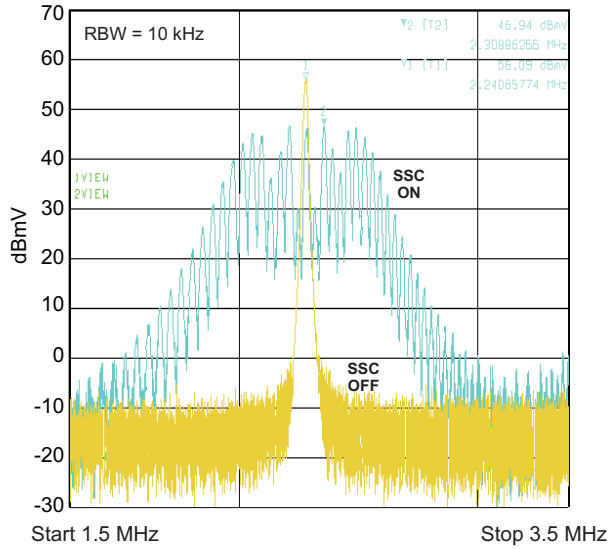

Figure 21. Zoom In of SSC On and Off Comparison from 1.5 MHz to 3.5 MHz

7.3.5 Power Good

The open-drain $\overline{PG}$ output is used to indicate the condition of the step-down converter and each LDO. This is a combined output, with the outputs being compared when the appropriate enable signal is high. The pin is pulled low when all enabled outputs are greater than 90% of the target voltage, and it is pulled into Hi-Z when an enabled output is less than 90% of its intended value or when all the enable signals are pulled low.

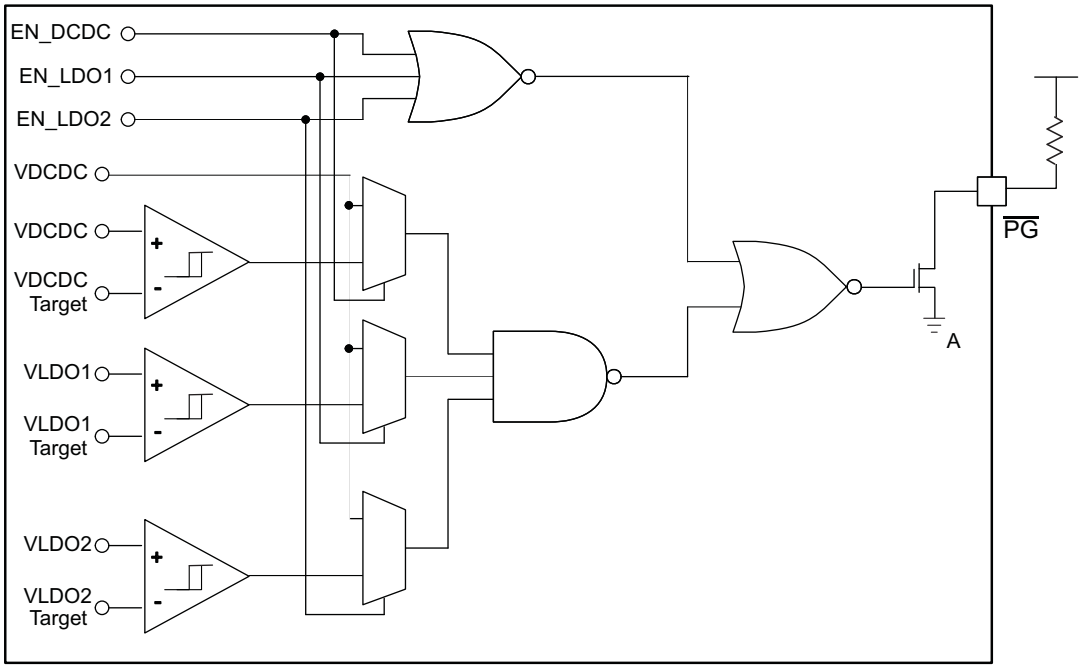

Figure 22. Power-Good Functionality

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7.4 Device Functional Modes

The step-down converter has two modes of operation to maximize efficiency:

1. PFM
   - For light loads
   - For automatic transition to between this mode and PWM mode automatically when MODE pin is pulled low over all load ranges
   - To increase in output voltage setting by 1%
   - For better accuracy
2. PWM
   - For moderate to heavy loads
   - For a small output ripple
   - For maintaining the specified switching frequency variation by pulling the MODE pin high which places the device in a forced PWM mode over the entire load range.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65000-Q1 can be used in an automotive-camera sensor module to generate the AVDD, DVDD, and IOVDD voltage rails. For noise immunity, one of the LDOs should be used to generate the AVDD voltage rail. To minimize power dissipation, the DC-DC converter should be used to power the DVDD rail because the DVDD rail normally has a lower operating voltage and higher current consumption.

8.2 Typical Application

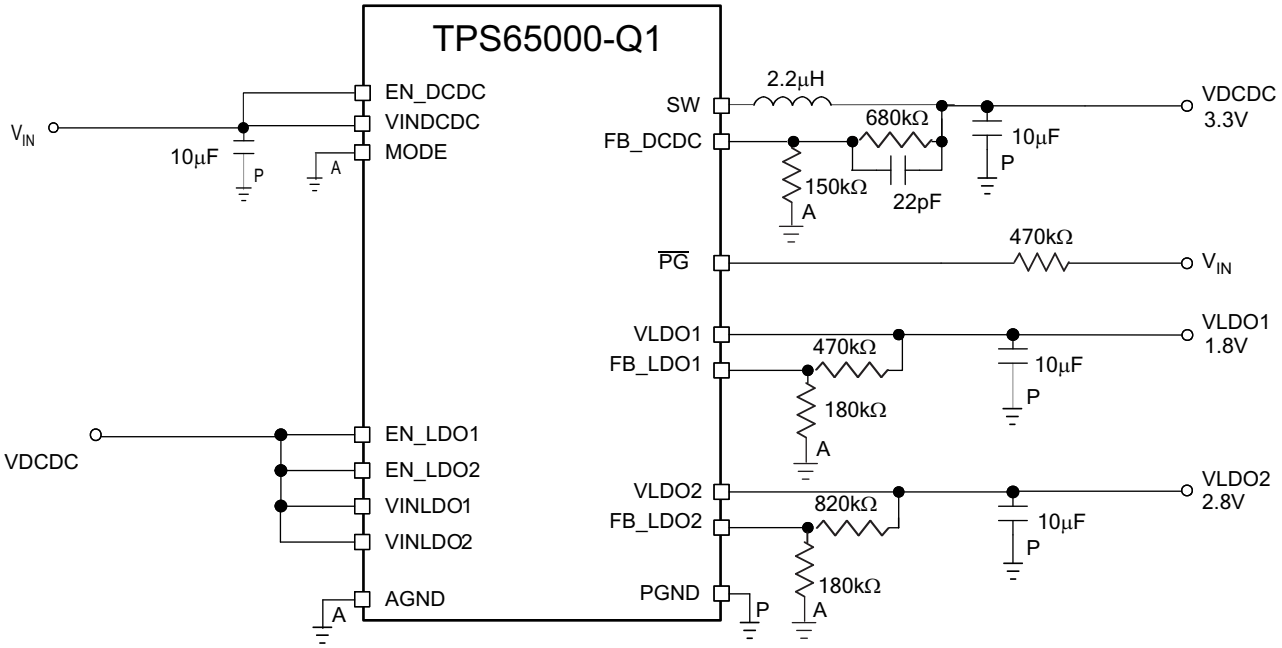

Figure 23. Typical TPS65000-Q1 Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

RESOURCES	VOLTAGE
SW	3.3 V
VLDO1	1.8 V
VLDO2	2.8 V

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8.2.2 Detailed Design Procedure

8.2.2.1 Output Filter Design (Inductor and Output Capacitor)

8.2.2.1.1 Inductor Selection

The typical value for the converter inductor is 2.2-µH output inductor. Larger or smaller inductor values in the range of 1.5 µH to 3.3 µH can optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly. An inductor with lowest DC resistance must be selected for highest efficiency. For more information on inductor selection, refer to *Choosing Inductors and Capacitors for DC/DC Converters*.

Equation 3 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. TI recommends this because during heavy load transient, the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}$$

where

- f = Switching Frequency (2.25-MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-peak Inductor Ripple Current (3)

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2}$$

where

- I_{Lmax} = Maximum Inductor Current (4)

The highest inductor current occurs at maximum V_{IN}.

Open-core inductors have a soft saturation characteristic and can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consider that the core material from inductor to inductor differs and impacts the efficiency especially at high-switching frequencies.

The step down converter has internal loop compensation. TI designed the internal loop compensation to work with a certain output filter corner frequency calculated as in Equation 5:

$$f_C = \frac{1}{2\pi \sqrt{L \times C_{OUT}}} \text{ with } L = 2.2\mu H,\ C_{OUT} = 10\mu F \quad (5)$$

The selection of external L-C filter must be coped with Equation 5. The product of L × C_{OUT} must be constant while selecting smaller inductor or increasing output capacitor value.

8.2.2.1.2 Output Capacitor Selection

The advanced fast response voltage mode control scheme of the converter allows the use of small ceramic capacitors with a typical value of 22 µF, without having large output voltage under and overshoots during heavy load transients. TI recommends ceramic capacitors with low ESR values because they result in lowest output voltage ripple. See for the TI-recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. The RMS ripple current is calculated as in Equation 6:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{6}$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor as calculated in Equation 7:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \tag{7}$$

Where the highest output voltage ripple occurs at the highest input voltage V_{IN}.

At light load currents, the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

The adjustable output voltage of the DC-DC converter is calculated by Equation 1 in the *Step-Down Converter*. To keep the external resistor divider network robust against noise, an external feed forward capacitor is required for optimum load transient response. The value of feed forward capacitor must be in the range between 22 pF and 33 pF provided the equivalent resistance of RDC1 || RDC2 in Equation 1 is approximately 300 kΩ. Scale change on RDC1||RDC2 would apply a scale change to the feed forward capacitor to keep the RC product a constant.

8.2.2.1.3 Input Capacitor Selection

Due to the DC-DC converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high-input voltage spikes . Place the input capacitor as close as possible to the VINDCDC pin with the clean GND connection. Do the same for the output capacitor and the inductor. The converters require a ceramic input capacitor of 10 µF. The input capacitor can increase without any limit for better input voltage filtering.

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8.2.3 Application Curves

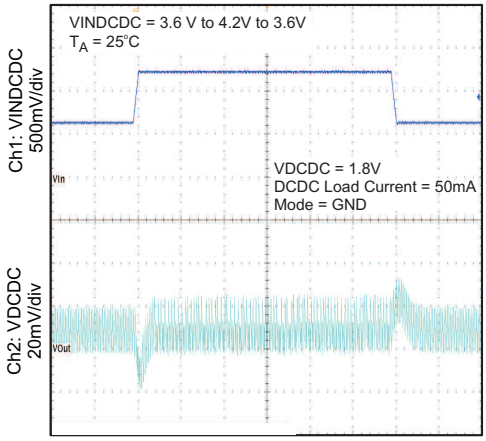

Figure 24. Line Transient Response (DC-DC PFM Mode)

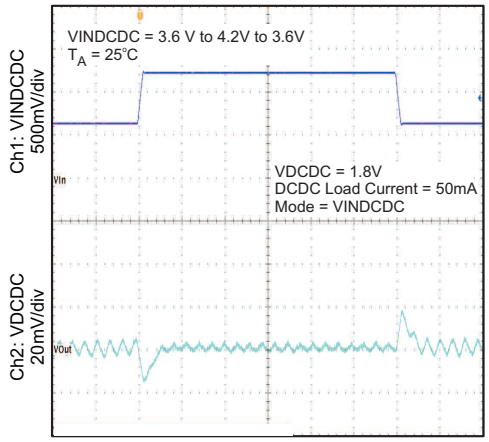

Figure 25. Line Transient Response (DC-DC PWM Mode)

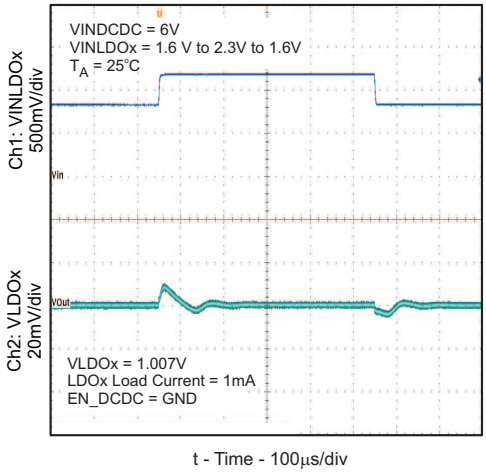

Figure 26. Line Transient Response (LDOx)

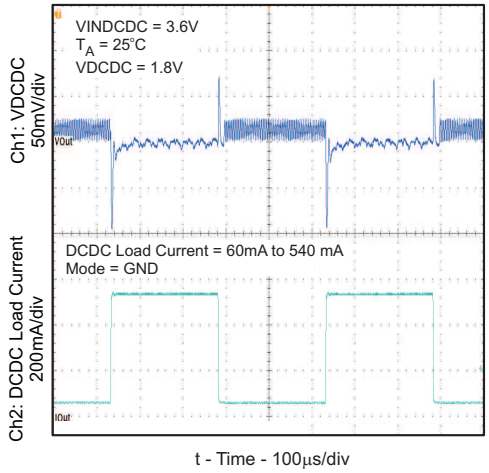

Figure 27. Load Transient Response (DC-DC PFM Mode)

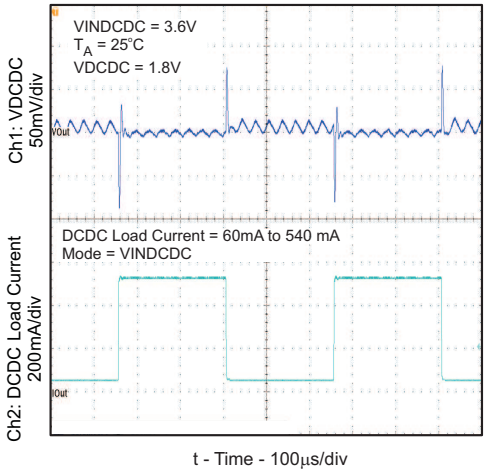

Figure 28. Load Transient Response (DC-DC PWM Mode)

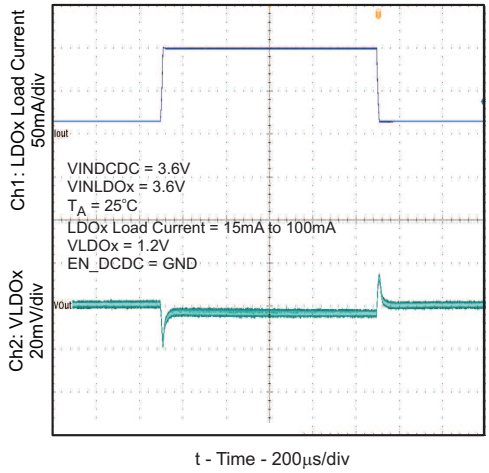

Figure 29. Load Transient Response (LDOx)

9 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 1.6 V to 6 V. This input supply can be from a DC supply, or other externally regulated supply. If the input supply is located more than a few inches from the TPS65000-Q1, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- The VINDCDC and VINLDOx pins must be bypassed to ground with a low-ESR ceramic bypass capacitor. TI recommends the typical bypass capacitance is 10 µF and 2.2 µF with a X5R dielectric.
- The optimum placement is closest to the VINDCDCx and VINLDOx pins of the device. Minimize the loop area formed by the bypass capacitor connection, the VINDCDC and VINLDO pins, and the thermal pad of the device.
- The thermal pad must be tied to the PCB ground plane with multiple vias.
- The traces of the VLDOx and VDCDCx pins (feedback pins) must be routed away from any potential noise source to avoid coupling.
- VODC output capacitance must be placed immediately at the VODC pin. Excessive distance between the capacitance and DCDCx pin may cause poor converter performance.
- AGND star back to PGND as close to the device as possible.
- DGND connect to the thermal pad

10.2 Layout Examples

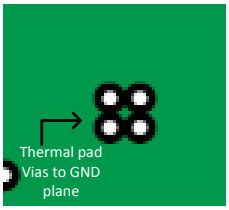

Figure 30. Layout Recommendation

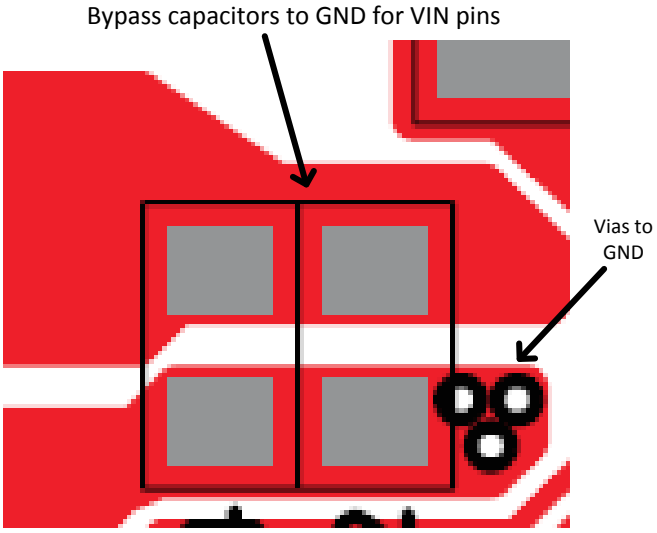

Figure 31. Bypass Capacitor and Via Placement Recommendation

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11 器件和文档支持

11.1 器件支持

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65000TRTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SJO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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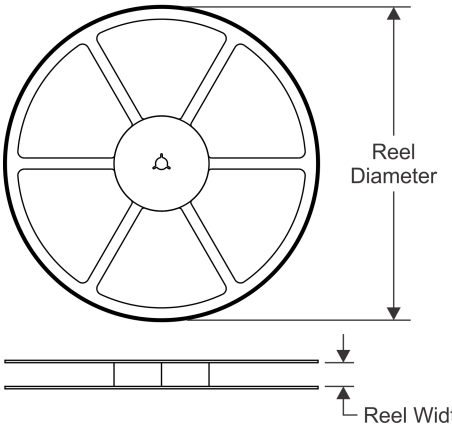
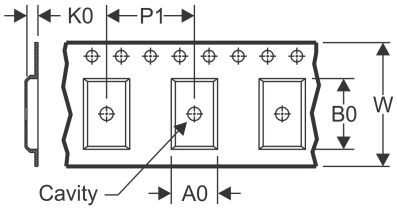
TAPE AND REEL INFORMATION

REEL DIMENSIONS

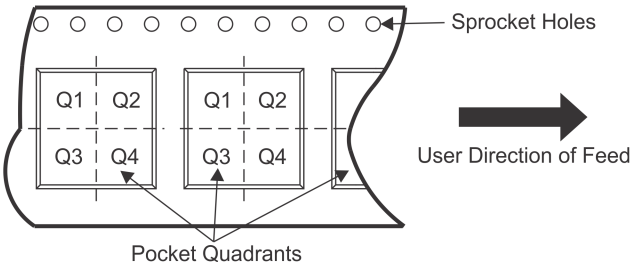


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

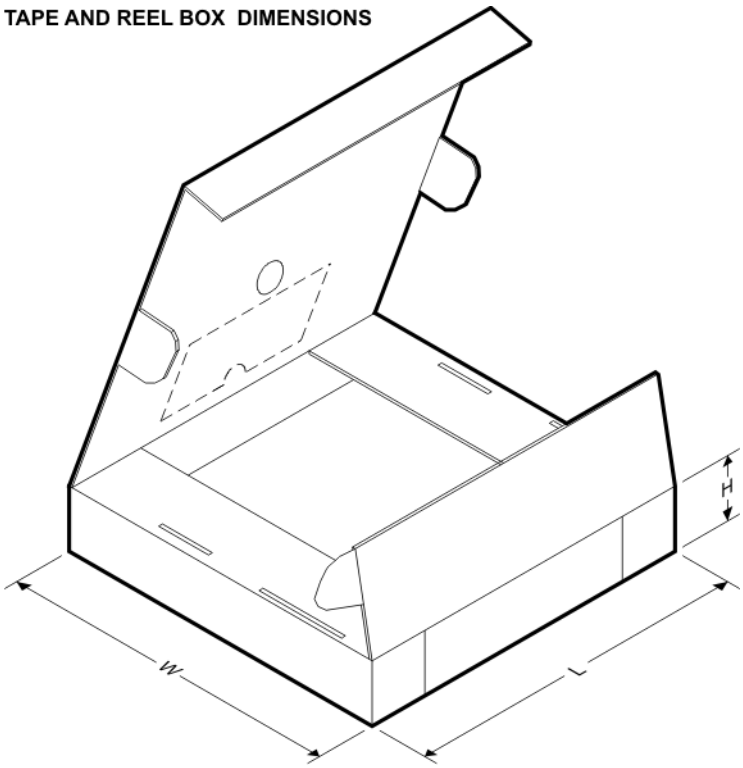
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65000TRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65000TRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

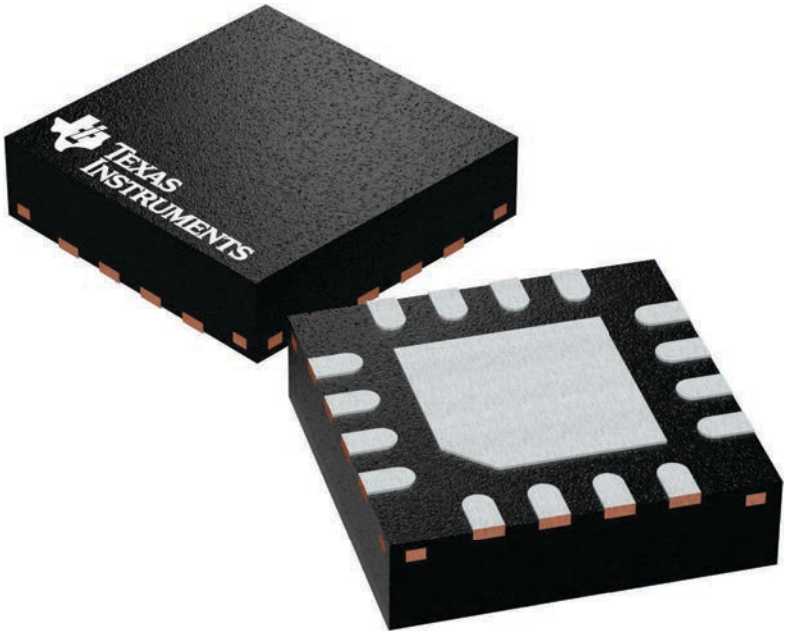
RTE 16

WQFN - 0.8 mm max height

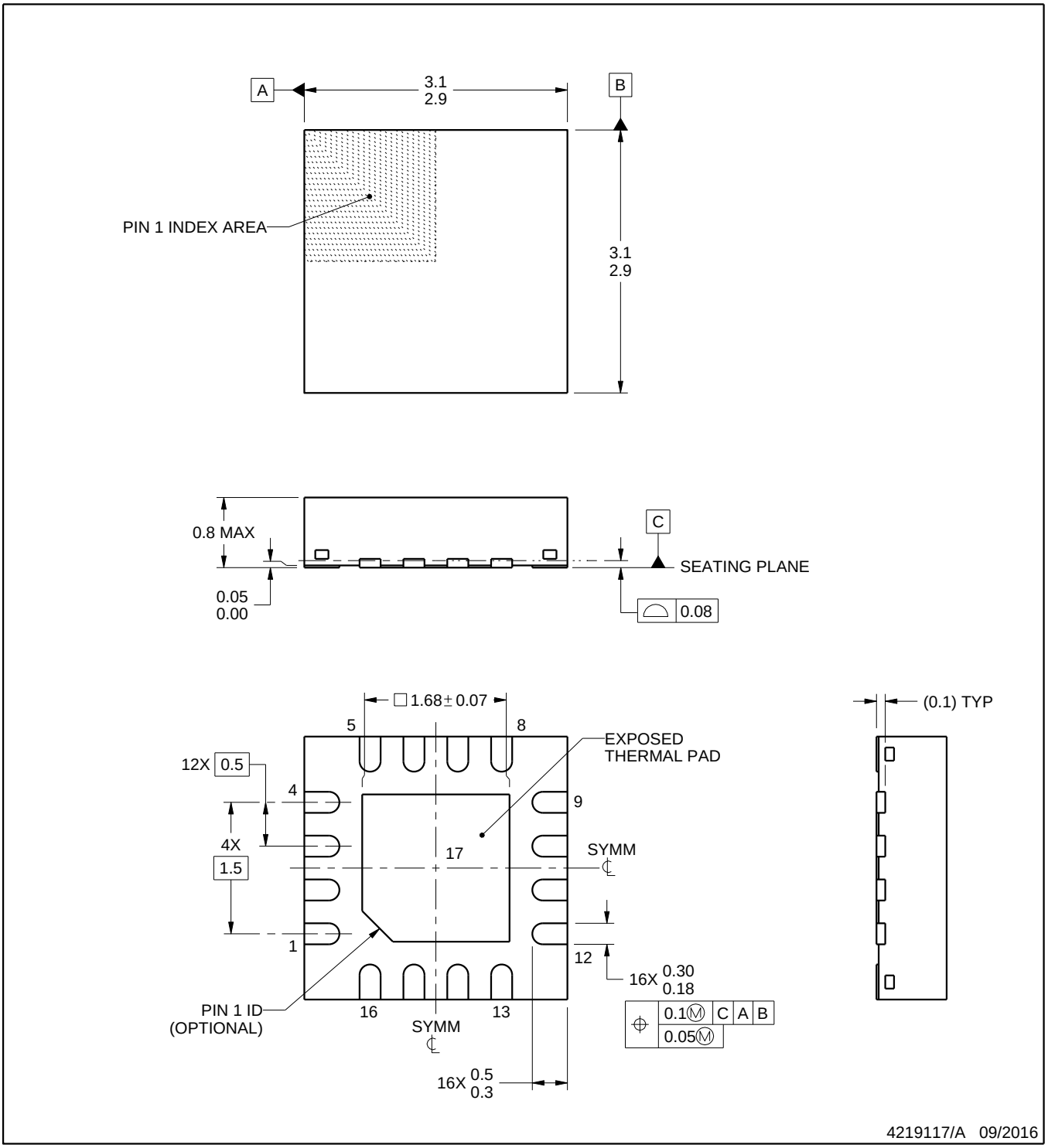
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

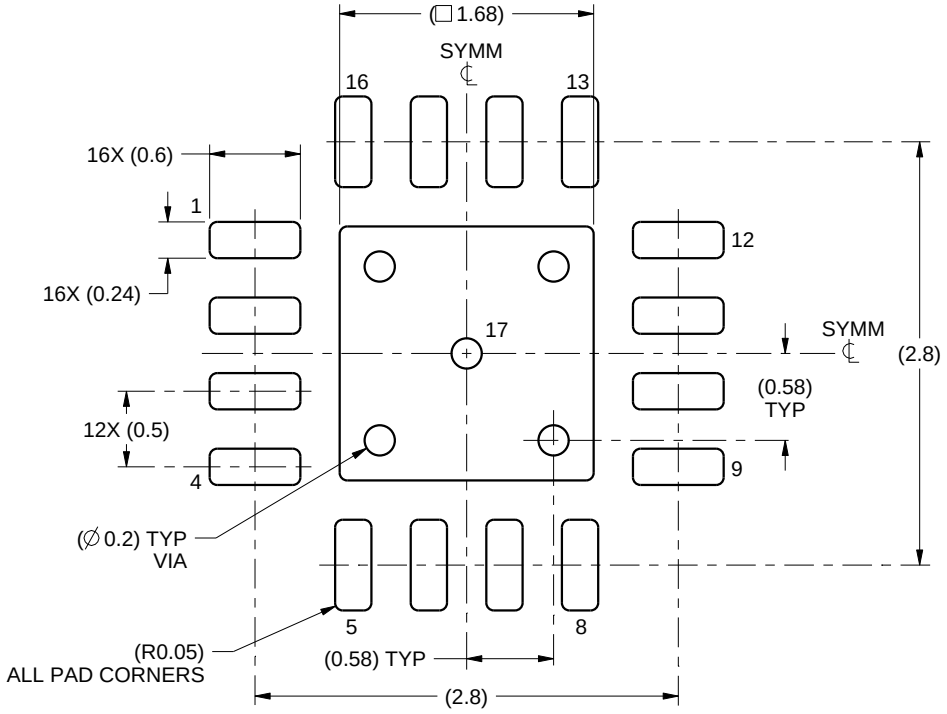


4225944/A

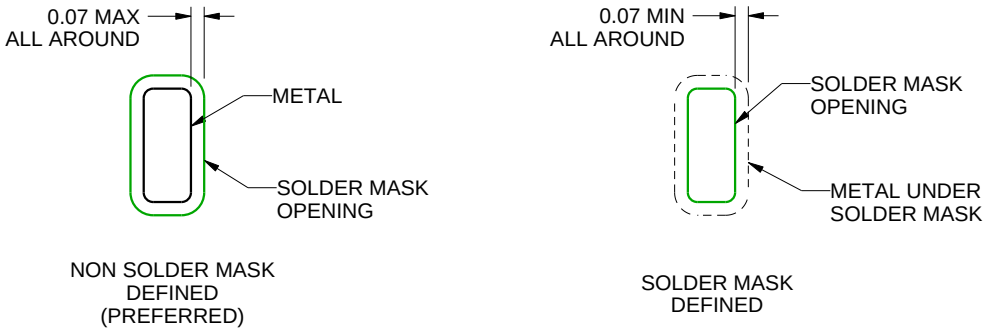


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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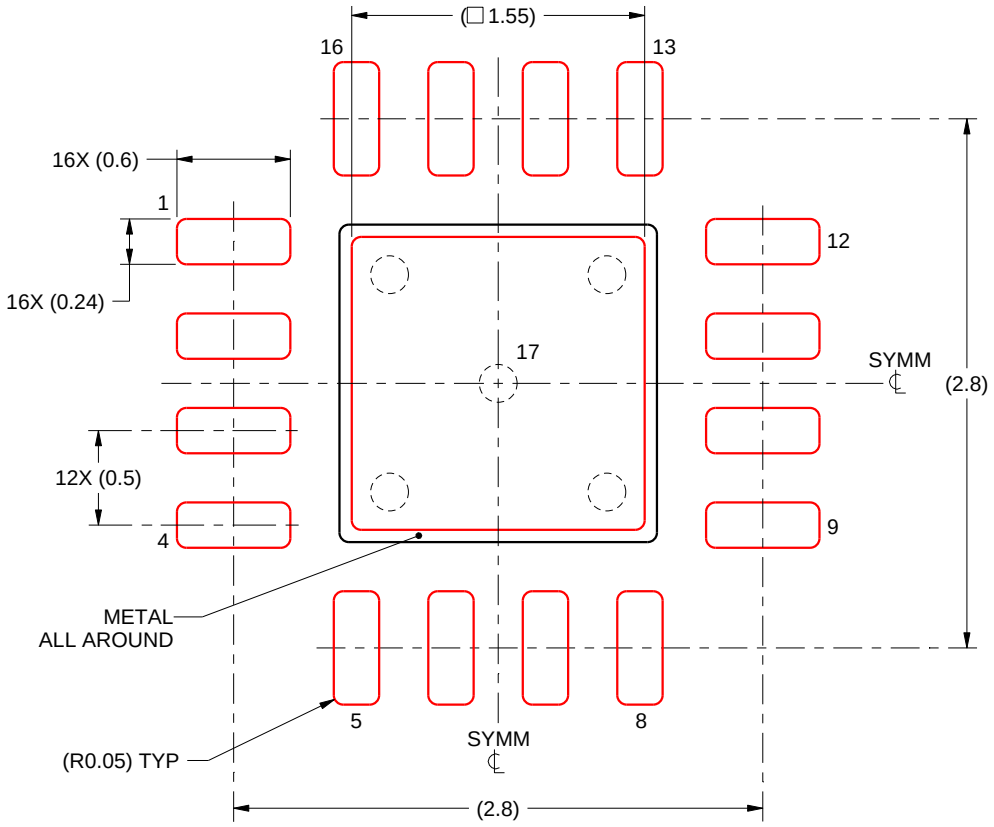
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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