

TSV91x 轨至轨输入/输出、8MHz 运算放大器

1 具有

- 轨至轨输入和输出
- 低噪声：1kHz 时为 18nV/√Hz
- 低功耗：550μA（典型值）
- 高增益带宽：8MHz
- 工作电源电压范围：2.5V 至 5.5V
- 低输入偏置电流：1pA（典型值）
- 低输入失调电压：1.9mV（最大值）
- 低偏移电压漂移：±0.5μV/°C（典型值）
- ESD 内部保护：±4kV 人体模型 (HBM)
- 扩展温度范围：-40°C 至 +125°C

2 应用

- 电池供电类 应用
- 电机控制
- 电源模块
- HVAC：采暖、通风和空调
- 洗衣机
- 冰箱
- 医疗仪器
- 有源滤波器
- 传感器信号调节
- 音频接收器
- 车用信息娱乐

3 说明

TSV91x 系列单通道、双通道和四通道运算放大器专为通用 应用。此系列器件具有轨至轨输入和输出 (RRIO) 摆幅、宽带宽 (8MHz) 和低失调电压 (0.3mV 典型值) 等特性，专为需要在速度与功耗之间实现良好平衡的各种 应用 而设计。该运算放大器单位增益稳定，具有极低输入偏置电流，这些特性使其适用于具有高源阻抗的 应用。该系列器件还具有低输入偏置电流，适用于传感器接口、电池供电和便携式 应用以及有源滤波。

TSV91x 采用稳健耐用的设计，方便电路设计人员使用。特性 包括具有单位增益稳定的集成 RFI-EMI 抑制滤波器，在过驱条件下不会出现反相，以及具有高静电放电 (ESD) 保护 (4kV HBM)。

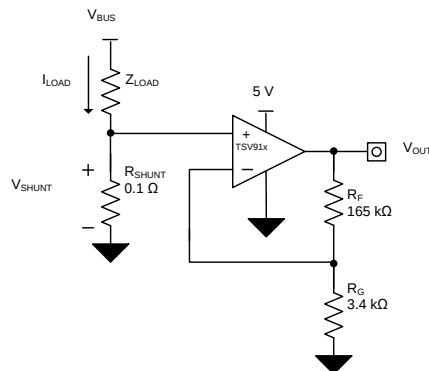
器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TSV911	SOT-23 (5) ⁽²⁾	1.60mm × 2.90mm
TSV912	SOIC (8)	3.91mm × 4.90mm
	WSOIC (8)	2.00mm × 2.00mm
TSV914	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	4.40mm × 5.00mm

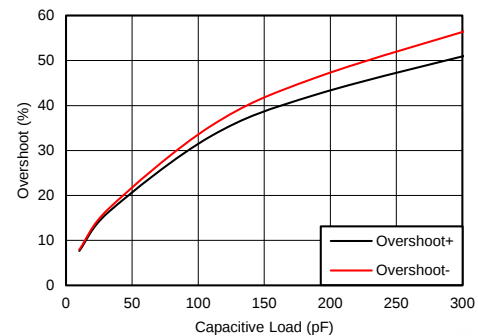
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装仅为预览版。

低侧电机控制



小信号过冲与负载电容间的关系



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4 修订历史记录

Changes from Revision A (October 2017) to Revision B	Page
• 已更改 在器件信息 表格中将 TSV914 14 引脚 TSSOP 封装从预览更改为生产数据	1
• 已删除 器件信息 表格中 8 引脚 WSON 封装的封装预览说明	1
• Deleted 删除了器件比较 表中 PW (TSSOP) 封装的封装预览说明	3
• Deleted 删除了器件比较 表中 DSG (WSON) 封装的封装预览说明	3
• Deleted 删除了引脚配置和功能 部分中 TSV912 DSG 封装引脚图中的封装预览说明	5
• Added 将 DGK (VSSOP) 热性能信息添加到热性能信息: TSV912 表中	8
• Deleted 删除了热性能信息 表中 TSV914 PW (TSSOP) 封装的封装预览说明	8
• Added 将 PW (TSSOP) 封装信息添加到热性能信息: TSV914 表中	8
• Changed 将 TSV914 PW (TSSOP) 结至环境热阻从 135.8°C/W 更改为 205.8°C/W	8
• Changed 将 TSV914 PW (TSSOP) 结至外壳 (顶部) 热阻从 64°C/W 更改为 106.7°C/W	8
• Changed 将 TSV914 PW (TSSOP) 结至电路板热阻从 79°C/W 更改为 133.9°C/W	8
• Changed 将 TSV914 PW (TSSOP) 结至顶部特征参数从 15.7°C/W 更改为 34.4°C/W	8
• Changed 将 TSV914 PW (TSSOP) 结至电路板特征参数从 78.4°C/W 更改为 132.6°C/W	8

Changes from Original (July 2017) to Revision A	Page
• 已更改 在器件信息 表格中将 TSV914 14 引脚 SOIC 封装从预览更改为生产数据	1
• 已删除 器件信息 表格中的 TSV911 SC70、SOT-553 和 SOIC 封装	1
• 已删除 器件信息 表格中的 TSV912 VSSOP 封装	1
• Deleted 删除了引脚图和引脚功能 表	4
• Deleted 删除了引脚图像和引脚功能 表	5
• Deleted 删除了 TSV914 引脚图和引脚功能 表中的封装预览说明	6
• Added 添加了 TSV914 热性能信息 表	8
• 已添加 在图 35 中添加了 2017 年版权声明	19

5 器件比较表

器件	通道数	封装引线			
		DBV ⁽¹⁾	D	DSG	PW
TSV911 ⁽²⁾	1	5	—	—	—
TSV912	2	—	8	8	—
TSV914	4	—	14	—	14

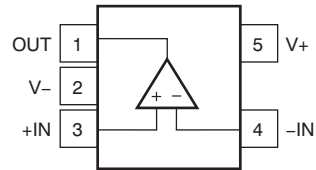
(1) 封装预览

(2) 器件预览

中的 TSV911 SC70 和 SOIC 封装

6 引脚配置和功能

TSV911 DBV 封装 ⁽¹⁾
5 引脚 SOT-23
俯视图



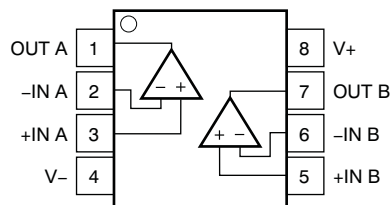
(1) 封装预览

引脚功能：TSV911

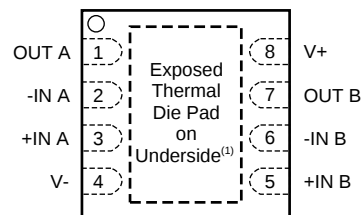
引脚		I/O	说明
名称	编号		
-IN	4	I	反相输入
+IN	3	I	同相输入
OUT	1	O	输出
V-	2	—	负 (最低) 电源或接地 (对于单电源供电)
V+	5	—	正 (最高) 电源

中的 TSV912 DGK 和 DGS 封装

TSV912 D, DGK 封装 ⁽¹⁾
8 引脚 SOIC、VSSOP
俯视图



TSV912 DSG 封装
带有外露散热焊盘的 8 引脚 WSON 封装
俯视图



引脚功能：TSV912

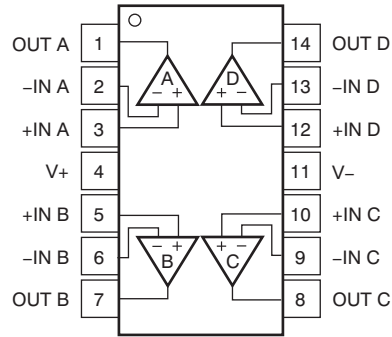
引脚		I/O	说明
名称	编号		
-IN A	2	I	反相输入，通道 A
+IN A	3	I	同相输入，通道 A
-IN B	6	I	反相输入，通道 B
+IN B	5	I	同相输入，通道 B
OUT A	1	O	输出，通道 A
OUT B	7	O	输出，通道 B
V-	4	—	负（最低）电源或接地（对于单电源供电）
V+	8	—	正（最高）电源

TSV911, TSV912, TSV914

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**TSV914 D、PW 封装
14 引脚 SOIC、TSSOP
俯视图**



引脚功能：TSV914

引脚		I/O	说明
名称	编号		
-IN A	2	I	反相输入，通道 A
+IN A	3	I	同相输入，通道 A
-IN B	6	I	反相输入，通道 B
+IN B	5	I	同相输入，通道 B
-IN C	9	I	反相输入，通道 C
+IN C	10	I	同相输入，通道 C
-IN D	13	I	反相输入，通道 D
+IN D	12	I	同相输入，通道 D
OUT A	1	O	输出，通道 A
OUT B	7	O	输出，通道 B
OUT C	8	O	输出，通道 C
OUT D	14	O	输出，通道 D
V-	11	—	负（最低）电源或接地（对于单电源供电）
V+	4	—	正（最高）电源

7 规格

7.1 绝对最大额定值

在自然通风温度下测得（除非另有说明）⁽¹⁾

			最小值	最大值	单位
电源电压			6		V
信号输入引脚	电压 ⁽²⁾	共模	(V-) - 0.5	(V+) + 0.5	V
		差模	(V+) - (V-) + 0.2		
	电流 ⁽²⁾			-10	10
输出短路 ⁽³⁾			连续		mA
额定温度, T _A			-40	125	°C
结温, T _J			150		
贮存温度, T _{stg}			-65	150	

(1) 应力超出“绝对最大额定值”下列出的值可能会对器件造成永久损坏。这些列出的值仅仅是极端条件下的应力额定值，并不表示器件在这些条件下以及在“建议运行条件”以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。

(2) 输入引脚被二极管钳制至电源轨。对于摆幅能超过电源轨 0.5V 的输入信号，应将其电流限制在 10mA 或者更低。

(3) 对地短路，每个封装对应一个放大器。

7.2 ESD 额定值

在自然通风温度范围内测得（除非另有说明）

		值	单位
$V_{(ESD)}$ 静电释放	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101 ⁽²⁾	±1500	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。

(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

7.3 建议运行条件

在自然通风温度范围内测得（除非另有说明）

		最小值	最大值	单位
V_S	电源电压	2.5	5.5	V
	额定温度范围	-40	125	°C

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7.4 热性能信息：TSV912

热指标 ⁽¹⁾	TSV912			单位
	D (SOIC)	DGK (VSSOP)	DSG (WSON)	
	8 引脚	8 引脚	8 引脚	
$R_{\theta JA}$ 结至环境热阻	157.6	201.2	94.4	°C/W
$R_{\theta JC(top)}$ 结至外壳 (顶部) 热阻	104.6	85.7	116.5	°C/W
$R_{\theta JB}$ 结至电路板热阻	99.7	122.9	61.3	°C/W
Ψ_{JT} 结至顶部特征参数	55.6	21.2	13	°C/W
Ψ_{JB} 结至电路板特征参数	99.2	121.4	61.7	°C/W
$R_{\theta JC(bot)}$ 结至外壳 (底部) 热阻	不适用	不适用	34.4	°C/W

(1) 有关传统和新热指标的更多信息，请参阅应用报告《[半导体和 IC 封装热指标](#)》。

7.5 热性能信息：TSV914

热指标 ⁽¹⁾	TSV914		单位
	D (SOIC)	PW (TSSOP)	
	14 引脚	14 引脚	
$R_{\theta JA}$ 结至环境热阻	106.9	205.8	°C/W
$R_{\theta JC(top)}$ 结至外壳 (顶部) 热阻	69	106.7	°C/W
$R_{\theta JB}$ 结至电路板热阻	63	133.9	°C/W
Ψ_{JT} 结至顶部特征参数	25.9	34.4	°C/W
Ψ_{JB} 结至电路板特征参数	62.7	132.6	°C/W

(1) 有关传统和新热指标的更多信息，请参阅应用报告《[半导体和 IC 封装热指标](#)》。

7.6 电气特性： V_S (总电源电压) = $(V+) - (V-) = 2.5V$ 至 $5.5V$

 $T_A = 25^\circ C$, $R_L = 10k\Omega$ (连接至 $V_S / 2$), $V_{CM} = V_S / 2$, 且 $V_{OUT} = V_S / 2$ (除非另有说明)

参数		测试条件		最小值	典型值	最大值	单位
失调电压							
V _{OS}	输入失调电压	V _S = 5V		±0.3		±1.5	mV
		V _S = 5V T _A = −40°C 至 +125°C				±3	
dV _{OS} /dT	漂移	V _S = 5V T _A = −40°C 至 +125°C		±0.5			μV/°C
PSRR	电源抑制比	V _S = 2.5V – 5.5V, V _{CM} = (V−)		±7			μV/V
	通道分离, 直流	直流时		100			dB
输入电压范围							
V _{CM}	共模电压范围	V _S = 2.5V 至 5.5V		(V−) − 0.1		(V+)+0.1	V
CMRR	共模抑制比	V _S = 5.5V (V−) − 0.1V < V _{CM} < (V+) − 1.4V T _A = −40°C 至 +125°C		80	103		dB
		V _S = 5.5V, V _{CM} = −0.1V 至 5.6V T _A = −40°C 至 +125°C		57	87		
		V _S = 2.5V, (V−) − 0.1V < V _{CM} < (V+) − 1.4V T _A = −40°C 至 +125°C			88		
		V _S = 2.5V, V _{CM} = −0.1V 至 1.9V T _A = −40°C 至 +125°C			81		
输入偏置电流							
I _B	输入偏置电流			±1			pA
I _{OS}	输入失调电流			±0.05			pA
噪声							
E _n	输入电压噪声 (峰峰值)	V _S = 5V, f = 0.1Hz 至 10Hz		4.77			μV _{PP}
e _n	输入电压噪声密度	V _S = 5V, f = 10kHz		12			nV/√Hz
		V _S = 5V, f = 1kHz		18			nV/√Hz
i _n	输入电流噪声密度	f = 1kHz		10			fA/√Hz
输入电容							
C _{ID}	差分			2			pF
C _{IC}	共模			4			pF
开环增益							
A _{OL}	开环电压增益	V _S = 2.5V, (V−) + 0.04V < V _O < (V+) − 0.04V R _L = 10kΩ		100			dB
		V _S = 5.5V, (V−) + 0.05V < V _O < (V+) − 0.05V R _L = 10kΩ		104	130		
		V _S = 2.5V, (V−) + 0.06V < V _O < (V+) − 0.06V R _L = 2kΩ		100			
		V _S = 5.5V, (V−) + 0.15V < V _O < (V+) − 0.15V R _L = 2kΩ		130			
频率响应							
GBP	增益带宽积	V _S = 5V, G = 1		8			MHz
φ _m	相位裕度	V _S = 5V, G = 1		55			度
SR	压摆率	V _S = 5V, G = 1 R _L = 2kΩ C _L = 100pF		4.5			V/μs
t _S	建立时间	精度达到 0.1%, V _S = 5V, 2V 阶跃, G = 1 C _L = 100pF		0.5			μs
		精度达到 0.01%, V _S = 5V, 2V 阶跃, G = 1 C _L = 100pF		1			
t _{OR}	过载恢复时间	V _S = 5V, V _{IN} × 增益 > V _S		0.2			μs
THD + N	总谐波失真 + 噪声 ⁽¹⁾	V _S = 5V, V _O = 1V _{RMS} , G = 1, f = 1kHz		0.0008%			
输出							
V _O	相对于电源轨的电压输出摆幅	V _S = 5.5V, R _L = 10kΩ		15			mV
		V _S =5.5V, R _L =2kΩ		50			

(1) 三阶滤波器；-3dB 时的带宽 = 80kHz。

TSV911, TSV912, TSV914

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电气特性： V_S (总电源电压) = (V+) – (V–) = 2.5V 至 5.5V (continued)
 $T_A = 25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ (连接至 $V_S / 2$) , $V_{CM} = V_S / 2$, 且 $V_{OUT} = V_S / 2$ (除非另有说明)

参数		测试条件	最小值	典型值	最大值	单位
I_{SC}	短路电流	$V_S = 5\text{V}$		± 50		mA
Z_O	开环输出阻抗	$V_S = 5\text{V}$, $f = 10\text{MHz}$		100		Ω
电源						
I_Q	每个放大器的静态电流	$V_S = 5.5\text{V}$, $I_O = 0\text{mA}$		550	750	μA
		$V_S = 5.5\text{V}$, $I_O = 0\text{mA}$, $T_A = -40^\circ\text{C}$ 至 $+125^\circ\text{C}$			1100	

7.7 典型特性

$T_A = 25^\circ\text{C}$ 时, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ 连接至 $V_S / 2$, $V_{CM} = V_S / 2$, 且 $V_{OUT} = V_S / 2$ (除非另有说明)

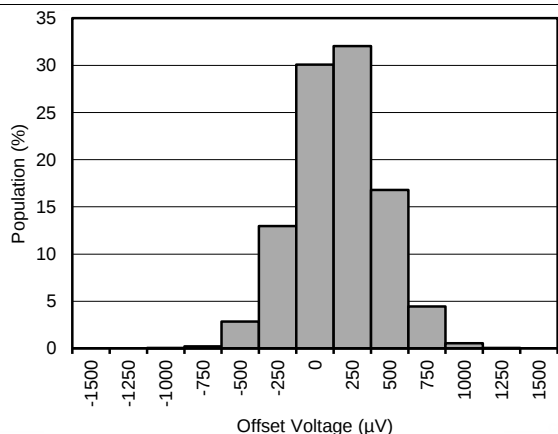
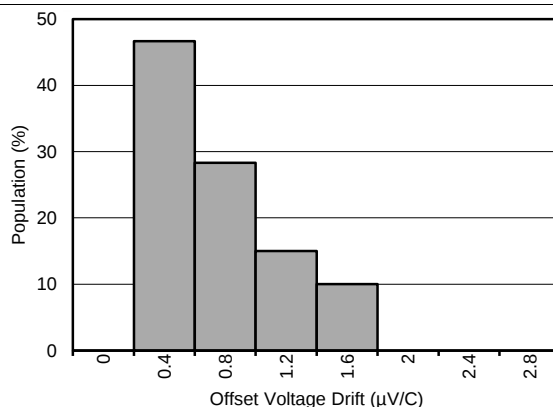


图 1. 失调电压产生分布



$T_A = -40^\circ\text{C}$ 至 $+125^\circ\text{C}$

图 2. 失调电压漂移分布

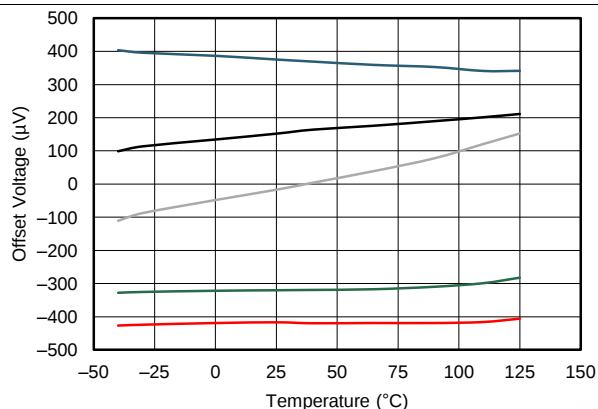
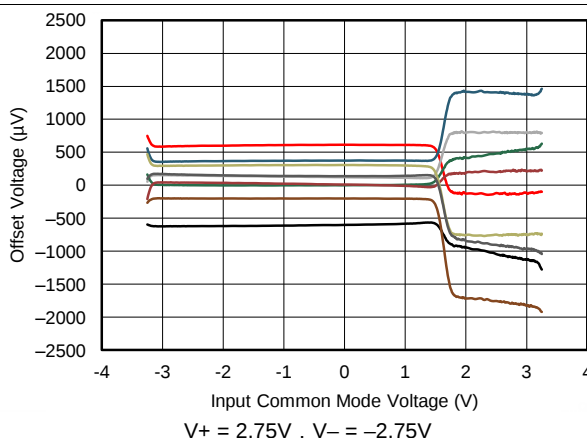
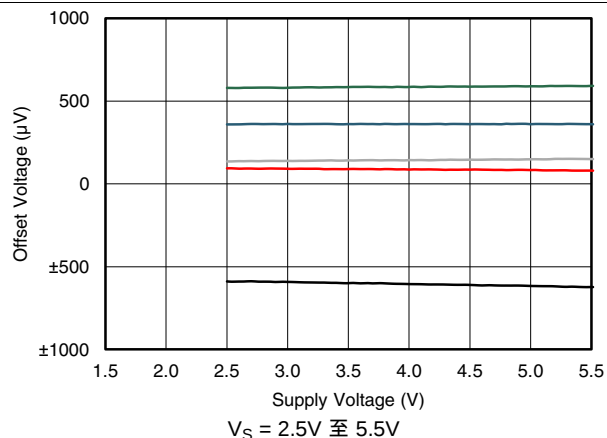


图 3. 失调电压与温度间的关系



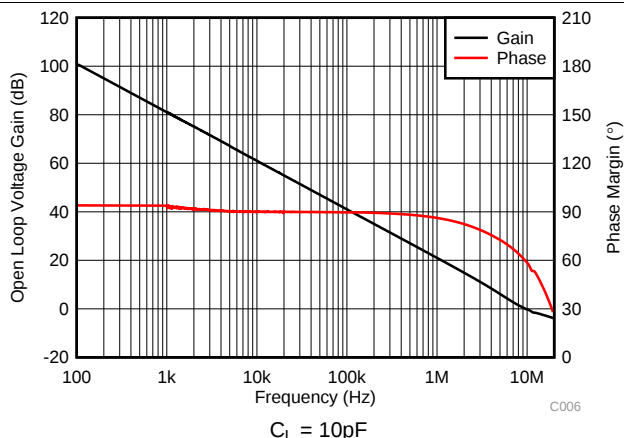
$V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$

图 4. 失调电压与共模电压间的关系



$V_S = 2.5\text{V}$ 至 5.5V

图 5. 失调电压与电源间的关系



$C_L = 10\text{pF}$

图 6. 开环增益和相位与频率间的关系

典型特性 (接下页)

$T_A = 25^\circ\text{C}$ 时, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ 连接至 $V_S / 2$, $V_{CM} = V_S / 2$, 且 $V_{OUT} = V_S / 2$ (除非另有说明)

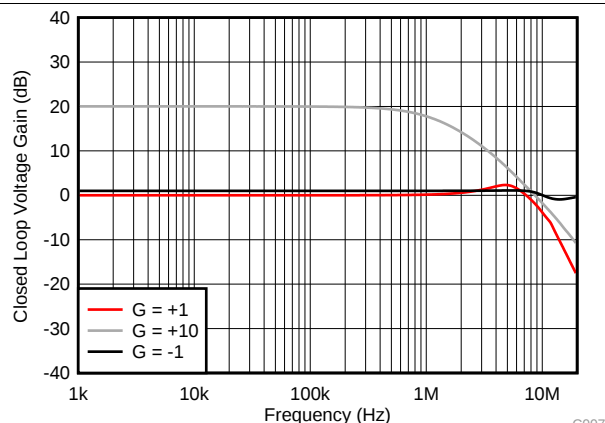


图 7. 闭环增益与频率间的关系

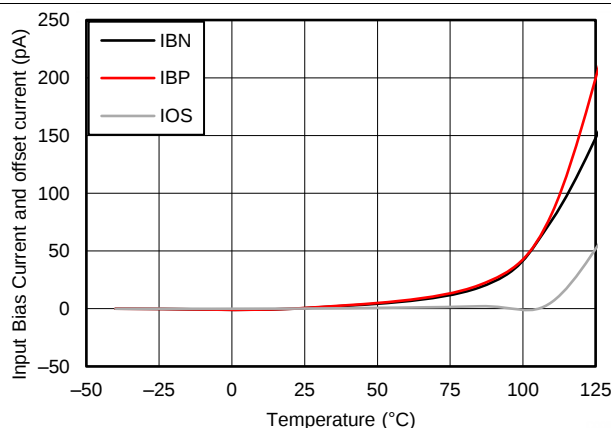


图 8. 输入偏置电流与温度间的关系

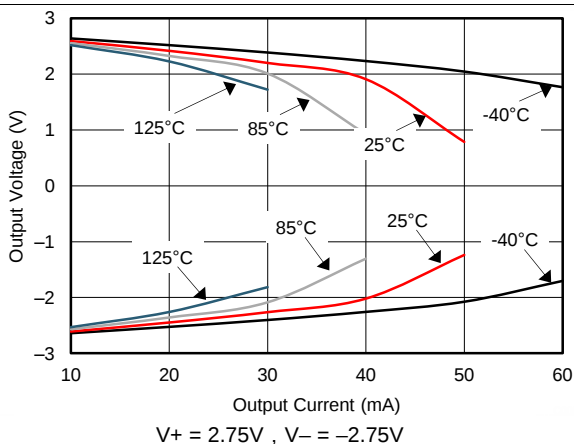


图 9. 输出电压摆幅与输出电流间的关系

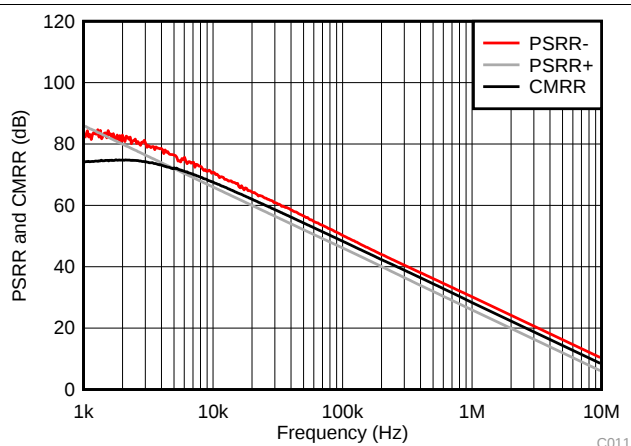


图 10. CMRR 和 PSRR 与频率间的关系
(以输入为参考)

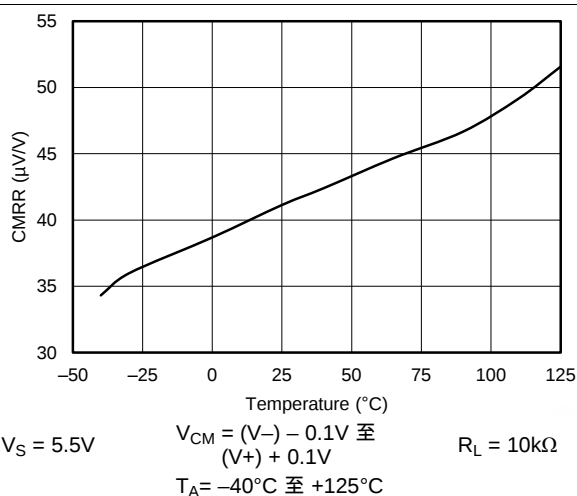


图 11. CMRR 与温度间的关系

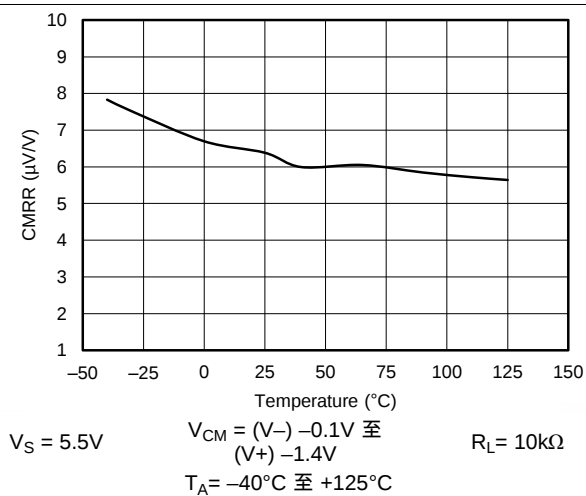


图 12. CMRR 与温度间的关系

典型特性 (接下页)

$T_A = 25^\circ\text{C}$ 时, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ 连接至 $V_S / 2$, $V_{CM} = V_S / 2$, 且 $V_{OUT} = V_S / 2$ (除非另有说明)

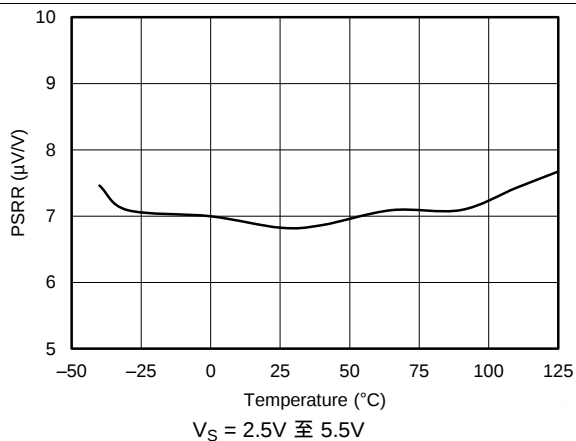


图 13. PSRR 与温度间的关系

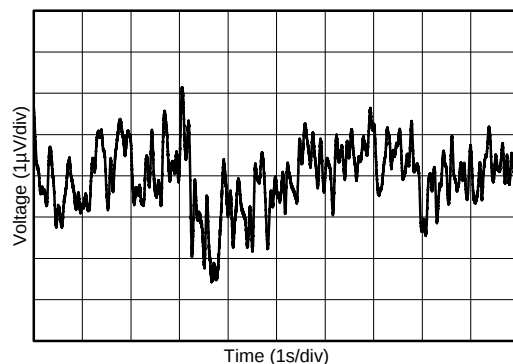


图 14. 0.1Hz 至 10Hz 输入电压噪声

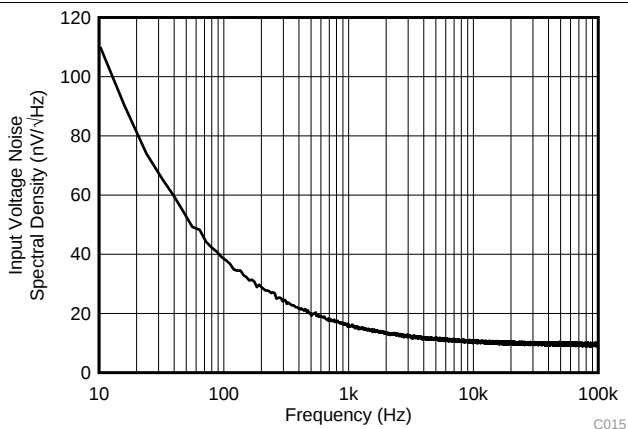


图 15. 输入电压噪声频谱密度与频率间的关系

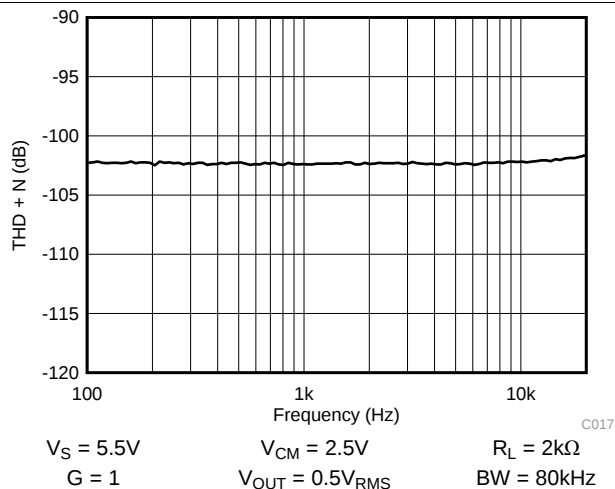


图 16. THD + N 与频率间的关系

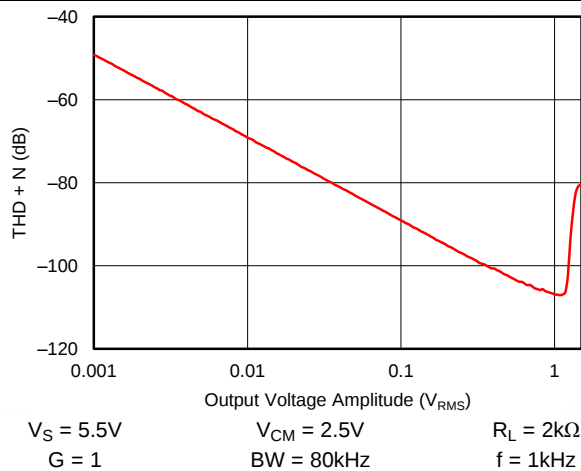


图 17. THD + N 与幅度间的关系

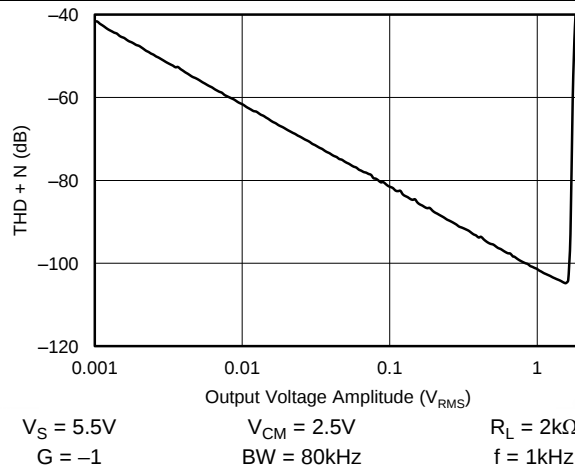


图 18. THD + N 与幅度间的关系

典型特性 (接下页)

$T_A = 25^\circ\text{C}$ 时, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ 连接至 $V_S / 2$, $V_{CM} = V_S / 2$, 且 $V_{OUT} = V_S / 2$ (除非另有说明)

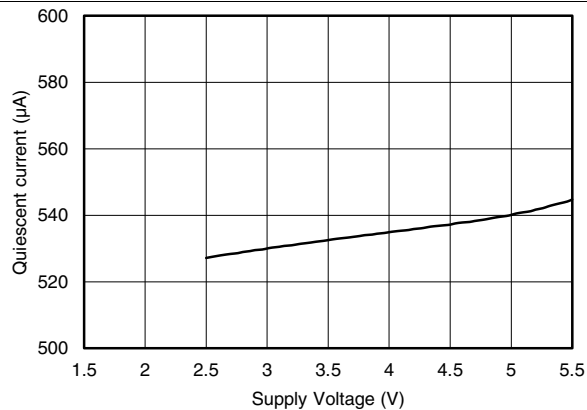


图 19. 静态电流与电源电压间的关系

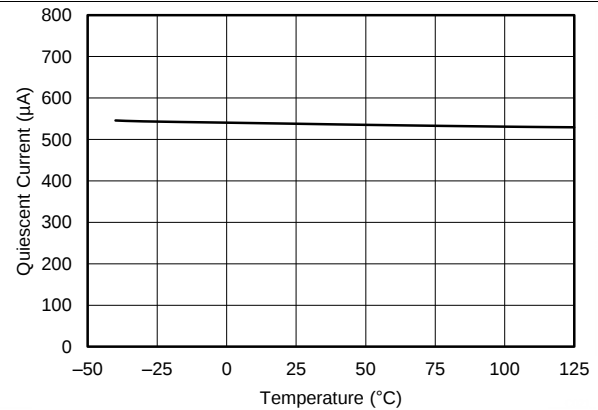


图 20. 静态电流与温度间的关系

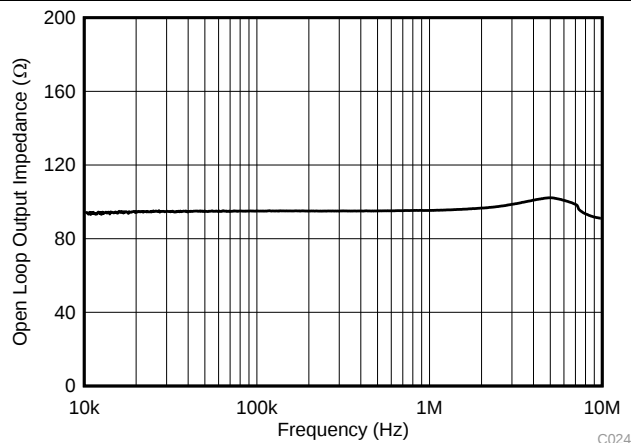


图 21. 开环输出阻抗与频率间的关系

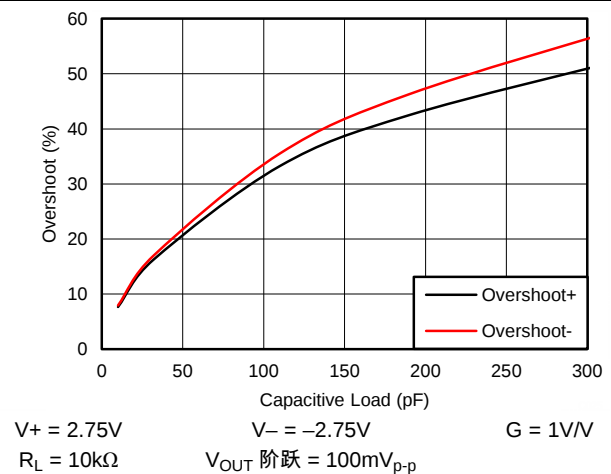


图 22. 小信号过冲与负载电容间的关系

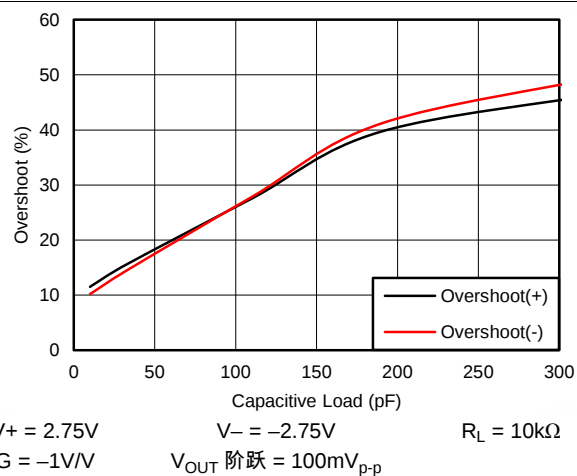


图 23. 小信号过冲与负载电容间的关系

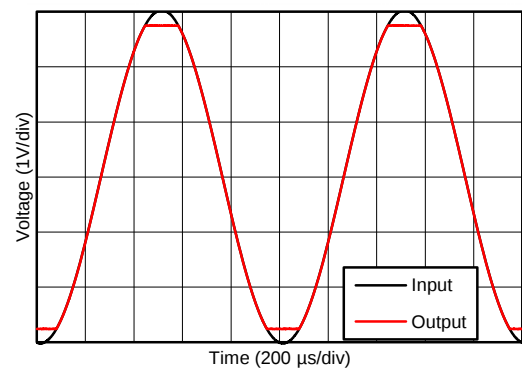
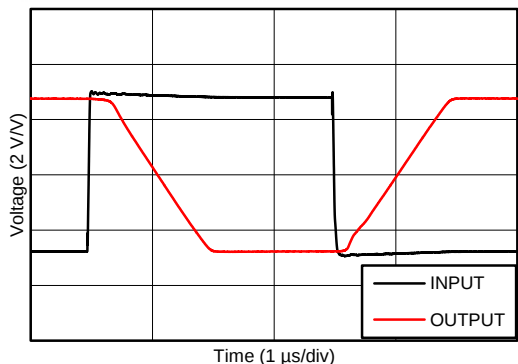


图 24. 无相位反转

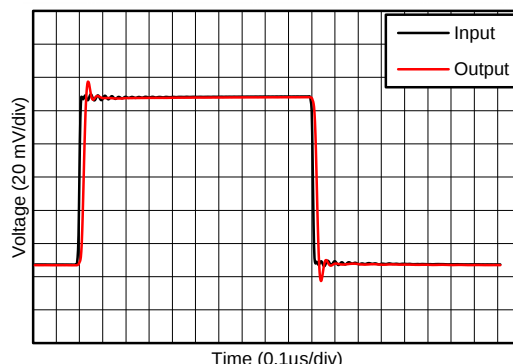
典型特性 (接下页)

$T_A = 25^\circ\text{C}$ 时, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ 连接至 $V_S / 2$, $V_{CM} = V_S / 2$, 且 $V_{OUT} = V_S / 2$ (除非另有说明)



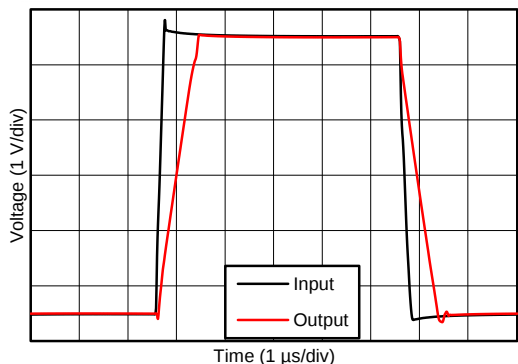
$V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $G = -10\text{V/V}$

图 25. 过载恢复



$V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $G = 1\text{V/V}$

图 26. 小信号阶跃响应



$V_+ = 2.75\text{V}$ $V_- = -2.75\text{V}$ $C_L = 100\text{pF}$
 $G = 1\text{V/V}$

图 27. 大信号阶跃响应

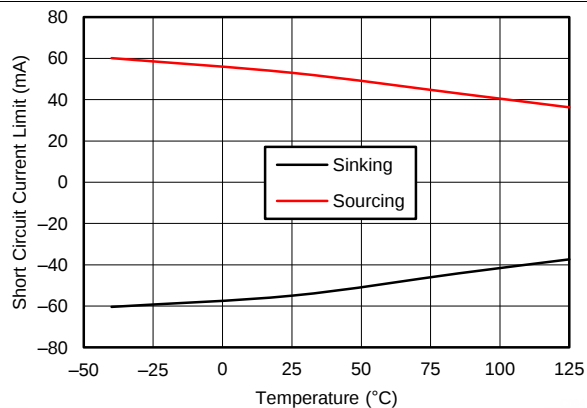


图 28. 短路电流与温度间的关系

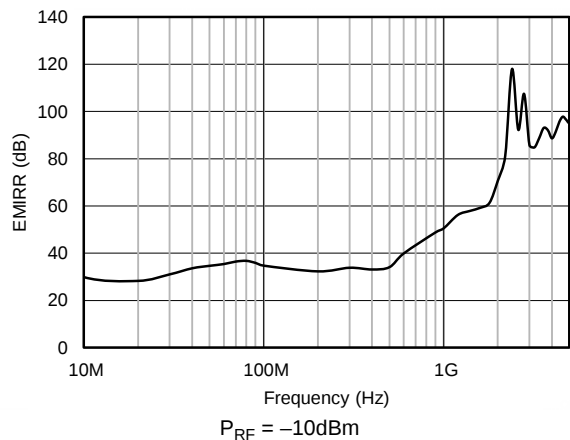


图 29. 以同相输入为参考的电磁干扰抑制比 (EMIRR+) 与频率间的关系

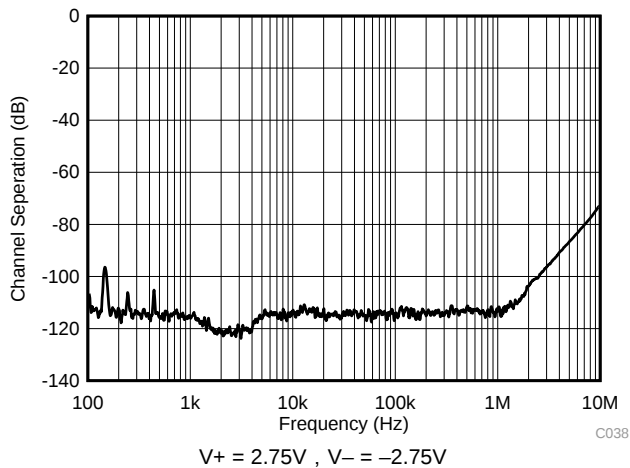


图 30. 通道分离与频率间的关系

典型特性 (接下页)

$T_A = 25^\circ\text{C}$ 时, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ 连接至 $V_S / 2$, $V_{CM} = V_S / 2$, 且 $V_{OUT} = V_S / 2$ (除非另有说明)

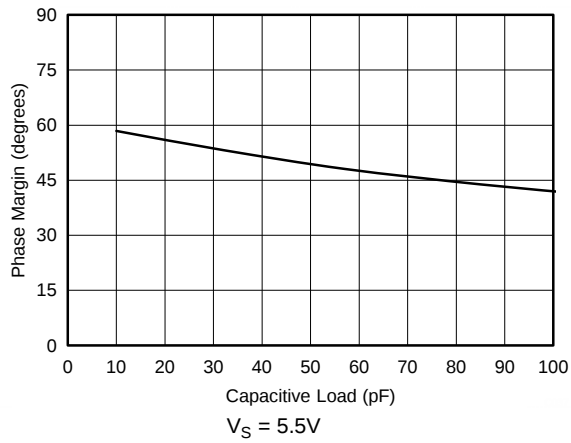


图 31. 相位裕度与容性负载间的关系

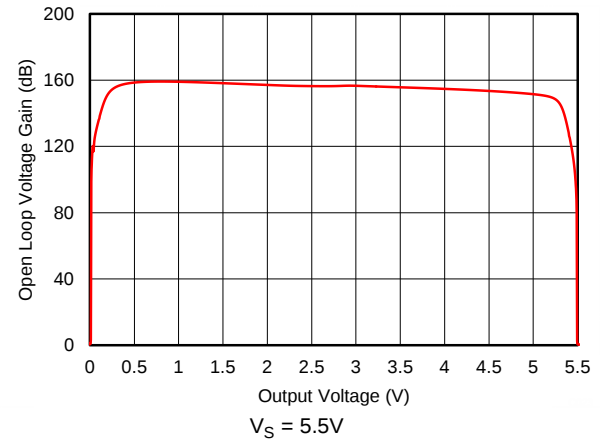


图 32. 开环电压增益与输出电压间的关系

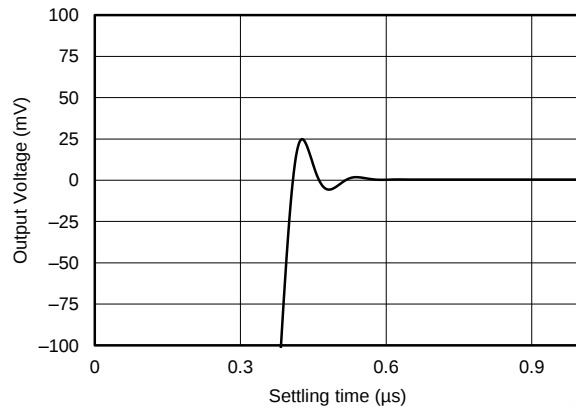


图 33. 大信号建立时间 (正)

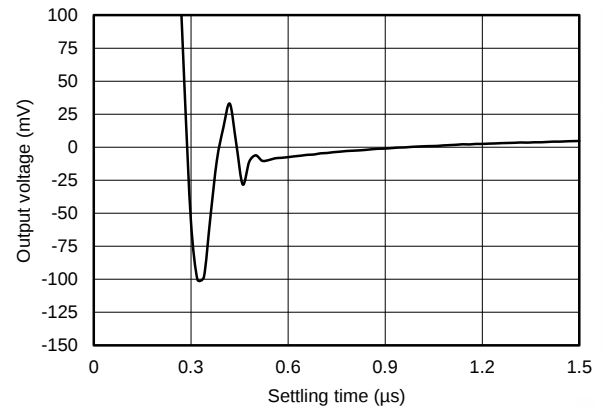


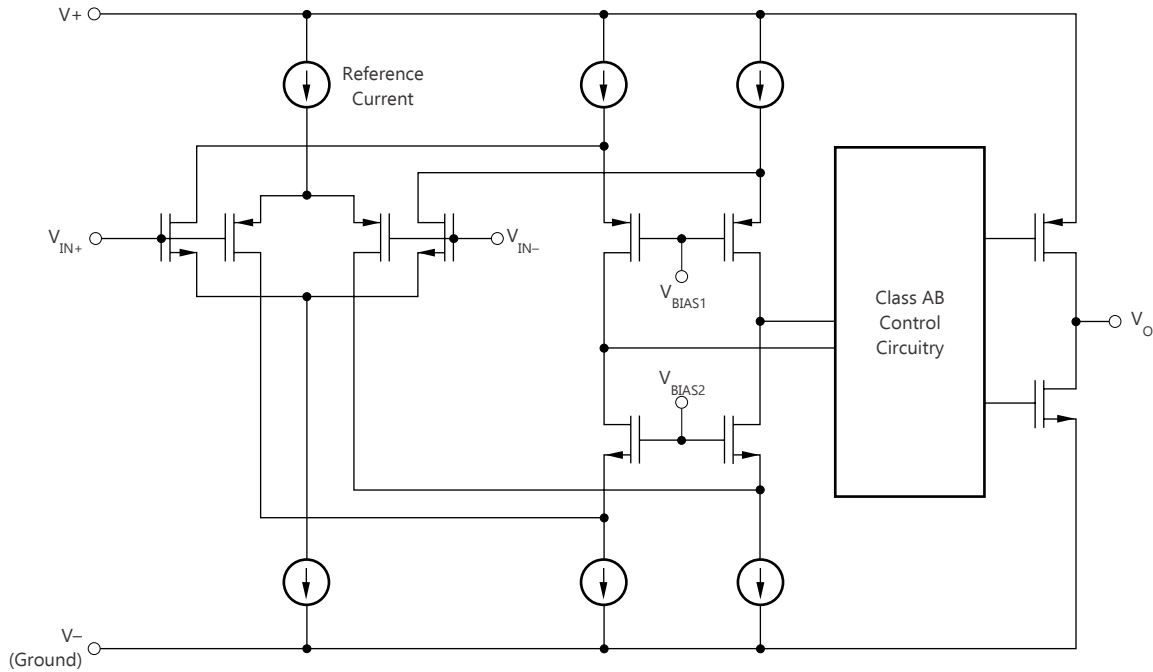
图 34. 大信号建立时间 (负)

8 详细 说明

8.1 概要

TSV91x 系列是低功耗、轨至轨输入和输出运算放大器系列。这些器件的工作电压范围为 2.5V 至 5.5V，具有单位增益稳定特性，并且适用于各种通用 应用。输入共模电压范围包括两个电源轨，并支持将 TSV91x 系列器件用于几乎任何单电源应用。轨至轨输入和输出摆幅可大幅扩大动态范围（尤其在低电源 应用 中），并且适用于驱动采样模数转换器 (ADC)。

8.2 功能框图



8.3 特性描述

8.3.1 轨至轨输入

TSV91x 系列的输入共模电压范围相对于电源轨向外扩展了 100mV，从而支持 2.5V 至 5.5V 的完整电源电压范围。此性能由一个互补输入级实现：一个 N 通道输入差分对和一个 P 通道差分对并联，如 [功能框图](#) 所示。当输入电压靠近正轨（通常在 $(V+) - 1.4V$ 到高于正电源电压 100mV 之间）时，N 沟道对有效；而当输入在低于负电源电压 100mV 到大约 $(V+) - 1.4V$ 之间时，P 沟道对有效。通常当介于 $(V+) - 1.2V$ 到 $(V+) - 1V$ 之间的小切换区域内，两个通道对都会打开。此 200mV 转换区域可能会随工艺不同而发生变化，最高可达 200mV。因此，此转换区域（两个级都打开）在低端上的范围介于 $(V+) - 1.4V$ 至 $(V+) - 1.2V$ 之间，而在高端上的范围高达 $(V+) - 1V$ 至 $(V+) - 0.8V$ 。在此转换区域内，与器件在该区域外运行相比，PSRR、CMRR、失调电压、温漂和 THD 等性能可能会下降。

8.3.2 轨至轨输出

TSV91x 系列器件是一种低功耗、低电压运算放大器，可提供强大的输出驱动能力。一个具有共源晶体管的 AB 类输出级可实现完全的轨至轨输出摆幅功能。对于 10kΩ 的阻性负载，无论施加的电源电压是多少，输出摆幅都在两个电源轨的 15mV 范围内。不同的负载情况会改变放大器在靠近电源轨范围内摆动的能力。

8.3.3 过载恢复

过载恢复定义为运算放大器输出从饱和状态恢复到线性状态所需的时间。当输出电压由于高输入电压或高增益而超过额定工作电压时，运算放大器的输出器件进入饱和区。器件进入饱和区后，输出器件中的电荷载体需要时间回到线性状态。当电荷载体回到线性状态时，器件开始以指定的压摆率进行转换。因此，传播延迟（过载情况下）等于过载恢复时间与转换时间之和。TSV91x 系列器件的过载恢复时间大约为 200ns。

8.4 器件功能模式

TSV91x 系列拥有单功能模式。只要电源电压在 2.5V ($\pm 1.25V$) 与 5.5V ($\pm 2.75V$) 之间，这些器件就处于通电状态。

9 应用和实现

注

以下 应用 部分中的信息不属于 TI 组件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定组件是否适用于其应用。客户应验证并测试其设计实现，以确认系统功能。

9.1 应用信息

TSV91x 系列 可实现 8MHz 带宽和 4.5V/ μ s 压摆率，且每个通道仅有 550 μ A 的电源电流，从而在低功耗的情况下提供良好的交流性能。在直流 应用 中也具有良好性能，其输入噪声电压低（在 1kHz 时为 18nV/ $\sqrt{\text{Hz}}$ ），输入偏置电流低，且典型的输入失调电压为 0.3mV。

9.2 典型应用

图 35 显示了低侧电机控制应用中配置的 TSV91x。

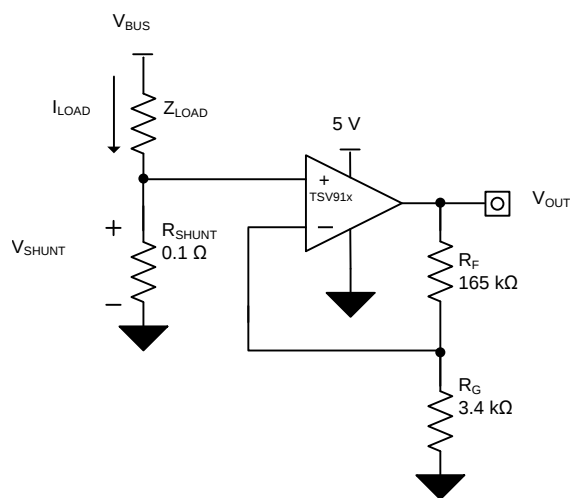


图 35. 低侧电机控制应用中的 TSV91x

9.2.1 设计要求

此设计的设计要求如下：

- 负载电流：0A 至 1A
- 输出电压：4.95V
- 最大分流电压：100mV

典型应用 (接下页)

9.2.2 详细设计流程

图 35 中电路的传递函数如公式 1 所示

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

负载电流 (I_{LOAD}) 在分流电阻器 (R_{SHUNT}) 上产生压降。负载电流设置为 0A 至 1A。为了在最大负载电流下保持分流电压低于 100mV，公式 2 中定义了最大分流电阻。

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

根据公式 2， R_{SHUNT} 为 100mΩ。 I_{LOAD} 和 R_{SHUNT} 产生的电压降由 TSV91x 放大，从而产生大约 0V 至 4.95V 的输出电压。TSV91x 产生必要输出电压时所需的增益根据公式 3 算出：

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

根据公式 3 计算出的所需增益为 49.5V/V，由电阻器 R_F 和 R_G 设定此值。公式 4 用于调整电阻器 R_F 和 R_G 的大小，从而将 TSV91x 的增益设置为 49.5V/V。

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

选择 R_F 为 165kΩ 而 R_G 为 3.4kΩ 的组合时可获得大约 49.5V/V 的增益。图 36 显示了图 35 所示电路的测量传递函数。

9.2.3 应用曲线

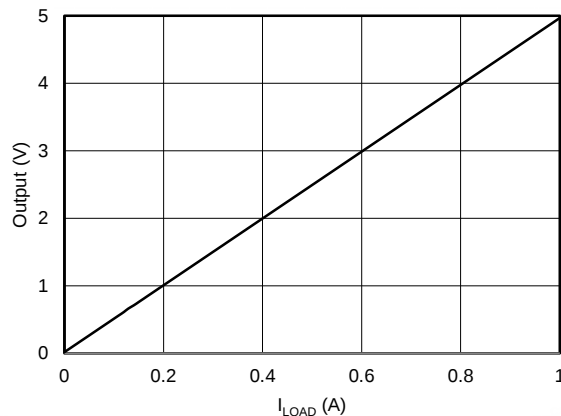


图 36. 低侧电流检测传递函数

10 电源建议

TSV91x 系列器件的额定工作电压范围是 2.5V 至 5.5V ($\pm 1.25\text{V}$ 至 $\pm 2.75\text{V}$)；许多规格在 -40°C 至 $+125^{\circ}\text{C}$ 的温度下适用。[典型特性](#) 部分提供的参数可能随工作电压或温度的变化而出现显著变化。

CAUTION

电源电压超过 6V 可能会对器件造成永久损坏；请参阅[绝对最大额定值](#) 表。

将 $0.1\mu\text{F}$ 旁路电容器置于电源引脚附近，以减小从高噪声电源或高阻抗电源中耦合进来的误差。有关旁路电容器位置的更多详细信息，请参阅 [部分](#)。

10.1 输入和 ESD 保护

TSV91x 系列器件在所有引脚上均整合了内部 ESD 保护电路。对于输入和输出引脚，这种保护包括输入和电源引脚之间连接的导流二极管。只要电流如[绝对最大额定值](#) 表中所述不超过 10mA，这些 ESD 保护二极管就能提供电路内输入过驱保护。[图 37](#)显示了如何通过将串联输入电阻器添加到被驱动的输入端来限制输入电流。添加的电阻器会增加放大器输入端的热噪声；在对噪声敏感的应用中，该值必须保持在最低值。

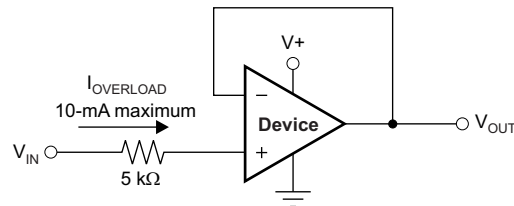


图 37. 输入电流保护

11 布局

11.1 布局指南

为了实现器件的最佳运行性能，应使用良好的印刷电路板 (PCB) 布局规范，包括：

- 噪声可以通过整个电路的电源引脚和运算放大器本身的电源引脚传入模拟电路。旁路电容为局部模拟电路提供低阻抗电源，用于降低耦合噪声。
 - 在每个电源引脚和接地端之间连接低 ESR 0.1 μ F 陶瓷旁路电容器，放置位置尽量靠近器件。从 V+ 到接地端的单个旁路电容器适用于单通道电源应用。
- 将电路的模拟和数字部分单独接地是最简单和最有效的噪声抑制方法之一。多层 PCB 中通常将一层或多层专门作为接地层。接地层有助于散热和降低电磁干扰 (EMI) 噪声拾取。确保对数字接地和模拟接地进行物理隔离，同时应注意接地电流。有关更多详细信息，请参阅《电路板布局技巧》。
- 为了减少寄生耦合，请让输入走线尽可能远离电源或输出走线。如果这些走线不能保持分离，则敏感走线与有噪声走线垂直相交比平行更好。
- 外部组件的位置应尽量靠近器件。如图 39 所示，使 RF 和 RG 接近反相输入可最大限度地减小反相输入端的寄生电容。
- 尽可能缩短输入迹线。切记：输入走线是电路中最敏感的部分。
- 考虑在关键走线周围设定驱动型低阻抗保护环。这样可显著减少附近走线在不同电势下产生的泄漏电流。
- 为获得最佳性能，建议在组装 PCB 板后进行清洗。
- 任何精密集成电路都可能因湿气渗入塑料封装中而出现性能变化。请遵循所有的 PCB 水清洁流程，建议将 PCB 组装烘干，以去除清洗时渗入器件封装中的湿气。大多数情形下，清洗后在 85°C 下低温烘干 30 分钟即可。

11.2 布局示例

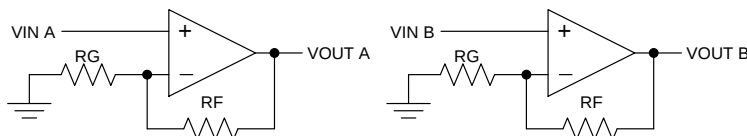


图 38. 图 39 的原理图表示

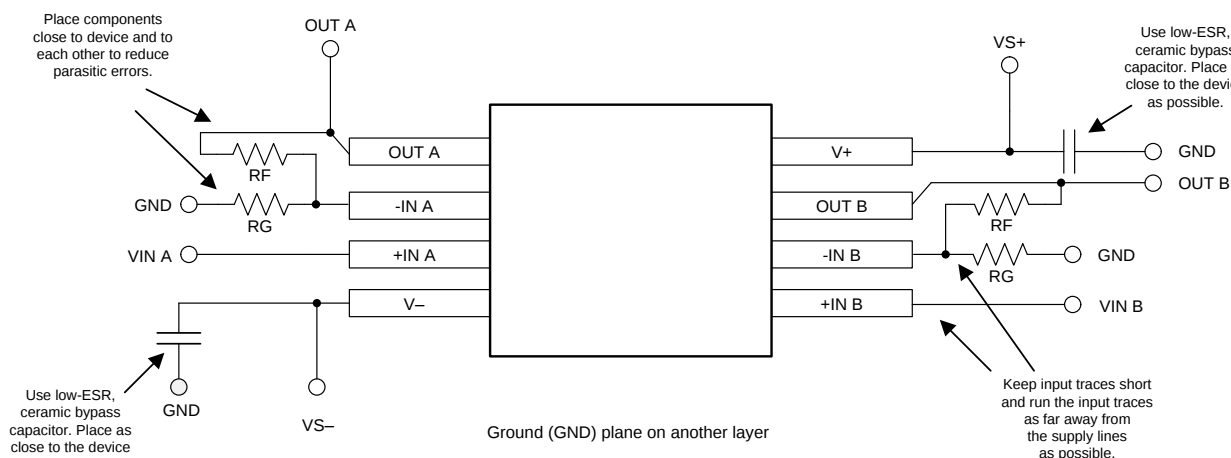


图 39. 布局示例

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

如需相关文档，请参阅：

德州仪器 (TI)，《[电路板布局技巧](#)》

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 1. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TSV911	单击此处	单击此处	单击此处	单击此处	单击此处
TSV912	单击此处	单击此处	单击此处	单击此处	单击此处
TSV914	单击此处	单击此处	单击此处	单击此处	单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。单击右上角的[通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

TI E2E™ 在线社区 **TI 的工程师对工程师 (E2E) 社区。**此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](#) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

SLYZ022 — **TI 术语表。**

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSV911AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U2F	Samples
TSV911AIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1EK	Samples
TSV912AIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T12A	Samples
TSV912AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T912	Samples
TSV912AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T912	Samples
TSV912AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TSV912	Samples
TSV912AIDSGR	ACTIVE	WSO	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T912	Samples
TSV912AIDSGT	ACTIVE	WSO	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T912	Samples
TSV912AIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	TSV912	Samples
TSV914AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AD	Samples
TSV914AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TSV914	Samples
TSV914AIPWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TSV914	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

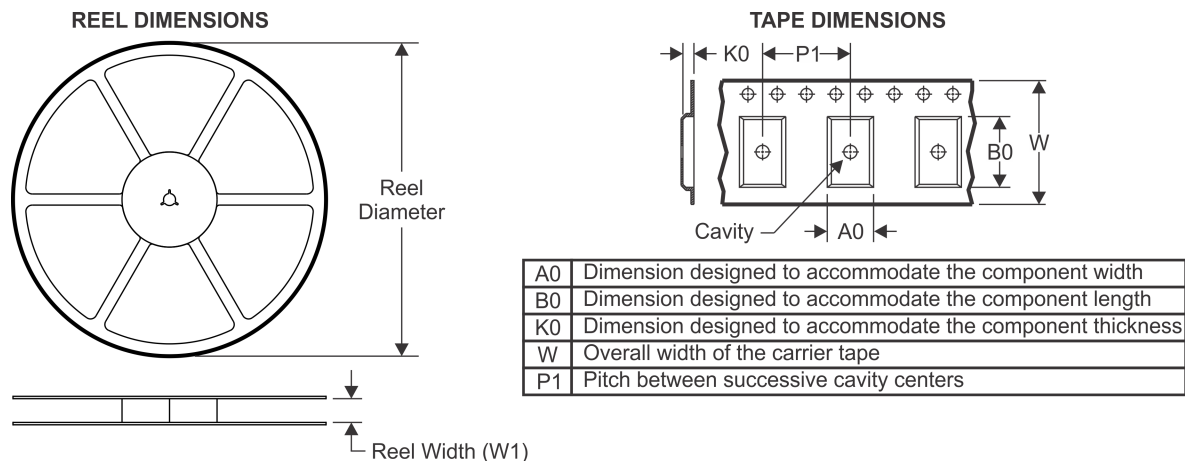
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

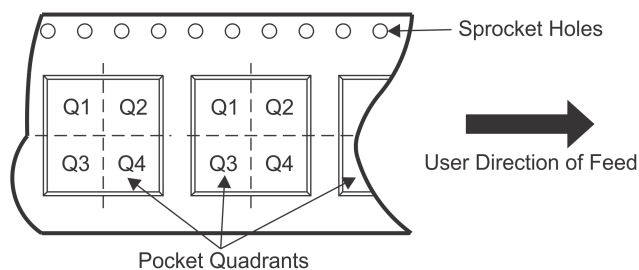
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



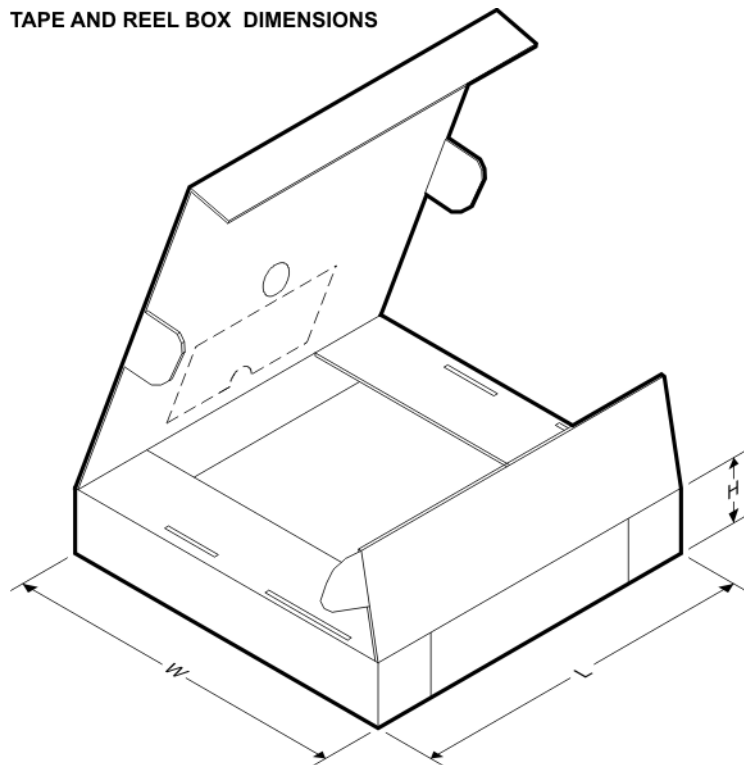
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSV911AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV911AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TSV912AIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV912AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TSV912AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TSV912AIDR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
TSV912AIDSGR	WSOP	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TSV912AIDSGT	WSOP	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TSV912AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TSV912AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TSV914AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TSV914AIDR	SOIC	D	14	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
TSV914AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSV914AIPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSV911AIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TSV911AIDCKR	SC70	CKR	5	3000	190.0	190.0	30.0
TSV912AIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TSV912AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TSV912AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TSV912AIDR	SOIC	D	8	2500	333.2	345.9	28.6
TSV912AIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TSV912AIDSGT	WSON	DSG	8	250	210.0	185.0	35.0
TSV912AIPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TSV912AIPWR	TSSOP	PW	8	2000	366.0	364.0	50.0
TSV914AIDR	SOIC	D	14	2500	853.0	449.0	35.0
TSV914AIDR	SOIC	D	14	2500	336.6	336.6	41.3
TSV914AIPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TSV914AIPWT	TSSOP	PW	14	250	366.0	364.0	50.0

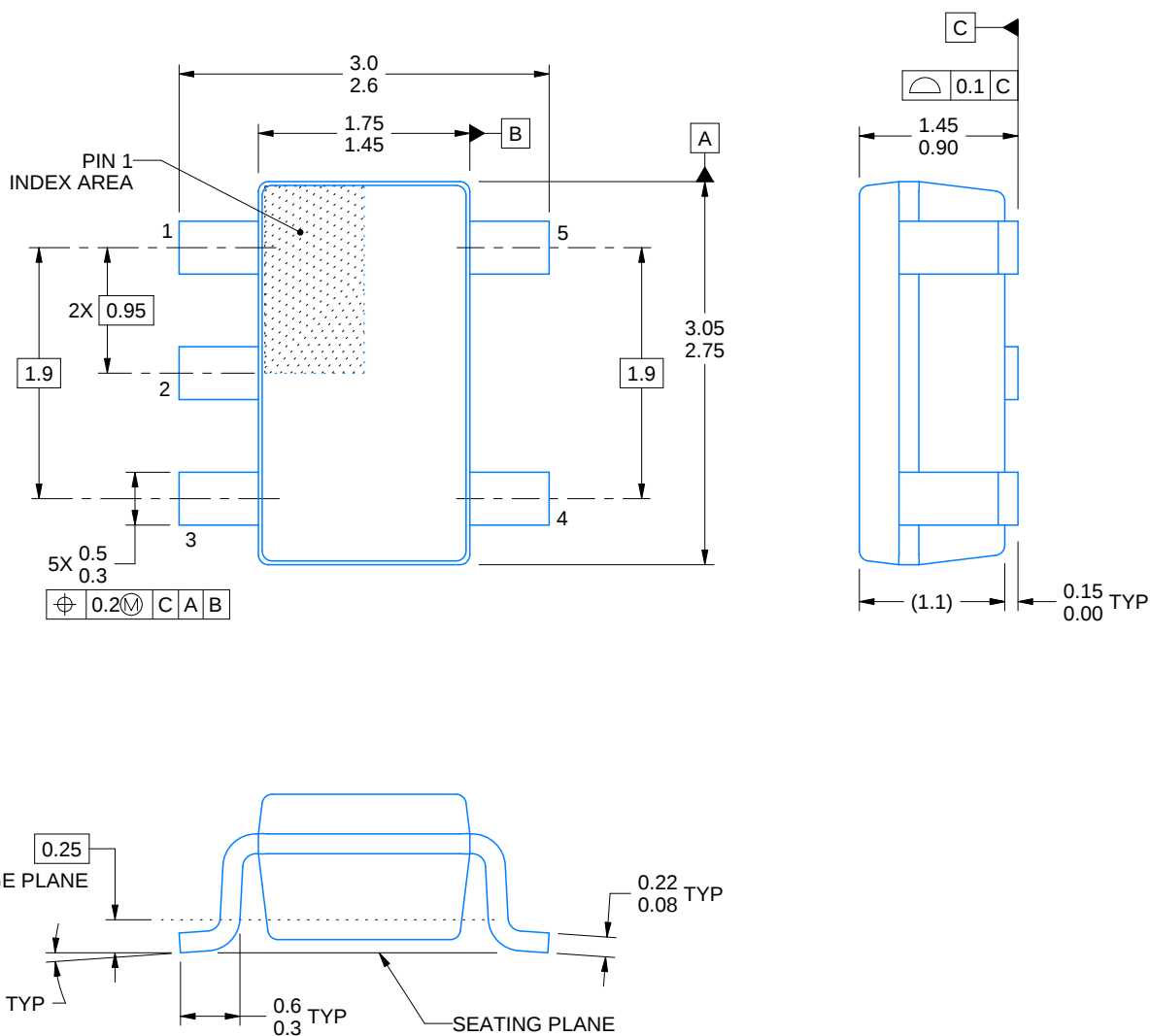


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

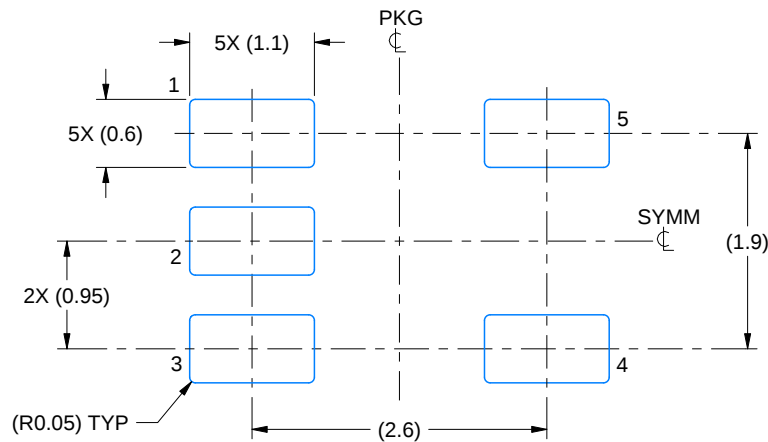
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

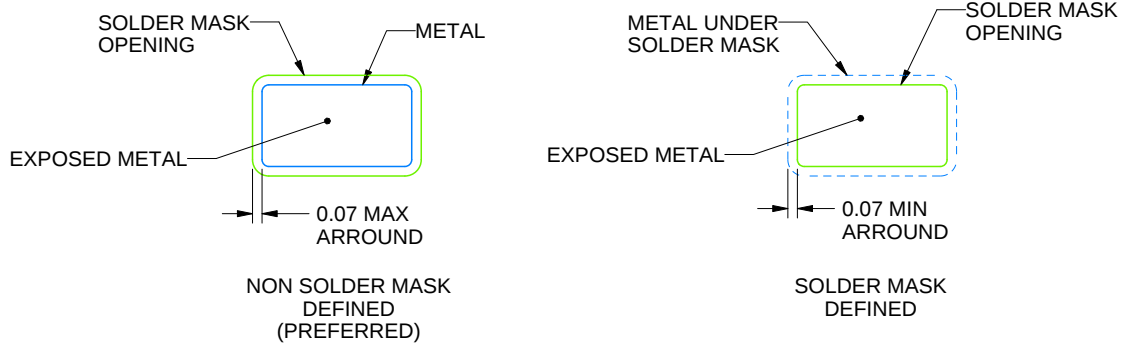
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

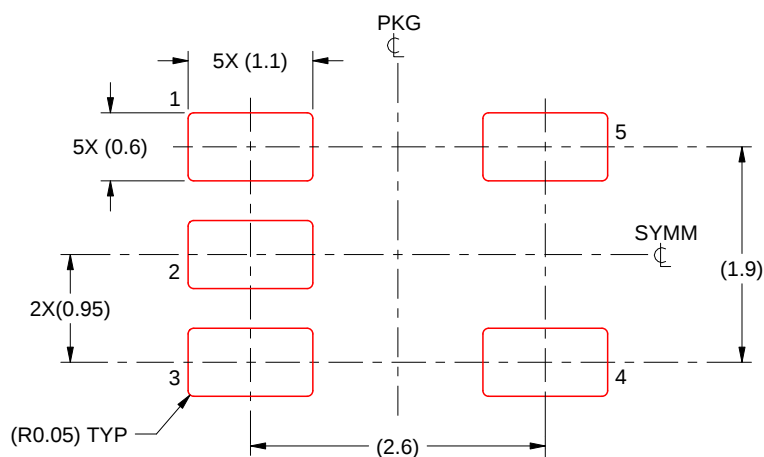
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

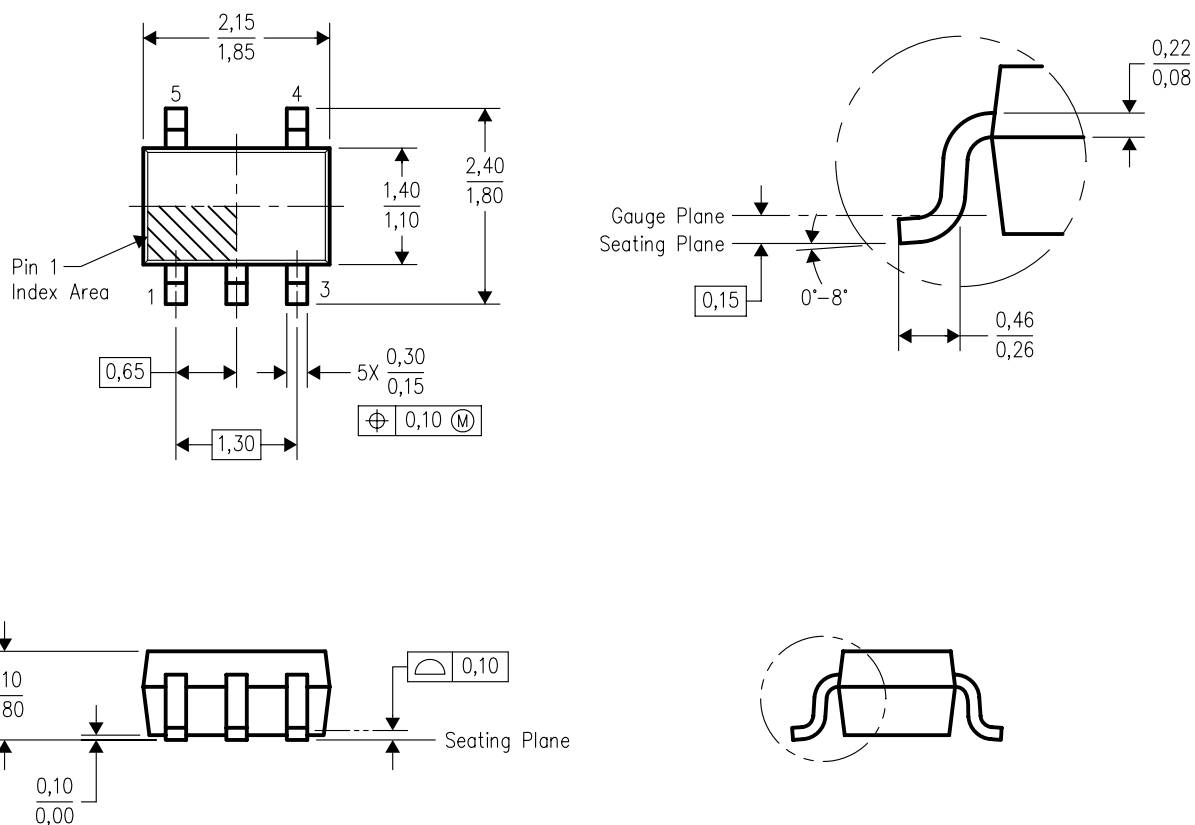
4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

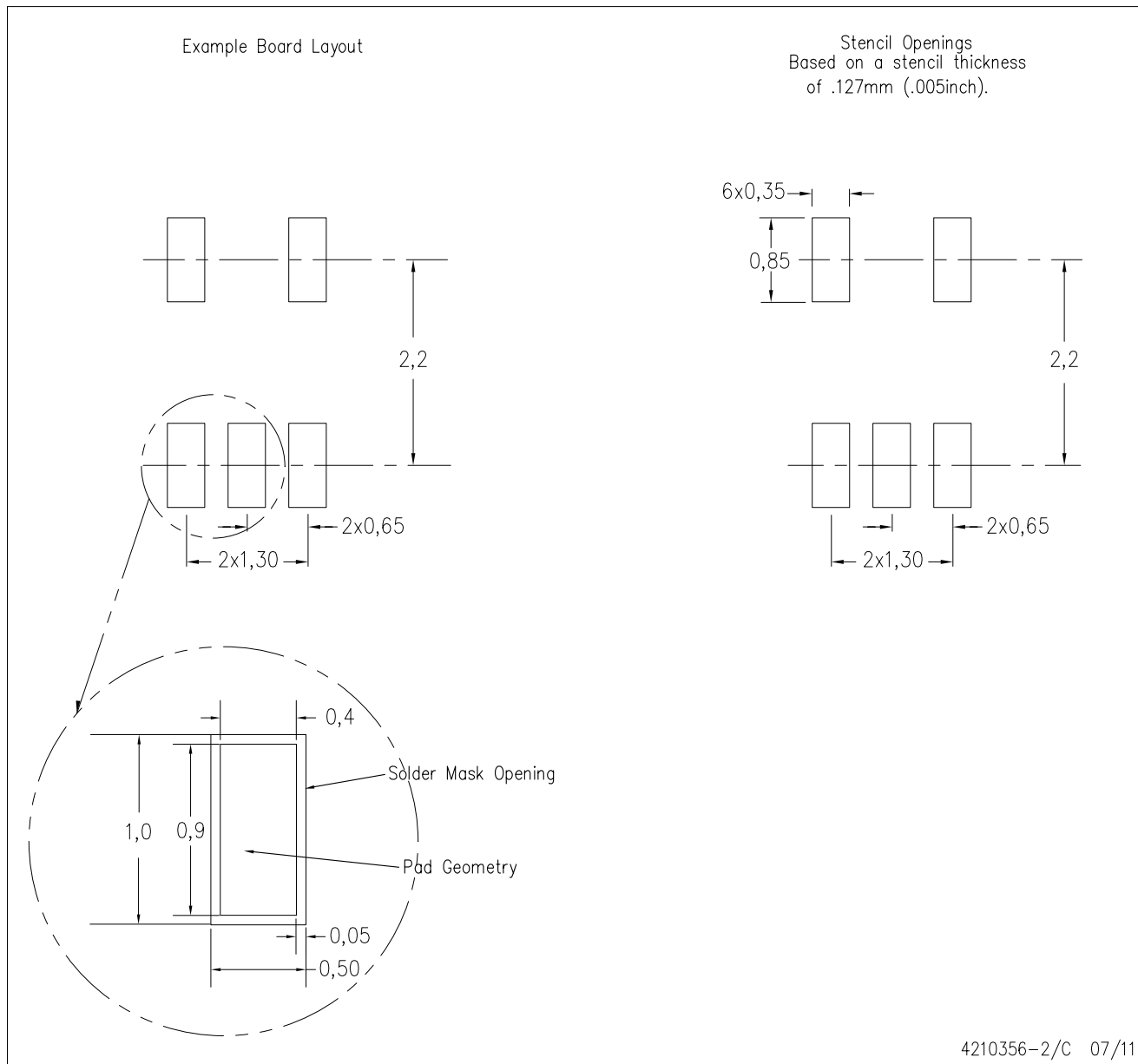


4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

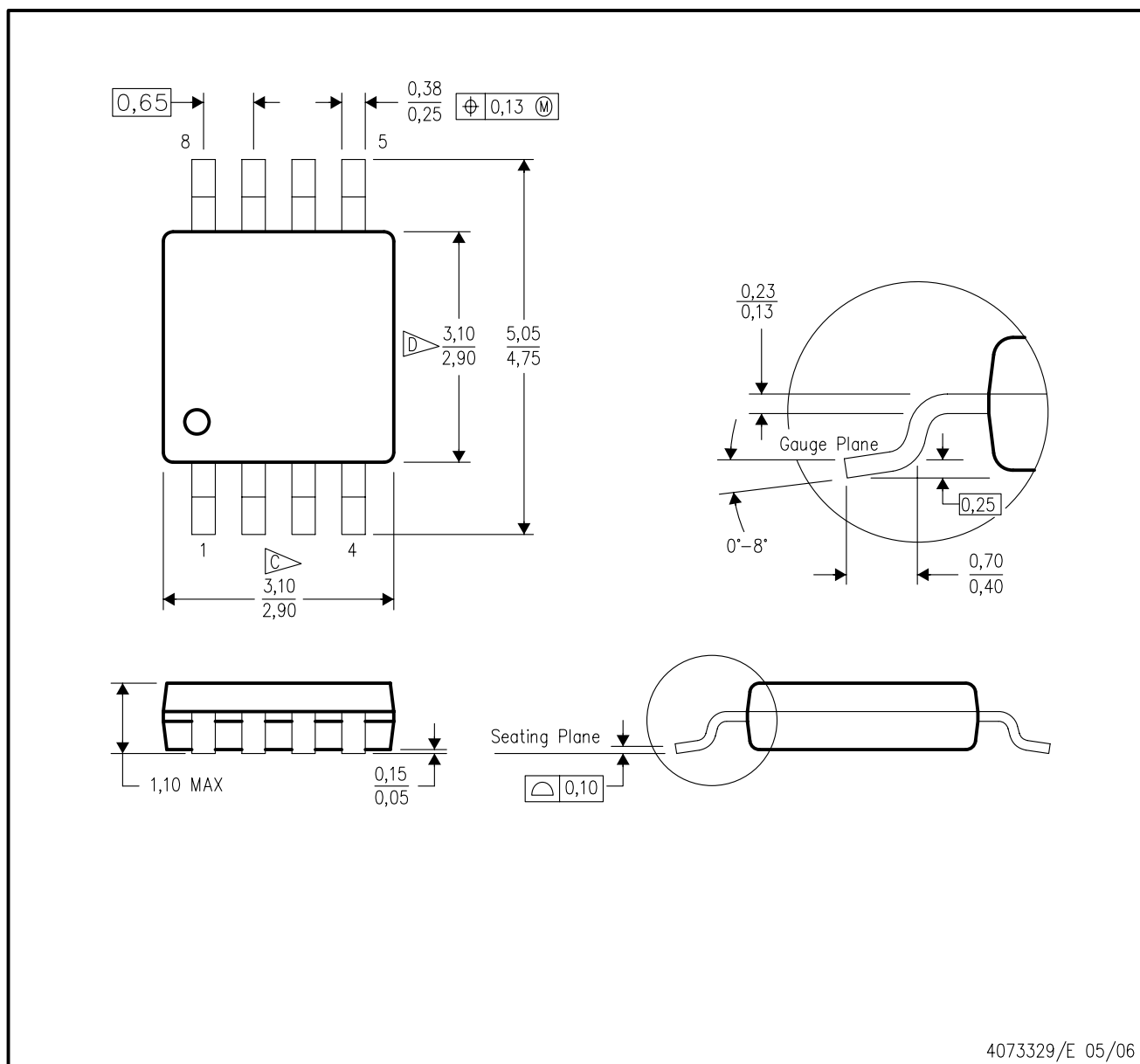
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



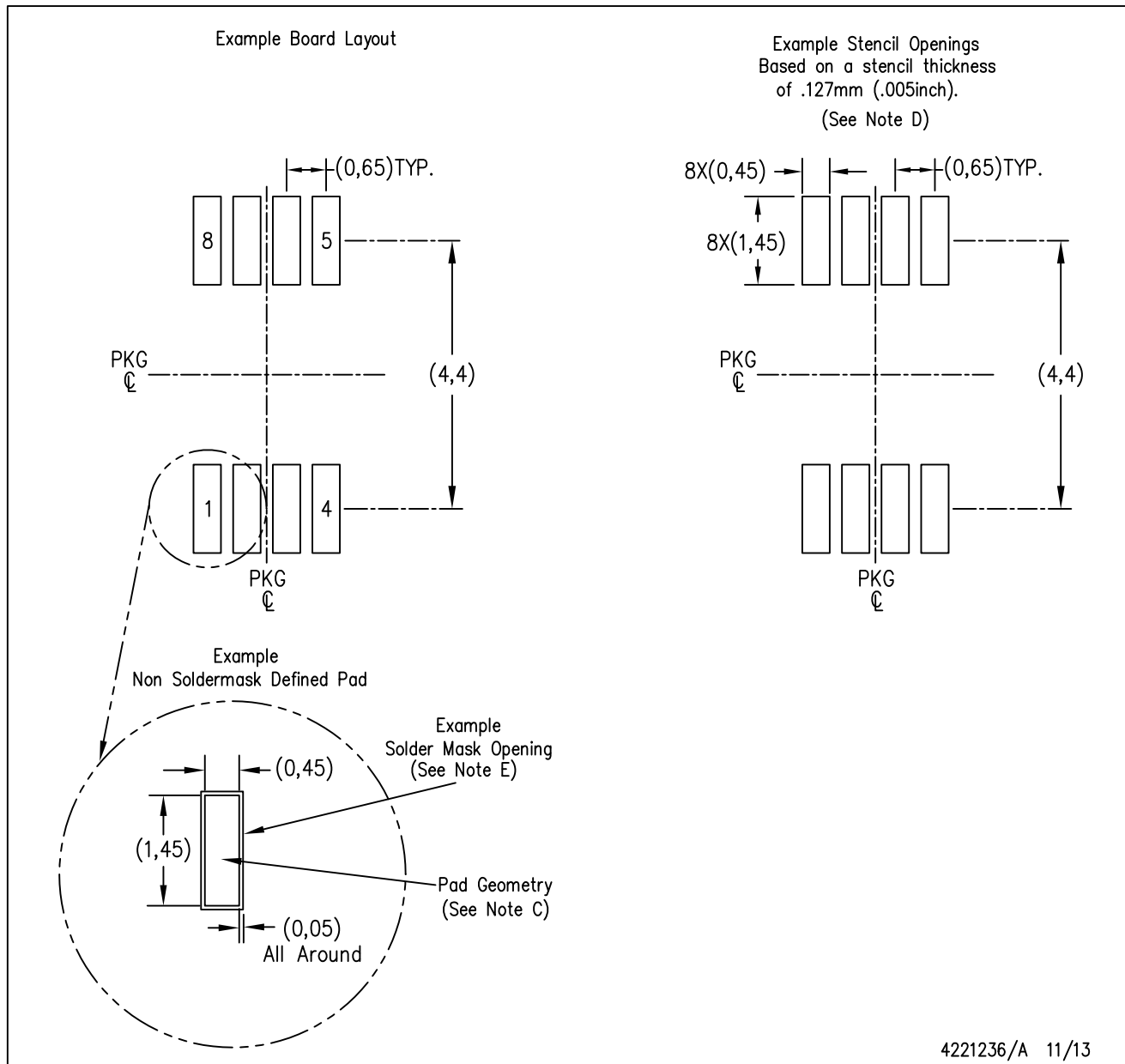
4073329/E 05/06

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

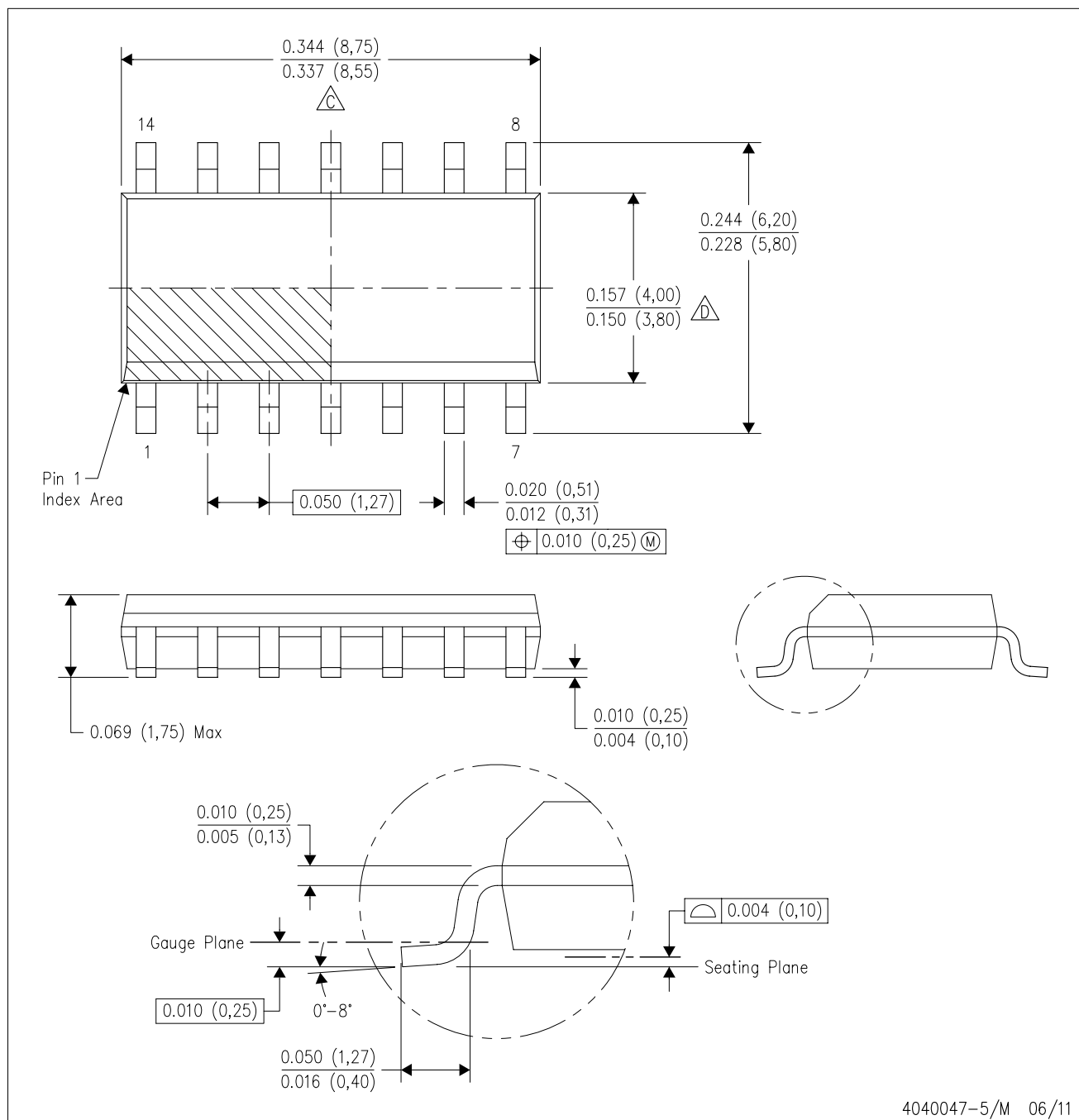
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

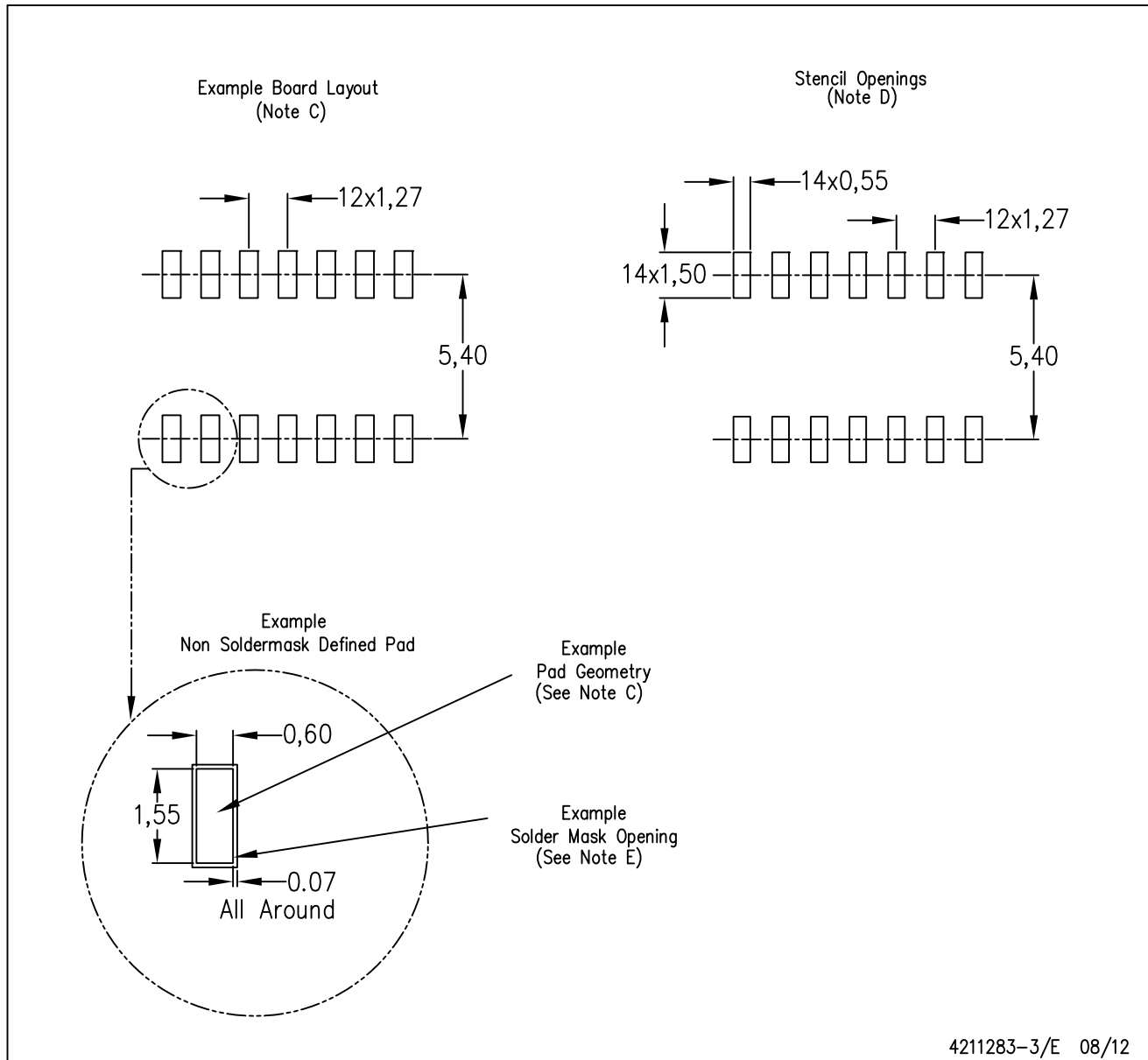


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

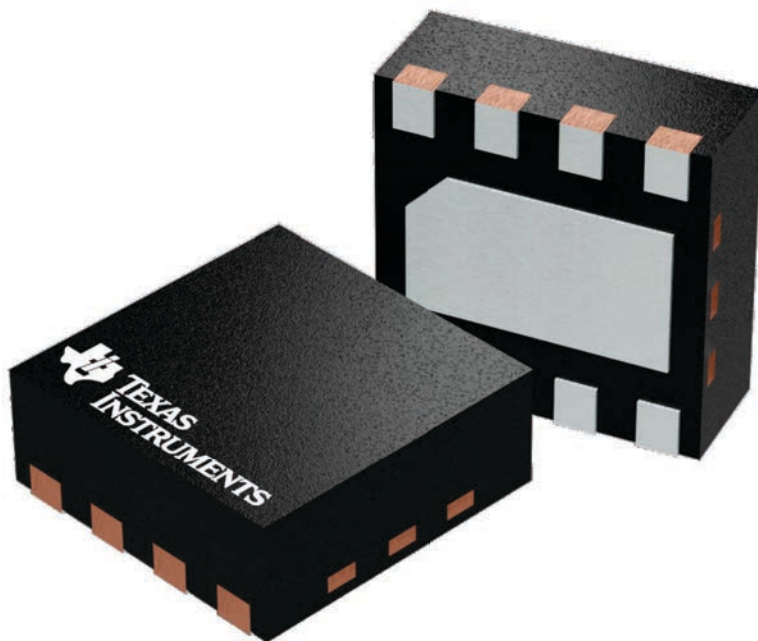
DSG 8

WSON - 0.8 mm max height

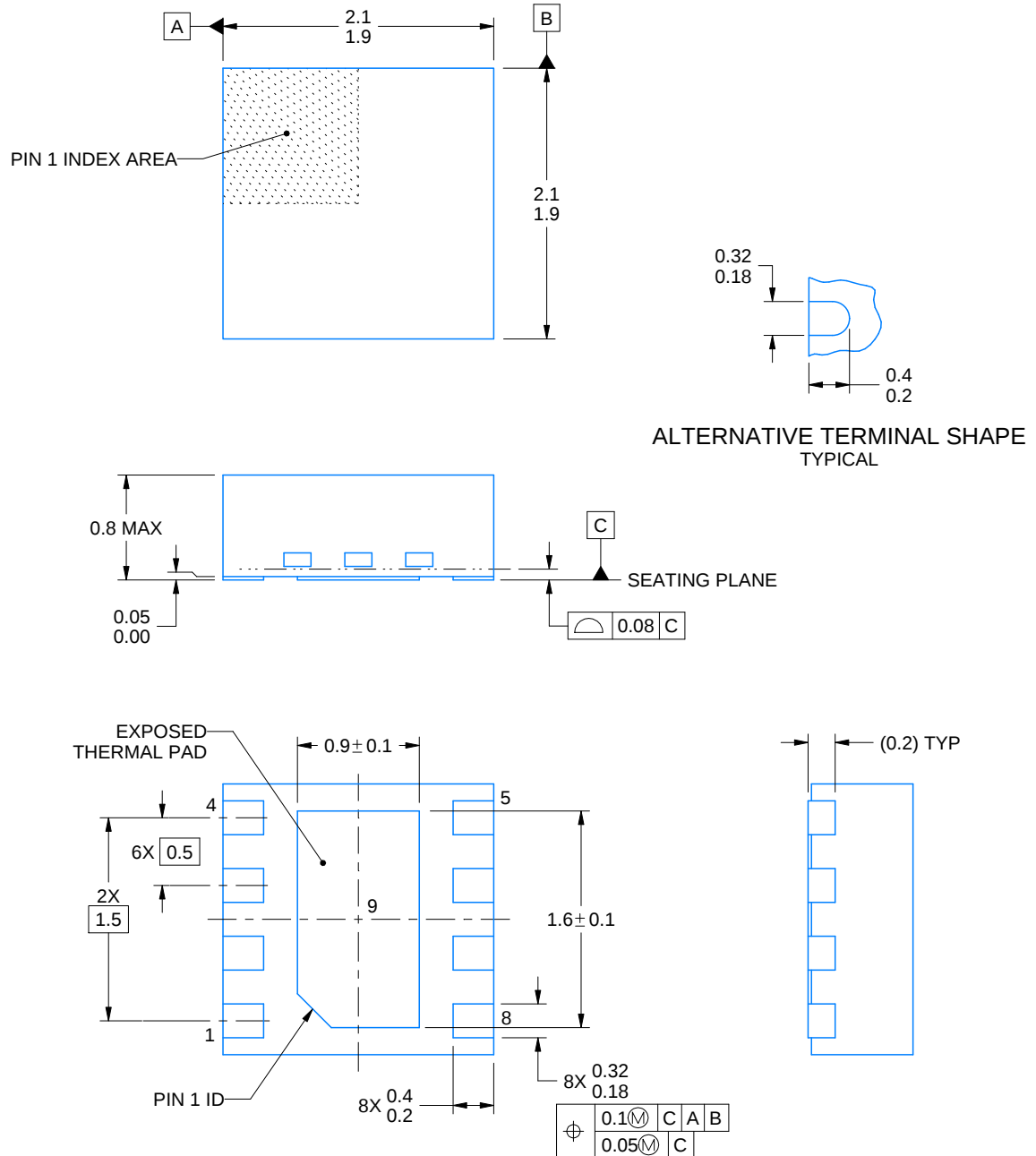
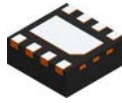
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A



4218900/D 04/2020

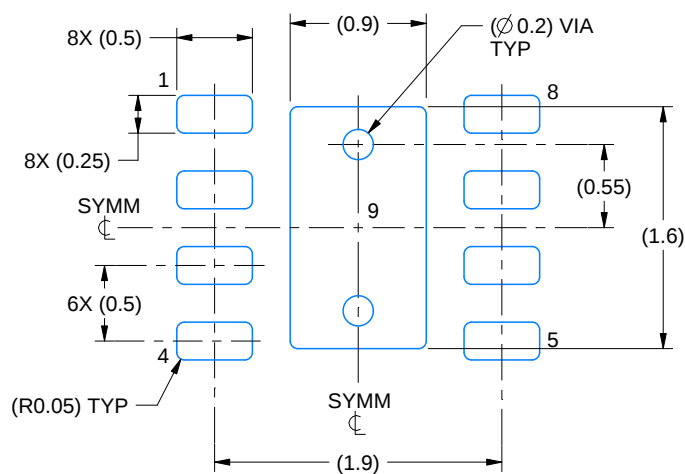
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

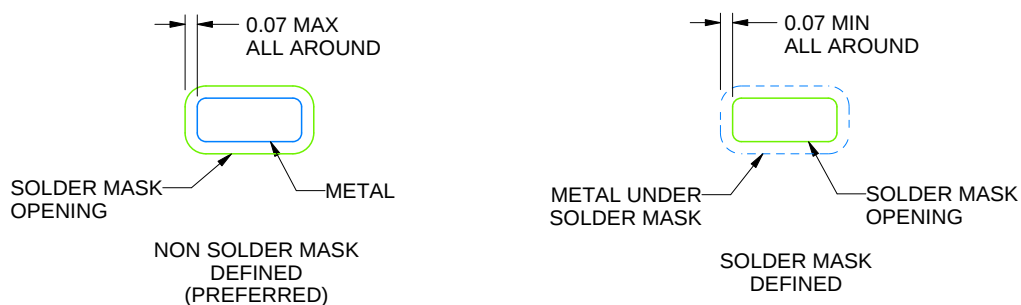
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

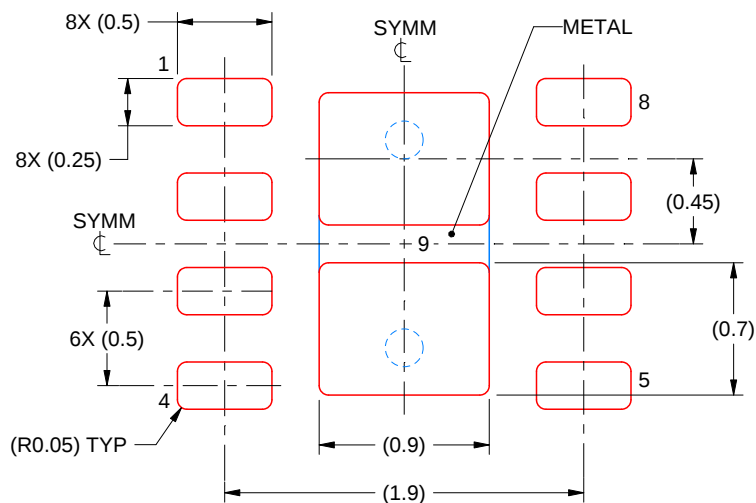
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

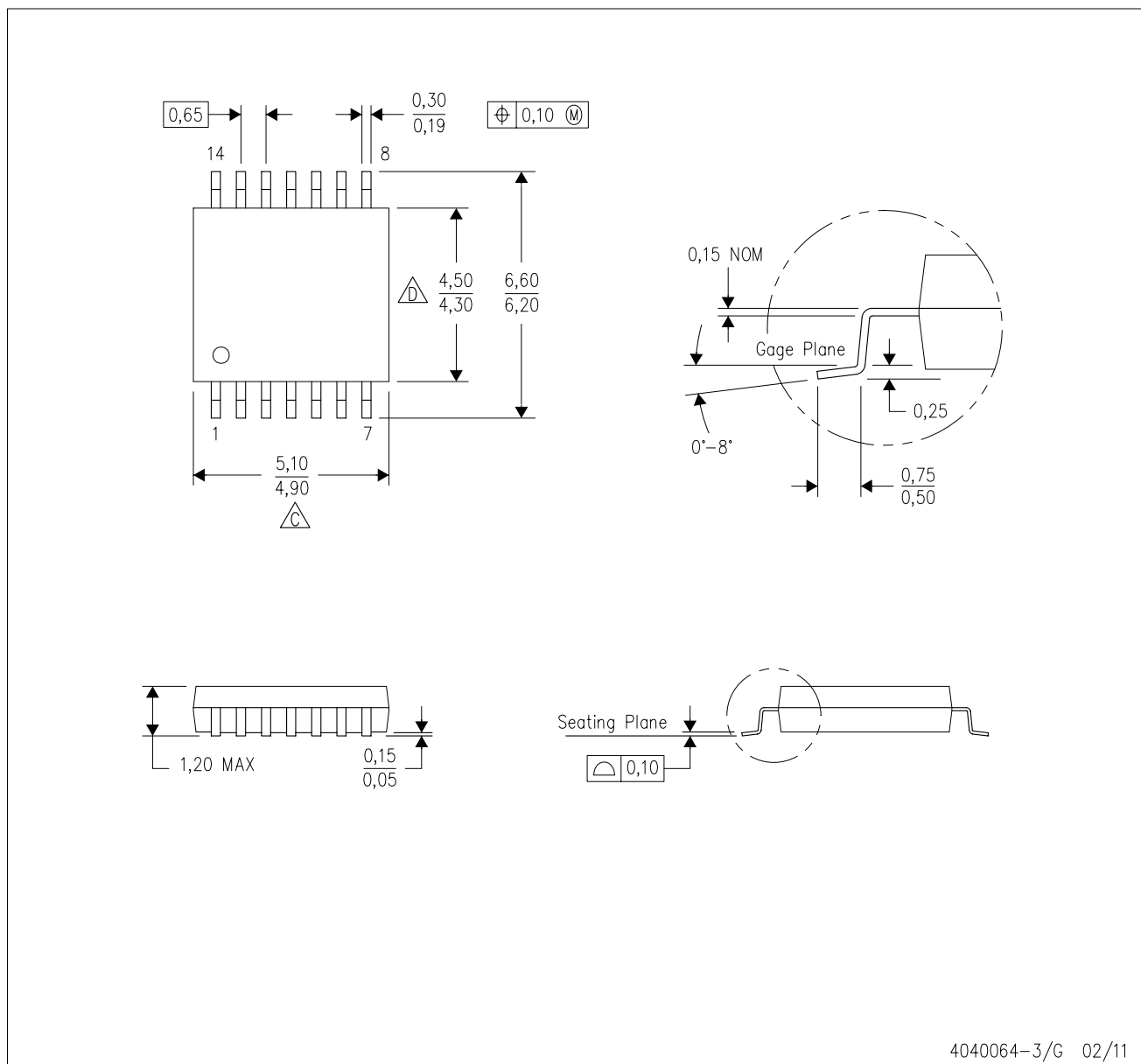
4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

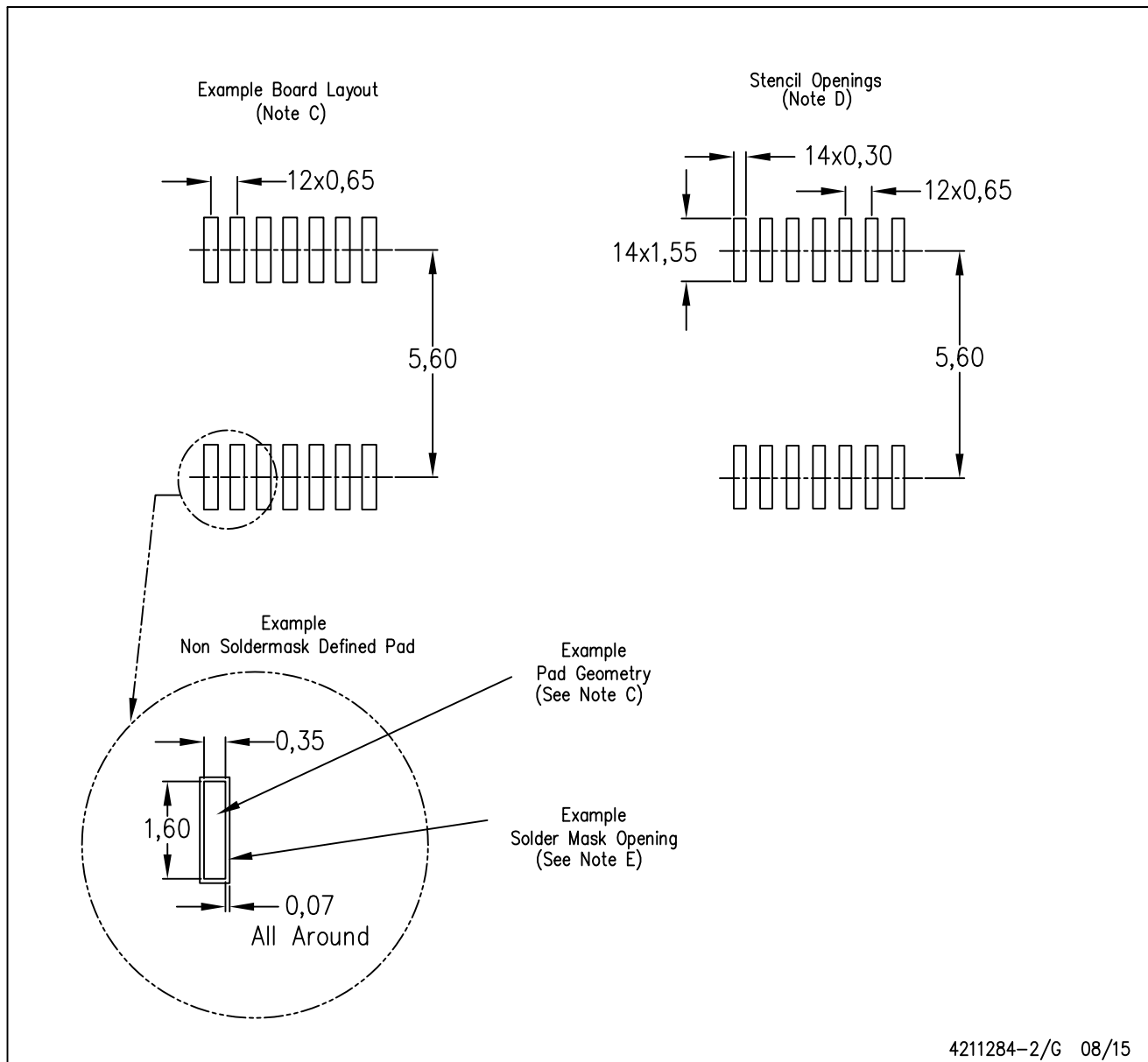
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

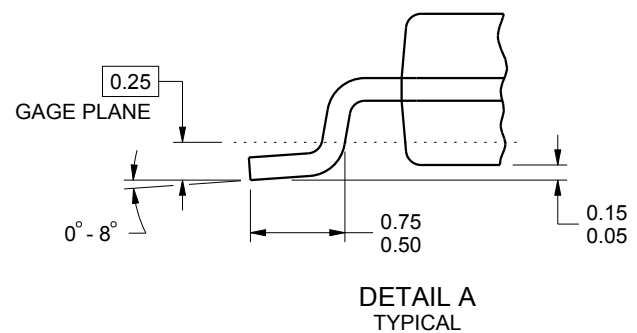
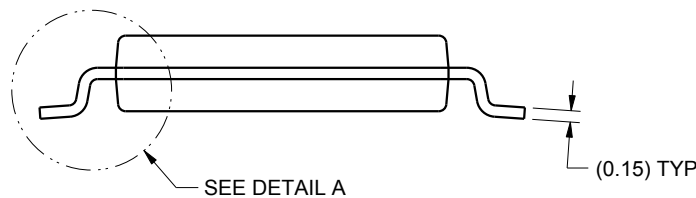
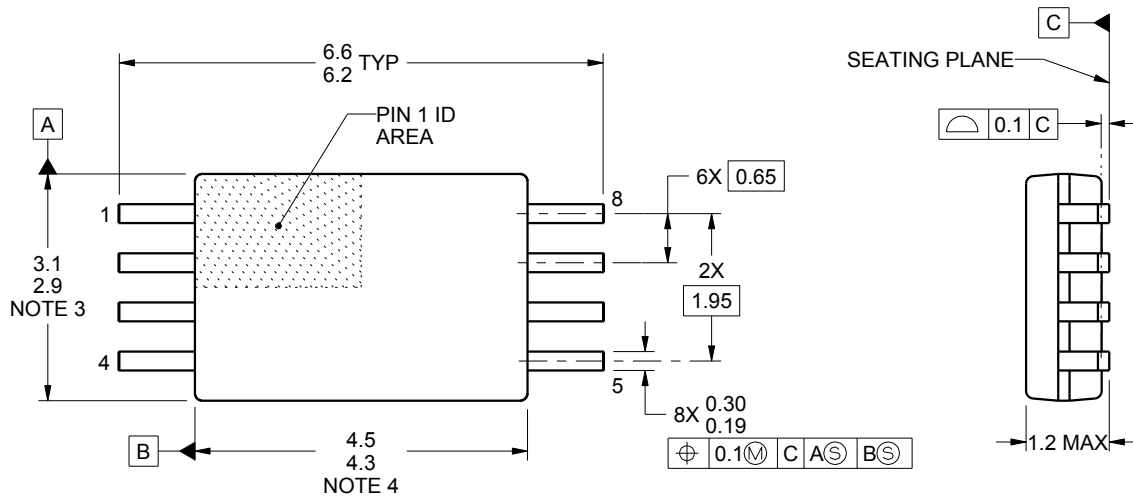
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

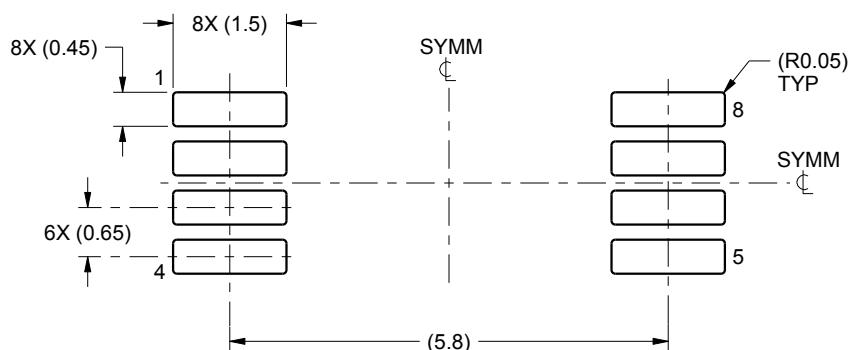
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

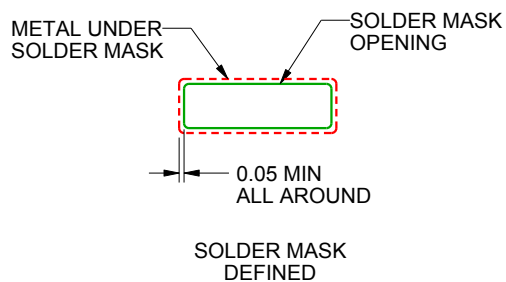
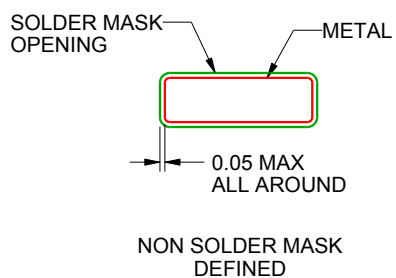
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

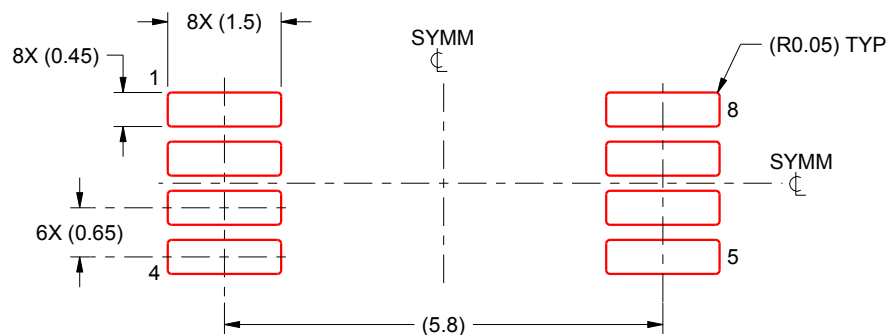
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

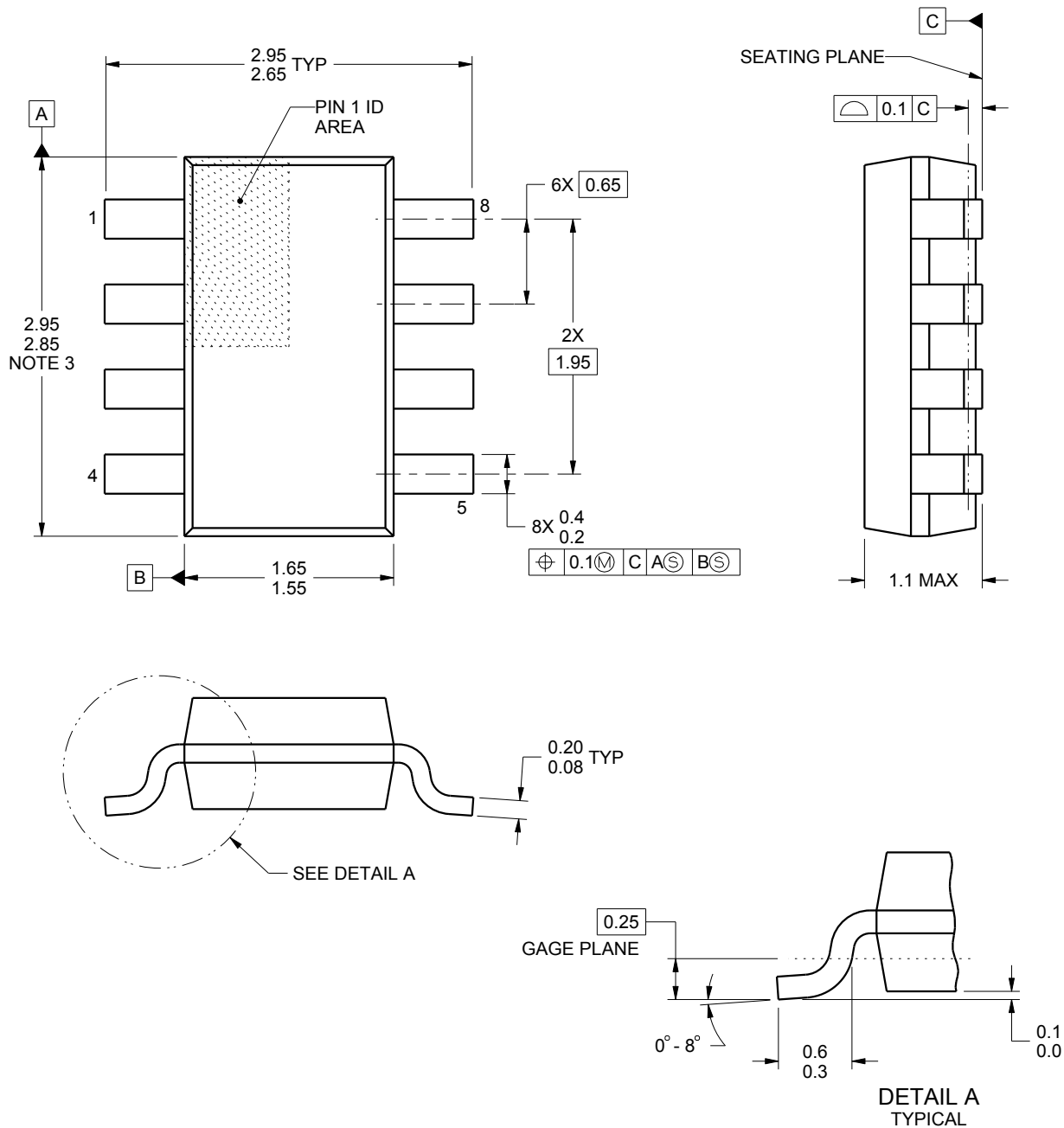
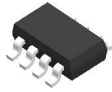


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4222047/B 11/2015

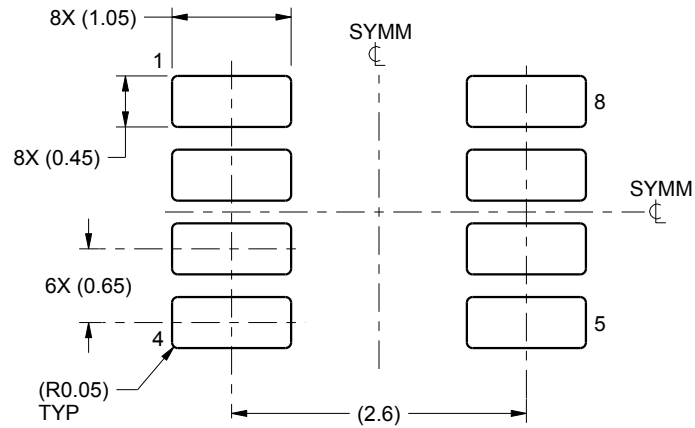
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

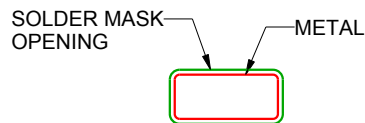
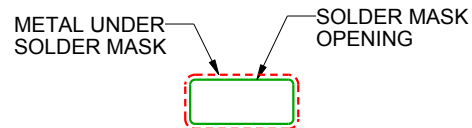
DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

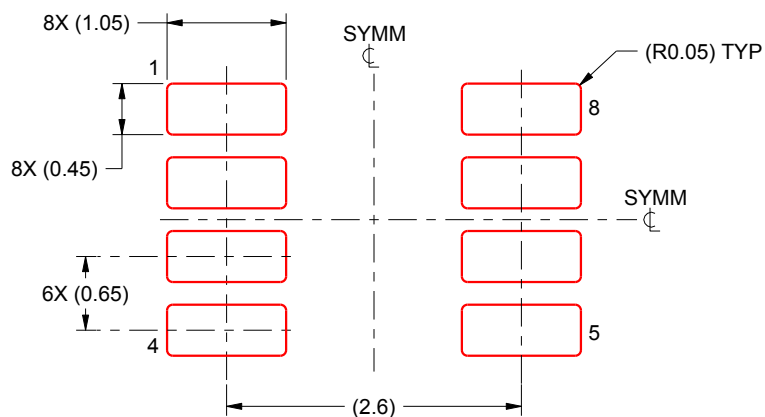
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

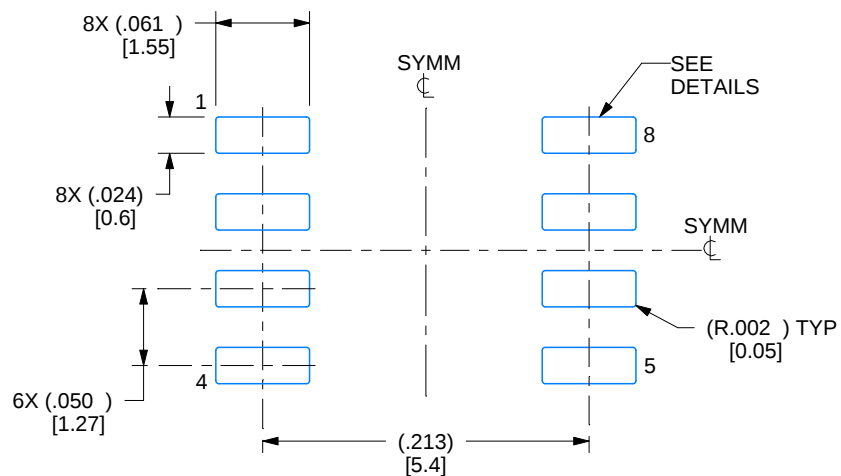


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

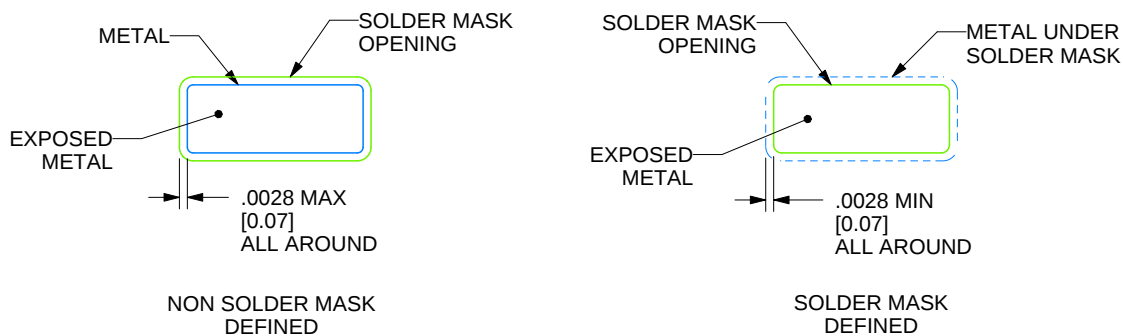
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

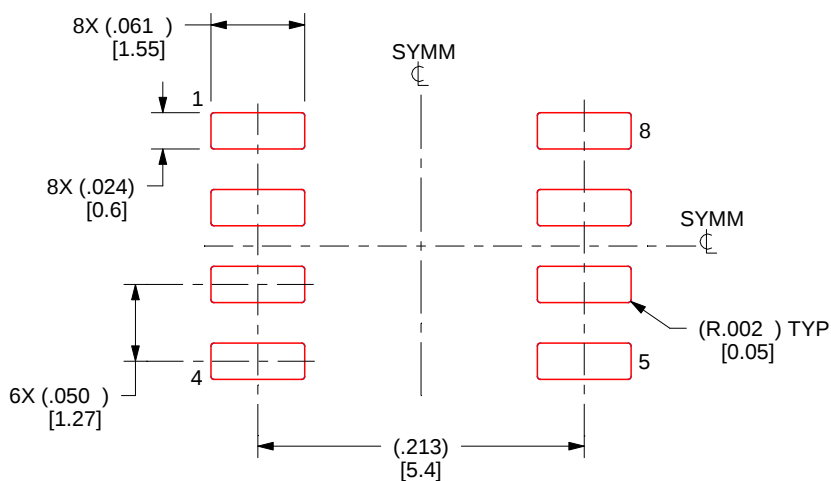
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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