

- Operating Range 2-V to 5.5-V  $V_{CC}$
- Latch-Up Performance Exceeds 250 mA  
Per JESD 17

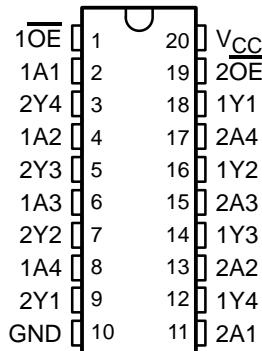
### description/ordering information

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

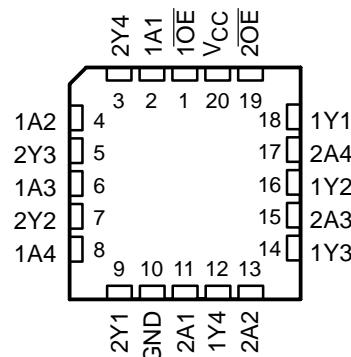
The 'AHC240 devices are organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHC240 . . . J OR W PACKAGE  
SN74AHC240 . . . DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHC240 . . . FK PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

$T_A$	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}C$ to $85^{\circ}C$	PDIP – N	Tube	SN74AHC240N	SN74AHC240N
	SOIC – DW	Tube	SN74AHC240DW	AHC240
		Tape and reel	SN74AHC240DWR	
	SOP – NS	Tape and reel	SN74AHC240NSR	AHC240
	SSOP – DB	Tape and reel	SN74AHC240DBR	HA240
	TSSOP – PW	Tube	SN74AHC240PW	HA240
		Tape and reel	SN74AHC240PWR	
$-55^{\circ}C$ to $125^{\circ}C$	TVSOP – DGV	Tape and reel	SN74AHC240DGVR	HA240
	CDIP – J	Tube	SNJ54AHC240J	SNJ54AHC240J
	CFP – W	Tube	SNJ54AHC240W	SNJ54AHC240W
	LCCC – FK	Tube	SNJ54AHC240FK	SNJ54AHC240FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

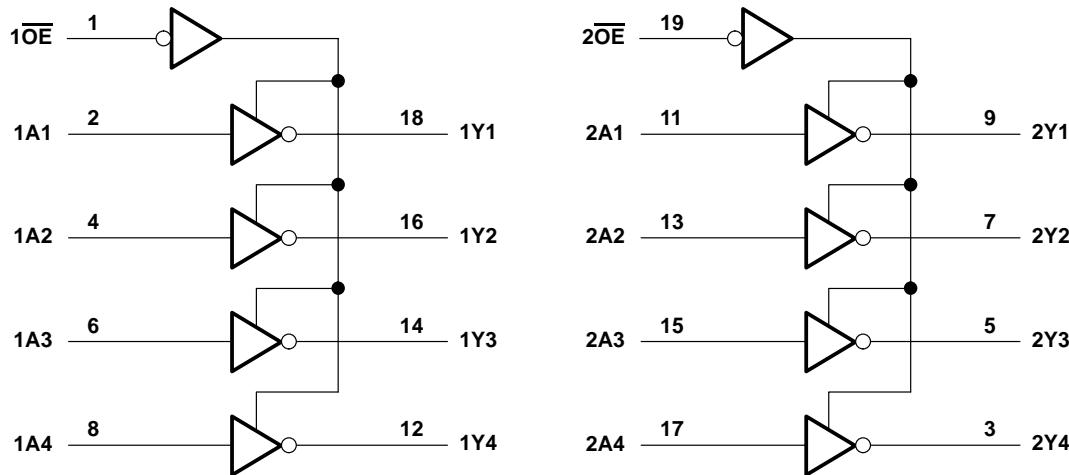
## SN54AHC240, SN74AHC240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS251H – OCTOBER 1995 – REVISED JULY 2003

## FUNCTION TABLE (each 4-bit buffer/driver)

INPUTS		OUTPUT
<u>OE</u>	A	Y
L	H	L
L	L	H
H	X	Z

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 75$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package .....	70°C/W
DGV package .....	92°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
PW package .....	83°C/W
Storage temperature range, $T_{Stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		SN54AHC240		SN74AHC240		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5	1.5	V
		V <sub>CC</sub> = 3 V	2.1	2.1	2.1	
		V <sub>CC</sub> = 5.5 V	3.85	3.85	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	0.5	0.5	V
		V <sub>CC</sub> = 3 V	0.9	0.9	0.9	
		V <sub>CC</sub> = 5.5 V	1.65	1.65	1.65	
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	-50	-50	-50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	-4	-4	-4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V	-8	-8	-8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	50	50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	4	4	4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V	8	8	8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	100	100	100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V	20	20	20	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC240	SN74AHC240	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2	1.9	1.9	1.9	V
		3 V	2.9	3	2.9	2.9	2.9	
		4.5 V	4.4	4.5	4.4	4.4	4.4	
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48	2.48	
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8	3.8	
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V		0.1	0.1	0.1	0.1	V
		3 V		0.1	0.1	0.1	0.1	
		4.5 V		0.1	0.1	0.1	0.1	
	I <sub>OL</sub> = 4 mA	3 V		0.36	0.5	0.5	0.44	
	I <sub>OL</sub> = 8 mA	4.5 V		0.36	0.5	0.5	0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1	±1*	±1	±1	μA
I <sub>OZ</sub> †	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V		±0.25	±2.5	±2.5	±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4	40	40	40	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		3.5				pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† The parameter I<sub>OZ</sub> includes the input leakage current.

**SN54AHC240, SN74AHC240  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC240	SN74AHC240	UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	5.3*	7.5*	1*	9*	1	9
$t_{PHL}$				5.3*	7.5*	1*	9*	1	9
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	6.6*	10.6*	1*	12.5*	1	12.5
$t_{PZL}$				6.6*	10.6*	1*	12.5*	1	12.5
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	7.8*	11.5*	1*	12.5*	1	12.5
$t_{PLZ}$				7.8*	11.5*	1*	12.5*	1	12.5
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	7.8	11	1	12.5	1	12.5
$t_{PHL}$				7.8	11	1	12.5	1	12.5
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	9.1	14.1	1	16	1	16
$t_{PZL}$				9.1	14.1	1	16	1	16
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	10.3	14	1	16	1	16
$t_{PLZ}$				10.3	14	1	16	1	16
$t_{sk(o)}$			$C_L = 50 \text{ pF}$	1.5**				1.5	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC240	SN74AHC240	UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	3.6*	5.5*	1*	6.5*	1	6.5
$t_{PHL}$				3.6*	5.5*	1*	6.5*	1	6.5
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	4.7*	7.3*	1*	8.5*	1	8.5
$t_{PZL}$				4.7*	7.3*	1*	8.5*	1	8.5
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	5.2*	7.2*	1*	8.5*	1	8.5
$t_{PLZ}$				5.2*	7.2*	1*	8.5*	1	8.5
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	5.1	7.5	1	8.5	1	8.5
$t_{PHL}$				5.1	7.5	1	8.5	1	8.5
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	6.2	9.3	1	10.5	1	10.5
$t_{PZL}$				6.2	9.3	1	10.5	1	10.5
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	6.7	9.2	1	10.5	1	10.5
$t_{PLZ}$				6.7	9.2	1	10.5	1	10.5
$t_{sk(o)}$			$C_L = 50 \text{ pF}$	1**				1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

**noise characteristics,  $V_{CC} = 5$  V,  $C_L = 50$  pF,  $T_A = 25^\circ\text{C}$  (see Note 4)**

PARAMETER	SN74AHC240			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.6	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.6	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.6	V
$V_{IH(D)}$	High-level dynamic input voltage		3.5	V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

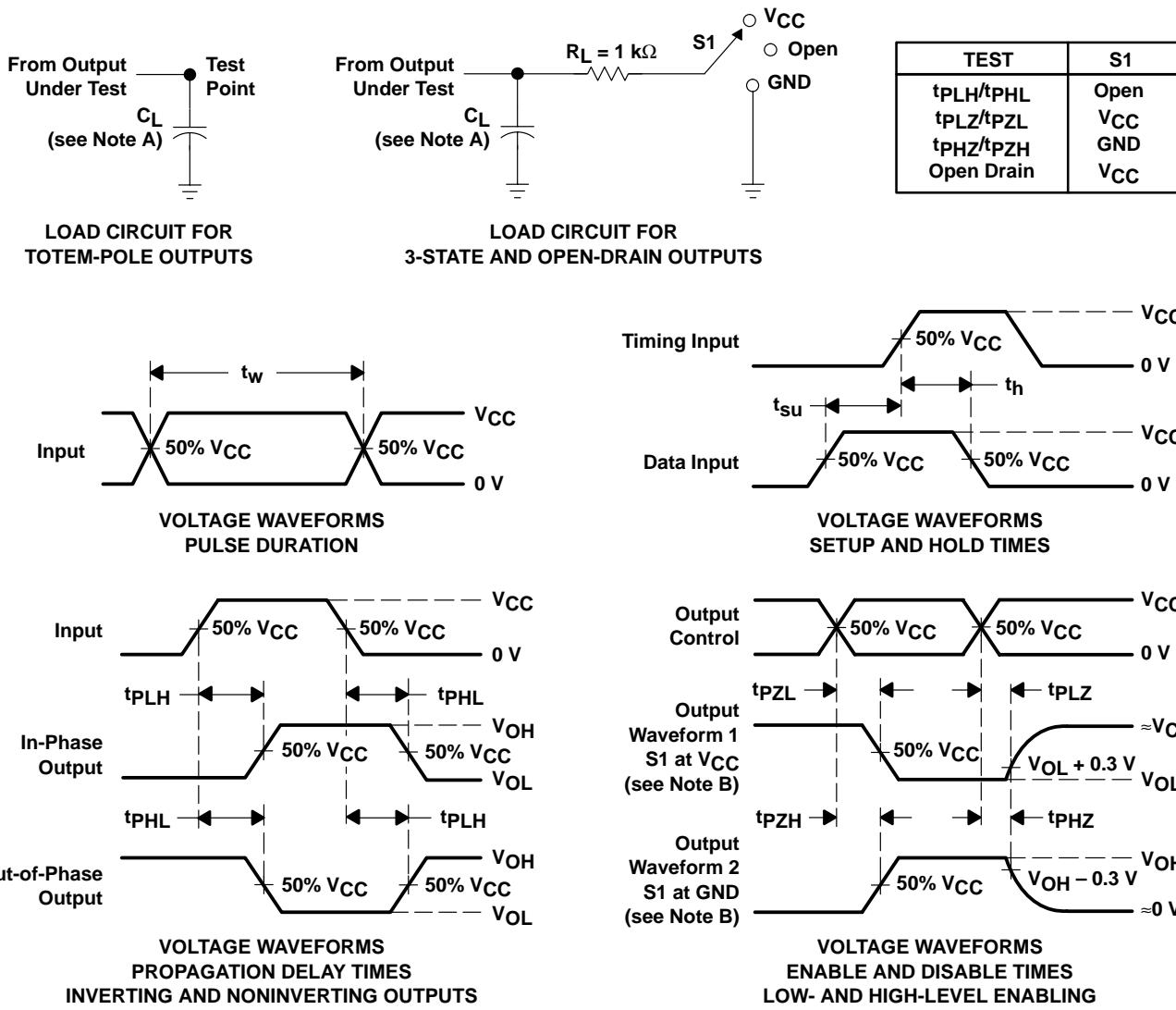
**operating characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1$ MHz	10	pF

# SN54AHC240, SN74AHC240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9680701Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701Q2A SNJ54AHC240FK	<a href="#">Samples</a>
5962-9680701QRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J	<a href="#">Samples</a>
5962-9680701QSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W	<a href="#">Samples</a>
SN74AHC240DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240	<a href="#">Samples</a>
SN74AHC240DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240	<a href="#">Samples</a>
SN74AHC240N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC240N	<a href="#">Samples</a>
SN74AHC240NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240	<a href="#">Samples</a>
SN74AHC240PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA240	<a href="#">Samples</a>
SN74AHC240PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA240	<a href="#">Samples</a>
SN74AHC240PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA240	<a href="#">Samples</a>
SNJ54AHC240FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701Q2A SNJ54AHC240FK	<a href="#">Samples</a>
SNJ54AHC240J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J	<a href="#">Samples</a>
SNJ54AHC240W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3) MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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#### **OTHER QUALIFIED VERSIONS OF SN54AHC240, SN74AHC240 :**

- Catalog : [SN74AHC240](#)
- Military : [SN54AHC240](#)

**NOTE: Qualified Version Definitions:**

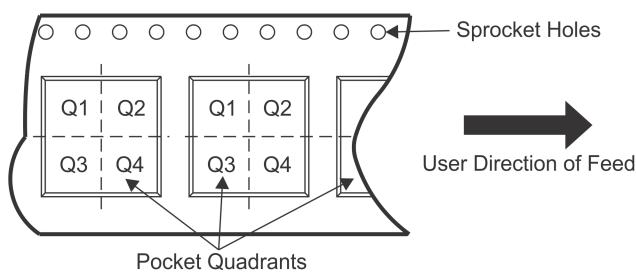
- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


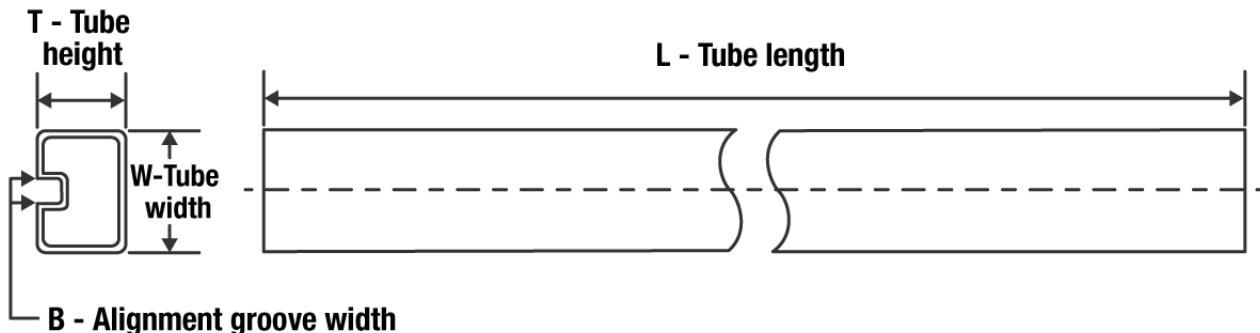
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC240NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC240NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHC240PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

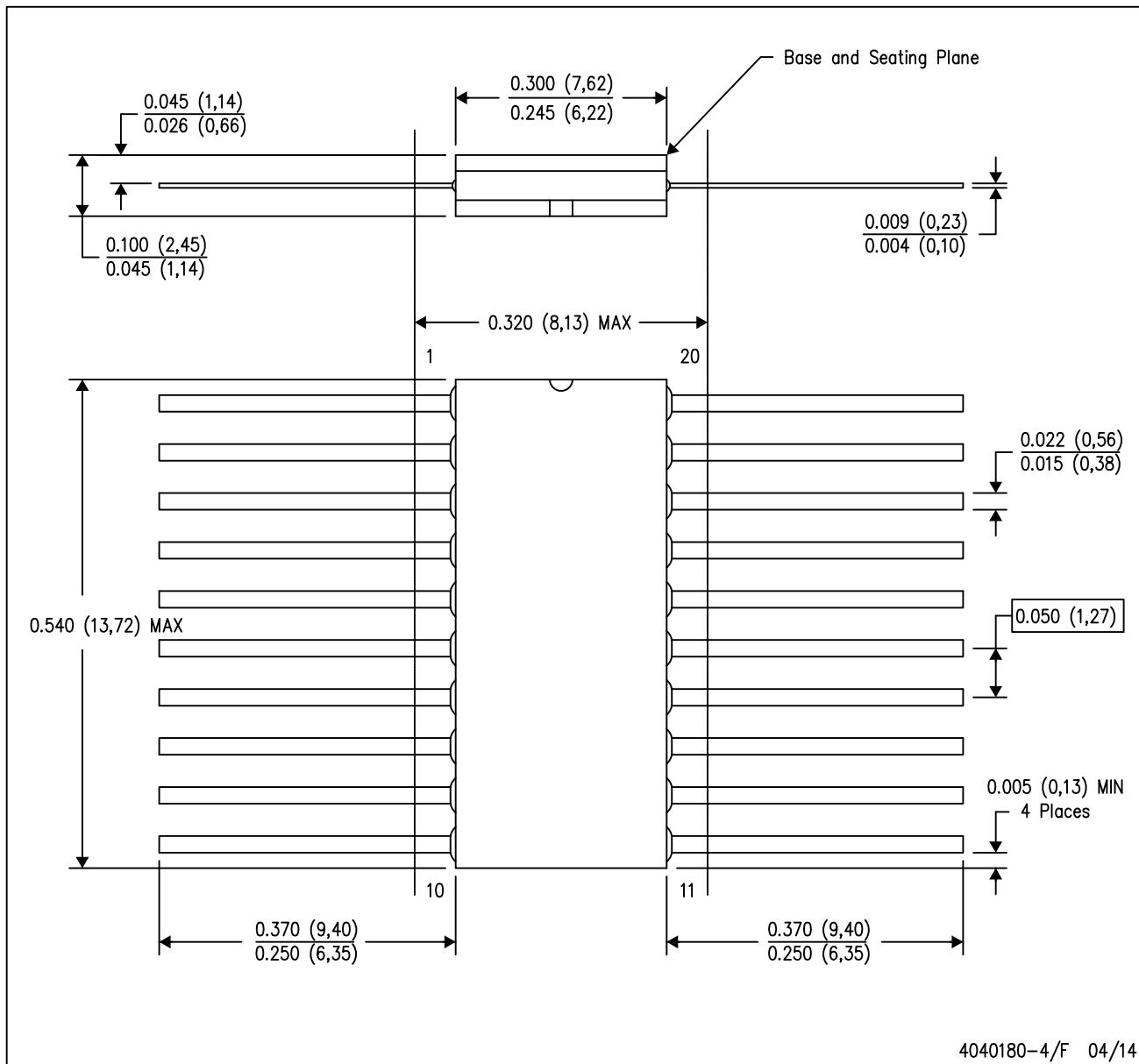
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
5962-9680701Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74AHC240DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AHC240N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC240PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54AHC240FK	FK	LCCC	20	1	506.98	12.06	2030	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

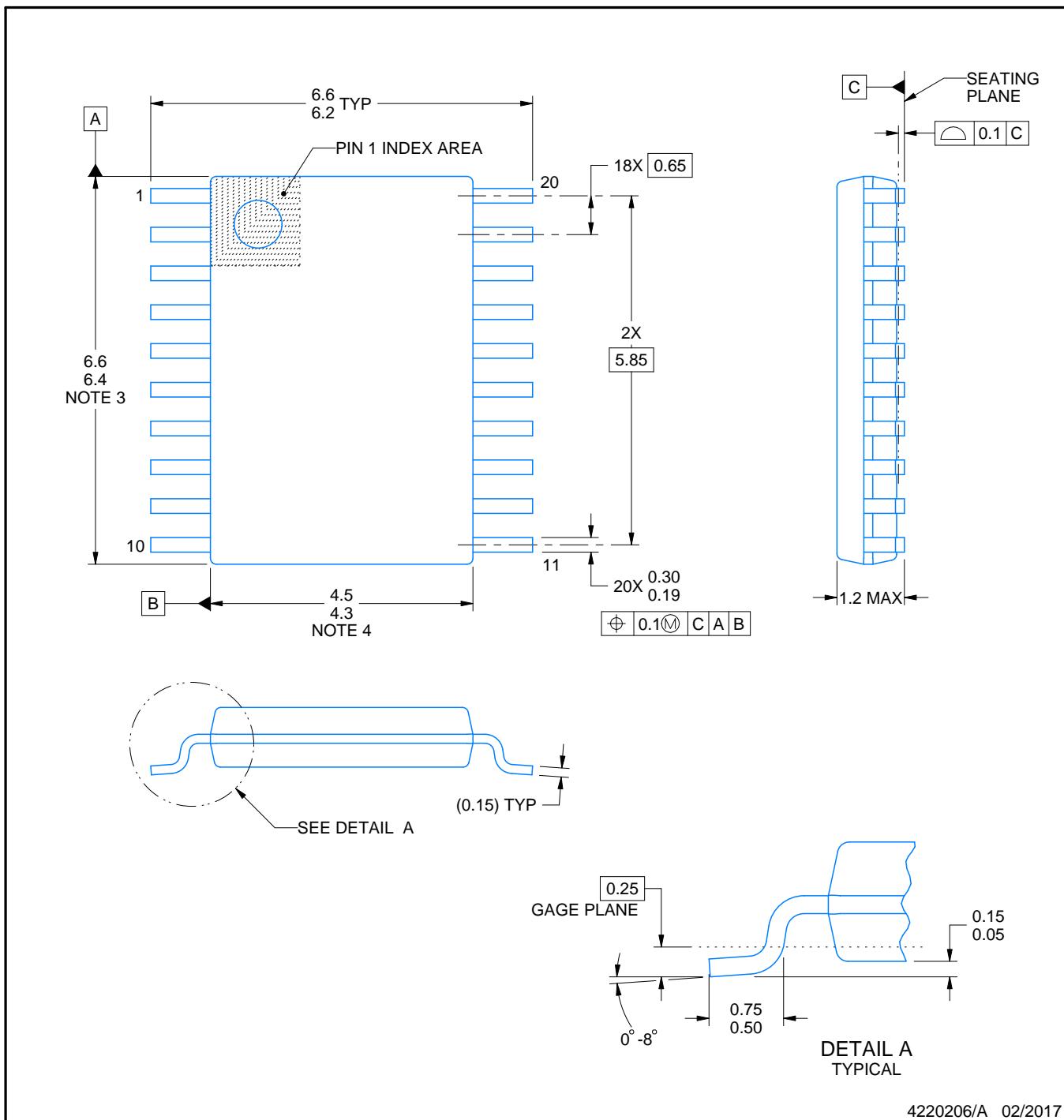
## PACKAGE OUTLINE

**PW0020A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

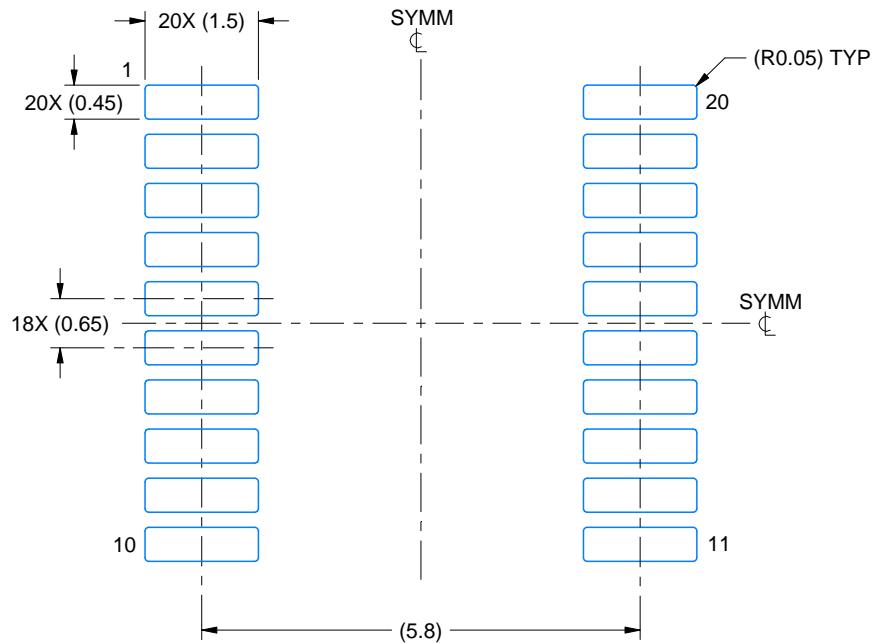
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

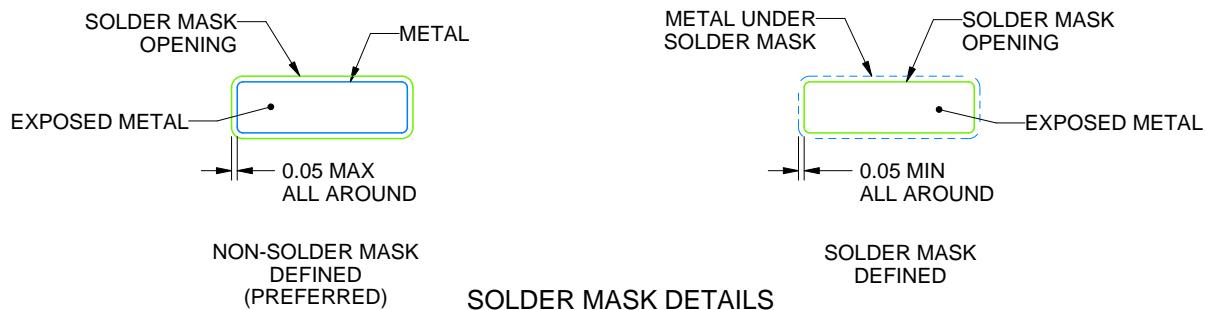
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

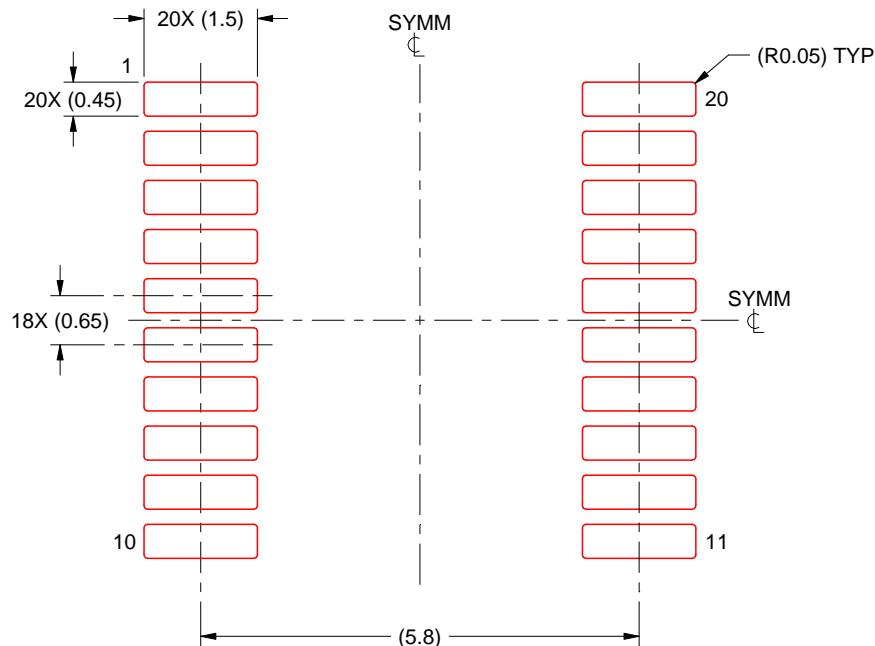
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

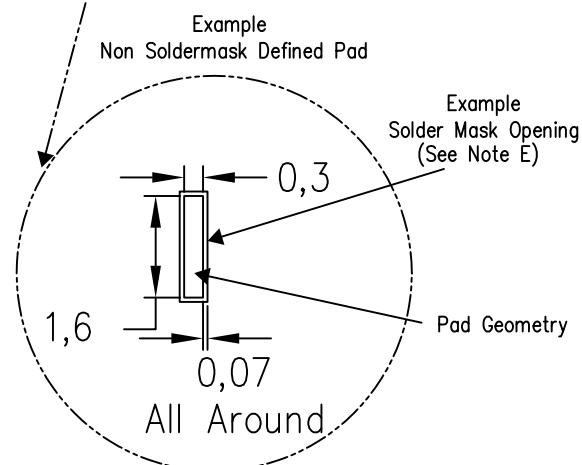
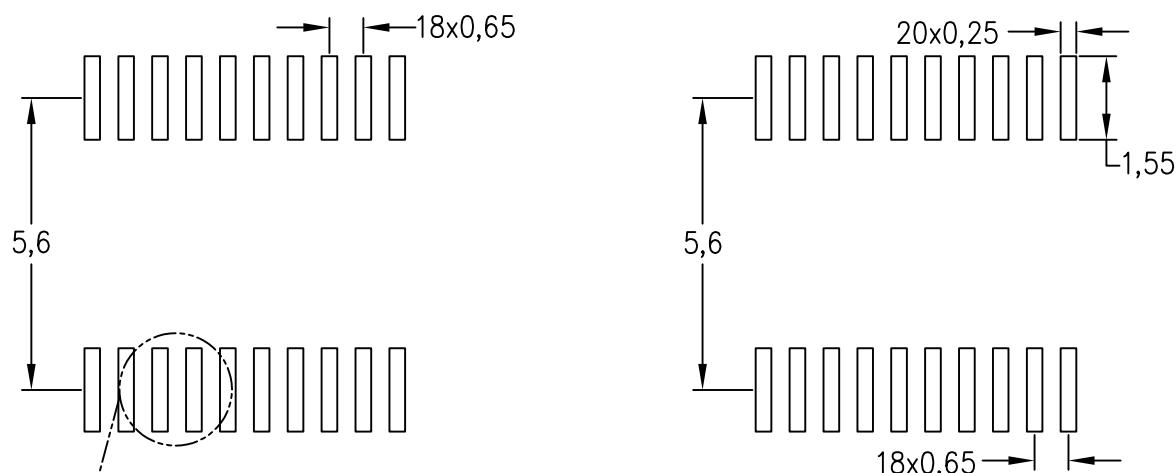
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).

4211284-5/G 08/15

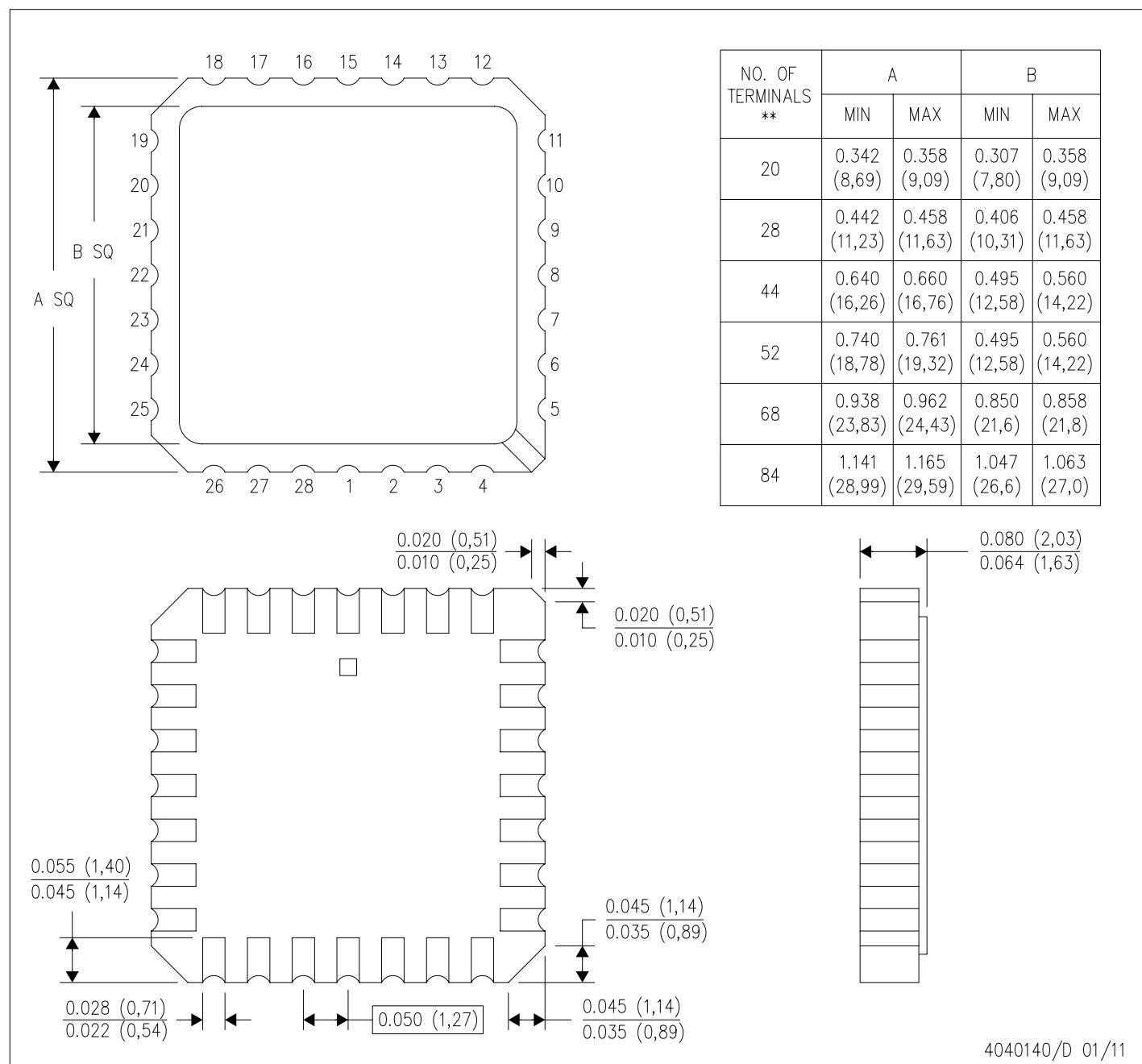
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



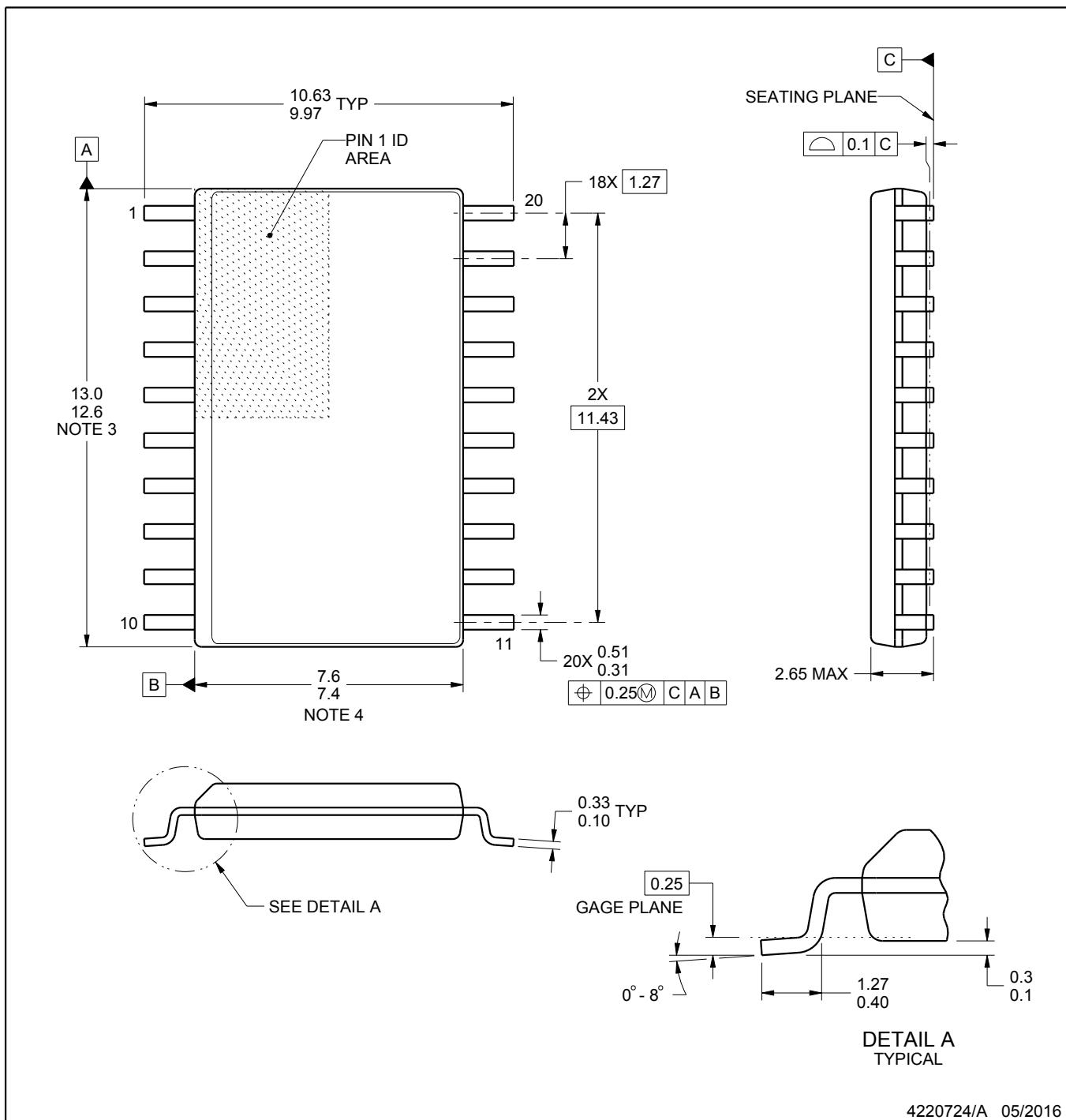
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



## NOTES:

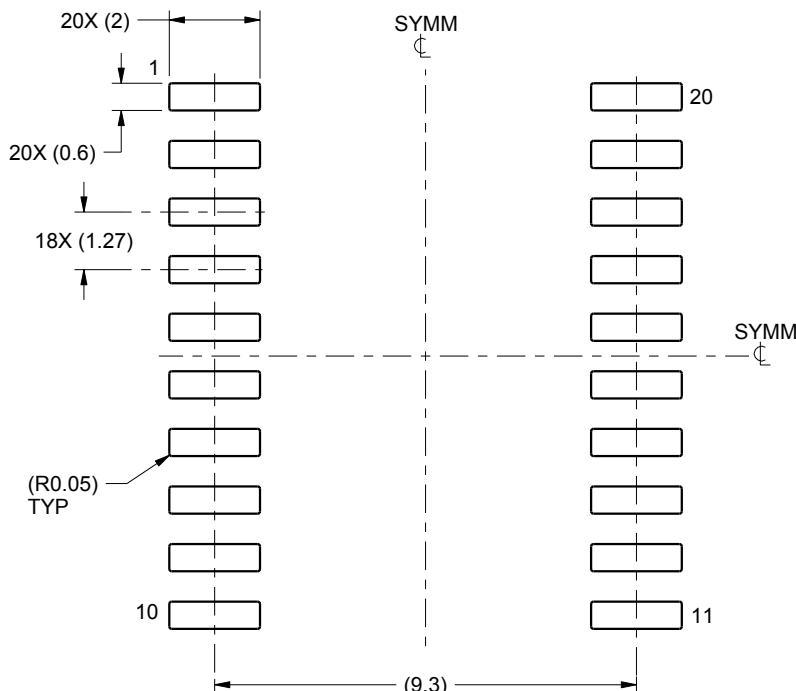
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

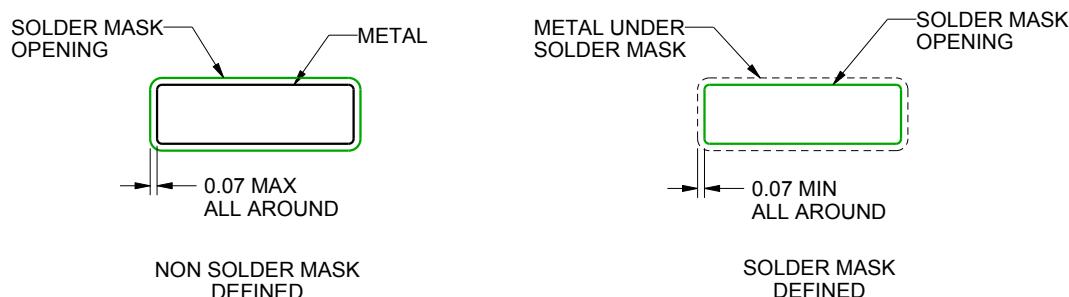
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

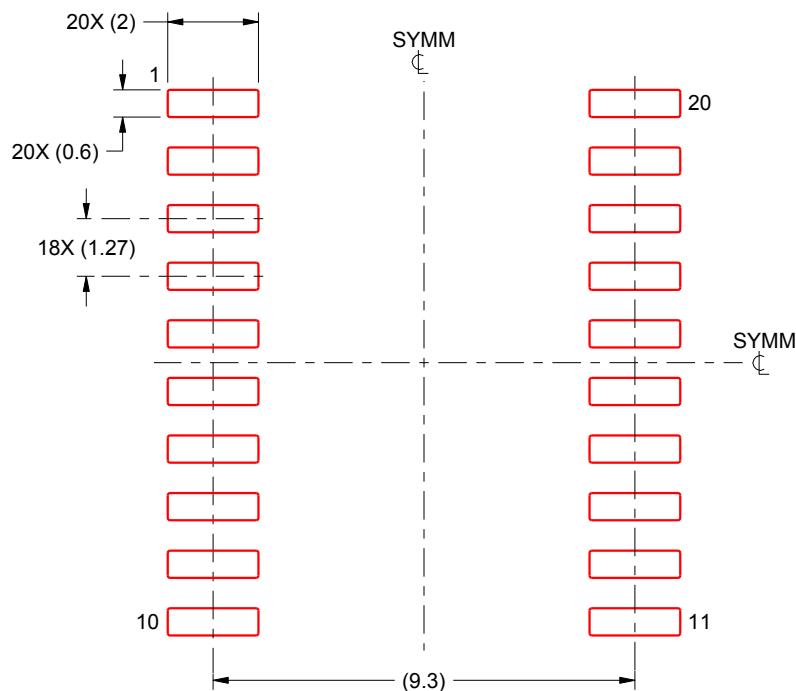
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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