TEXAS INSTRUMENTS
TLC6983
SLVSFT9 – DECEMBER 2020

TLC6983 48x16 Common Cathode Matrix LED Display Driver with Ultra Low Power

1 Features

- Separated V_{CC} and $V_{R/G/B}$ power supply
  - V_{CC} voltage range: 2.5 V - 5.5 V
  - $V_{R/G/B}$ voltage range: 2.5 V - 5.5 V
- 48 current source channels from 0.2 mA to 20 mA
  - Channel-to-channel accuracy: ±0.5% (typ.), ±2% (max.); device-to-device accuracy: ±0.5% (typ.), ±2% (max.)
  - Low knee voltage: 0.26 V (max.) when I_{OUT} = 5 mA
  - 3-bits (8 steps) global brightness control
  - 8-bits (256 steps) color brightness control
  - Maximum 16-bits (65536 steps) PWM grayscale control
- 16 scan line switches with 190-mΩ $R_{DS(ON)}$
- Ultra-low power consumption
  - Independent V_{CC} down to 2.5 V
  - Lowest I_{CC} down to 3.9 mA with 50-MHz GCLK
  - Intelligent power saving mode
- Built-in SRAM to support 1 - 32 multiplexing
  - Single device with 16 multiplexing to support 32 × 16 LEDs or 16 × 16 RGB pixels
  - Dual devices stackable with 32 multiplexing to support 96 × 32 LEDs or 32 × 32 RGB pixels
- High speed and low EMI Continuous Clock Series Interface (CCSI)
  - Only three wires: SCLK/SIN/SOUT
  - External 25-MHz (max.) SCLK with dual-edge transimission mechanism (internal 50 MHz)
  - Internal frequency multiplier to support GCLK range from 40 MHz - 160 MHz
- Optimized display performance
  - Upside and downside ghosting removal
  - Low grayscale enhancement
  - LED open/short/weak short detection and removal

2 Applications

- Narrow Pixel Pitch (NPP) LED display
- Mini & micro-LED products

3 Description

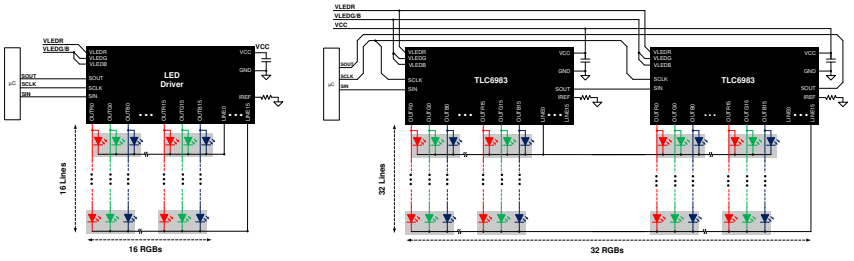
With the pixel density getting higher in narrow pixel pitch LED Display or Mini & Micro-LED products, there are urgent demands for LED drivers to address those critical challenges: ultra high integration to meet the strict board space limitation, ultra low power to minimize the system level power dissipation, new interface to enable high data refresh rate with low EMI impact, excellent display performance to serve the growing needs of higher display quality.

The TLC6983 is a highly integrated common cathode matrix LED display driver with 48 constant current sources and 16 scanning FETs. A single TLC6983 is capable of driving 16 × 16 RGB LED pixels while stacking two TLC6983s can drive 32 × 32 RGB LED pixels. To achieve low power consumption, the device supports separated power supplies for the red, green, and blue LEDs by its common cathode structure. Furthermore, the operation power of the TLC6983 is significantly reduced by ultra-low operation voltage range (Vcc down to 2.5 V) and ultra-low operation current (Icc down to 3.9 mA).

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TLC6983	VQFN (76)	9 mm x 9 mm
	BGA (96)	6 mm x 6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TLC6983 with Single Device or Dual Devices Stackable Connection

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
December 2020	*	Initial release.

5 Description (continued)

The TLC6983 implements a high speed dual-edge transmission interface to support high device count daisy-chained and high refresh rate while minimizing electrical-magnetic interference (EMI). The device supports up to 25-MHz SCLK (external) and up to 160-MHz GCLK (internal). Meanwhile, the device integrates enhanced circuits and intelligent algorithms to solve the various display challenges in Narrow Pixel Pitch (NPP) LED display applications and Mini / Micro-LED products: Dim at the fist scan line, Upper and downside ghosting, Non-uniformity in low grayscale, Coupling, and Caterpillar caused by open or short LEDs, which make the TLC6983 a perfect choice in such applications.

The TLC6983 also implements LED open/weak short/short detections and removals during operations and can also report this information to the accompanying digital processor.

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.3 Trademarks

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6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6983RRFR	ACTIVE	VQFN	RRF	76	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6983	Samples
TLC6983ZXLR	ACTIVE	NFBGA	ZXL	96	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	TLC6983	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

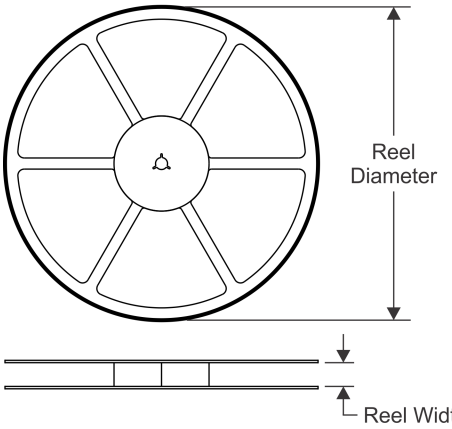
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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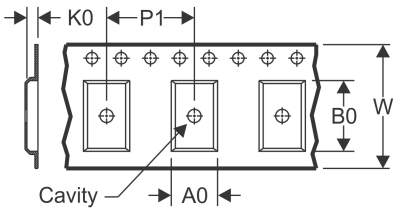
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

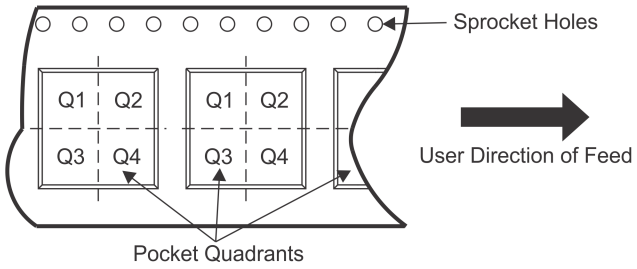


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

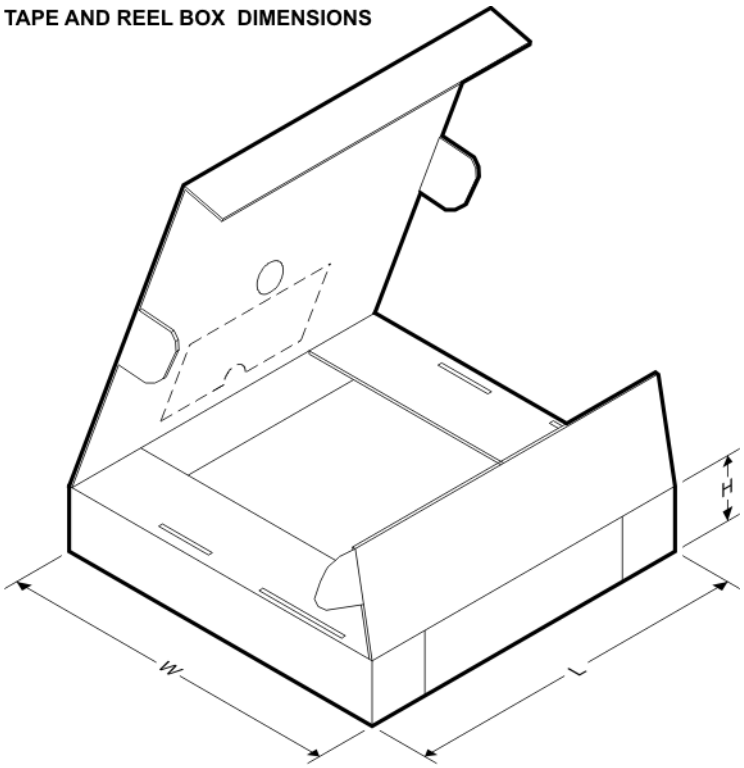
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6983RRFR	VQFN	RRF	76	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TLC6983ZXLR	NFBGA	ZXL	96	2500	330.0	16.4	6.3	6.3	2.1	8.0	16.0	Q1

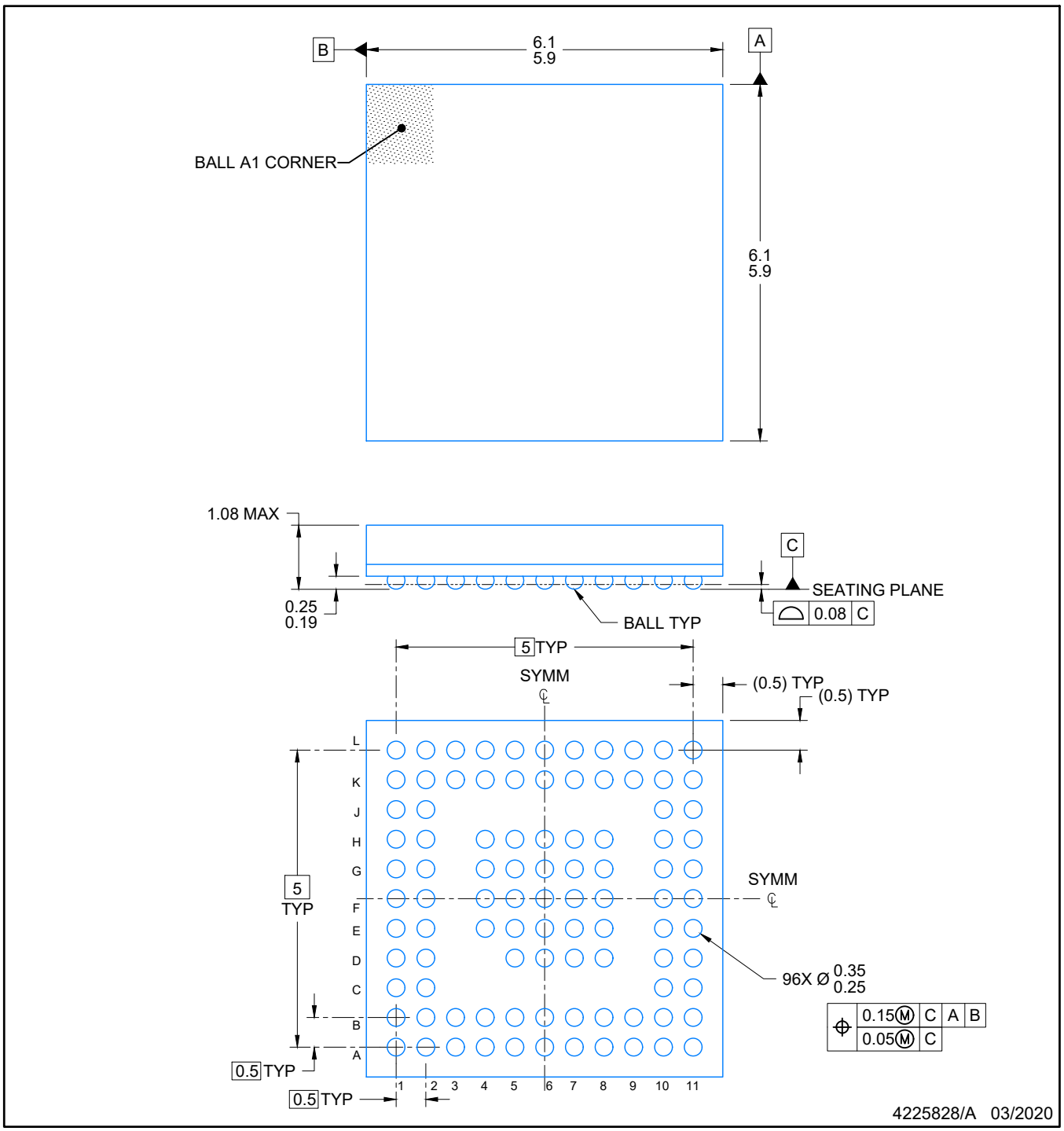
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6983RRFR	VQFN	RRF	76	2000	367.0	367.0	35.0
TLC6983ZXLR	NFBGA	ZXL	96	2500	336.6	336.6	31.8

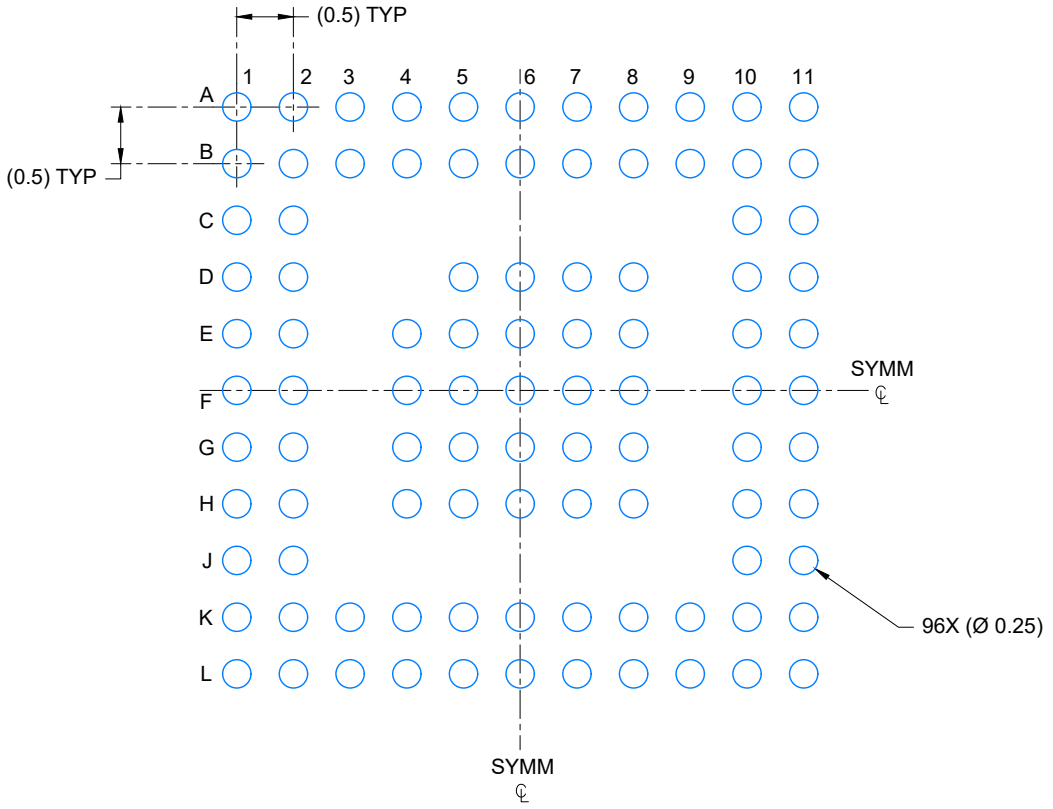
PLASTIC BALL GRID ARRAY



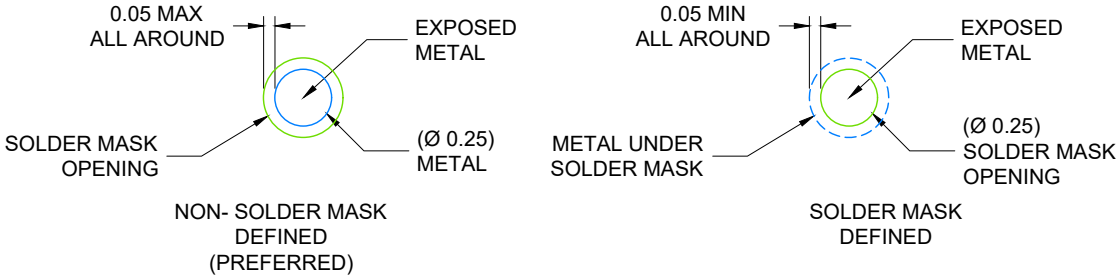
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

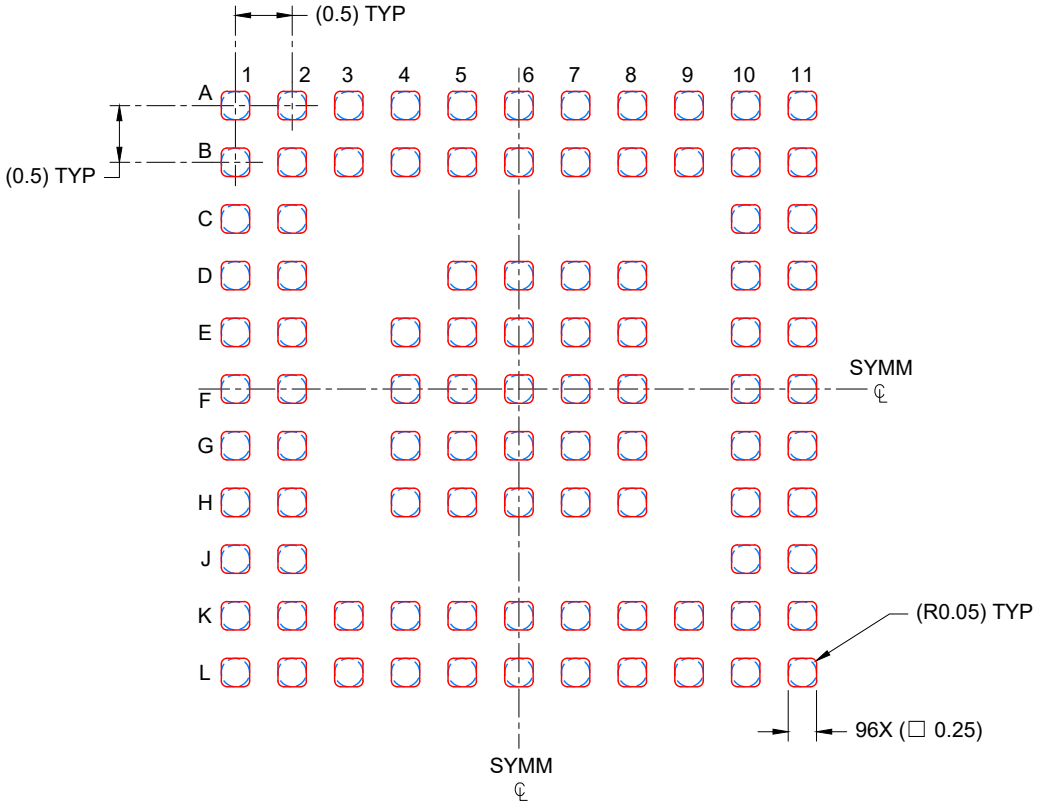


SOLDER MASK DETAILS
NOT TO SCALE

4225828/A 03/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 15X

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NOTES: (continued)

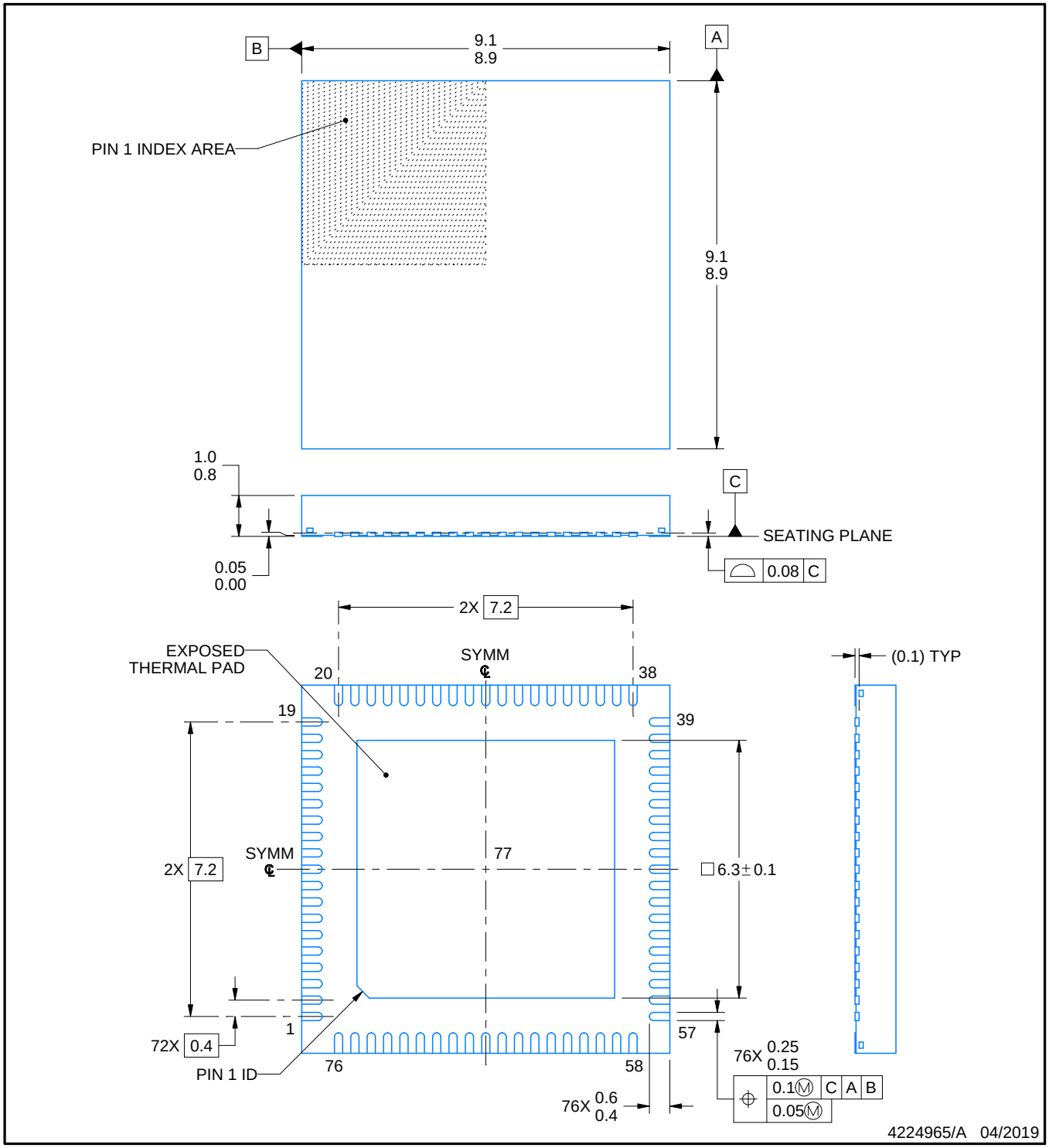
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

RRF0076A

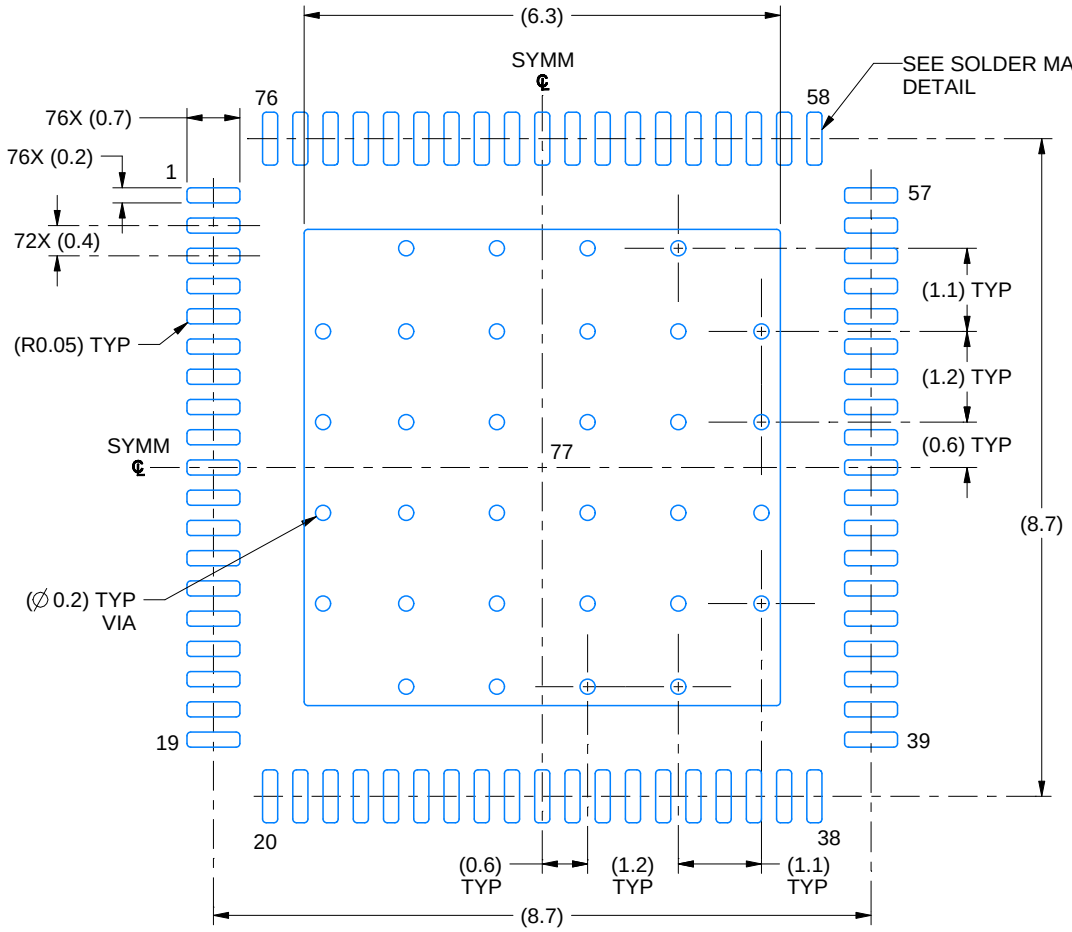
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

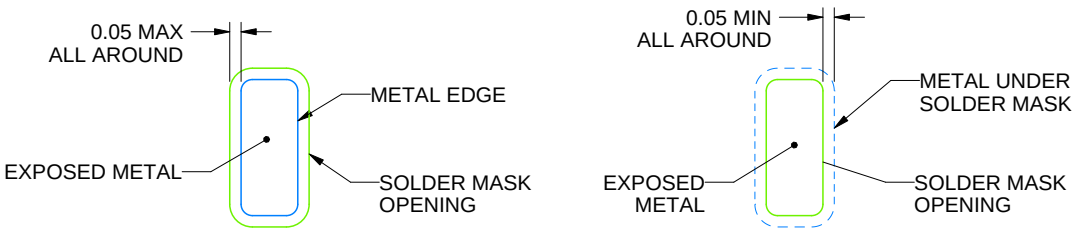


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

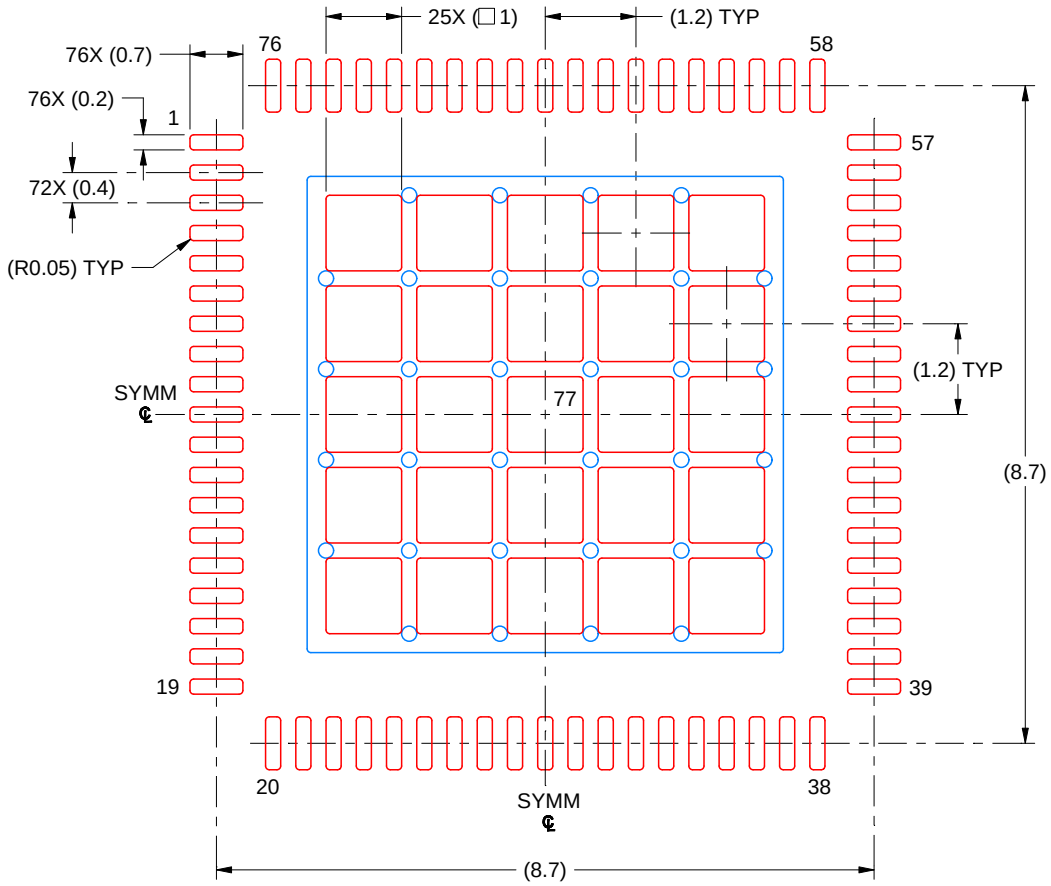


SOLDER MASK DETAILS

4224965/A 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 77
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224965/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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