

具有 $\pm 15\text{kV}$ ESD 保护功能的 TRIS3232 3V 至 5.5V 多通道 RS-232 线路驱动器和接收器

1 特性

- RS-232 总线终端 ESD 保护大于 $\pm 15\text{kV}$ 人体放电模型 (HBM)
- 符合或超出 TIA/EIA-232-F 和 ITU V.28 标准的要求
- 由 3V 至 5.5V V_{CC} 电源供电
- 运行速率高达 250kbps
- 两个驱动器和两个接收器
- 低电源电流: $300\ \mu\text{A}$ (典型值)
- 外部电容器: $4 \times 0.1\ \mu\text{F}$
- 接受 5V 逻辑输入及 3.3V 电源
- 备选高速端子兼容器件 (1Mbps)
 - SN65C3232 (-40°C 至 85°C)
 - SN75C3232 (0°C 至 70°C)

2 应用

- 工业 PC
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

3 说明

TRIS3232 器件由两个线路驱动器、两个线路接收器和一个双路电荷泵电路组成, 具有端子间 (串行端口连接端子, 包括 GND) $\pm 15\text{kV}$ ESD 保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持

通过一个 3V 至 5.5V 电源供电运行。这些器件以高达 250kbps 的数据信号传输速率和最大值为 $30\text{V}/\mu\text{s}$ 的驱动器输出压摆率运行。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TRIS3232	SOIC (16)	9.90mm x 3.91mm
	SSOP (16)	6.20mm x 5.30mm
	SOIC 宽 (16)	10.30mm x 7.50mm
	TSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

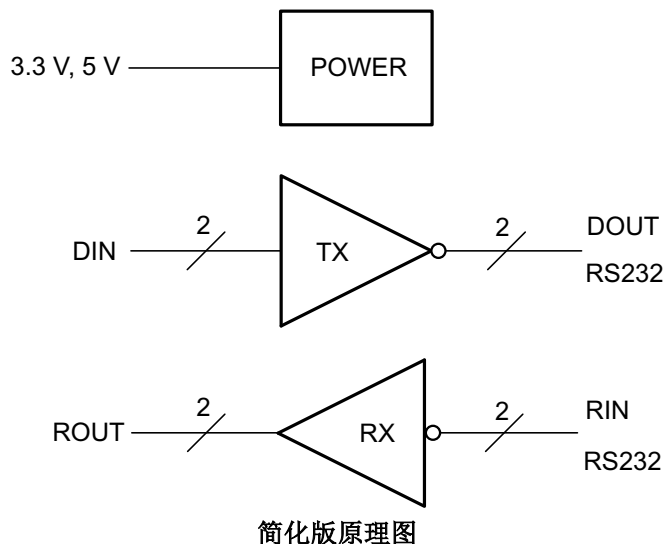


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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (July 2015) to Revision B (June 2021)	Page
• 添加了应用：工业 PC、有线网络、数据中心和企业级计算.....	1
• Added additional thermal parameters for all packages in <i>Thermal Information</i> table.....	5

Changes from Revision * (July 2007) to Revision A (June 2015)	Page
• 更改了引脚功能表、ESD 等级表、热性能信息表、典型特性部分、详细说明部分、电源建议和布局部分、器件和文档支持和机械、封装和可订购信息.....	1
• Deleted <i>Ordering Information</i> table.....	3

5 Pin Configuration and Functions

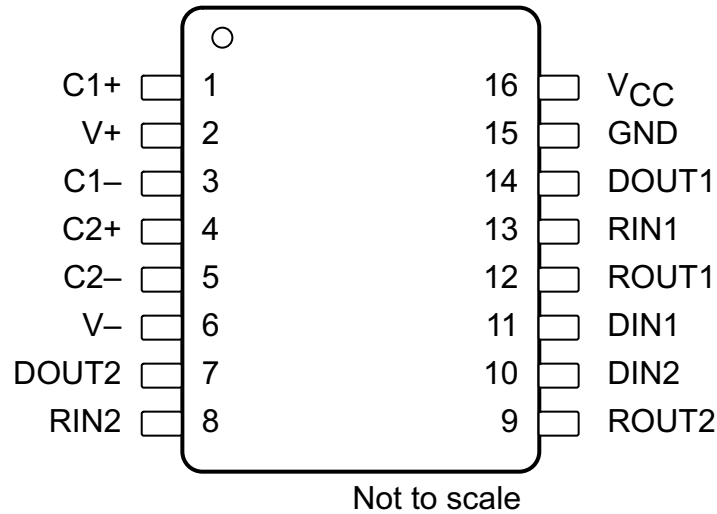


图 5-1. D, DB, DW, PW Packages 16-Pin SOIC, SSOP, SOIC (Wide), TSSOP Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
C1 -	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2 -	5	—	Negative lead of C2 capacitor
DIN1	11	I	Logic data input (from UART)
DIN2	10	I	Logic data input (from UART)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
DOUT2	7	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
RIN1	13	I	RS232 line data input (from remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT1	12	O	Logic data output (to UART)
ROUT2	9	O	Logic data output (to UART)
V+	2	O	Positive charge pump output for storage capacitor only
V -	6	O	Negative charge pump output for storage capacitor only
V _{CC}	16	—	Supply Voltage, Connect to external 3-V to 5.5-V power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾	– 0.3	6	V
V ₊	Positive output supply voltage ⁽²⁾	– 0.3	7	V
V _–	Negative output supply voltage ⁽²⁾	– 7	0.3	V
V ₊ – V _–	Supply voltage difference ⁽²⁾		13	V
V _I	Input voltage	Drivers	– 0.3	6
		Receivers	– 25	25
V _O	Output voltage	Drivers	– 13.2	13.2
		Receivers	– 0.3	V _{CC} + 0.3
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature	– 65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN, DOUT, and GND pins ⁽¹⁾	±15000
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 All other pins ⁽¹⁾	±3000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see [图 9-1](#))⁽¹⁾

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver high-level input voltage	DIN	V _{CC} = 3.3 V	2		V
			V _{CC} = 5 V	2.4		
V _{IL}	Driver low-level input voltage	DIN			0.8	V
V _I	Driver input voltage	DIN		0	5.5	V
	Receiver input voltage	RIN		– 25	25	
T _A	Operating free-air temperature	TRS3232C		0	70	°C
		TRS3232I		– 40	85	°C

- (1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TRS3232				UNIT
	D (SOIC)	DB (SSOP)	DW (SOIC-wide)	PW (TSSOP)	
	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	73	82	57	108	°C/W
$R_{\theta JC(top)}$ Junction-to-case (bottom) thermal resistance	38.5	45.8	32.4	39	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	36.3	44.6	31.9	54.4	°C/W
ψ_{JT} Junction-to-top characterization parameter	8.0	11.1	8.4	3.3	°C/W
ψ_{JB} Junction-to-board characterization parameter	36.0	44	31.5	53.8	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics—Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾ (see 图 9-1)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I_{CC} Supply current	No load, $V_{CC} = 3.3 \text{ V to } 5 \text{ V}$		0.3	1	mA

- (1) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.
 (2) Test conditions are $C1 - C4 = 0.1 \mu\text{F}$ at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $C1 = 0.047 \mu\text{F}$, $C2 - C4 = 0.33 \mu\text{F}$ at $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.

6.6 Electrical Characteristics—Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see 图 9-1)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH} High-level output voltage	D_{OUT} at $R_L = 3 \text{ k}\Omega$ to GND, $D_{IN} = \text{GND}$	5	5.4		V
V_{OL} Low-level output voltage	D_{OUT} at $R_L = 3 \text{ k}\Omega$ to GND, $D_{IN} = V_{CC}$	-5	-5.4		V
I_{IH} High-level input current	$V_I = V_{CC}$		± 0.01	± 1	μA
I_{IL} Low-level input current	V_I at GND		± 0.01	± 1	μA
I_{OS} ⁽³⁾ Short-circuit output current	$V_{CC} = 3.6 \text{ V}$ $V_O = 0 \text{ V}$		± 35	± 60	mA
	$V_{CC} = 5.5 \text{ V}$ $V_O = 0 \text{ V}$				
r_O Output resistance	$V_{CC} = 0 \text{ V}$, $V_+ = 0 \text{ V}$, and $V_- = 0 \text{ V}$ $V_O = \pm 2 \text{ V}$	300	10M		Ω

- (1) Test conditions are $C1 - C4 = 0.1 \mu\text{F}$ at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $C1 = 0.047 \mu\text{F}$, $C2 - C4 = 0.33 \mu\text{F}$ at $V_{CC} = 5 \text{ V} \pm 0.5$
 (2) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.
 (3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Electrical Characteristics—Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see 图 9-1)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL} Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+} Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
	V _{CC} = 5 V		1.8	2.4	
V _{IT-} Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
	V _{CC} = 5 V	0.8	1.5		
V _{hys} Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
r _I Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see 图 9-1)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
	Maximum data rate	R _L = 3 kΩ, One D _{OUT} switching,	C _L = 1000 pF See 图 7-1	150	250		kbps
t _{sk(p)}	Driver Pulse skew ⁽³⁾	R _L = 3 kΩ to 7 kΩ,	C _L = 150 to 2500 pF See 图 7-2		300		ns
SR(tr)	Driver Slew rate, transition region (see 图 7-1)	R _L = 3 kΩ to 7 kΩ, V _{CC} = 5 V	C _L = 150 to 1000 pF	6		30	V/ μ s
			C _L = 150 to 2500 pF	4		30	
t _{PLH}	Receiver Propagation delay time, low- to high-level output	C _L = 150 pF		300			ns
t _{PHL}	Receiver Propagation delay time, high- to low-level output			300			ns
t _{sk(p)}	Receiver Pulse skew ⁽¹⁾			300			ns

(1) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

6.9 Typical Characteristics

$V_{CC} = 3.3\text{ V}$

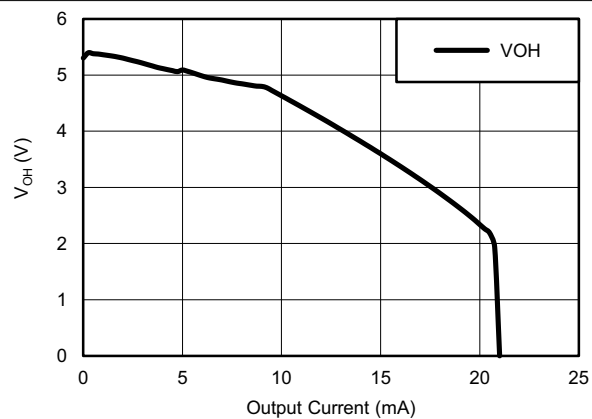


图 6-1. DOUT V_{OH} vs Load Current, Both Drivers Loaded

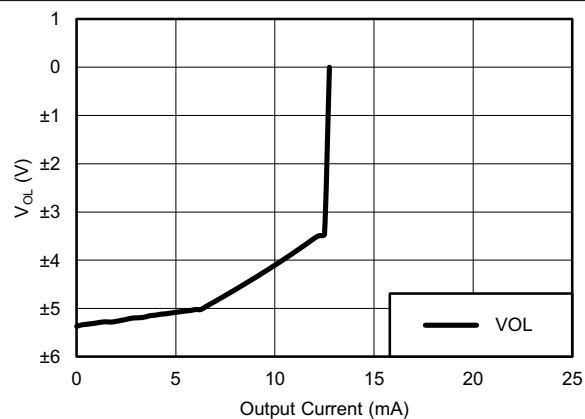
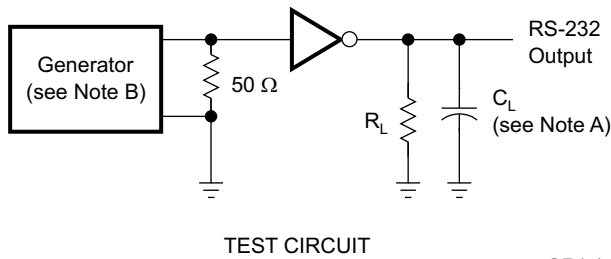
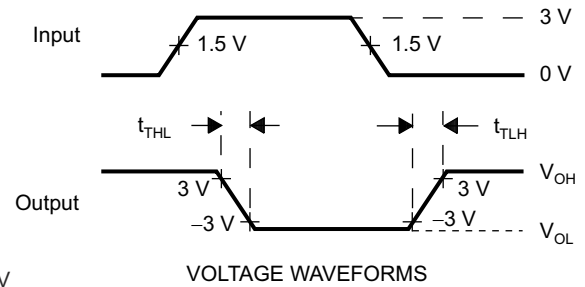


图 6-2. DOUT V_{OL} vs Load Current, Both Drivers Loaded

7 Parameter Measurement Information

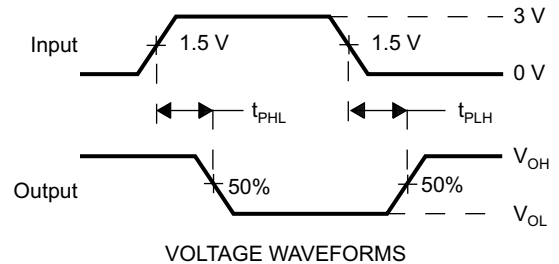
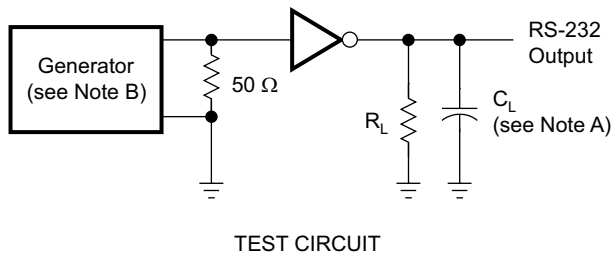


$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$



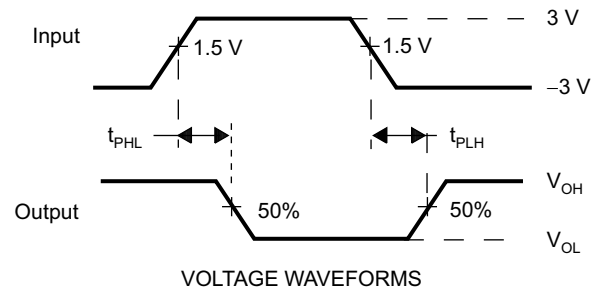
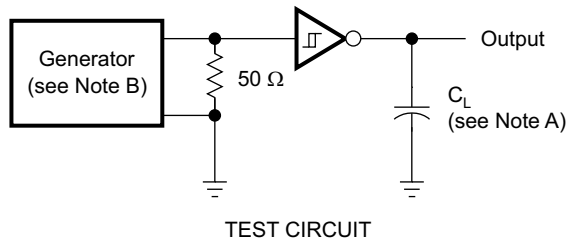
- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-1. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-2. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

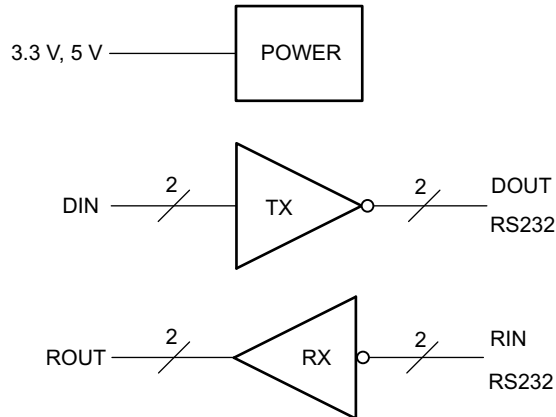
图 7-3. Receiver Propagation Delay Times

8 Detailed Description

8.1 Overview

The TRS3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbps and a maximum of 30-V/ μ s driver output slew rate. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V_+ and V_- pins using a charge pump that requires four external capacitors.

8.3.2 RS232 Driver

Two drivers interface the standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input results in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.4 Device Functional Modes

表 8-1. Each Driver

INPUT DIN ⁽¹⁾	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

表 8-2. Each Receiver

INPUT RIN ⁽¹⁾	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

8.4.1 V_{CC} Powered by 3 V to 5.5 V

The device is in normal operation.

8.4.2 V_{CC} Unpowered, V_{CC} = 0 V

When the TRS3232 device is unpowered, it can be safely connected to an active remote RS232 device.

9 Application and Implementation

Note

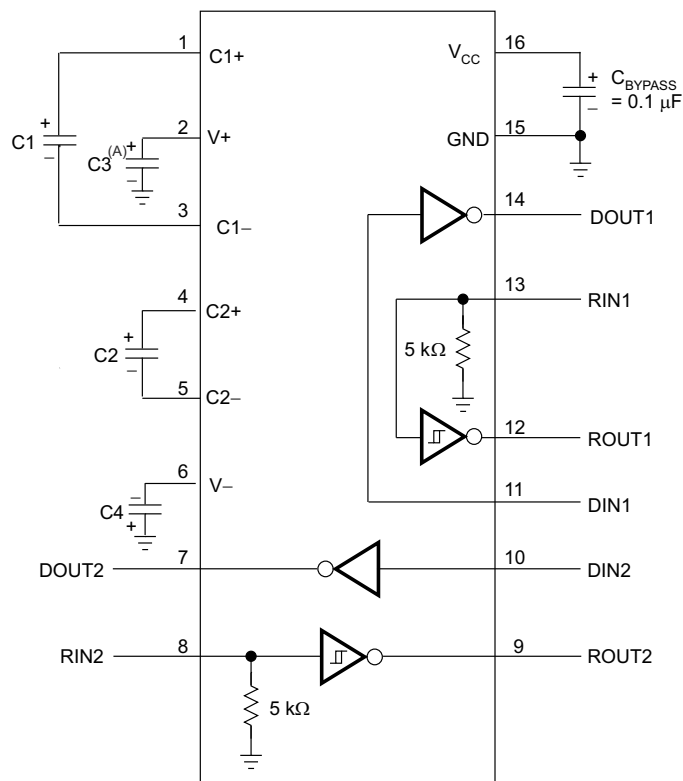
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TRS3232 is designed to convert single-ended signals into RS232-compatible signals, and vice-versa.

This device can be used in any application where an RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector.

9.2 Typical Application



- A. C3 can be connected to V_{CC} or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.
- D. See 表 9-1 for capacitor values.

图 9-1. Typical Operating Circuit

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V
 - 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbites

表 9-1. V_{CC} versus Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

9.2.2 Detailed Design Procedure

For proper operation, add capacitors as shown in 图 9-1 和 表 9-1.

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curve

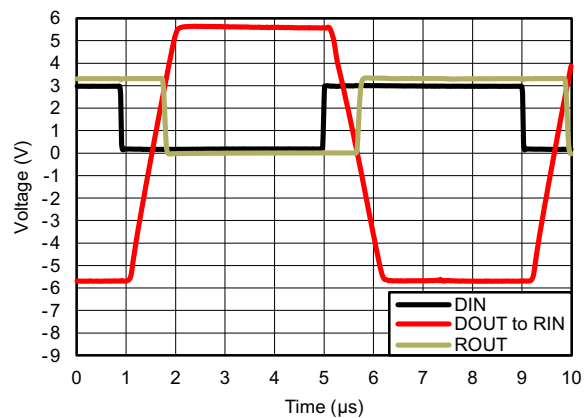


图 9-2. 250 kbps Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3 V

10 Power Supply Recommendations

V_{CC} must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using 表 9-1.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

11.2 Layout Example

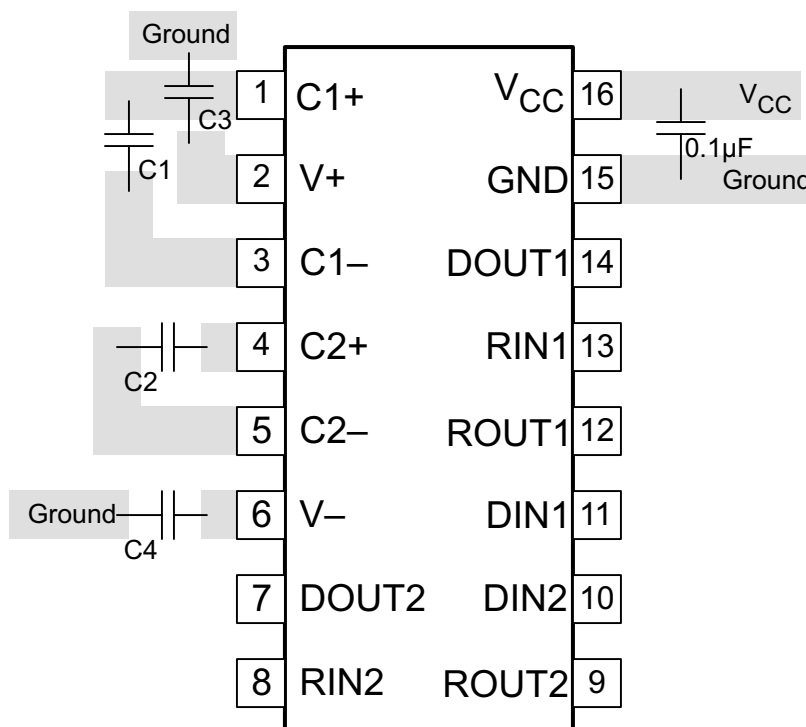


图 11-1. Layout Diagram

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

12.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3232CDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32C	Samples
TRS3232CDR	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232C	
TRS3232CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232C	Samples
TRS3232CPW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32C	
TRS3232IDR	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232I	
TRS3232IPW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32I	
TRS3232IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3232CDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRS3232CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS3232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3232CDBR	SSOP	DB	16	2000	853.0	449.0	35.0
TRS3232CDR	SOIC	D	16	2500	340.5	336.1	32.0
TRS3232CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TRS3232IDR	SOIC	D	16	2500	340.5	336.1	32.0
TRS3232IPWR	TSSOP	PW	16	2000	853.0	449.0	35.0
TRS3232IPWR	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE

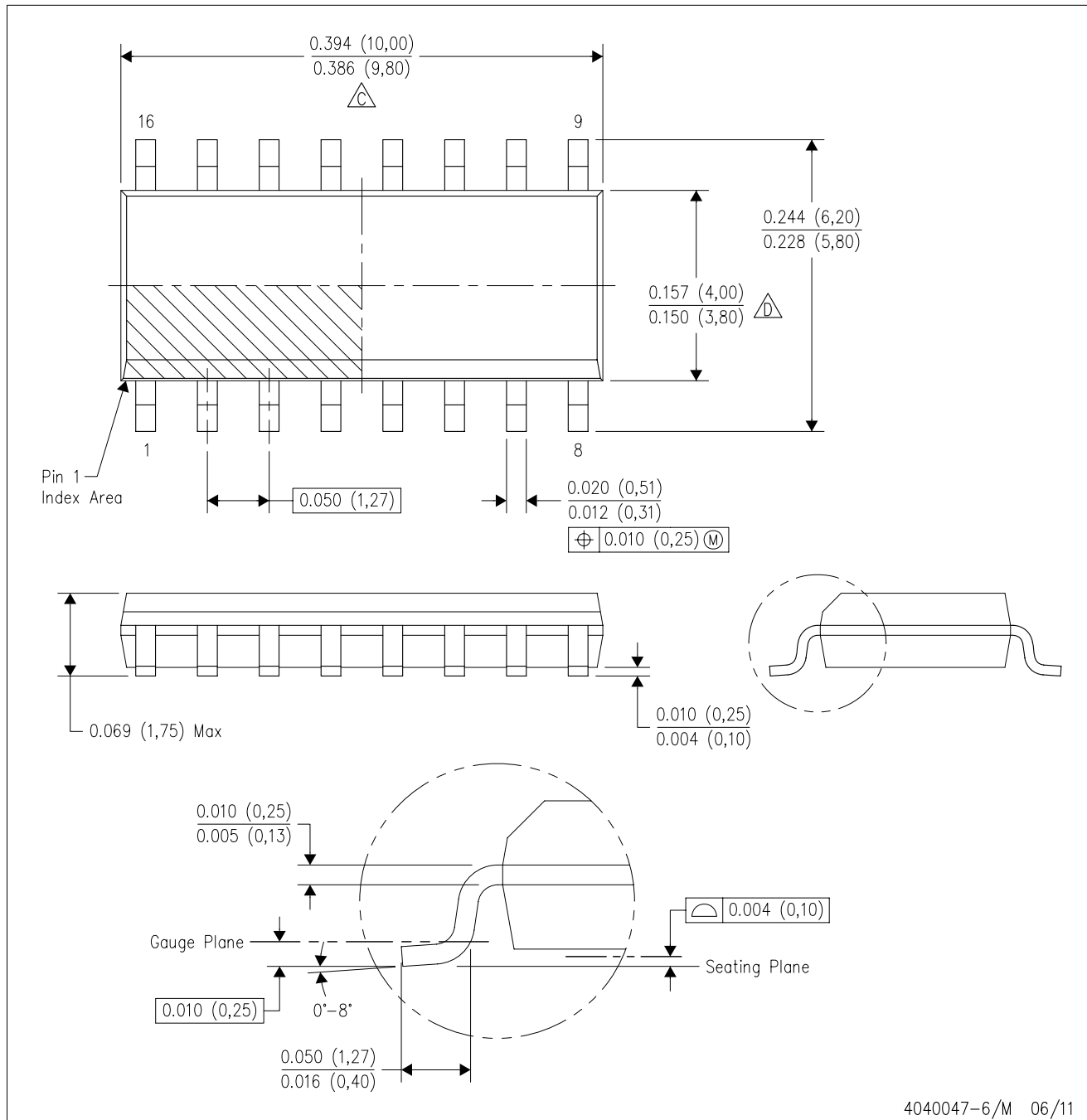


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TRS3232CPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TRS3232IPW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

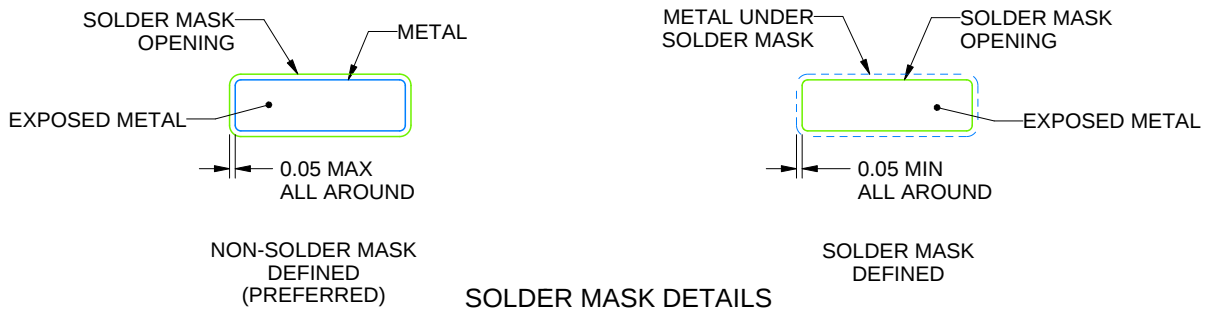
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

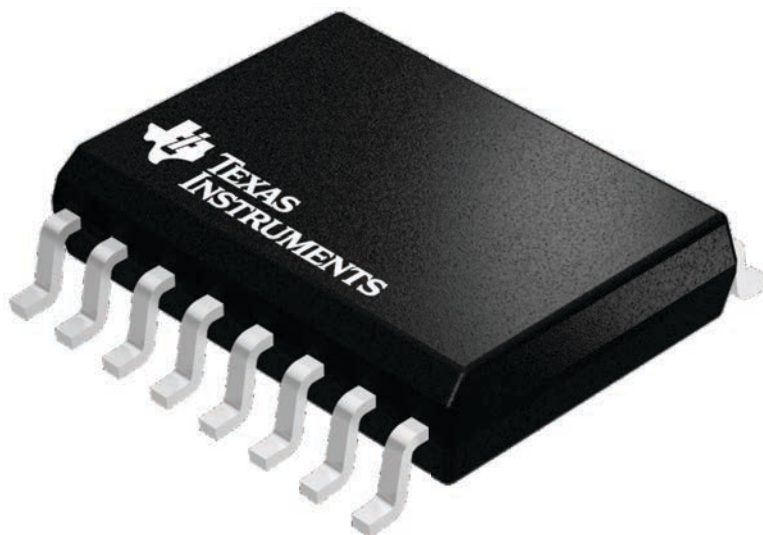
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

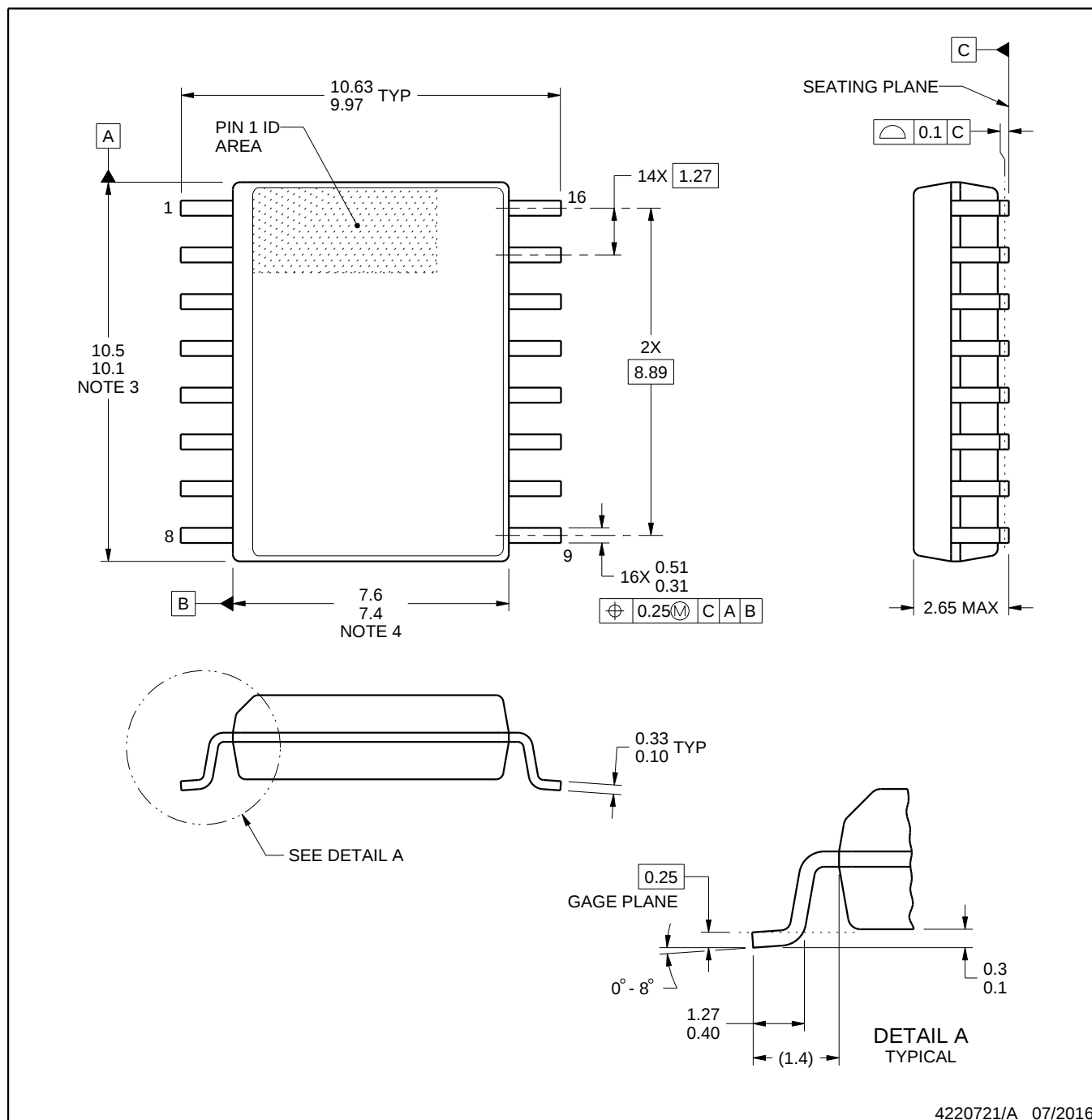


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

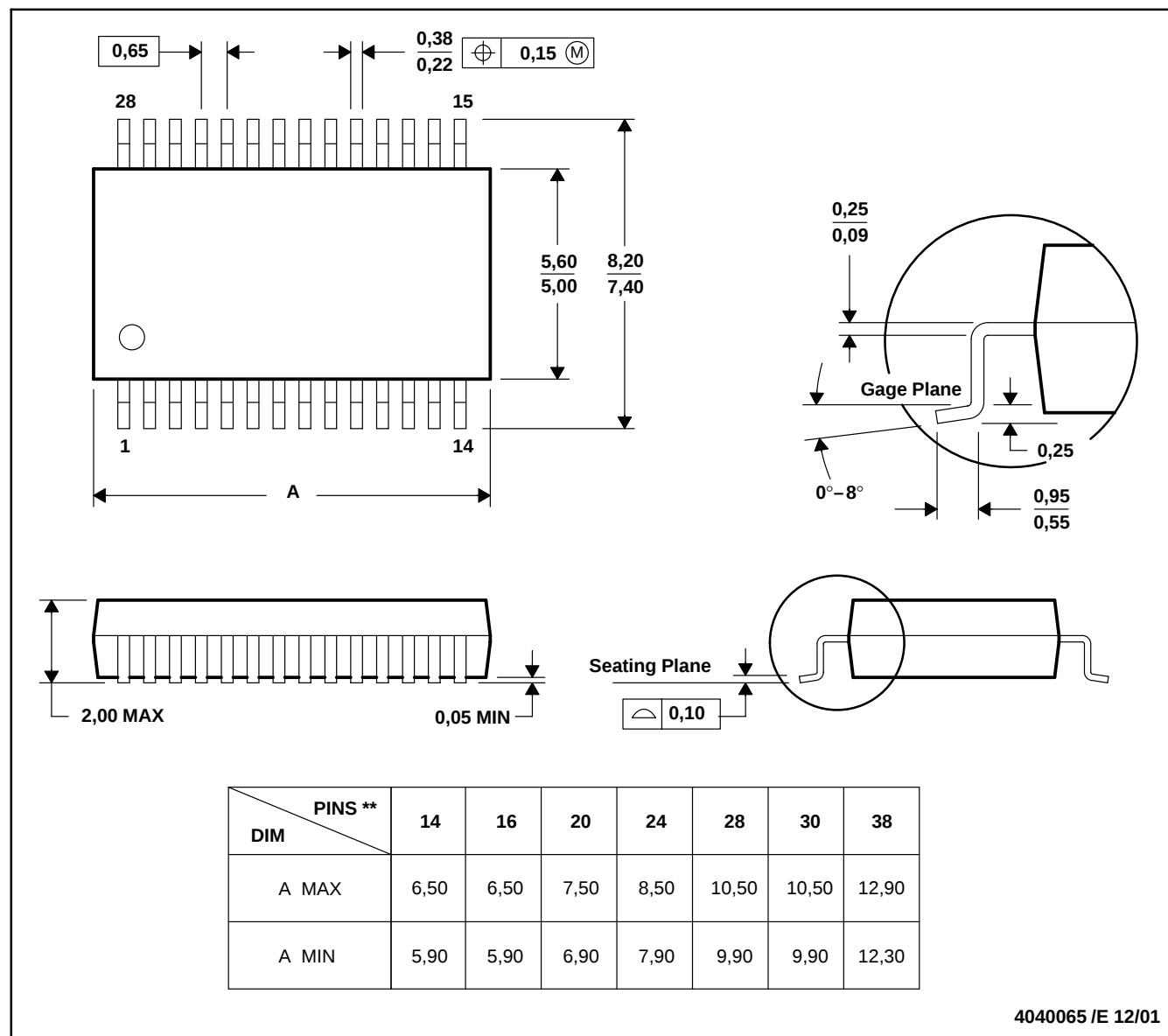
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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